

[Upgrade to Revision] Renesas Starter Kit for RX64M, RX65N-1MB, RX65N-2MB, RX71M, RX72M, RX72N, RX671, RX23T, RX24T, RX24U, RX66T, RX72T, RX111, RX113, RX231, RX130-128KB, RX130-512KB, Renesas Solution Starter Kit for RX23W

R20TS0868EJ0100  
Rev.1.00  
Aug. 01, 2022

## Outline

The board description files (BDFs: files that include pin setting information) of the products in the title have been updated.

### 1. Updated Files

No.	File name	Applicable board Download file name	Latest version
1	RSKR64M_V1.01.bdf	Renesas Starter Kit+ for RX64M rbdf0002xj0101-rskrx64m.zip	1.01
2	RSKR65N_V1.01.bdf	Renesas Starter Kit+ for RX65N-1MB rbdf0003xj0101-rskrx65n.zip	1.01
3	RSKR65N-2MB(TSIP)_V1.01.bdf	Renesas Starter Kit+ for RX65N-2MB(TSIP) rbdf0040xj0101-rskrx65n-2mb(tsip).zip	1.01
4	RSKR65N-2MB_V1.04.bdf	Renesas Starter Kit+ for RX65N-2MB rbdf0001xj0104-rskrx65n-2mb.zip	1.04
5	RSKR71M_V1.01.bdf	Renesas Starter Kit+ for RX71M rbdf0004xj0101-rskrx71m.zip	1.01
6	RSKR72M_V1.01.bdf	Renesas Starter Kit+ for RX72M rbdf0020xj0101-rskrx72m.zip	1.01
7	RSKR72N_V1.02.bdf	Renesas Starter Kit+ for RX72N rbdf0022xj0102-rskrx72n.zip	1.02
8	RSKR671_V1.01.bdf	Renesas Starter Kit+ for RX671 rbdf0033xj0101-rskrx671.zip	1.01
9	RSKR23T_V1.01.bdf	Renesas Starter Kit for RX23T rbdf0014xj0101-rskrx23t.zip	1.01
10	RSKR24T_V1.02.bdf	Renesas Starter Kit for RX24T rbdf0012xj0102-rskrx24t.zip	1.02
11	RSKR24U_V1.02.bdf	Renesas Starter Kit for RX24U rbdf0013xj0102-rskrx24u.zip	1.02
12	RSKR66T_V1.03.bdf	Renesas Starter Kit for RX66T rbdf0010xj0103-rskrx66t.zip	1.03
13	RSKR72T_V1.01.bdf	Renesas Starter Kit for RX72T rbdf0011xj0101-rskrx72t.zip	1.01
14	RSKR111_V1.01.bdf	Renesas Starter Kit for RX111 rbdf0005xj0101-rskrx111.zip	1.01
15	RSKR113_V1.01.bdf	Renesas Starter Kit for RX113 rbdf0006xj0101-rskrx113.zip	1.01
16	RSKR130_V1.01.bdf	Renesas Starter Kit for RX130-128MB rbdf0007xj0101-rskrx130.zip	1.01
17	RSKR130-512KB_V1.02.bdf	Renesas Starter Kit for RX130-512KB rbdf0008xj0102-rskrx130-512kb.zip	1.02
18	RSKR231_V1.01.bdf	Renesas Starter Kit for RX231 rbdf0009xj0101-rskrx231.zip	1.01
19	RSSKR23W_V1.01.bdf	Renesas Solution Starter Kit for RX23W rbdf0023xj0101-rsskrx23w.zip	1.01

## 2. Description

The files have been updated as follows.

No.	File name	Changes
1	RSKR64M_V1.01.bdf	<p>[Updates due to BDF spec changes]</p> <ul style="list-style-type: none"> <li>Added an option to debug interface setting: JTAG</li> <li>Added clock configuration</li> </ul> <p>[Corrections to/changes in setting information]</p> <ul style="list-style-type: none"> <li>Pin 7 id: Corrected "RXD6" to "SMISO6"</li> <li>Pin 8 id: Corrected "TXD6" to "SMOSI6"</li> <li>Pin 44 id: Corrected "IRQ9" to "P21"</li> <li>Pin 45 id: Corrected "IRQ8" to "P20"</li> </ul>
2	RSKR65N_V1.01.bdf	<p>[Updates due to BDF spec changes]</p> <ul style="list-style-type: none"> <li>Added an option to debug interface setting: JTAG</li> <li>Added clock configuration</li> </ul> <p>[Corrections to/changes in setting information]</p> <ul style="list-style-type: none"> <li>Pin 6 id: Corrected "IRQ10" to "P02"</li> <li>Pin 9 id: Corrected "PF5" to "IRQ4"</li> <li>Pin 127 id: Corrected "CTS7#" to "P93"</li> <li>Pin 128 id: Corrected "RXD7" to "SMISO7"</li> <li>Pin 131 id: Corrected "TXD7" to "SMOSI7"</li> <li>Pin 32: Deleted HSYNC</li> <li>Deleted pin 133 P47, pin 134 P46, pin 135 P45, pin 136 P44</li> <li>Pin 34 to 39, 41, 42: Deleted PDC-related information</li> <li>Deleted pin 67 QIO0, pin 78 SDSDI_D1</li> </ul>
3	RSKR65N-2MB(TSIP)_V1.01.bdf	<p>[Corrections to/changes in setting information]</p> <ul style="list-style-type: none"> <li>Pin 18: Added MD</li> <li>Pin 32 id: Corrected "P31" to "SSLB0" and group="A"</li> <li>Pin 33 id: Corrected "SMISO1" to "MISOB" and group="A"</li> <li>Pin 36 id: Corrected "SCK1" to "RSPCKB" and group="A"</li> <li>Pin 37 id: Corrected "SMOSI1" to "MOSIB" and group="A"</li> <li>Pin 38 SDHI_CD: Corrected group="C" to group=""</li> <li>Pin 40 SDHI_WP: Corrected group="C" to group=""</li> <li>Pin 42 id: Corrected "EDACK0" to "SDHI_D1" and group="C"</li> <li>Pin 43 id: Corrected "EDREQ0" to "SDHI_D0" and group="C"</li> <li>Pin 55: Added USB0_DM</li> <li>Pin 56: Added USB0_DP</li> <li>Pin 95, 98, 120, 124, 128, 135 to 139, 156, 158: Deleted SDRAM-related information</li> <li>SDRAM clock: Corrected enabled to disabled</li> </ul>
4	RSKR65N-2MB_V1.04.bdf	<p>[Updates due to BDF spec changes]</p> <ul style="list-style-type: none"> <li>Added an option to debug interface setting: JTAG</li> <li>Added clock configuration</li> </ul> <p>[Corrections to/changes in setting information]</p> <ul style="list-style-type: none"> <li>Pin 18: Added MD</li> <li>Pin 32 id: Corrected "P31" to "SSLB0" and group="A"</li> <li>Pin 33 id: Corrected "SMISO1" to "MISOB" and group="A"</li> <li>Pin 36 id: Corrected "SCK1" to "RSPCKB" and group="A"</li> <li>Pin 37 id: Corrected "SMOSI1" to "MOSIB" and group="A"</li> <li>Pin 38 SDHI_CD: Corrected group="C" to group=""</li> <li>Pin 40 SDHI_WP: Corrected group="C" to group=""</li> <li>Pin 42 id: Corrected "EDACK0" to "SDHI_D1" and group="C"</li> <li>Pin 43 id: Corrected "EDREQ0" to "SDHI_D0" and group="C"</li> </ul>

No.	File name	Changes
		<ul style="list-style-type: none"> <li>Pin 55: Added USB0_DM</li> <li>Pin 56: Added USB0_DP</li> <li>Pin 95, 98, 120, 124, 128, 135 to 139, 156, 158: Deleted SDRAM-related information</li> </ul>
5	RSKR71M_V1.01.bdf	[Updates due to BDF spec changes] <ul style="list-style-type: none"> <li>Added an option to debug interface setting: JTAG</li> <li>Added clock configuration</li> </ul> [Corrections to/changes in setting information] <ul style="list-style-type: none"> <li>Pin 7 id: Corrected "RXD6" to "SMISO6"</li> <li>Pin 8 id: Corrected "TXD6" to "SMOSI6"</li> <li>Pin 44 id: Corrected "IRQ9" to "P21"</li> <li>Pin 45 id: Corrected "IRQ8" to "P20"</li> <li>Pin 11, 168, 171: Deleted Direct LCD</li> <li>Pin 38, 40, 42, 43, 47, 49: Deleted PDC-related information</li> <li>Deleted pin 93 P73, pin 111 ET1_TX_ER</li> </ul>
6	RSK+RX72M	[Updates due to BDF spec changes] <ul style="list-style-type: none"> <li>Added an option to debug interface setting: JTAG</li> <li>Added clock configuration</li> </ul> [Corrections to/changes in setting information] <ul style="list-style-type: none"> <li>Pin D3 id: Corrected "P03" to "IRQ11"</li> <li>Pin G1: Added XCOUT</li> </ul>
7	RSKR72N_V1.02.bdf	[Updates due to BDF spec changes] <ul style="list-style-type: none"> <li>Added an option to debug interface setting: JTAG</li> <li>Added clock configuration</li> </ul> [Corrections to/changes in setting information] <ul style="list-style-type: none"> <li>Pin E5 id: Corrected "IRQ15" to "ADTTRG0#"</li> <li>Pin J4 id: Corrected "PMGI1_MDC" to "ET1_MDC"</li> <li>Pin J5 id: Corrected "PMGI1_MDIO" to "ET1_MDIO"</li> <li>Pin P2 id: Corrected "IRQ7" to "P17"</li> </ul>
8	RSKR671_V1.01.bdf	[Updates due to BDF spec changes] <ul style="list-style-type: none"> <li>Added an option to debug interface setting: JTAG</li> </ul> [Corrections to/changes in setting information] <ul style="list-style-type: none"> <li>Pin 79 to 84, 87 to 90, 92, 94 to 96, 98 to 102, 104, 106 to 115, 119 to 126: Added SDRAM-related information</li> <li>Pin 117 id: Corrected "P60" to "IRQ0"</li> <li>Pin 144 id: Corrected "IRQ15" to "ADTRG0#"</li> <li>Deleted pin 11 PJ5, pin 63 P82, pin 77 P73, pin 117 P60, pin 131 P90</li> <li>USB clock SCKCR2: Changed off to on</li> </ul>
9	RSKR23T_V1.01.bdf	[Updates due to BDF spec changes] <ul style="list-style-type: none"> <li>Added an option to debug interface setting: FINE</li> <li>Added clock configuration</li> </ul> [Corrections to/changes in setting information] <ul style="list-style-type: none"> <li>Pin 4 id: Corrected "IRQ4" to "P01"</li> <li>Pin 5 id: Added "FINED"</li> <li>Pin 21 id: Corrected "PB4" to "IRQ3"</li> <li>Pin 30 id: Corrected "IRQ0" to "P93"</li> </ul>
10	RSKR24T_V1.02.bdf	[Updates due to BDF spec changes] <ul style="list-style-type: none"> <li>Added an option to debug interface setting: FINE</li> <li>Added clock configuration</li> </ul> [Corrections to/changes in setting information]

No.	File name	Changes
		<ul style="list-style-type: none"> <li>Pin 6 id: Corrected "MD" to "FINED"</li> <li>Pin 27 id: Corrected "RXD5" to "SMISO5"</li> <li>Pin 28 id: Corrected "TXD5" to "SMOSI5"</li> <li>Pin 30 id: Corrected "CTS5#" to "PB4"</li> <li>Pin 78 id: Corrected "IRQ3" to "P55"</li> <li>Pin 79 id: Corrected "IRQ2" to "P54"</li> </ul>
11	RSKRX24U_V1.02.bdf	<p>[Updates due to BDF spec changes]</p> <ul style="list-style-type: none"> <li>Added an option to debug interface setting: FINE</li> <li>Added clock configuration</li> </ul> <p>[Corrections to/changes in setting information]</p> <ul style="list-style-type: none"> <li>Deleted pin 1 P14, pin 2 P13</li> <li>Pin 12 id: Corrected "MD" to "FINED"</li> <li>Pin 24 id: Added "PE0"</li> <li>Pin 87 id: Added "IRQ6"</li> <li>Pin 91 id: Added "P27"</li> </ul>
12	RSKRX66T_V1.03.bdf	<p>[Updates due to BDF spec changes]</p> <ul style="list-style-type: none"> <li>Added an option to debug interface setting: JTAG</li> <li>Added clock configuration</li> <li>Added a VCC option: 3.3 V (item id="vccinput" value="3.3")</li> <li>Analog voltage setting: Set to 3.3 V (item id="avccinput" value="3.3")</li> <li>Negative voltage input settings: Disabled all (item id=an001 - pgavss1)</li> </ul> <p>[Corrections to/changes in setting information]</p> <ul style="list-style-type: none"> <li>Pin 6: Added MD_FINED</li> <li>Pin 65 id: Added "P24"</li> <li>Pin 66 id: Added "TXDX12"</li> <li>Pin 67 id: Added "RXDX12"</li> </ul>
13	RSKRX72T_V1.01.bdf	<p>[Updates due to BDF spec changes]</p> <ul style="list-style-type: none"> <li>Added an option to debug interface setting: JTAG</li> <li>Added clock configuration</li> <li>Added a VCC option: 3.3 V (item id="vccinput" value="3.3")</li> <li>Analog voltage setting: Set to 3.3 V (item id="avccinput" value="3.3")</li> <li>Negative voltage input settings: Disabled all (item id=an001 - pgavss1)</li> </ul> <p>[Corrections to/changes in setting information]</p> <ul style="list-style-type: none"> <li>Pin 11: Added MD_FINED</li> <li>Pin 95 id: Added "P24"</li> <li>Pin 96 id: Added "TXDX12"</li> <li>Pin 97 id: Added "RXDX12"</li> </ul>
14	RSKRX111_V1.01.bdf	<p>[Updates due to BDF spec changes]</p> <ul style="list-style-type: none"> <li>Added an option to debug interface setting: FINE</li> <li>Added clock configuration</li> </ul> <p>[Corrections to/changes in setting information]</p> <ul style="list-style-type: none"> <li>Pin 6: Added MD/FINED</li> <li>Pin 31 id: Corrected "TXD5" to "SMOSI5"</li> <li>Pin 32 id: Corrected "RXD5" to "SMISO5"</li> <li>Pin 33 id: Corrected "MTIOC3B" to "PB7"</li> <li>Pin 34 id: Corrected "MTIOC3D" to "PB6"</li> </ul>

No.	File name	Changes
		<ul style="list-style-type: none"> <li>• Pin 42 id: Corrected "IRQ5" to "PA4"</li> <li>• Pin 43 id: Corrected "IRQ6" to "PA3"</li> <li>• Pin 45 id: Corrected "MTIOC4A" to "PA0"</li> <li>• Pin 49 id: Corrected "RXD12" to "RXDX12"</li> <li>• Pin 50 id: Corrected "TXD12" to "TXDX12"</li> <li>• Pin 2: Deleted P27</li> </ul>
15	RSKRX113_V1.01.bdf	<p>[Updates due to BDF spec changes]</p> <ul style="list-style-type: none"> <li>• Added an option to debug interface setting: FINE</li> <li>• Added clock configuration</li> </ul> <p>[Corrections to/changes in setting information]</p> <ul style="list-style-type: none"> <li>• Pin 5 id: Corrected "MTIOC4C" to "P25"</li> <li>• Pin 6 id: Corrected "MTIOC4A" to "P24"</li> <li>• Pin 7 id: Corrected "MTIOC3D" to "P23"</li> <li>• Pin 8 id: Corrected "MTIOC3B" to "P22"</li> <li>• Pin 15: Added MD/FINED</li> <li>• Pin 92, 93: Deleted VREFL, VREFH</li> </ul>
16	RSKRX130_V1.01.bdf	<p>[Updates due to BDF spec changes]</p> <ul style="list-style-type: none"> <li>• Added an option to debug interface setting: FINE</li> <li>• Added clock configuration</li> </ul> <p>[Corrections to/changes in setting information]</p> <ul style="list-style-type: none"> <li>• Pin 6: Added MD_FINED</li> <li>• Pin 23 id: Corrected "IRQ7" to "P17"</li> <li>• Pin 60 id: Corrected "RTS12" to "PE3"</li> <li>• Pin 37 id: Added "PC5"</li> <li>• Pin 61 id: Added "RXDX12"</li> <li>• Pin 62 id: Added "TXDX12"</li> <li>• Pin 66 id: Corrected "IRQ0" to "PD0"</li> </ul>
17	RSKRX130-512KB_V1.02.bdf	<p>[Updates due to BDF spec changes]</p> <ul style="list-style-type: none"> <li>• Added an option to debug interface setting: FINE</li> <li>• Added clock configuration</li> </ul> <p>[Corrections to/changes in setting information]</p> <ul style="list-style-type: none"> <li>• Pin 7: Added MD_FINED</li> <li>• Pin 47 id: Added "PC5"</li> <li>• Pin 76 id: Added "RXDX12"</li> <li>• Pin 77 id: Added "TXDX12"</li> <li>• Pin 86 id: Corrected "IRQ0" to "PD0"</li> <li>• Pin 94, 96: Deleted VREFL0, VREFH0</li> </ul>
18	RSKRX231_V1.01.bdf	<p>[Updates due to BDF spec changes]</p> <ul style="list-style-type: none"> <li>• Added an option to debug interface setting: FINE</li> <li>• Added clock configuration</li> </ul> <p>[Corrections to/changes in setting information]</p> <ul style="list-style-type: none"> <li>• Pin 7: Added MD/FINED</li> <li>• Pin 8 id: Corrected "XCOUT" to "XCIN"</li> <li>• Pin 9 id: Corrected "XCIN" to "XCOUT"</li> <li>• Pin 29 id: Corrected "MTIOC3B" to "P17"</li> <li>• Pin 39, 40: Added CRXD0, CTXD0</li> <li>• Pin 42 id: Corrected "RD#" to "P52"</li> <li>• Pin 43 id: Corrected "WR1#" to "P51"</li> <li>• Pin 44 id: Corrected "WR0#" to "P50"</li> <li>• Pin 45 id: Corrected "PC7" to "SMOSI8"</li> <li>• Pin 46 id: Corrected "RXD8" to "SMISO8"</li> <li>• Pin 49 id: Corrected "SDD0" to "SDHI_D0"</li> </ul>

No.	File name	Changes
		<ul style="list-style-type: none"> <li>• Pin 50 id: Corrected "SDD3" to "SDHI_D3"</li> <li>• Pin 53 id: Corrected "SDD2" to "SDHI_D2"</li> <li>• Pin 54 id: Corrected "SDD1" to "SDHI_D1"</li> <li>• Pin 55 id: Corrected "SDCD" to "SDHI_CD"</li> <li>• Pin 57 id: Corrected "SDWP" to "SDHI_WP"</li> <li>• Pin 58 id: Corrected "SDPWRCRL" to "PB2"</li> <li>• Pin 59 id: Corrected "SDCLK" to "SDHI_CLK"</li> <li>• Pin 61 id: Corrected "SDCMD" to "SDHI_CMD"</li> <li>• Pin 71 id: Corrected "IRQ7" to "PE7"</li> <li>• Pin 72 id: Corrected "IRQ6" to "PE6"</li> </ul>
19	RSSKRX23W_V1.01.bdf	[Updates due to BDF spec changes] <ul style="list-style-type: none"> <li>• Added an option to debug interface setting: FINE</li> <li>• Added clock configuration</li> </ul> [Corrections to/changes in setting information] <ul style="list-style-type: none"> <li>• Pin B7 id: Corrected "MD" to "FINED"</li> <li>• Pin D1: Added USB0_DM</li> <li>• Pin K9: Deleted DCLOUT</li> </ul>

### 3. Updating the File

Update in either of the following ways.

#### 3.1 Update the Smart Configurator

If you are using CS+, update the Smart Configurator for RX to V2.14.0, and then update the BDF.

If you are using e<sup>2</sup> studio, update it to e<sup>2</sup> studio v2022-07 (22.7.0), and then update the BDF.

#### 3.2 Import the BDF

Download a desired BDF from the URL below, import it using the Smart Configurator for RX, and then update the file.

<https://www.renesas.com/us/en/software-tool/smart-configurator#download>

For how to import a BDF using Smart Configurator, refer to "How to use Board Description File(bdf) at the Smart Configurator"(Japanese only).

<https://www.renesas.com/jp/ja/document/apn/962701>

## Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Aug.01.22	-	First edition issued

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The URLs in the Tool News also may be subject to change or become invalid without prior notice.

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