[Notes]
Smart Configurator for RH850

R20TS0668EC0100
Rev.1.00
Feb. 16, 2021

Outline

When using Smart Configurator for RH850, note the following points.

1. When using CSI master

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1.1 Applicable Products

Smart Configurator for RH850 V1.3.0 or previous version

1.2 Applicable Devices

RH850 family: RH850/F1KM group

- RH850/F1KM-S1 (48-pin, 64-pin, 80-pin, and 100-pin products)
- RH850/F1KM-S4 (100-pin, 144-pin, 176-pin, and 233-pin products)

1.3 Details

When using CSI mater mode on the following peripherals, all interrupts can't be set up to be delayed by half cycle of the transmission clock, even if user config the interrupt delay mode as "half delay" on GUI (refer to Figure 1 Setting of interrupt delay mode.).

- RH850/F1KM-S1: 48-pin, 64-pin products

  CSIG0, CSIH0
- RH850/F1KM-S1: 80-pin products

  CSIG0, CSIH0, CSIH1, CSIH2
- RH850/F1KM-S1: 100-pin products

  CSIG0, CSIH0, CSIH1, CSIH2, CSIH3
- RH850/F1KM-S4: 100-pin products

  CSIG0, CSIH0, CSIH1, CSIH2, CSIH3
- RH850/F1KM-S4: 144-pin products

  CSIG0, CSIG1, CSIH0, CSIH1, CSIH2, CSIH3
- RH850/F1KM-S4: 176-pin, 233-pin products

  CSIG0, CSIG1, CSIG2, CSIG3, CSIH0, CSIH1, CSIH2, CSIH3

Figure 1 Setting of interrupt delay mode

1.4 Workaround

User can manually modify the register setting code in the following source file

- Source file: “<Configuration-name>.c”.
- Function: “void R_<*Configuration-name*>_ Create (void)”

Note: If code is generated again, the previous state is restored. Modification is necessary each time you perform code generation.

The following is an example of the required modification when <*Configuration-name*> is Config_CSIG0 in the RH850/F1KM group. Manually add the code in red.

```
 void R_Config_CSIG0_Create(void)
 {
     uint32_t tmp_port;


     CSIG0.CTL0 = _CSIG_OPERATION_CLOCK_STOP;
     ……
     /* Set CSIG0 control setting */
     CSIG0.CTL1 = _CSIG_CLOCK_INVERTING_HIGH |
_CSIG_INTERRUPT_TIMING_TRANSFERRED | _CSIG_HALF_CLOCK_DELAY |
_CSIG_DATA_CONSISTENCY_CHECK_DISABLE | _CSIG_HANDSHAKE_DISABLE |
_CSIG_SLAVE_SELECT_DISABLE;
     CSIG0.CTL2 = _CSIG0_SELECT_BASIC_CLOCK | _CSIG0_BAUD_RATE;
     ……
 }
```

1.5 Schedule for Fixing the Problem

This problem will be fixed in the next version. (Scheduled to be released in May 2021.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Feb.16.21	-	First edition issued

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