

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0076A/E	Rev.	1.00
Title	RZ/G2M V1.3 Specification Change for Ethernet AVB-IF Module Signal Timing		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2M V1.3	Lot No.	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.01 (R01UH0808EJ0101)		
		All lots				

This technical update describes specification change of RZ/G Series, 2nd Generation product.

[Summary]

Specification change for "Hardware Electrical Characteristics Common to RZ/G Series, 2nd Generation products".

[Priority level]

Importance: "Normal"

Urgency: "Normal"

[Products]

RZ/G2M V1.3

[Section number and title]

73.16 Ethernet AVB-IF Module Signal Timing

[Correction]

- Section 73.16 Ethernet AVB-IF Characteristics, Page 73-74, Table 73.16.3 Ethernet Control Timing (RGMII Tx clock internal Delay Mode). AVB_TX_CTL and AVB_TD[3:0] setup time of RZ/G2M V1.3 have been fixed.

Current (from):

Table 73.16.3 Ethernet Control Timing (RGMII Tx clock internal Delay Mode) [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

Conditions: VDDQ33 = 3.3 ± 0.2 V, VDDQ25_ETH = 2.5 ± 0.1V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N],

Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3],

Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N],

Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N], GND = VSS = 0 V, CL = 30 pF

Recommend: Connection of series 25 Ω as damping resistor to RGMII output buffer. [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
AVB_TXCREFCLK cycle time	—	125 – 50 ppm	—	125 + 50 ppm	MHz	—
AVB_TXC cycle time*	Tcyc	7.2	8	8.8	ns	
AVB_TXC duty cycle (in 1 Gbps)	Duty_G	45	50	55	%	
AVB_TXC duty cycle (in 100 Mbps)	Duty_T	40	50	60	%	
AVB_TX_CTL setup time	TsetupT	1.2	2.0	—	ns	Figure 73.16.5
AVB_TX_CTL hold time	TholdT	1.2	2.0	—	ns	
AVB_TD[3:0] setup time	TsetupT	1.2	2.0	—	ns	
AVB_TD[3:0] hold time	TholdT	1.2	2.0	—	ns	

Note: * For 100 Mbps, Tcyc will scale to 40 ns +- 4 ns respectively.

Correction (to):

Table 73.16.3 Ethernet Control Timing (RGMII Tx clock internal Delay Mode) [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

Conditions: VDDQ33 = 3.3 ± 0.2 V, VDDQ25_ETH = 2.5 ± 0.1V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N],

Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3],

Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N],

Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N], GND = VSS = 0 V, CL = 30 pF

Recommend: Connection of series 25 Ω as damping resistor to RGMII output buffer. [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
AVB_TXCREFLK cycle time	—	125 – 50 ppm	—	125 + 50 ppm	MHz	—
AVB_TXC cycle time ^{*1}	Tcyc	7.2	8	8.8	ns	
AVB_TXC duty cycle (in 1 Gbps)	Duty_G	45	50	55	%	
AVB_TXC duty cycle (in 100 Mbps)	Duty_T	40	50	60	%	
AVB_TX_CTL setup time	TsetupT	1.2 ^{*2} 0.95 ^{*3}	2.0	—	ns	Figure 73.16.5
AVB_TX_CTL hold time	TholdT	1.2	2.0	—	ns	
AVB_TD[3:0] setup time	TsetupT	1.2 ^{*2} 0.95 ^{*3}	2.0	—	ns	
AVB_TD[3:0] hold time	TholdT	1.2	2.0	—	ns	

Notes: 1. For 100 Mbps, Tcyc will scale to 40 ns ± 4 ns respectively.

2. For [RZ/G2H, RZ/G2M V3.0, RZ/G2N].

3. For [RZ/G2M V1.3].

[Description]

Fix defects due to design mistakes.

[Reason for Correction]

Specification change.

- End of Document -