Date: Jan. 16, 2023

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RZ*-A0106A/E	Rev.	1.00
Title	RZ/G2H, G2M V1.3, G2M V3.0, G2N and G2E Additional Descriptions for Advanced Power Management Unit for AP-System Core (APMU)		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2H, RZ/G2M V1.3, V3.0 RZ/G2N, RZ/G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.10 (R01UH0808EJ0110)		

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Additional Descriptions for “Section 08B.Advanced Power Management Unit for AP-System Core (APMU) of RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.10”.

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Product]

RZ/G2H

RZ/G2M V1.3, V3.0

RZ/G2N

RZ/G2E

[section number and title]

13. Advanced Power Management Unit for AP-System Core (APMU)

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 13, Page 13-15, 13.2.5 Cortex-A53/Cortex-A57 Debug Resource Reset Control Register (CA53DBGRCR, CA57DBGRCR), explanation changed.

Current (from):

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	—	B'1	R	Reserved This bit is always read as 1. The write value should always be 1.
23	—	B'1	R	Reserved This bit is always read as 1. The write value should always be 1.
22	—	B'1	R	Reserved This bit is always read as 1. The write value should always be 1.
21	—	B'1	R	Reserved This bit is always read as 1. The write value should always be 1.
20	—	B'1	R	Reserved This bit is always read as 1. The write value should always be 1.
19	DBGCPUPREN	B'0	R/W	Enable the reset request derived from power shut off to CPU Peripheral (SCU and L2 cache controller) in the debug mode. 0: Disables the reset request derived from power shut off to CPU Peripheral (SCU and L2 cache controller) in the debug mode. 1: Enables the reset request derived from power shut off to CPU Peripheral (SCU and L2 cache controller) in the debug mode.
18	—	B'0	R	Reserved This bit is always read as 0. The write value should always be 0.
17, 16	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).

Correction (to):

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	—	B'1	R	Reserved This bit is always read as 1. The write value should always be 1.
23	—	B'1	R	Reserved This bit is always read as 1. The write value should always be 1.
22	—	B'1	R	Reserved This bit is always read as 1. The write value should always be 1.
21	—	B'1	R	Reserved This bit is always read as 1. The write value should always be 1.
20	—	B'1	R	Reserved This bit is always read as 1. The write value should always be 1.
19	DBGCPUPREN	B'0	R/W	Enable the reset request derived from power shut off to CPU Peripheral (SCU and L2 cache controller). 0: Disables the reset request derived from power shut off to CPU Peripheral (SCU and L2 cache controller). 1: Enables the reset request derived from power shut off to CPU Peripheral (SCU and L2 cache controller). See also the explanation of these registers at the top of 13.2.5 for note about bit 19.
18	—	B'0	R	Reserved This bit is always read as 0. The write value should always be 0.
17, 16	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).

[Description]

Descriptions that could be a cause of misunderstandings have been corrected.

The detail description for the reference is that “In the normal mode (i.e. not debug mode), writing all 1 to bit 19 doesn’t disturb normal operation. Therefore, the same code to write these registers can be applied for both debug mode and normal mode. About CA53DBGRCR and CA57DBGRCR, refer to Appendix B.”.

[Reason for Correction]

Expression improvement

- End of Document -