To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

RENESAS TECHNICAL NEWS No.M16C-116-0311

Replace Sheets of Renesas Technical News No. M16C-115-0311
M16C/62P   Precautions When Supplying Power to Microcomputer
　　　　　　　(Explanation of Addition in M16C/62P Group Data Sheet.)

Classification	**Concerned Products**

Corrections and supplementary
     explanation of document
√ Notes
  Knowhow
  Others
	M16C/62P

A section of RENESAS TECHNICAL NEWS "No. M16C-115-0311" has been revised.
RENESAS TECHNICAL NEWS "M16C/62P Precautions when supplying power to microcomputer (Explanation of addition in M16C/62P group data sheet.)" should be replaced with the attached one "No. M16C-116-0311".

Revised contents
Figure 3 and 4 have been added on "4. Reference".

RENESAS TECHNICAL NEWS   No.M16C-116-0311

M16C/62P
Precautions When Supplying Power to Microcomputer
(Explanation of Addition in M16C/62P Group Data Sheet)

Classification	Concerned Products
Corrections and supplementary explanation of document √ Notes Knowhow Others	M16C/62P

1. Precautions

SV_{CC} conditions are indicated in the Recommended Operating Conditions in the Electrical Characteristics section (See Figure 2.) of all M16C/62P group Data Sheet Rev. 2.10. When supplying power to the microcomputer, power applied to the VCC1 pin must meet the conditions of the power supply rising gradient (SV_{CC}).

If the power supply gradient before power applied to the VCC1 pin reached 2.7V does not meet the SV_{CC} conditions, the microcomputer may malfunction.

[Examples of Possible Causes of Malfunction]

- Other devices are turned on before M16C/62P, causing voltage applied to M16C/62P to rise halfway via other LSIs.

- Voltage applied to M16C/62P rises through communication lines to which voltage is applied before M16C/62P is turned on.

- Source impedance for M16C/62P is significantly higher than usual such as auxiliary power supply for back-up operation or power supply through communication lines to the microcomputer.

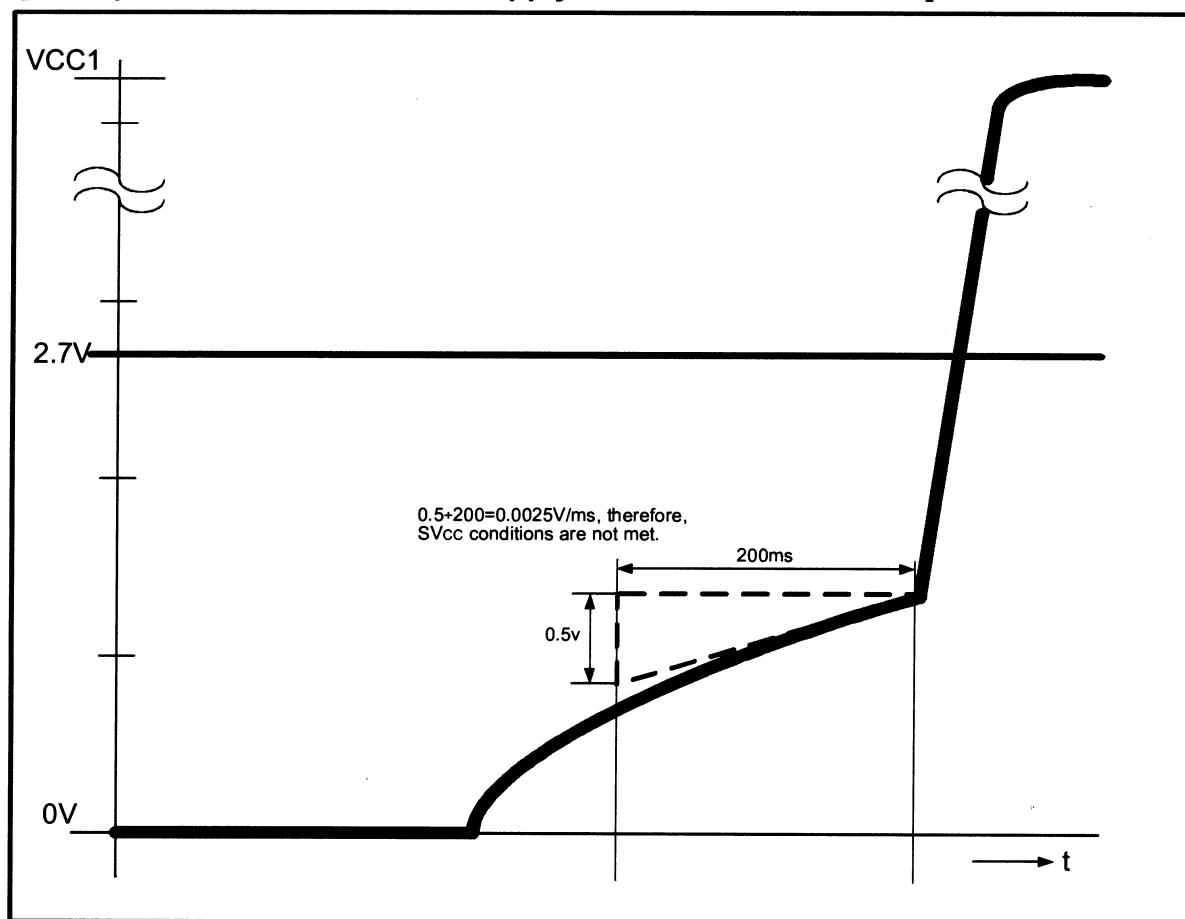**[Example of a Possible Power Supply-associated Malfunction]**

VCC1

2.7V

0.5÷200=0.0025V/ms, therefore,
SVcc conditions are not met.

200ms

0.5v

0V

→ t

Figure 1. Power Supply Example

2. Solutions

When supplying power to the microcomputer, the power supply voltage applied to the VCC1 pin must meet the conditions of the power supply rising gradient (SV_{CC}).

In those cases listed in the Examples of Possible Causes of Malfunction, take such measures as eliminating power supply interferences or tuning power supply impedance to meet SV_{CC} conditions.

3. Affected Products

M16C/62P

4. Reference

5. Electrical Characteristics (M16C/62P)

Table 5.2 Recommended Operating Conditions (1) [1]

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V_{CC1}, V_{CC2}	Supply voltage($V_{CC1} \geq V_{CC2}$)		2.7	5.0	5.5	V
AV_{CC}	Analog supply voltage			V_{CC1}		V
$f_{(ripple)}$[2]	Power supply ripple allowable frequency				10	MHz
$V_{P-P(ripple)}$[2]	Power supply ripple allowable amplitude voltage	(V_{CC1}=5V)			0.5	V
		(V_{CC1}=3V)			0.3	V
$V_{CC(\Delta V / \Delta T)}$ [2]	Power supply ripple rising / falling gradient	(V_{CC1}=5V)			0.3	V/ms
		(V_{CC1}=3V)			0.3	V/ms
SV_{CC}[2]	Power supply rising gradient		0.05			V/ms
V_{SS}	Supply voltage			0		V
AV_{SS}	Analog supply voltage			0		V
V_{IH}	HIGH input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	0.8V_{CC2}		V_{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode)	0.8V_{CC2}		V_{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor modes)	0.5V_{CC2}		V_{CC2}	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	0.8V_{CC1}		V_{CC1}	V
		P7_0, P7_1	0.8V_{CC1}		6.5	V
V_{IL}	LOW input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	0		0.2V_{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode)	0		0.2V_{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (data input during memory expansion and microprocessor modes)	0		0.16V_{CC2}	V
		P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	0		0.2V_{CC1}	V
$I_{OH (peak)}$	HIGH peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			-10.0	mA
$I_{OH (avg)}$	HIGH average output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			-5.0	mA
$I_{OL (peak)}$	LOW peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			10.0	mA
$I_{OL (avg)}$	LOW average output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			5.0	mA

NOTES:
1. Referenced to V_{CC1} = V_{CC2} = 2.7 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
2. SV_{CC} indicates the minimum time gradient until V_{CC1} reaches 2.7V.
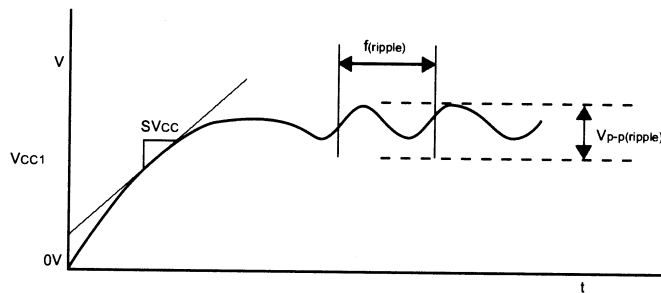
3. The mean output current is the mean value within 100ms.
4. The total $I_{OL (peak)}$ for ports P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14_0 and P14_1 must be 80mA max. The total $I_{OL (peak)}$ for ports P3, P4, P5, P6, P7, P8_0 to P8_4, P12, and P13 must be 80mA max. The total $I_{OH (peak)}$ for ports P0, P1, and P2 must be -40mA max. The total $I_{OH (peak)}$ for ports P3, P4, P5, P12, and P13 must be -40mA max. The total $I_{OH (peak)}$ for ports P6, P7, and P8_0 to P8_4 must be -40mA max. The total $I_{OH (peak)}$ for ports P8_6, P8_7, P9, P10, P11, P14_0, and P14_1 must be -40mA max.
5. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Figure 2. M16C/62P Recommended Operating Conditions (1) (Add SV_{CC} Conditions)

Table 5.3 Recommended Operating Conditions (2) [1]

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
f (XIN)	Main clock input oscillation frequency [2]	Vcc1=3.0 to 5.5V	0		16	MHz
		Vcc1=2.7 to 3.0V	0		20 X Vcc1-44	MHz
f (XCIN)	Sub-clock oscillation frequency			32.768	50	kHz
f (Ring)	Ring oscillation frequency		0.5	1	2	MHz
f (PLL)	PLL clock oscillation frequency [2]	Vcc1=3.0 to 5.5V	10		24	MHz
		Vcc1=2.7 to 3.0V	10		46.67 X Vcc1-116	MHz
f (BCLK)	CPU operation clock		0		24	MHz
tsu(PLL)	PLL frequency synthesizer stabilization wait time	Vcc1=5.0V			20	ms
		Vcc1=3.0V			50	ms

NOTES:
1. Referenced to Vcc1 = Vcc2 = 2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
2. Relationship between main clock oscillation frequency, PLL clock oscillation frequency and supply voltage.
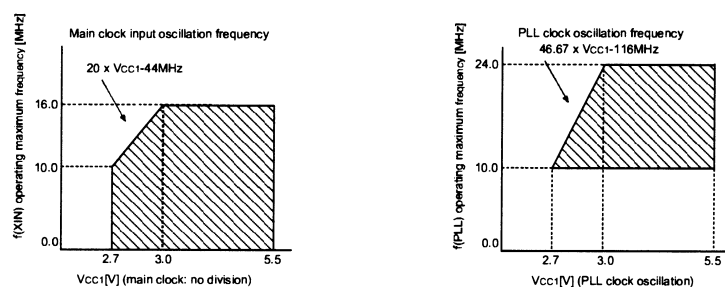
Figure 3. M16C/62P Recommended Operating Conditions (2)

5. Electrical Characteristics (M16C/62PT)

Table 5.50 Recommended Operating Conditions [1]

Symbol	Parameter		Min.	Typ.	Max.	Unit
			Standard			
Vcc1, Vcc2	Supply voltage(Vcc1=vcc2)		4.0	5.0	5.5	V
AVcc	Analog supply voltage			Vcc1		V
Vss	Supply voltage			0		V
AVss	Analog supply voltage			0		V
VIH	HIGH input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	0.8Vcc2		Vcc2	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode)	0.8Vcc2		Vcc2	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	0.8Vcc1		Vcc1	V
		P7_0 , P7_1	0.8Vcc1		6.5	V
VIL	LOW input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7	0		0.2Vcc2	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (during single-chip mode)	0		0.2Vcc2	V
		P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	0		0.2Vcc1	V
IOH (peak)	HIGH peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			-10.0	mA
IOH (avg)	HIGH average output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			-5.0	mA
IOL (peak)	LOW peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			10.0	mA
IOL (avg)	LOW average output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			5.0	mA
f (XIN)	Main clock input oscillation frequency	Vcc1=4.0 to 5.5V	0		16	MHz
f (XCIN)	Sub-clock oscillation frequency			32.768	50	kHz
f (Ring)	Ring oscillation frequency		0.5	1	2	MHz
f (PLL)	PLL clock oscillation frequency [4]	Vcc1=4.0 to 5.5V	10		24	MHz
f (BCLK)	CPU operation clock		0		24	MHz
tsu(PLL)	PLL frequency synthesizer stabilization wait time	Vcc1=5.0V			20	ms

NOTES:
1. Referenced to Vcc1 = Vcc2 = 4.7 to 5.5V at Topr = -40 to 85 °C / -40 to 125 °C unless otherwise specified.
   T version = -40 to 85 °C, V version = -40 to 125 °C.
2. The mean output current is the mean value within 100ms.
3. The total IOL(peak) for ports P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14_0 and P14_1 must be 80mA max. The total IOL(peak) for ports P3, P4, P5, P6, P7, P8_0 to P8_4, P12, and P13 must be 80mA max. The total IOH(peak) for ports P0, P1, and P2 must be -40mA max. The total IOH(peak) for ports P3, P4, P5, P12, and P13 must be -40mA max. The total IOH(peak) for ports P6, P7, and P8_0 to P8_4 must be -40mA max. The total IOH(peak) for ports P8_6, P8_7, P9, P10, P11, P14_0, and P14_1 must be -40mA max.
   As for 80-pin version, the total IOL(peak) for all ports and IOH(peak) must be 80mA. max. due to one Vcc and one Vss.
4. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Figure 4. M16C/62PT Recommended Operating Conditions