

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-R8C-A017A/E	Rev.	1.00
Title	R8C/M11A, R8C/M12A Group Notes on Timer RJ2		Information Category	Technical Notification		
Applicable Product	R8C/M11A Group R8C/M12A Group	Lot No.	Reference Document			

Note the following when using timer RJ2 in pulse width measurement mode or pulse period measurement mode for above applicable products:

- Note when writing 0 to the TEDGF bit in the TRJCR register in pulse width measurement mode or pulse period measurement mode.

Set the TRJIF bit in the TRJIR register to 0 before setting the TEDGF bit to 0.

When reading the TEDGF bit immediately after setting it to 0, it is read as 0. However the internal signal of the TEDGF bit remains 1 for one to two cycles of the count source. If an active edge is input during this period, the internal signal of the TEDGF bit does not become 0 and the TEDGF bit is read as 1.

Since the TRJIF bit becomes 1 when the internal signal of the TEDGF bit changes from 0 to 1, the TRJIF bit does not become 1 and no interrupt is generated.

After setting the TEDGF bit to 0, confirm that 0 can be read after waiting for three or more count source cycles in order to accept the next interrupt request.