Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-16C-A161A/E	Rev.	1.00
Title	R8C/20-29 Group Notes regarding Error Flags in Serial Interface		Information Category	Technical Notification		
Applicable Product	R8C/20 Group, R8C/21 Group, R8C/22 Group, R8C/23 Group, R8C/24 Group, R8C/25 Group, R8C/26 Group, R8C/27 Group, R8C/28 Group, R8C/29 Group	Lot No.	Reference Document			

1. Notes

When the clock synchronous serial I/O mode or clock asynchronous serial I/O (UART) mode for the serial interface is used, the error flags are not held as follows.

- 1) The overrun error flag (OER) is set to 1 when an overrun error occurs, but it is cleared to 0 when the next transfer clock is generated.

 ----- Point A in Figure 1, 2
- 2) The framing error flag (FER) is set to 1 when a framing error occurs, but it is cleared to 0 when the next transfer is completed.
 ----- Point B in Figure 2
- 3) The parity error flag (PER) is set to 1 when a parity error occurs, but it is cleared to 0 when the next transfer is completed.

NOTE: 2) and 3) apply to clock asynchronous serial I/O mode only.

2. Operational Description

1) Receive operation in clock synchronous serial I/O mode

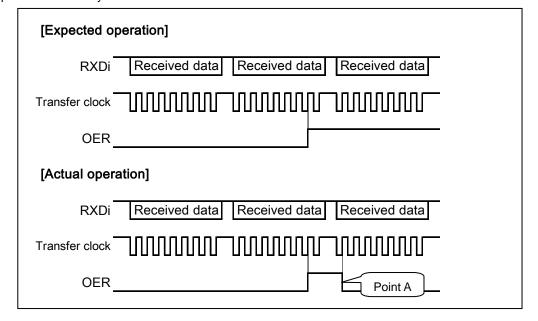


Figure 1. Receive Operation in Clock Synchronous Serial I/O Mode

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2) Receive operation in clock asynchronous serial I/O mode

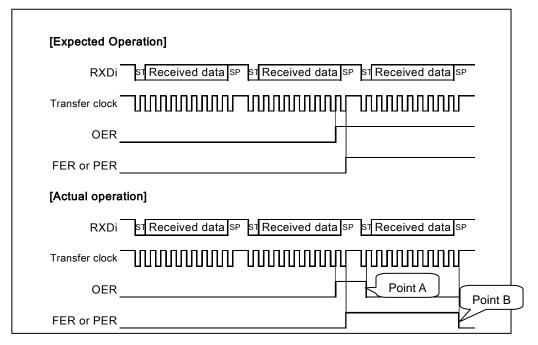


Figure 2. Receive Operation in Clock Asynchronous Serial I/O Mode

3. Action

The following actions should be taken.

1) Overrun error flag

Check the error flag before the next transfer clock is generated.

2) Framing error flag

Check the error flag before the next transfer is completed.

3) Parity error flag

Check the error flag before the next transfer is completed.

4) Error sum flag

This flag is set to 1 when any of the above flags is set to 1. Check this at the same timing as above.

4. Future Plan

Hardware modifications are to be implemented subsequently from the second quarter in 2007.

Please contact your Renesas sales office for further details on the modification schedule and identification by product type.

5. Others

There is no effect on connecting with a serial programmer or on-chip debugging emulator.

When using a full-spec emulator or compact emulator, perform the actions listed above.