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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A828A/E	Rev.	1.00
Title	Interrupts Generated during Programming/Erasure of Flash Memory		Information Category	Technical Notification		
Applicable Product	SH7137 Group SH7080 Group SH7146 Group SH7125 Group, SH7124 Group	Lot No. All lots	Reference Document	Refer to the table below.		

We would like to announce the limitation on interrupt processing during programming and erasure of flash memory in products of the SH7137, SH7080, SH7146, and SH7125/SH7124 Groups described below.

1. Limitations

   If processing of the programming or erasure interrupt is enabled during the programming or erasure of flash memory in the SH7137, SH7080, SH7146, and SH7125/SH7124 Groups, the programming or erasure of the flash memory will be forcibly terminated by the error monitoring function of the flash memory during the corresponding interrupt processing routine. Thus, the programming/erasure of flash memory may not be completed normally.

2. Countermeasure

   Ensure that no interrupts, including NMI and IRQ, are generated during programming or erasure.

3. Error Correction in the Hardware Manual

The description under (4) Programming/Erasing Execution, in 22.2.6*, Programming/Erasing Interface, of Section 22*, Flash Memory, is amended as follows.

[Before amendment]
There are limitations and notes on the interrupt processing during programming/erasing. For details, see section 22.8.2*, Interrupts during Programming/Erasing.

[After amendment]
Ensure that no interrupts, including NMI and IRQ, are generated during programming or erasure.

Note: * This is Section 23 in the SH7080 Group User's Manual, Section 19 in the SH7146 Group User's Manual, and Section 17 in the SH7125/SH7124 Group Hardware Manual.

The description under (2) Interrupts during programming/erasing, in 22.8.2*, Interrupts during Programming/Erasing, of Section 22*, Flash Memory, is amended as follows.

[Before amendment]

Though an interrupt processing can be executed at realtime during programming/erasing of the downloaded on-chip program, the following limitations and notes are applied.

1. When flash memory is being programmed or erased, both the user MAT and user boot MAT cannot be accessed. Prepare the interrupt vector table and interrupt processing routine in on-chip RAM or external memory. Make sure the flash memory being programmed or erased is not accessed by the interrupt processing routine. If flash memory is read, the read values are not guaranteed. If the relevant bank in flash memory that is being programmed or erased is accessed, the error protection state is entered, and programming or erasing is aborted. If a bank other than the relevant bank is accessed, the error protection state is not entered but the read values are not guaranteed.
2. Do not rewrite the program data specified by the FMPDR parameter. If new program data is to provided by the interrupt processing, temporarily save the new program data in another area. After confirming the completion of programming, save the new program data in the area specified by FMPDR or change the setting in FMPDR to indicated the other area in which the new program data was temporarily saved.
3. Make sure the interrupt processing routine does not rewrite the contents of the flash-memory related registers or data in the downloaded on-chip program area. During the interrupt processing, do not simultaneously perform RAM emulation, download of the on-chip program by an SCO request, or programming/erasing.
4. At the beginning of the interrupt processing routine, save the CPU register contents. Before returning from the interrupt processing, write the saved contents in the CPU registers again.
5. When a transition is made to sleep mode or software standby mode in the interrupt processing routine, the error protection state is entered and programming/erasing is aborted.
   If a transition is made to the reset state, the reset signal should only be released after providing a reset input over a period longer than the normal 100 μs to reduce the damage to flash memory.

[After amendment]

Ensure that no interrupts, including NMI and IRQ, are generated during programming/erasing of the downloaded on-chip program.

Note: * This is Section 23 in the SH7080 Group User's Manual, Section 19 in the SH7146 Group User's Manual, and 17.7.1 in Section 17 in the SH7125/SH7124 Group Hardware Manual.

The description in 22.9.2*, Areas for Storage of the Procedural Program and Data for Programming, in Section 22*, Flash Memory, is amended as follows.

[Before amendment]

The flash memory is not accessible during programming/erasing operations. Therefore, the programming/erasing program must be downloaded to on-chip RAM in advance. Areas for executing each procedure program for initiating programming/erasing, the user program at the user branch destination for programming/erasing, the interrupt vector table, and the interrupt processing routine must be located in on-chip memory other than flash memory or the external address space.

[After amendment]

The flash memory is not accessible during programming/erasing operations. Therefore, the programming/erasing program must be downloaded to on-chip RAM in advance. Areas for executing each procedure program for initiating programming/erasing and the user program at the user branch destination for programming/erasing must be located in on-chip memory other than flash memory or the external address space.

Note: * This is Section 23 in the SH7080 Group User's Manual, Section 19 in the SH7146 Group User's Manual, and 17.8.2 in Section 17 in the SH7125/SH7124 Group Hardware Manual.

In the description in Table 22.18 (1)*, Usable Area for Programming in User Program Mode, to Table 22.18 (4)*, Usable Area for Erasure in User Boot Mode, in Section 22*, Flash Memory, is amended as follows.

[Before amendment]

Table 22.18 (1)* to Table 22.18 (4)*

	Storable/Executable Area			Selected MAT	
Item	On-Chip RAM	User MAT	External Space	User MAT	Embedded Program Storage MAT
Interrupt processing routine	√	X	√	√	

[After amendment]

Table 22.18 (1)* to Table 22.18 (4)*

	Storable/Executable Area			Selected MAT	
Item	On-Chip RAM	User MAT	External Space	User MAT	Embedded Program Storage MAT

(One line deleted)

Note: * This is Section 23 in the SH7080 Group User's Manual, Section 19 in the SH7146 Group User's Manual, and Table 17.17 (1) to Table 17.17 (2) in Section 17 in the SH7125/SH7124 Group Hardware Manual.

[Applicable Products and Related Documents]

Family	Group	Related Documents	Rev.	Control Code
SH7137	SH7131, SH7132, SH7136, SH7137	SH7137 Group Hardware Manual	3.00	REJ09B0402-0300
SH7080	SH7083, SH7084, SH7085, SH7086	SH7080 Group User's Manual: Hardware	5.00	R01UH0198EJ0500
SH7146	SH7146, SH7149	SH7146 Group User's Manual: Hardware	4.00	R01UH0049EJ0400
SH/Tiny	SH7125, SH7124	SH7125 Group, SH7124 Group Hardware Manual	5.00	REJ09B0243-0500