To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Date: Oct.04.2005

RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Renesas Technology Corp.

Product Category	MPU&MCU		Document No.	TN-H8*-A309B/E	Rev.	2.00
Title	H8/38086R Group, H8/38076R Group, H8/38602R Group Watchdog Timer Usage note.		Information Category	Technical Notification		
Applicable Product	H8/38086R Group H8/38076R Group H8/38602R Group	Lot No. All	Reference Document	H8/38086R Hardware Manual (REJ09B0182-0200 Rev2.00) H8/38076R Hardware Manual (REJ09B0093-0300 Rev3.00) H8/38602R Hardware Manual (REJ09B0152-0200 Rev2.00)		

We would like to inform you about Watchdog Timer Usage note for H8/38086R Group, H8/38076R Group, and H8/38602R Group.

This usage note is only applied when the watchdog timer module is used in interval timer mode, and not applied to usage in watchdog timer mode.

H8/38086R Group Hardware Manual (Page 306)
H8/38076R Group Hardware Manual (Page 304)
14.5.3 Cleaning of WT/$\overline{IT}$ and IEOVF Bits in TCSRWD2
H8/38602R Group Hardware Manual (Page 208)
12.5.3 Cleaning of WT/$\overline{IT}$ and IEOVF Bits in TCSRWD2

Add the following description as section 14.5.3 or 12.5.3

… watchdog timer enters module standby mode.

1x.5.3 Cleaning of WT/$\overline{IT}$ and IEOVF Bits in TCSRWD2

When clearing the WT/$\overline{IT}$ or IEOVF bit in timer control/status register WD2 (TCSRWD2) to 0, always use the assembly code shown in figure.12.5

If this code is not used, operation depends on the address where the instruction for clearing is allocated and the writing may not succeed. Specifically, whether the clearing succeeds or not is dependent on the second lowest bit in the address at which the instruction for transfer to TCSRWD2 is allocated. Therefore, make sure that the allocation of the assembly code matches the address offsets shown in figure 12.5.

Address offset	Assembly code

```
+H'0000         MOV.B   #xx,Rn
+H'0002         MOV.B   Rn,@TCSRWD2:8     ; Clear (first time)
+H'0004         MOV.B   @TCSRWD2:8,Rm     ; Read TCSRWD2
+H'0006         AND.B   #yy,Rm            ; Check if the bit has been cleared
+H'0008         BEQ     LABEL:16          ; Jump to LABEL if it is cleared
+H'000C         MOV.B   Rn,@TCSRWD2:8     ; Clear (second time)
+H'000E LABEL:  NOP
```

Bit(s) to be cleared	Value of "xx" in line 1	Value of "yy" in line 4
Both WT/$\overline{IT}$ and IEOVF	H'87	H'28
WT/$\overline{IT}$ only	H'97	H'20
IEOVF only	H'C7	H'08

[Notes]
- Specify the address of TCSRWD2 in 8-bit absolute address, and specify the branching destination for the BEQ instruction in 16-bit absolute address.
- Use different 8-bit general registers as Rn and Rm.
- Do not change or add any instructions, nor the order of instructions in the assembly code above. These changes may unintentionally be made by the compiler and/or linker depending on their option settings. So, always make sure the address offsets.

Figure.12.5 Assembly Code for Clearing Bits WT/$\overline{IT}$ and IEOVF