RENESAS TECHNICAL UPDATE

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Product Category	System LSI			Document No.	TN-RZ*-A0099A/E	Rev.	1.00
Title	Ethernet MAC (GMAC) function issue			Information Category	Technical Notification		
Applicable Product	RZ/N1D Group RZ/N1S Group RZ/N1L Group	Lot No.		Reference Document	RZ/N1D Group RZ/N1S Group RZ/N1L Group User's Manual: R-IN Engine and Ethernet Peripherals Rev.1.30 (R01UH0753EJ0130)		
		All					

We would like to inform about issues regarding Ethernet MAC (GMAC) function as described below.

No.1 to 5 are applicable to both GMAC1 and GMAC2. No.6 is applicable to GMAC1 only.

No.	Issues	Workaround
1	When the Receive FIFO operates in the cut-through mode, the Receive FIFO Read Controller may stop functioning. If this issue happens, software reset is needed to recover functioning.	Operate Receive FIFO in store and forward mode by setting bit 25 (RSF) in operation mode register (Operation_Mode) to 1.
2	Filter i Command in Remote Wake-Up Frame Filter Register (wkupfmfilter_reg[n] n＝0 to 7) is a 4-bit read-write field. When reding it, bit 1 (And_Previous) and bit 2 (INV) always return zero.	Do not use value read from this field. Software should maintain a copy of the value written to this field and use that instead of reading it.
3	Even if bit 3 (CAST) of Filter i Command in Remote Wake-Up Frame Filter Register (wkupfmfilter_reg[n] n＝0 to 7) is set to 0 to process packet with unicast address, if the packet with broadcast address is received, it is also processed to determine whether it is remote wake up packet or not. If CRC matches, it is regarded as remote wake up packet incorrectly.	Use packet with multicast address for remote wake up packet and set CAST to 1. Otherwise, when using packet with unicast address, don't use it which match the condition of packet with broadcast address.
4	When bit 1 (And_Previous) of Filter i Command in Remote Wake-Up Frame Filter Register (wkupfmfilter_reg[n] n＝0 to 7) is used to chain multiple filters, PMT interrupt is generated incorrectly if individual filters match different packets. (For example, the first packet received matches filter 0 only and then the second packet received matches filter 1 only.)	Do not use And_Previous and set it to 0. Otherwise, do not use remote wake up packet which matches defect condition.
5	When LPITXA and LPIEN bits in LPI Control and Status register (LPI_Control_Status) are set to 1, MAC transmitter may enter LPI state prematurely if TX MAC is idle but TX DMA is still active.	Set the LPITXA and LPIEN bits only after ensuring that TX DMA is in IDLE state. When bits[22:20] (TS[2:0]) in the status register (Status) indicate that the TX DMA is in Stopped or Suspend state, the TX DMA is in IDLE.
6	When the Flexible PPS Output feature is used in Pulse Train mode and the Fine Correction method is used for correcting the IEEE 1588 internal time reference due to drift in the frequency of the clock that drives it, flexible PPS Output interval is incorrect.	Use coarse method for correcting the IEEE 1588 internal time reference when the Flexible PPS Output features is used.

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