Date: Apr. 3, 2020

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A0222A/E	Rev.	1.00
Title	Errata to RX72N Group User's Manual: Hardware Rev.1.00		Information Category	Technical Notification		
Applicable Product	RX72N Group	Lot No. All	Reference Document	RX72N Group User's Manual: Hardware Rev.1.00 (R01UH0824EJ0100)		

This document describes corrections to the RX72N Group User's Manual: Hardware Rev.1.00.

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Signals ET1_MDC, ET1_MDIO, ET1_LINKSTA, ET1_EXOUT, and ET1_WOL for ETHERC channel 1 are not listed in Table 1.8, List of Pin and Pin Functions (145-Pin TFLGA) in section 1.5, Pin Assignments. The table is corrected as follows.

After correction

Table 1.8 List of Pin and Pin Functions (145-Pin TFLGA)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer		Communication		Memory I/F Camera I/F	GLCDC	Interrupt	A/D D/A
145-Pin TFLGA				(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, PGMI)	(QSPI, SDHI, MMCIF, PDC)			
Omitted											
A8		PD2	D2[A2/D2]	MTIOC4D/ TIC2	GTIOC0B	MISOC-A/ CRX0	ET1_EXOUT	QIO2-B/ SDHI_D2-B/ MMC_D2-B	LCD_DATA22-B	IRQ2	AN110
Omitted											
B9		PD4	D4[A4/D4]	MTIOC8B/ POE11#		SSLC0-A	ET1_MDIO / PMGI1_MDIO	QSSL-B/ SDHI_CMD-B/ MMC_CMD-B	LCD_DATA20-B	IRQ4	AN112
Omitted											
C8		PD3	D3[A3/D3]	MTIOC8D/ TOC2/POE8#	GTIOC0A	RSPCKC-A	ET1_WOL	QIO3-B/ SDHI_D3-B/ MMC_D3-B	LCD_DATA21-B	IRQ3	AN111
Omitted											
D6		P93	A19	POE0#		CTS7#/ RTS7#/SS7#	ET1_LINKSTA				AN117
D7		PD5	D5[A5/D5]	MTIC5W/ MTIOC8C/ MTCLKA/ POE10#		SSLC1-A	ET1_MDC/ PMGI1_MDC	QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B	LCD_DATA19-B	IRQ5	AN113
Omitted											
J4	TDI	P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#		RXD1/ SMISO1/ SSCL1/ MISOB-A	ET1_MDIO / PMGI1_MDIO			IRQ0-DS	
Omitted											
K1	TCK	P27	CS7#	MTIOC2B/ TMCI3/PO7		SCK1/ RSPCKB-A	ET1_WOL				
K2	TDO	P26	CS6#	MTIOC2A/ TMO1/PO6		TXD1/ SMOSI1/ SSDA1/ CTS3#/ RTS3#/ SS3#/ MOSIB-A	ET1_EXOUT				
K3	TMS	P31		MTIOC4D/ TMCI2/PO9/ RTCIC1		CTS1#/ RTS1#/ SS1#/ SSLB0-A	ET1_MDC/ PMGI1_MDC			IRQ1-DS	
Omitted											

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Signals ET1_MDC, ET1_MDIO, ET1_LINKSTA, ET1_EXOUT, and ET1_WOL for ETHERC channel 1 are not listed in Table 1.9, List of Pin and Pin Functions (145-Pin LFQFP) in section 1.5, Pin Assignments. The table is corrected as follows.

After correction

Table 1.9 List of Pin and Pin Functions (144-Pin LFQFP)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer		Communication		Memory I/F Camera I/F	GLCDC	Interrupt	A/D D/A
144-Pin LFQFP				(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, PGMI)	(QSPI, SDHI, MMCIF, PDC)			
Omitted											
28	TMS	P31		MTIOC4D/ TMCI2/PO9/ RTCIC1		CTS1#/ RTS1#/ SS1#/ SSLB0-A	ET1_MDC/ PMGI1_MDC			IRQ1-DS	
29	TDI	P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#		RXD1/ SMISO1/ SSCL1/ MISOB-A	ET1_MDIO/ PMGI1_MDIO			IRQ0-DS	
30	TCK	P27	CS7#	MTIOC2B/ TMCI3/PO7		SCK1/ RSPCKB-A	ET1_WOL				
31	TDO	P26	CS6#	MTIOC2A/ TMO1/PO6		TXD1/ SMOSI1/ SSDA1/ CTS3#/ RTS3#/ SS3#/ MOSIB-A	ET1_EXOUT				
Omitted											
121		PD5	D5[A5/D5]	MTIC5W/ MTIOC8C/ MTCLKA/ POE10#		SSLC1-A	ET1_MDC/ PMGI1_MDC	QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B	LCD_DATA19-B	IRQ5	AN113
122		PD4	D4[A4/D4]	MTIOC8B/ POE11#		SSLC0-A	ET1_MDIO/ PMGI1_MDIO	QSSL-B/ SDHI_CMD-B/ MMC_CMD-B	LCD_DATA20-B	IRQ4	AN112
123		PD3	D3[A3/D3]	MTIOC8D/ TOC2/POE8#	GTIOC0A	RSPCKC-A	ET1_WOL	QIO3-B/ SDHI_D3-B/ MMC_D3-B	LCD_DATA21-B	IRQ3	AN111
124		PD2	D2[A2/D2]	MTIOC4D/ TIC2	GTIOC0B	MISOC-A/ CRX0	ET1_EXOUT	QIO2-B/ SDHI_D2-B/ MMC_D2-B	LCD_DATA22-B	IRQ2	AN110
Omitted											
127		P93	A19	POE0#		CTS7#/ RTS7#/SS7#	ET1_LINKSTA				AN117
Omitted											

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Signals ET1_MDC, ET1_MDIO, ET1_LINKSTA, ET1_EXOUT, and ET1_WOL for ETHERC channel 1 do not have check marks in the 145-pin and 144-pin column of Table 23.1, Functions Assigned to Each Multiplexed Pin in section 23.1, Overview. The table is corrected and note 2 is deleted as follows.

After correction

Table 23.1 Functions Assigned to Each Multiplexed Pin

Module/Function	Channel	Pin Functions	Allocation Port	Package			
				224-pin	176-pin	145-pin 144-pin	100-pin
Omitted							
Ethernet controller	MII1~~*2~~	Omitted					
		ET1_EXOUT (output)	P26	✓	✓	✓	×
			PD2	✓	✓	✓	×
		ET1_LINKSTA (input)	P84	✓	✓	×	×
			P93	✓	✓	✓	×
		Omitted					
		ET1_WOL (output)	P27	✓	✓	✓	×
			PD3	✓	✓	✓	×
		ET1_MDC (output)	P31	✓	✓	✓	×
			PD5	✓	✓	✓	×
			PN5	✓	×	×	×
		ET1_MDIO (input/output)	P30	✓	✓	✓	×
			PD4	✓	✓	✓	×
			PN4	✓	×	×	×
Omitted							

Note 1. To use this pin function, set the corresponding pin as general input (set the PORTm.PDR.Bn and PORTm.PMR.Bn bits to 0).
~~Note 2. This setting is only supported by 224- and 176-pin products.~~

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The note for signals ET1_EXOUT and ET1_WOL of ETHERC channel 1 in Table 23.6, Register Settings for Input/Output Pin Function in 224-/176-Pin LFBGA, 176-/144-/100-Pin LFQFP, 145-Pin TFLGA of section 23.2.4, P2n Pin Function Control Register (P2nPFS) (n = 0 to 7) is corrected as follows. Note 2 is deleted because the correction makes it unnecessary.

Before correction

Table 23.6 Register Settings for Input/Output Pin Function in 224-/176-Pin LFBGA, 176-/144-/100-Pin LFQFP, 145-Pin TFLGA

	Pin							
PSEL[5:0] Settings	P20	P21	P22	P23	P24	P25	P26	P27
				Omitted				
010100b	—	—	—	—	—	—	ET1_EXOUT *2	ET1_WOL *2
				Omitted				

—: Do not specify this value.
Note 1. This setting is not supported by 100-pin products.
Note 2. This setting is not supported by 145-/144-/100-pin products.

After correction

Table 23.6 Register Settings for Input/Output Pin Functions in 224-/176-Pin LFBGA, 176-/144-/100-Pin LFQFP, and 145-Pin TFLGA

	Pin							
PSEL[5:0] Settings	P20	P21	P22	P23	P24	P25	P26	P27
				Omitted				
010100b	—	—	—	—	—	—	ET1_EXOUT *1	ET1_WOL *1
				Omitted				

—: Do not specify this value.
Note 1. This setting is not supported by 100-pin products.

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The note for signals ET1_MDC and ET1_MDIO of ETHERC channel 1 in Table 23.7, Register Settings for Input/Output Pin Function in 224-/176-Pin LFBGA, 176-/144-/100-Pin LFQFP, 145-Pin TFLGA of section 23.2.5, P3n Pin Function Control Register (P3nPFS) (n = 0 to 4) is corrected as follows. Note 2 is deleted because the correction makes it the same as note 1.

Before correction

Table 23.7 Register Settings for Input/Output Pin Function in 224-/176-Pin LFBGA, 176-/144-/100-Pin LFQFP, 145-Pin TFLGA

	Pin				
PSEL[5:0] Settings	P30	P31	P32	P33	P34
Omitted					
010100b	ET1_MDIO*1	ET1_MDC*1	—	—	—
011000b	—	—	—	EDREQ1	—
011100b	—	—	VSYNC*2	PCKO*2	—
100001b	—	—	POE10#	POE11#	—
101000b	PMGI1_MDIO*2	PMGI1_MDC*2	—	—	—

—: Do not specify this value.
Note 1. This setting is not supported by 145-/144-/100-pin products.
Note 2. This setting is not supported by 100-pin products.

After correction

Table 23.7 Register Settings for Input/Output Pin Functions in 224-/176-Pin LFBGA, 176-/144-/100-Pin LFQFP, and 145-Pin TFLGA

	Pin				
PSEL[5:0] Settings	P30	P31	P32	P33	P34
Omitted					
010100b	ET1_MDIO*1	ET1_MDC*1	—	—	—
011000b	—	—	—	EDREQ1	—
011100b	—	—	VSYNC*1	PCKO*1	—
100001b	—	—	POE10#	POE11#	—
101000b	PMGI1_MDIO*1	PMGI1_MDC*1	—	—	—

—: Do not specify this value.
Note 1. This setting is not supported by 100-pin products.

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The ET1_LINKSTA signal of ETHERC channel 1 is added to Table 23.16, Register Settings for Input/Output Pin Function in 145-Pin TFLGA, 144-Pin LFQFP of section 23.2.11, P9n Pin Function Control Register (P9nPFS) (n = 0 to 7) as follows.

After correction

Table 23.16 Register Settings for Input/Output Pin Functions in145-Pin TFLGA and 144-Pin LFQFP

	Pin			
PSEL[5:0] Settings	**P90**	**P91**	**P92**	**P93**
000000b (initial value)	Hi-Z			
001000b	—	—	POE4#	POE0#
001010b	TXD7 SMOSI7 SSDA7	SCK7	RXD7 SMISO7 SSCL7	—
001011b	—	—	—	CTS7# RTS7# SS7#
010100b	—	—	—	ET1_LINKSTA
010101b	—	—	RMII1_CRS_DV	—

—: Do not specify this value.

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The notes for signals ET1_MDC, ET1_MDIO, ET1_EXOUT, and ET1_WOL of ETHERC channel 1 in Table 23.20, Register Settings for Input/Output Pin Function in 224-/176-Pin LFBGA, 176-/144-/100-Pin LFQFP, 145-Pin TFLGA of section 23.2.15, PDn Pin Function Control Register (PDnPFS) (n = 0 to 7) are corrected as follows.

Before correction

Table 23.20 Register Settings for Input/Output Pin Function in 224-/176-Pin LFBGA, 176-/144-/100-Pin LFQFP, 145-Pin TFLGA

	Pin							
PSEL[5:0] Settings	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7
Omitted								
010100b	—	—	ET1_EXOUT *1	ET1_WOL *1	ET1_MDIO*1	ET1_MDC *1	ET1_RX_CLK*1	ET1_RX_ER *1
Omitted								

—: Do not specify this value.
Note 1. This setting is not supported by 145-/144-/100-pin products.
Note 2. This setting is not supported by 100-pin products.

After correction

Table 23.20 Register Settings for Input/Output Pin Functions in 224-/176-Pin LFBGA, 176-/144-/100-Pin LFQFP, and 145-Pin TFLGA

	Pin							
PSEL[5:0] Settings	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7
Omitted								
010100b	—	—	ET1_EXOUT *2	ET1_WOL *2	ET1_MDIO*2	ET1_MDC *2	ET1_RX_CLK*1	ET1_RX_ER *1
Omitted								

—: Do not specify this value.
Note 1. This setting is not supported by 145-/144-/100-pin products.
Note 2. This setting is not supported by 100-pin products.

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The equations in note 3 of Table 63.6, DC Characteristics (3) in section 63.3, DC Characteristics are corrected as follows.

Before correction

Note 3. I_{CC} depends on the f (ICLK) as follows.
(when ICLK : PCLKA : PCLKB/PCLKC/PCLKD : BCLK : BCLK pin = 4 : 2 : 1 : 2 : 1 and EXTAL = 12 MHz)

- D version
  I_{CC} max. = 0.77 × f + 74 (full operation in high-speed operating mode)
  I_{CC} typ. = 0.22 × f + 7 (normal operation in high-speed operating mode)
  I_{CC} typ. = 0.50 × f + 3.7 (ICLK 1 MHz max) (low-speed operating mode 1)
  I_{CC} max. = 0.29 × f + 74 (sleep mode)
- G version
  I_{CC} max. = 0.89 × f + 105 (full operation in high-speed operating mode)
  I_{CC} typ. = 0.22 × f + 7 (normal operation in high-speed operating mode)
  I_{CC} typ. = 0.50 × f + 3.7 (ICLK 1 MHz max) (low-speed operating mode 1)
  I_{CC} max. = 0.37 × f + 105 (sleep mode)

After correction

Note 4. I_{CC} depends on the f (ICLK) as follows.
(when ICLK : PCLKA : PCLKB/PCLKC/PCLKD : BCLK : BCLK pin = 4 : 2 : 1 : 2 : 1 and EXTAL = 12 MHz)

- D version
  I_{CC} max. = 0.62 × f + 113 (full operation in high-speed operating mode)
  I_{CC} typ. = 0.22 × f + 7 (normal operation in high-speed operating mode)
  I_{CC} typ. = 0.50 × f + 3.7 (ICLK 1 MHz max) (low-speed operating mode 1)
  I_{CC} max. = 0.13 × f + 113 (sleep mode)
- G version
  I_{CC} max. = 0.65 × f + 164 (full operation in high-speed operating mode)
  I_{CC} typ. = 0.22 × f + 7 (normal operation in high-speed operating mode)
  I_{CC} typ. = 0.50 × f + 3.7 (ICLK 1 MHz max) (low-speed operating mode 1)
  I_{CC} max. = 0.13 × f + 164 (sleep mode)