Date: Apr. 5, 2018

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RX*-A184A/E	Rev.	1.00
Title	Corrections to Descriptions for the P/E Suspend Command of Flash Memory in RX610 Group		Information Category	Technical Notification		
Applicable Product	RX610 Group	Lot No. All	Reference Document	RX610 Group User's Manual: Hardware Rev.1.20 (R01UH0032EJ0120)		

This document describes corrections to the descriptions for the SUSRDY bit and the flow chart of the P/E suspend command in the "ROM (Flash Memory for Code Storage)" section of RX610 Group User's Manual: Hardware.

• Page 826 of 1003

Clearing conditions of the SUSRDY bit in section 26.2.5, Flash Status Register 0 (FSTATR0) are corrected as follows.

Before Correction

[Clearing conditions]

- The FCU has accepted a P/E suspend command.
- During programming/erasure process, the FCU enters the command-locked state.

After Correction

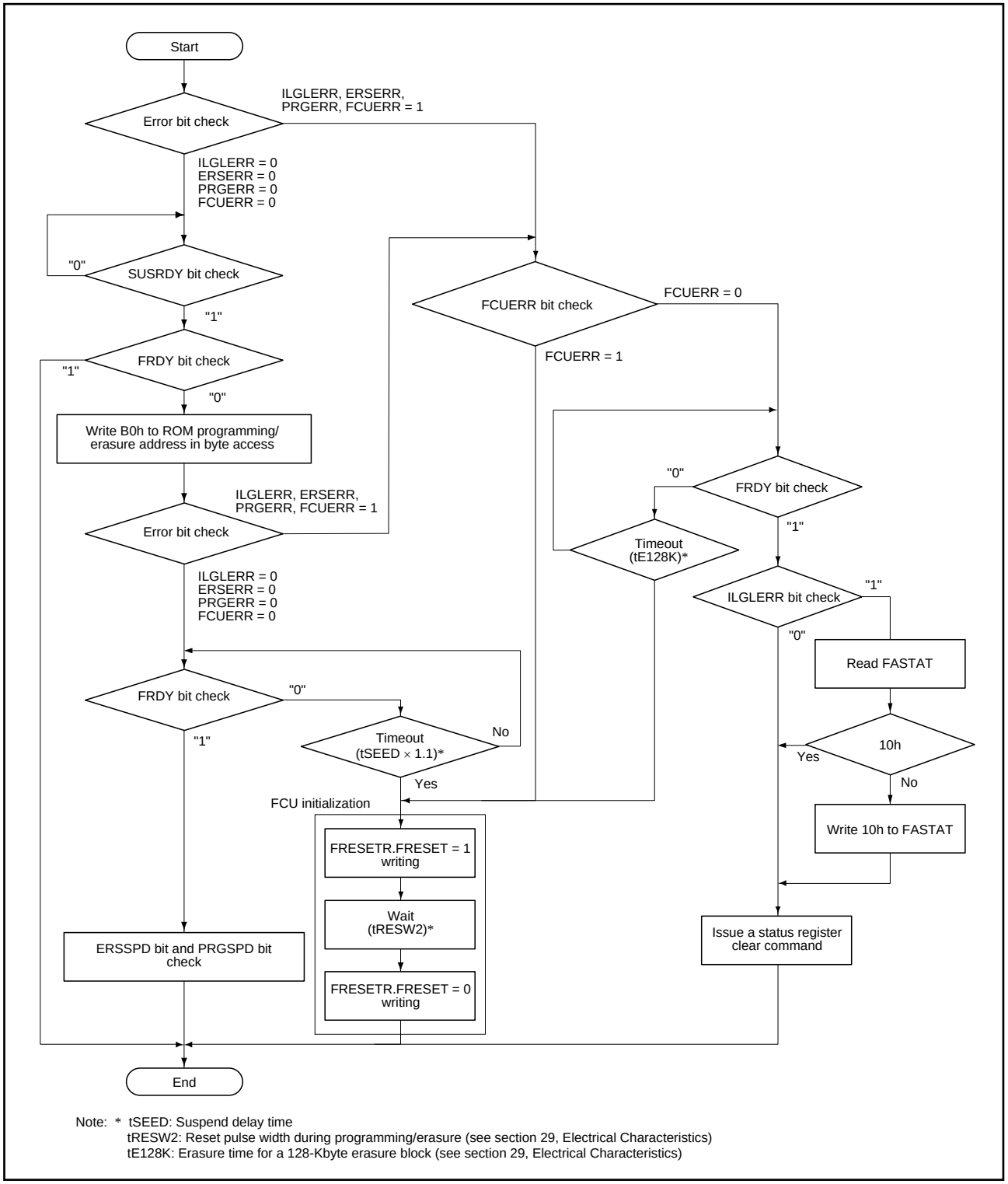
[Clearing conditions]

- The FCU has accepted a P/E suspend command.
- During programming/erasure process, the FCU enters the command-locked state.
- When programming/erasure process has been completed.

• Page 864 of 1003

In Figure 26.19, Procedure for Programming/Erasure Suspension, a processing flow never escapes from the loop for a checking procedure if the programming/erasure processing completed before checking the SUSRDY bit.
Therefore, a timeout processing and a breaking processing when the FRDY bit is 1 are to be added.

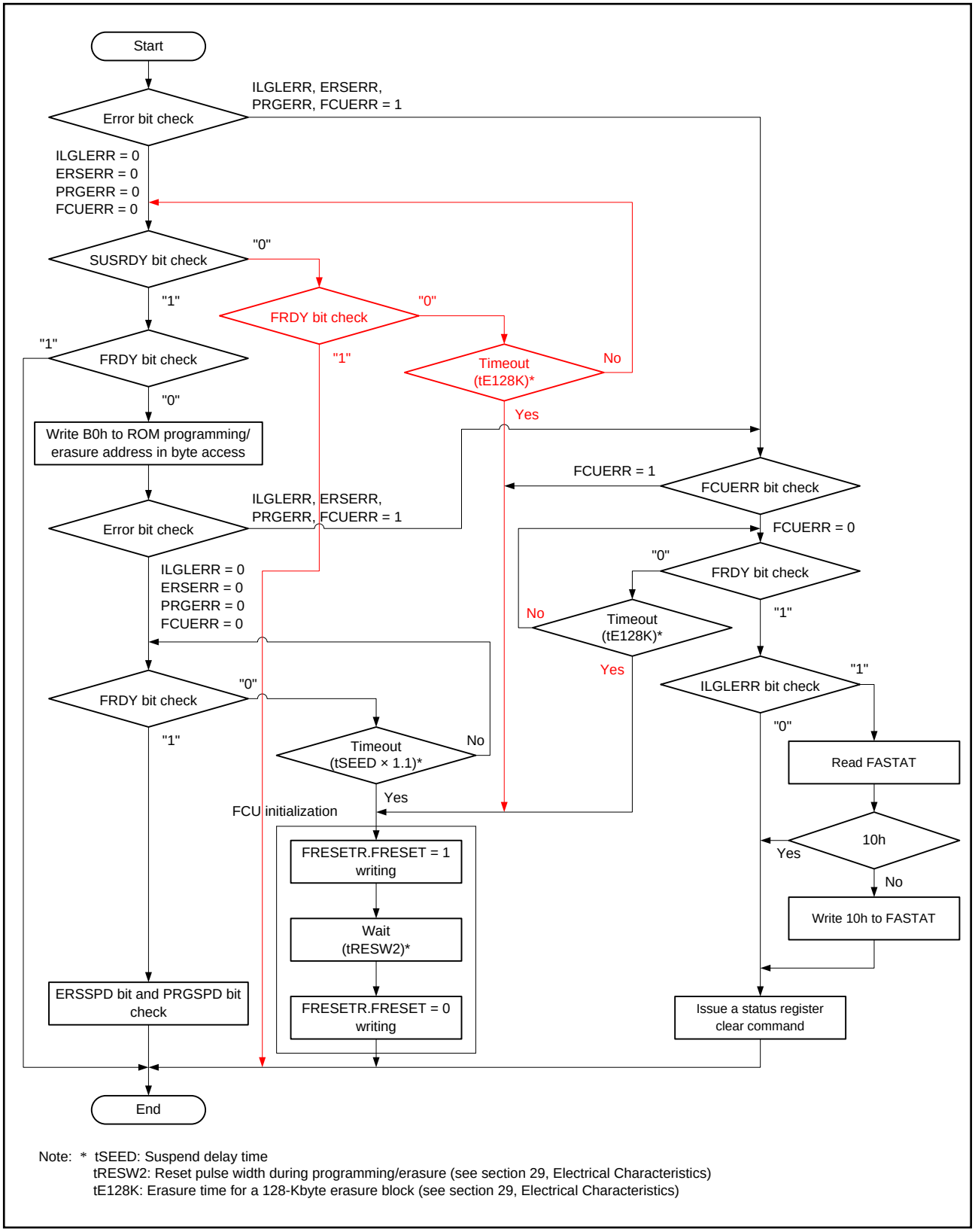
Before correction



Note: * tSEED: Suspend delay time
tRESW2: Reset pulse width during programming/erasure (see section 29, Electrical Characteristics)
tE128K: Erasure time for a 128-Kbyte erasure block (see section 29, Electrical Characteristics)

Figure 26.19 Procedure for Programming/Erasure Suspension

After correction



Note: * tSEED: Suspend delay time
tRESW2: Reset pulse width during programming/erasure (see section 29, Electrical Characteristics)
tE128K: Erasure time for a 128-Kbyte erasure block (see section 29, Electrical Characteristics)

Figure 26.19 Procedure for Programming/Erasure Suspension

End of document