

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A031C/E	Rev.	4.00
Title	Correction for Incorrect Description Notice RL78/L13 Descriptions in the User's Manual: Hardware Rev. 2.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/L13 Group	Lot No.	Reference Document	RL78/L13 User's Manual: Hardware Rev. 2.00 R01UH0382EJ0200 (Dec. 2013)		
		All lots				

This document describes misstatements found in the RL78/L13 User's Manual: Hardware Rev. 2.00 (R01UH0382EJ0200).

Corrections

Applicable Item	Applicable Page	Contents
2.1.1 64-pin products	p.15	Incorrect descriptions revised
2.1.2 80-pin products	p.19	Incorrect descriptions revised
2.4 Block Diagrams of Pins Figure 2-5. Pin Block Diagram for Pin Type 7-1-3	p.30	Incorrect descriptions revised / Caution added
2.4 Block Diagrams of Pins Figure 2-9. Pin Block Diagram for Pin Type 7-5-10	p.34	Caution added
2.4 Block Diagrams of Pins Figure 2-11. Pin Block Diagram for Pin Type 7-6-4	p.36	Caution added
2.4 Block Diagrams of Pins Figure 2-14. Pin Block Diagram for Pin Type 8-5-4	p.39	Caution added
2.4 Block Diagrams of Pins Figure 2-15. Pin Block Diagram for Pin Type 8-5-10	p.40	Caution added
2.4 Block Diagrams of Pins Figure 2-16. Pin Block Diagram for Pin Type 8-6-4	p.41	Caution added

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.				Pages in this document for corrections
	Document No.	English	R01UH0382EJ0200	
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13	33.3.1 Pin characteristics			Pages 19 and 20
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24	2.4 Block Diagrams of Pins Figure 2-16. Pin Block Diagram for Pin Type 8-6-4			Page 31

~~Incorrect: Old: Bold with underline; Correct, New: Gray hatched~~

Revision History

RL78/L13 Correction for incorrect description notice

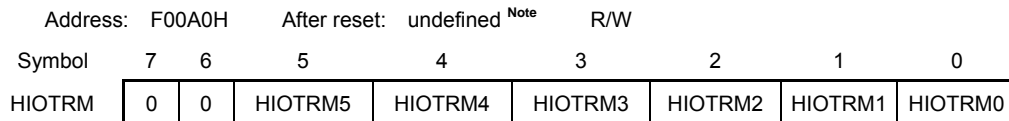
Document Number	Issue Date	Description
TN-RL*-A029A/E	Jun. 27, 2014	First edition issued Corrections No.1 to No.10 revised
TN-RL*-A031A/E	Aug 18, 2014	Second edition issued Correction No.11 to 13revised
TN-RL*-A046A/E	Jul. 6 , 2015	Correction No.15 revised
TN-RL*-A031B/E	July 31, 2015	Third edition issued Correction No.16 revised
TN-RL*-A031C/E	Feb. 22, 2016	Fourth edition issued Correction No.17 to 18 revised(this document)

1. **5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)**
(Page 243)

Incorrect:

5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)
 (omitted)

Figure 5-10. Format of High-Speed On-Chip Oscillator Trimming Register (HIOTRM)



HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0	High-speed on-chip oscillator
0	0	0	0	0	0	Minimum speed
0	0	0	0	0	1	↑
0	0	0	0	1	0	
0	0	0	0	1	1	
0	0	0	1	0	0	
• • •						
1	1	1	1	1	0	↓
1	1	1	1	1	1	

Note The value after reset is the value adjusted at shipment.

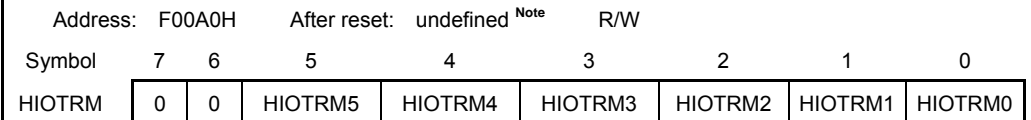
Remarks 1 ~~The HIOTRM register can be used to adjust the high-speed on-chip oscillator clock to an accuracy within about 0.05%.~~

2. For the usage example of the HIOTRM register, see the application note for RL78 MCU series High-speed On-chip Oscillator (HOCO) Clock Frequency Correction (R01AN0464).

Correct:

5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)
 (omitted)

Figure 5-10. Format of High-Speed On-Chip Oscillator Trimming Register (HIOTRM)



HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0	High-speed on-chip oscillator
0	0	0	0	0	0	Minimum speed
0	0	0	0	0	1	↑
0	0	0	0	1	0	
0	0	0	0	1	1	
0	0	0	1	0	0	
• • •						
1	1	1	1	1	0	↓
1	1	1	1	1	1	

Note The value after reset is the value adjusted at shipment.

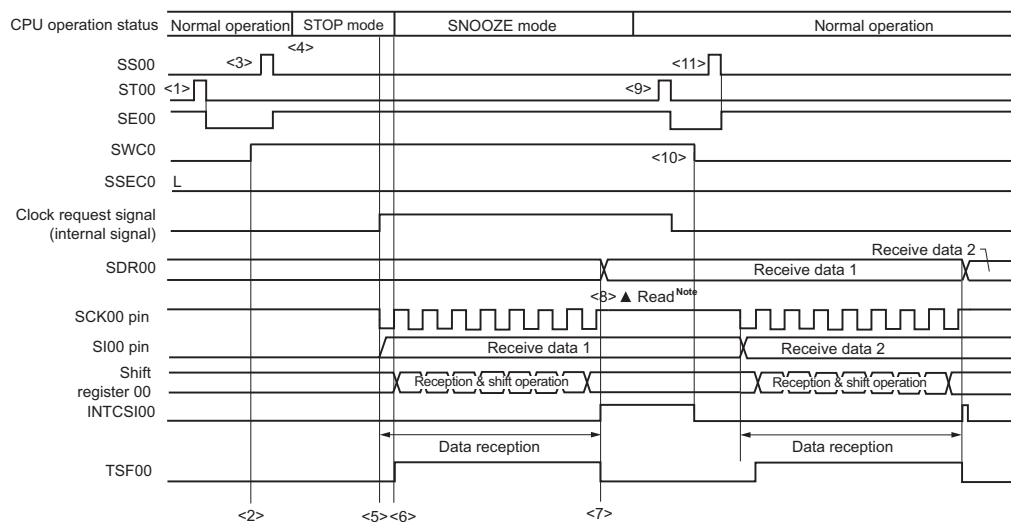
Remarks 1 The HIOTRM register holds a six-bit value used to adjust the high-speed on-chip oscillator with an increment of 1 corresponding to an increase of frequency by about 0.05%.

2. For the usage example of the HIOTRM register, see the application note for RL78 MCU series High-speed On-chip Oscillator (HOCO) Clock Frequency Correction (R01AN0464).

2. **14.5.7 SNOOZE mode function**
Timing Chart of SNOOZE Mode Operation (Figure 14-71. and Figure 14-73.) (Pages 592 and 594)

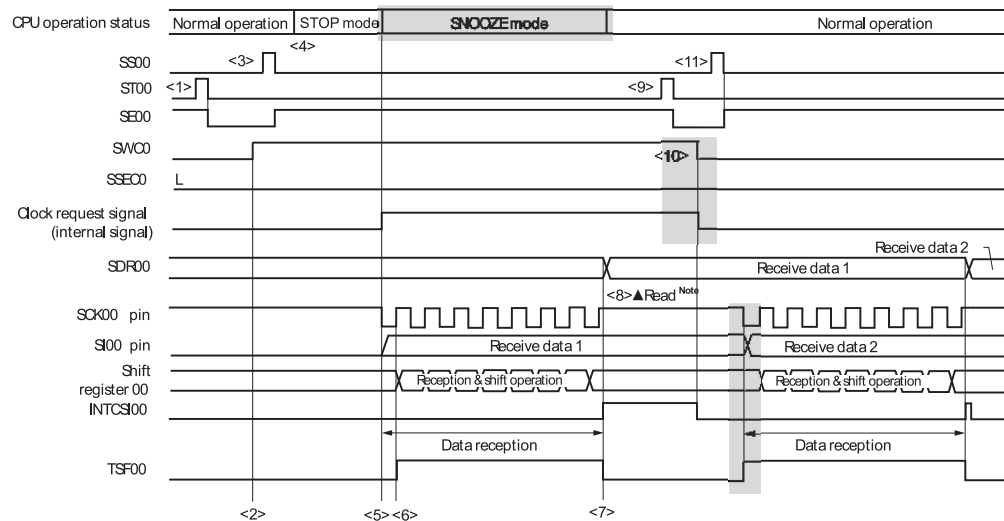
It is correction of “CPU operation status”, “Clock request signal (internal signal)” and “TSF00” in this Figure.

Incorrect:
Figure 14-71. Timing Chart of SNOOZE Mode Operation (once startup)
(Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

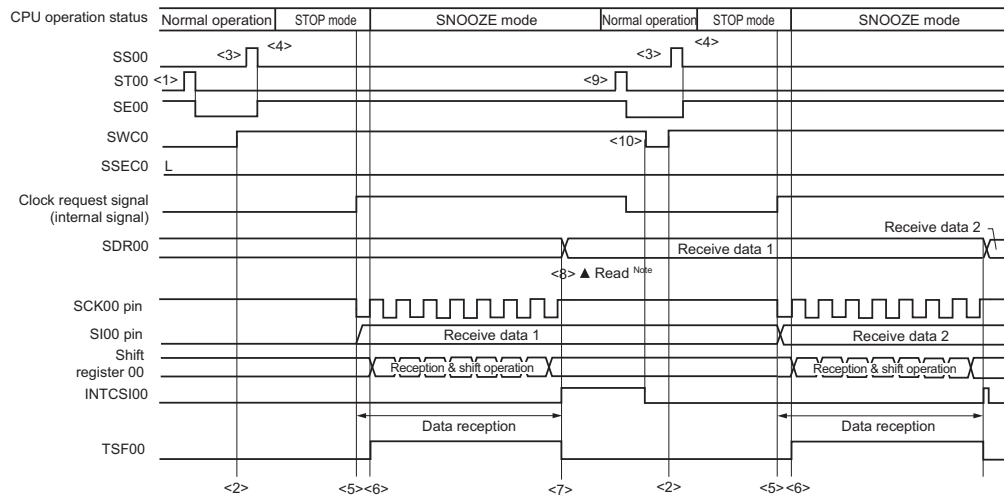
Correct:
Figure 14-71. Timing Chart of SNOOZE Mode Operation (once startup)
(Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

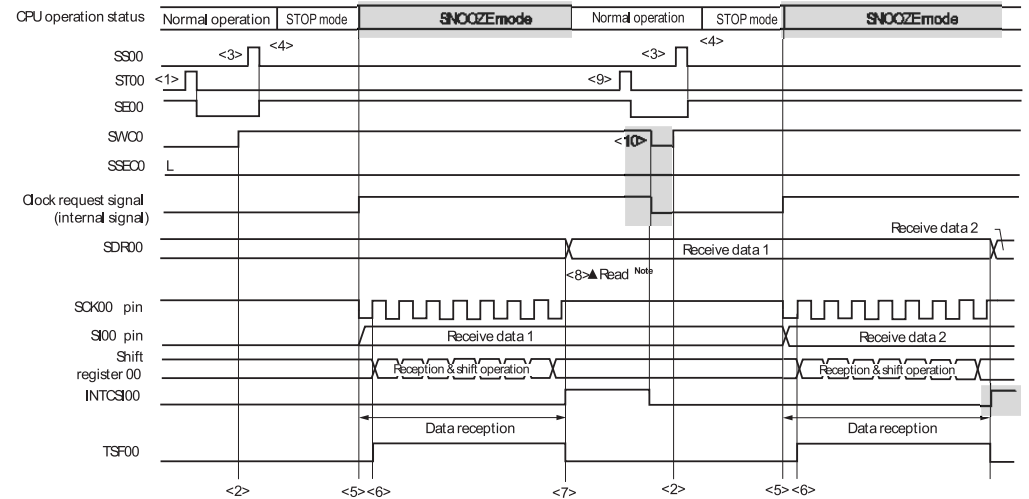
It is correction of “CPU operation status”, “Clock request signal (internal signal)” and “INTCSI00” in this Figure.

Incorrect:
Figure 14-73. Timing Chart of SNOOZE Mode Operation (continuous startup)
 (Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

Correct:
Figure 14-73. Timing Chart of SNOOZE Mode Operation (continuous startup)
 (Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

3. 14.6.3 SNOOZE mode function (Page 618)

Incorrect:

14.6.3 SNOOZE mode function

The SNOOZE mode makes the UART perform reception operations upon RxDq pin input detection while in the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation.

(omitted)

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK} .

(omitted)

4. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFmn, FEFmn, or OVFmn flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFmn, FEFmn, or OVFmn flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxDq register) of the SDRm1 register.

Correct:

14.6.3 SNOOZE mode function

The SNOOZE mode makes the UART perform reception operations upon RxDq pin input detection while in the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation.

(omitted)

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK} .

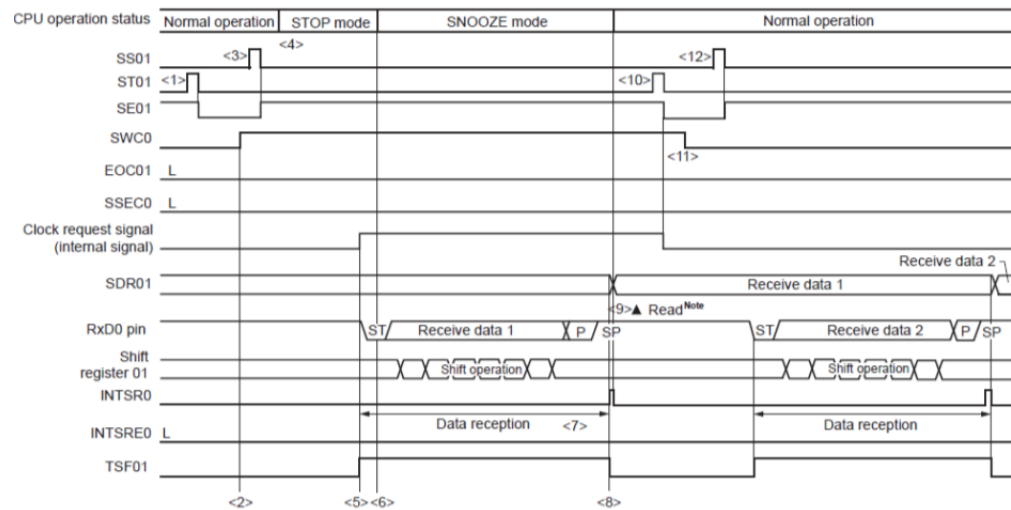
(omitted)

4. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFmn, FEFmn, or OVFmn flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFmn, FEFmn, or OVFmn flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxDq register) of the SDRm1 register.
5. The CPU shifts from the STOP mode to the SNOOZE mode on detecting the valid edge of the RxDq signal. Note, however, that transfer through the UART channel may not start and the CPU may remain in the SNOOZE mode if an input pulse on the RxDq pin is too short to be detected as a start bit. In such cases, data may not be received correctly, and this may lead to a framing error or parity error in the next UART transfer.

4. **14.6.3 SNOOZE mode function**
Timing Chart of SNOOZE Mode Operation (Figure 14-90., Figure 14-91. and Figure 14-93.) (Pages 620, 621 and 623)

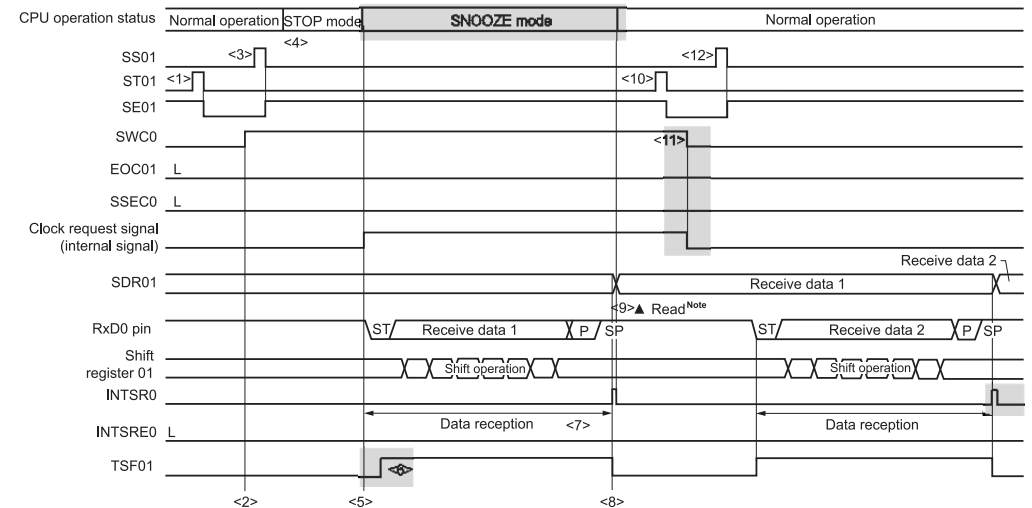
It is correction of “CPU operation status”, “Clock request signal (internal signal)”, “INTSR0” and “TSF01” in this Figure.

Incorrect:
Figure 14-90. Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECM = 0/1)



(omitted)

Correct:
Figure 14-90. Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECM = 0/1)

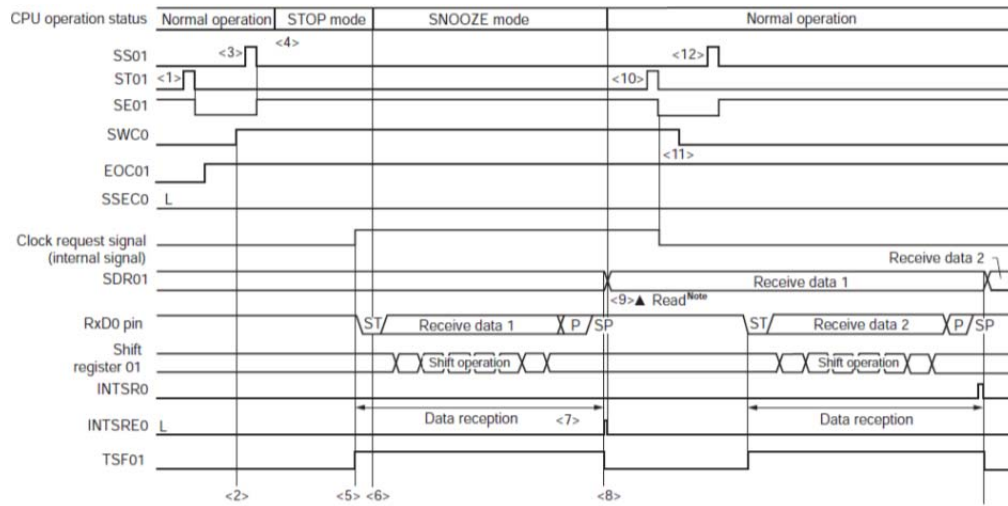


(omitted)

It is correction of “CPU operation status”, “Clock request signal (internal signal)”, “INTSR0” and “TSF01” in this Figure.

Incorrect:

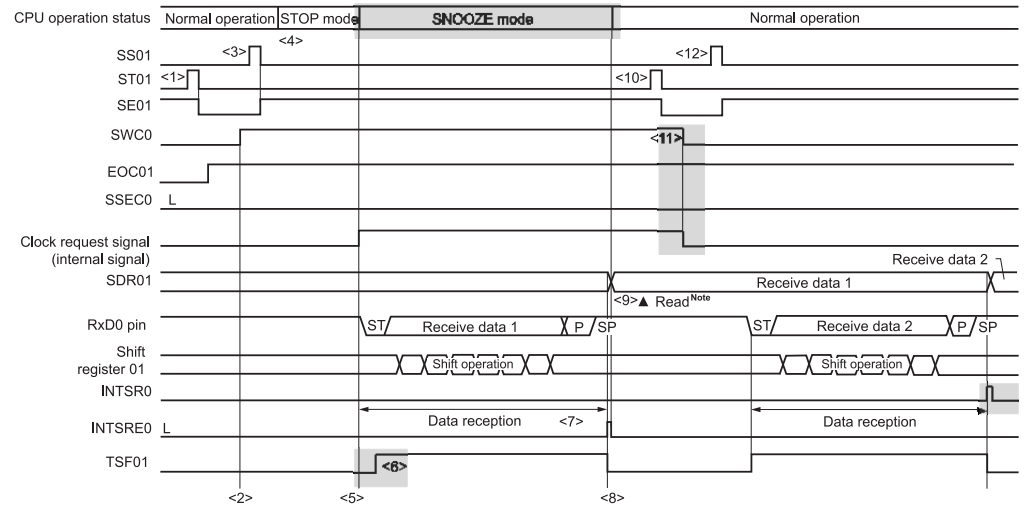
Figure 14-91. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 0)



(omitted)

Correct:

Figure 14-91. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 0)

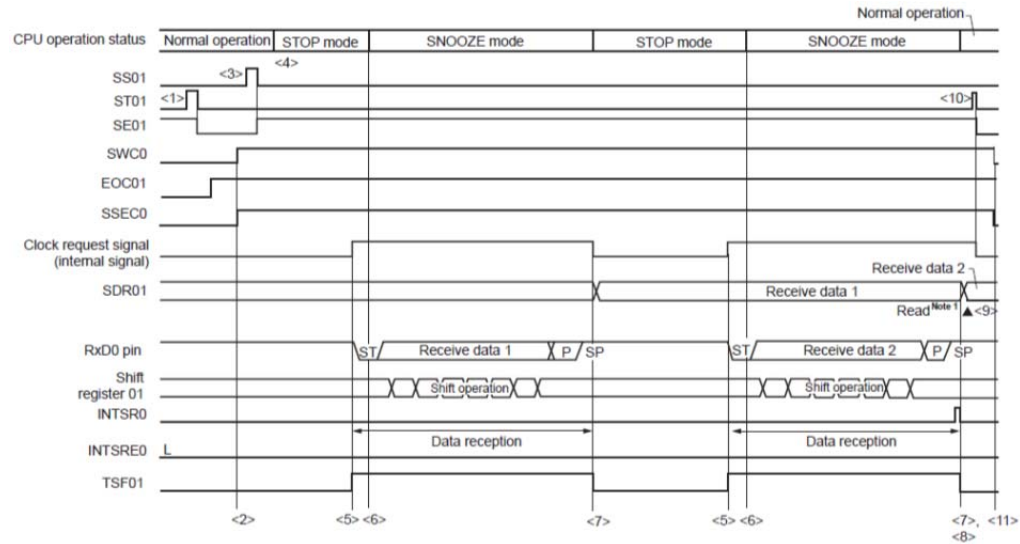


(omitted)

It is correction of “CPU operation status”, “Clock request signal (internal signal)”, “INTSR0” and “TSF01” in this Figure.

Incorrect:

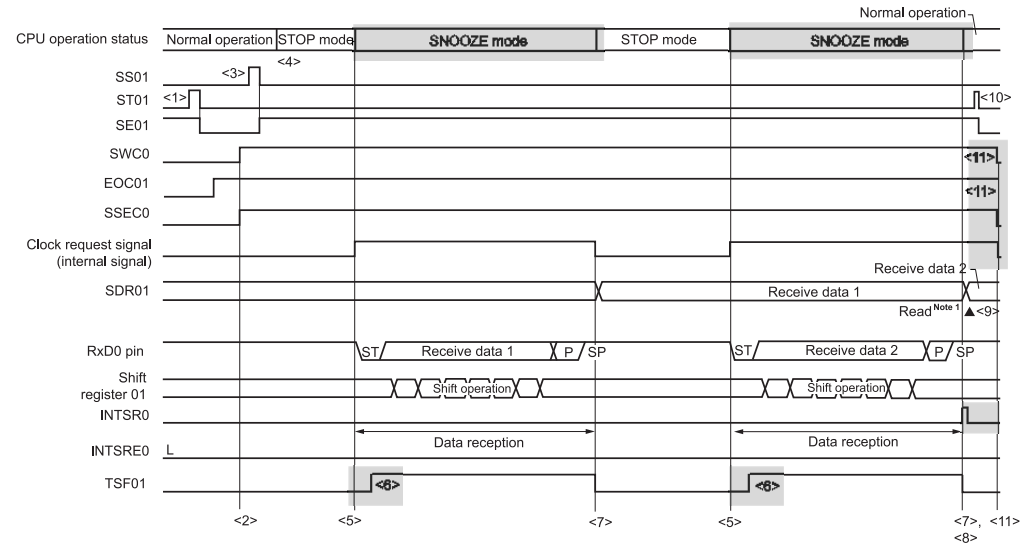
Figure 14-93. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1)



(omitted)

Correct:

Figure 14-93. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1)



(omitted)

5. **19.4.3 Multiple interrupt servicing**

Table 19-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing (Page 864)

Incorrect:

Table 19-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing

Multiple Interrupt Request Interrupt Being Serviced		Maskable Interrupt Request								Software Interrupt Request
		Priority Level 0 (PR = 00)		Priority Level 1 (PR = 01)		Priority Level 2 (PR = 10)		Priority Level 3 (PR = 11)		
		IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	
Maskable interrupt	ISP1 = 0 ISP0 = 0	○	×	×	×	×	×	×	×	○
	ISP1 = 0 ISP0 = 1	○	×	○	×	×	×	×	×	○
	ISP1 = 1 ISP0 = 0	○	×	○	×	○	×	×	×	○
	ISP1 = 1 ISP0 = 1	○	○	○	○	○	○	○	○	○
Software interrupt		○	×	○	×	○	×	○	×	○

(omitted)

Correct:

Table 19-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing

Multiple Interrupt Request Interrupt Being Serviced		Maskable Interrupt Request								Software Interrupt Request
		Priority Level 0 (PR = 00)		Priority Level 1 (PR = 01)		Priority Level 2 (PR = 10)		Priority Level 3 (PR = 11)		
		IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	
Maskable interrupt	ISP1 = 0 ISP0 = 0	○	×	×	×	×	×	×	×	○
	ISP1 = 0 ISP0 = 1	○	×	○	×	×	×	×	×	○
	ISP1 = 1 ISP0 = 0	○	×	○	×	○	×	×	×	○
	ISP1 = 1 ISP0 = 1	○	×	○	×	○	×	○	×	○
Software interrupt		○	×	○	×	○	×	○	×	○

(omitted)

6. **23.2 Configuration of Power-on-reset Circuit**
Figure 23-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1) (Page 900)

Incorrect:

Figure 23-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1/3)

(1) When the externally input reset signal on the $\overline{\text{RESET}}$ pin is used

(omitted)

Notes 3. ~~The time until normal operation starts includes the following reset processing time when the external reset is released (after the first release of POR) after the $\overline{\text{RESET}}$ signal is driven high (1) as well as the voltage stabilization wait time after VPOR (1.51 V, typ.) is reached.~~

~~Reset processing time when the external reset is released is shown below.~~

~~After the first release of POR:~~

~~0.672 ms (typ.), 0.832 ms (max.) (when the LVD is in use)~~

~~0.399 ms (typ.), 0.519 ms (max.) (when the LVD is off)~~

~~4. Reset processing time when the external reset is released after the second release of POR is shown below.~~

~~After the second release of POR:~~

~~0.531 ms (typ.), 0.675 ms (max.) (when the LVD is in use)~~

~~0.259 ms (typ.), 0.362 ms (max.) (when the LVD is off)~~

~~(omitted)~~

Correct:

Figure 23-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1/3)

(1) When the externally input reset signal on the $\overline{\text{RESET}}$ pin is used

(omitted)

Notes 3. The time until normal operation starts includes the following reset processing time when the external reset is released (release from the first external reset following release from the POR state) after the $\overline{\text{RESET}}$ signal is driven high (1) as well as the voltage stabilization wait time after VPOR (1.51 V, typ.) is reached.

Reset processing time when the external reset is released is shown below.

Release from the first external reset following release from the POR state:

0.672 ms (typ.), 0.832 ms (max.) (when the LVD is in use)

0.399 ms (typ.), 0.519 ms (max.) (when the LVD is off)

4. Reset times in cases of release from an external reset other than the above are listed below.

Release from the reset state for external resets other than the above case:

0.531 ms (typ.), 0.675 ms (max.) (when the LVD is in use)

0.259 ms (typ.), 0.362 ms (max.) (when the LVD is off)

(omitted)

7. 32.1 Absolute Maximum Ratings
(Page 1001)

Incorrect:
Absolute Maximum Ratings (3/3)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I _{OH1}	Per pin	P00 to P07, P14 to P17 , P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	-40	mA
		Total of all pins -170 mA	P00 to P07, P14 to P17 , P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	-170	mA
	I _{OH2}	Per pin	P10 to P13, P20 to P27	-0.5	mA
		Total of all pins		-2	mA
Output current, low	I _{OL1}	Per pin	P00 to P07, P14 to P17 , P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	40	mA
		Total of all pins 170 mA	P40 to P47, P130	70	mA
			P00 to P07, P14 to P17 , P30 to P35, P50 to P57, P60, P61, P70 to P77, P125 to P127	100	mA
	I _{OL2}	Per pin	P10 to P13, P20 to P27	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T _A	In normal operation mode		-40 to +85	°C
		In flash memory programming mode			
Storage temperature	T _{stg}			-65 to +150	°C

Correct:
Absolute Maximum Ratings (3/3)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I _{OH1}	Per pin	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	-40	mA
		Total of all pins -170 mA	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	-170	mA
	I _{OH2}	Per pin	P20, P21	-0.5	mA
		Total of all pins		-1	mA
Output current, low	I _{OL1}	Per pin	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	40	mA
		Total of all pins 170 mA	P40 to P47, P130	70	mA
			P00 to P07, P10 to P17, P22 to P27, P30 to P35, P50 to P57, P60, P61, P70 to P77, P125 to P127	100	mA
	I _{OL2}	Per pin	P20, P21	1	mA
		Total of all pins		2	mA
Operating ambient temperature	T _A	In normal operation mode		-40 to +85	°C
		In flash memory programming mode			
Storage temperature	T _{stg}			-65 to +150	°C

8. 32.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (Page 1056)

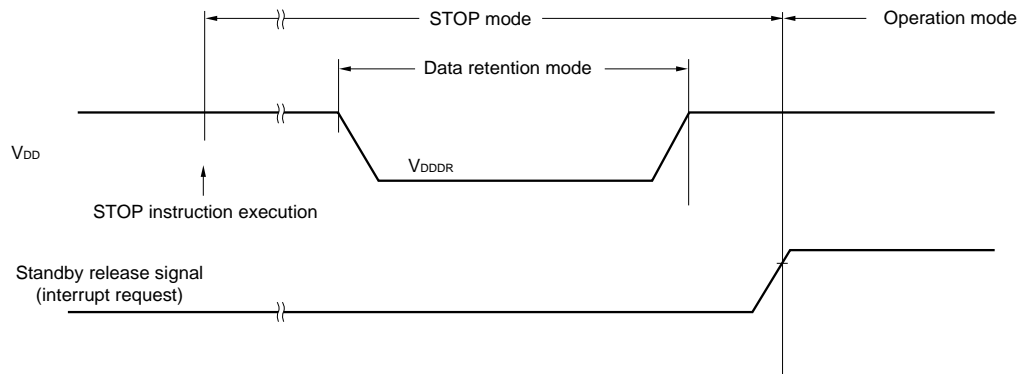
Old:

32.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 ^{Note}		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



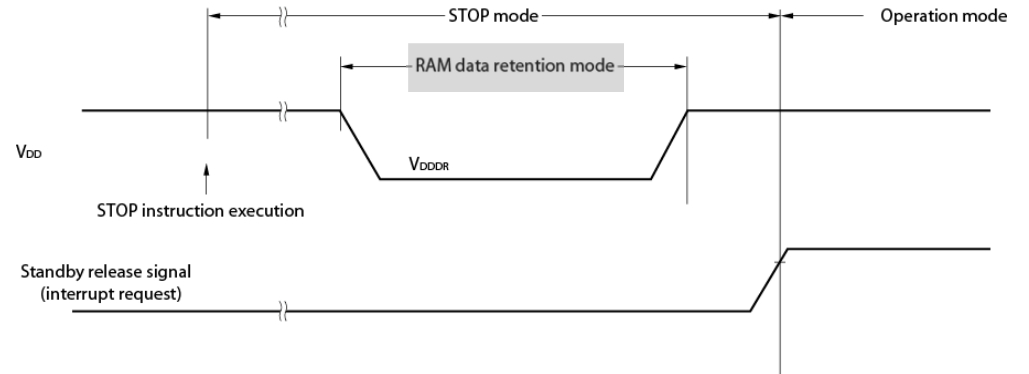
New:

32.8 RAM Data Retention Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 ^{Note}		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



9. 33.1 Absolute Maximum Ratings
(Page 1065)

Incorrect:
Absolute Maximum Ratings (3/3)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I _{OH1}	Per pin	P00 to P07, P14 to P17 , P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	-40	mA
		Total of all pins -170 mA	P00 to P07, P14 to P17 , P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	-170	mA
	I _{OH2}	Per pin	P10 to P13, P20 to P27	-0.5	mA
		Total of all pins		-2	mA
Output current, low	I _{OL1}	Per pin	P00 to P07, P14 to P17 , P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	40	mA
		Total of all pins 170 mA	P40 to P47, P130	70	mA
			P00 to P07, P14 to P17 , P30 to P35, P50 to P57, P60, P61, P70 to P77, P125 to P127	100	mA
	I _{OL2}	Per pin	P10 to P13, P20 to P27	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T _A	In normal operation mode		-40 to +105	°C
		In flash memory programming mode			
Storage temperature	T _{stg}			-65 to +150	°C

Correct:
Absolute Maximum Ratings (3/3)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I _{OH1}	Per pin	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	-40	mA
		Total of all pins -170 mA	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	-170	mA
	I _{OH2}	Per pin	P20, P21	-0.5	mA
		Total of all pins		-1	mA
Output current, low	I _{OL1}	Per pin	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	40	mA
		Total of all pins 170 mA	P40 to P47, P130	70	mA
			P00 to P07, P10 to P17, P22 to P27, P30 to P35, P50 to P57, P60, P61, P70 to P77, P125 to P127	100	mA
	I _{OL2}	Per pin	P20, P21	1	mA
		Total of all pins		2	mA
Operating ambient temperature	T _A	In normal operation mode		-40 to +105	°C
		In flash memory programming mode			
Storage temperature	T _{stg}			-65 to +150	°C

10. 33.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (Page 1114)

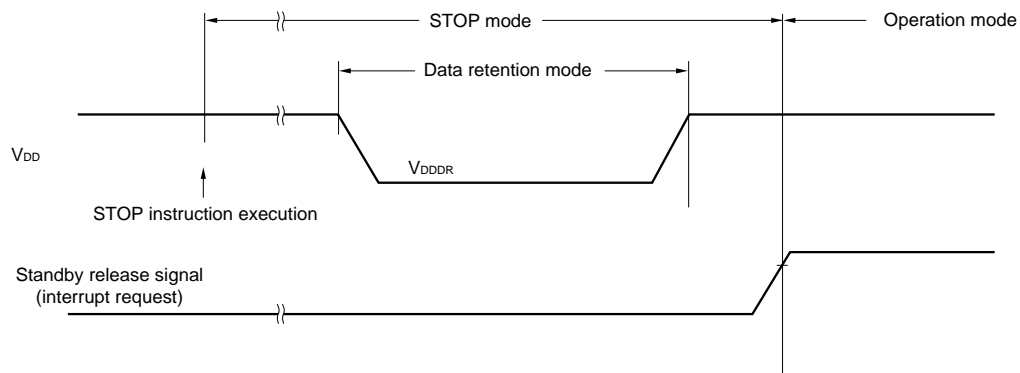
Old:

33.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = -40 to +105°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V _{DDDR}		1.44 ^{Note}		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



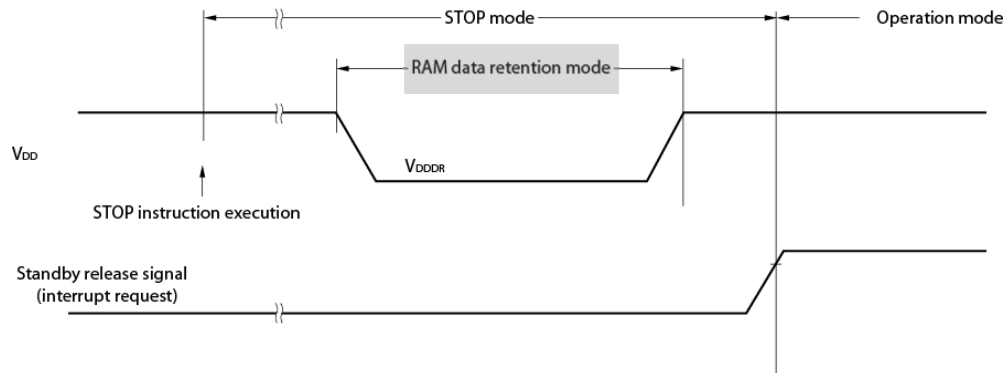
New:

33.8 RAM Data Retention Characteristics

(T_A = -40 to +105°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V _{DDDR}		1.44 ^{Note}		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



11. 6.3.3 Timer mode register mn (TMRmn)

Figure 6-12. Former of Timer mode Register mn (TMRmn)(4/4)

Incorrect:

Figure 6-12. Format of Timer Mode Register mn (TMRmn) (4/4)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W

Operation mode (Value set by the MDmn3 to MDmn1 bits (see the previous page)	MD mn 0	Setting of starting counting and interrupt
<ul style="list-style-type: none"> Interval timer mode (0, 0, 0) Capture mode (0, 1, 0) 	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
<ul style="list-style-type: none"> Event counter mode (0, 1, 1) 	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
<ul style="list-style-type: none"> One-count mode^{Note 2} (1, 0, 0) 	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation ^{Note 3} . At that time, interrupt is generated .
<ul style="list-style-type: none"> Capture & one-count mode (1, 1, 0) 	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated.
Other than above		Setting prohibited

Correct:

Figure 6-12. Format of Timer Mode Register mn (TMRmn) (4/4)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W

Operation mode (Value set by the MDmn3 to MDmn1 bits (see the previous page)	MD mn 0	Setting of starting counting and interrupt
<ul style="list-style-type: none"> Interval timer mode (0, 0, 0) Capture mode (0, 1, 0) 	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
<ul style="list-style-type: none"> Event counter mode (0, 1, 1) 	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
<ul style="list-style-type: none"> One-count mode^{Note 2} (1, 0, 0) 	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation ^{Note 3} . At that time, interrupt is not generated .
<ul style="list-style-type: none"> Capture & one-count mode (1, 1, 0) 	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated.
Other than above		Setting prohibited

12. 32.3.1 Pin characteristics(p.1004 , p1005)

Incorrect:

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	Per pin for P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130			-10.0 ^{Note 2}	mA
		Total of P00 to P07, P14 to P17	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		-90.0	mA
		P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130 (When duty = 70% ^{Note 3})	$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$		-15.0	mA
			$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$		-7.0	mA
			$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$		-3.0	mA
	I _{OH2}	Per pin for P20 and P21	$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		-0.1 ^{Note 2}	mA
	Total of all pins (When duty = 70% ^{Note 3})	$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		-0.2	mA	

Correct:

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	Per pin for P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130			-10.0 ^{Note 2}	mA
		Total of P00 to P07, P10 to P17, P22 to P27	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		-90.0	mA
		P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130 (When duty = 70% ^{Note 3})	$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$		-15.0	mA
			$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$		-7.0	mA
			$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$		-3.0	mA
	I _{OH2}	Per pin for P20 and P21	$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		-0.1 ^{Note 2}	mA
	Total of all pins (When duty = 70% ^{Note 3})	$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		-0.2	mA	

Incorrect:

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output current, low ^{Note 1}	I _{OL1}	Per pin for P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130			20.0 ^{Note 2}	mA	
		Per pin for P60 and P61			15.0 ^{Note 2}	mA	
		Total of P40 to P47, P130 (When duty = 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V			70.0	mA
			2.7 V ≤ V _{DD} < 4.0 V			15.0	mA
			1.8 V ≤ V _{DD} < 2.7 V			9.0	mA
			1.6 V ≤ V _{DD} < 1.8 V			4.5	mA
		Total of P00 to P07, P14 to P17 , P30 to P35, P50 to P57, P70 to P77, P125 to P127 (When duty = 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V			90.0	mA
			2.7 V ≤ V _{DD} < 4.0 V			35.0	mA
			1.8 V ≤ V _{DD} < 2.7 V			20.0	mA
			1.6 V ≤ V _{DD} < 1.8 V			10.0	mA
	Total of all pins (When duty = 70% ^{Note 3})				160.0	mA	
	I _{OL2}	Per pin for P20 and P21			0.4 ^{Note 2}	mA	
		Total of all pins (When duty = 70% ^{Note 3})	1.6 V ≤ V _{DD} ≤ 5.5 V			0.8	mA

Correct:

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output current, low ^{Note 1}	I _{OL1}	Per pin for P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130			20.0 ^{Note 2}	mA	
		Per pin for P60 and P61			15.0 ^{Note 2}	mA	
		Total of P40 to P47, P130 (When duty = 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V			70.0	mA
			2.7 V ≤ V _{DD} < 4.0 V			15.0	mA
			1.8 V ≤ V _{DD} < 2.7 V			9.0	mA
			1.6 V ≤ V _{DD} < 1.8 V			4.5	mA
		Total of P00 to P07, P10 to P17, P22 to P27, P30 to P35, P50 to P57, P70 to P77, P125 to P127 (When duty = 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V			90.0	mA
			2.7 V ≤ V _{DD} < 4.0 V			35.0	mA
			1.8 V ≤ V _{DD} < 2.7 V			20.0	mA
			1.6 V ≤ V _{DD} < 1.8 V			10.0	mA
	Total of all pins (When duty = 70% ^{Note 3})				160.0	mA	
	I _{OL2}	Per pin for P20 and P21			0.4 ^{Note 2}	mA	
		Total of all pins (When duty = 70% ^{Note 3})	1.6 V ≤ V _{DD} ≤ 5.5 V			0.8	mA

13. 33.3.1 Pin characteristics(p.1068 , p1069)

Incorrect:

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	IOH1	Per pin for P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		-3.0 ^{Note 2}	mA
		Total of P00 to P07, P14 to P17, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130 (When duty = 70% ^{Note 3})	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		-45.0	mA
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$		-15.0	mA
			$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$		-7.0	mA
	IOH2	Per pin for P20 and P21	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		-0.1 ^{Note 2}	mA
Total of all pins (When duty = 70% ^{Note 3})		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		-0.2	mA	

Correct:

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	IOH1	Per pin for P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		-3.0 ^{Note 2}	mA
		Total of P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130 (When duty = 70% ^{Note 3})	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		-45.0	mA
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$		-15.0	mA
			$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$		-7.0	mA
	IOH2	Per pin for P20 and P21	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		-0.1 ^{Note 2}	mA
Total of all pins (When duty = 70% ^{Note 3})		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		-0.2	mA	

Incorrect:

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low ^{Note 1}	I _{OL1}	Per pin for P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130			8.5 ^{Note 2}	mA
		Per pin for P60 and P61			15.0 ^{Note 2}	mA
		Total of P40 to P47, P130 (When duty = 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V			40.0
	2.7 V ≤ V _{DD} < 4.0 V				15.0	mA
	2.4 V ≤ V _{DD} < 2.7 V				9.0	mA
	Total of P00 to P07, P14 to P17 P30 to P35, P50 to P57, P70 to P77, P125 to P127 (When duty = 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V			60.0	mA
		2.7 V ≤ V _{DD} < 4.0 V			35.0	mA
		2.4 V ≤ V _{DD} < 2.7 V			20.0	mA
	Total of all pins (When duty = 70% ^{Note 3})				100.0	mA
	I _{OL2}	Per pin for P20 and P21				0.4 ^{Note 2}
Total of all pins (When duty = 70% ^{Note 3})		2.4 V ≤ V _{DD} ≤ 5.5 V			0.8	mA

Correct:

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output current, low ^{Note 1}	I _{OL1}	Per pin for P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130			8.5 ^{Note 2}	mA	
		Per pin for P60 and P61			15.0 ^{Note 2}	mA	
		Total of P40 to P47, P130 (When duty = 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V			40.0	mA
			2.7 V ≤ V _{DD} < 4.0 V			15.0	mA
			2.4 V ≤ V _{DD} < 2.7 V			9.0	mA
		Total of P00 to P07, P10 to P17, P22 to P27 P30 to P35, P50 to P57, P70 to P77, P125 to P127 (When duty = 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V			60.0	mA
	2.7 V ≤ V _{DD} < 4.0 V				35.0	mA	
	2.4 V ≤ V _{DD} < 2.7 V				20.0	mA	
	Total of all pins (When duty = 70% ^{Note 3})				100.0	mA	
	I _{OL2}	Per pin for P20 and P21				0.4 ^{Note 2}	mA
Total of all pins (When duty = 70% ^{Note 3})		2.4 V ≤ V _{DD} ≤ 5.5 V			0.8	mA	

14. 5.6.4 CPU clock status transition diagram (p.179)

Incorrect:

Table 5-3. CPU Clock Transition and SFR Setting Examples (3/5)

(6) Changing CPU clock from high-speed system clock (C) to high-speed on-chip oscillator clock (B)

(SFR setting sequence) →

Status Transition	SFR Flag to Set	CSC Register	Oscillation Accuracy Stabilization Time	CKC Register
		HIOSTOP		
(C) → (B)		0	Note	0

Setting unnecessary if the CPU is operating on the high-speed on-chip oscillator clock

Note When FRQSEL4 = 0: 18 to 65 μs

When FRQSEL4 = 1: 18 to 80 μs

(omitted)

(8) Changing CPU clock from subsystem clock (D) to high-speed on-chip oscillator clock (B)

(Setting sequence of SFRs) →

Status Transition	Setting Flag of SFR	CSC Register	Oscillation Accuracy Stabilization Time	CKC Register	
		HIOSTOP		CSS	MCM0
(D) → (B)		0	Note	0	0

Setting unnecessary if the CPU is operating on the high-speed on-chip oscillator clock

Setting unnecessary if this bit is already set

Note When FRQSEL4 = 0: 18 to 65 μs

When FRQSEL4 = 1: 18 to 80 μs

Remarks 1. (A) to (J) in Table 5-3 correspond to (A) to (J) in Figure 5-16.

2. The oscillation accuracy stabilization time changes according to the temperature conditions and the STOP mode period.

Correct:

Table 5-3. CPU Clock Transition and SFR Setting Examples (3/5)

(6) Changing CPU clock from high-speed system clock (C) to high-speed on-chip oscillator clock (B)

(SFR setting sequence) →

Status Transition	SFR Flag to Set	CSC Register	Oscillation Accuracy Stabilization Time	CKC Register
		HIOSTOP		
(C) → (B)		0	Note	0

Setting unnecessary if the CPU is operating on the high-speed on-chip oscillator clock

Note When FRQSEL4 = 0: 18 to 65 μs

When FRQSEL4 = 1: 18 to 135 μs

(omitted)

(8) Changing CPU clock from subsystem clock (D) to high-speed on-chip oscillator clock (B)

(Setting sequence of SFRs) →

Status Transition	Setting Flag of SFR	CSC Register	Oscillation Accuracy Stabilization Time	CKC Register	
		HIOSTOP		CSS	MCM0
(D) → (B)		0	Note	0	0

Setting unnecessary if the CPU is operating on the high-speed on-chip oscillator clock

Setting unnecessary if this bit is already set

Note When FRQSEL4 = 0: 18 to 65 μs

When FRQSEL4 = 1: 18 to 135 μs

Remarks 1. (A) to (J) in Table 5-3 correspond to (A) to (J) in Figure 5-16.

2. The oscillation accuracy stabilization time changes according to the temperature conditions and the STOP mode period.

15. 8.3.5 Real-time clock control register 1 (RTCC1)

Additional entry to Figure 8 - 6 Format of Real-time clock control register 1 (RTCC1) (3/3)

Old:

RWAIT	Wait control of real-time clock 2
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value
<p>This bit controls the operation of the counter. Be sure to write "1" to it to read or write the counter value. As the counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0. When RWAIT = 1, it takes up to 1 clock (f_{RTC}) until the counter value can be read or written (RWST = 1). When the counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up. However, when it wrote a value to second count register, it will not keep the overflow event</p>	

New:

RWAIT	Wait control of real-time clock 2
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value
<p>This bit controls the operation of the counter. Be sure to write "1" to it to read or write the counter value. As the counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0. When RWAIT = 1, it takes up to 1 clock (f_{RTC}) until the counter value can be read or written (RWST = 1). Notes1,2 When the counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up. However, when it wrote a value to second count register, it will not keep the overflow event</p>	

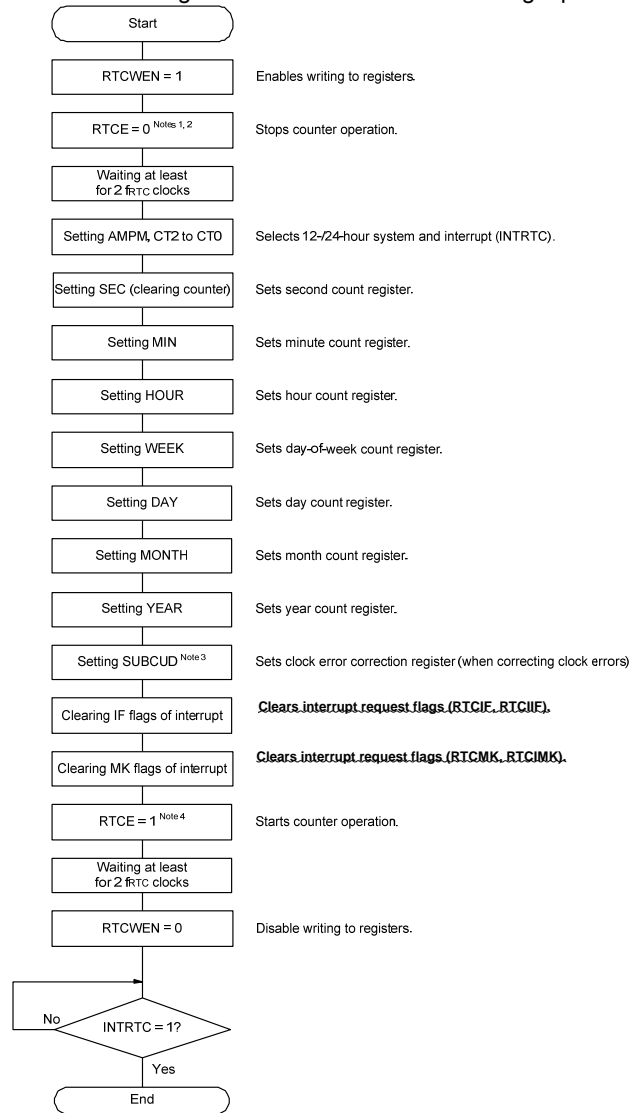
Note1. When setting RWAIT=1 during 1 operating clock (f_{RTC}), after setting RTCE=1, it may take two clock time of the operation clock (f_{RTC}), until RWST bit is set to "1".

Note2. When setting RWAIT=1 during 1 operating clock (f_{RTC}), after returning from a stand-by (HALT mode, STOP mode and SNOOZE mode), it may take two clock time of the operation clock (f_{RTC}), until RWST bit is set to "1".

16. 8.4.1 Starting operation of real-time clock 2 (Page 414)

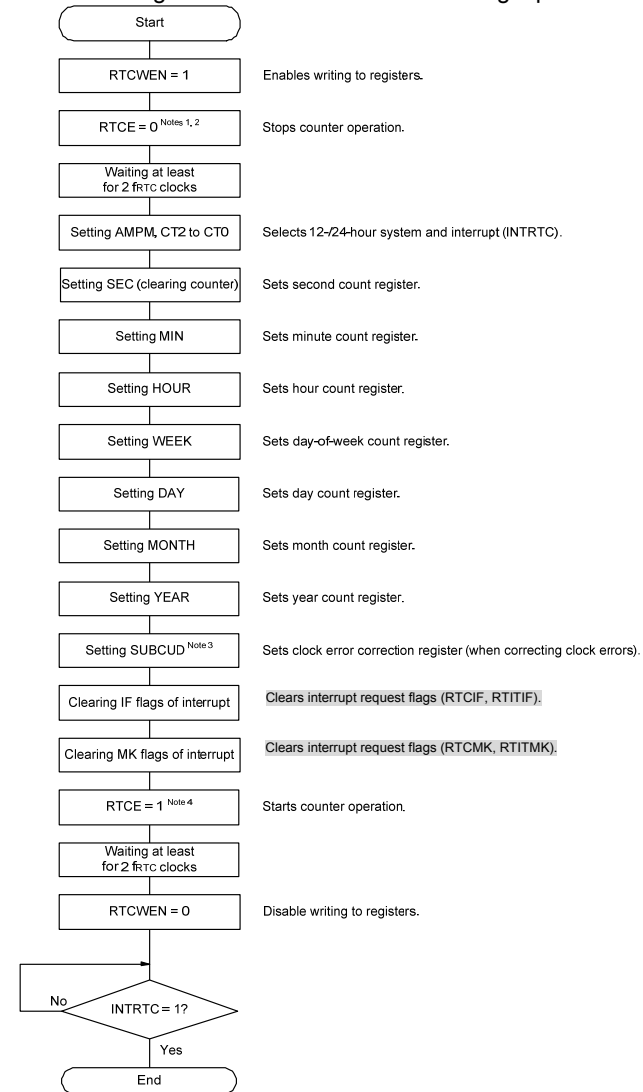
Incorrect:

Figure 8 - 20 Procedure for Starting Operation of Real-time Clock 2



Correct:

Figure 8 - 20 Procedure for Starting Operation of Real-time Clock 2



17. 2.1.1 64-pin products (Page 15)

Incorrect:

Function Name	Pin Type	I/O	After Reset	Alternate Function	Function
(omitted)					
P60	7-1-3	I/O	Input port	SCLA0/(TI01)/(TO01)	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. N-ch open-drain output (6 V tolerance).
P61				SDAA0/(TI02)/(TO02)	
P70	7-5-4	I/O	Digital input invalid ^{Note 1}	KR0/SEG12	Port 7. 5-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Can be set to LCD output ^{Note 2} .
P74	7-5-16			KR4/SEG16/TKBO00	
P75				KR5/SEG17/TKBO01-2	
P76				KR6/SEG18/TKBO01-1	
P77				KR7/SEG19/TKBO01-0	

Correct:

Function Name	Pin Type	I/O	After Reset	Alternate Function	Function
(omitted)					
P60	7-1-3	I/O	Input port	SCLA0/(TI01)/(TO01)	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. N-ch open-drain output (6 V tolerance).
P61				SDAA0/(TI02)/(TO02)	
P70	7-5-4	I/O	Digital input invalid ^{Note 1}	KR0/SEG12	Port 7. 5-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Can be set to LCD output ^{Note 2} .
P74	7-5-16			KR4/SEG16/TKBO00	
P75				KR5/SEG17/TKBO01-2	
P76				KR6/SEG18/TKBO01-1	
P77				KR7/SEG19/TKBO01-0	

18. 2.1.2 80-pin products (Page 19)

Incorrect:

Function Name	Pin Type	I/O	After Reset	Alternate Function	Function
P60	7-1-3	I/O	Input port	SCLA0/(TI01)/(TO01)	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. N-ch open-drain output (6 V tolerance).
P61				SDAA0/(TI02)/(TO02)	
P70	7-5-4	I/O	Digital input invalid ^{Note 1}	KR0/SEG12	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units.
P71				KR1/SEG13	
P72				KR2/SEG14	
P73				KR3/SEG15	
P74	7-5-16			KR4/SEG16/TKBO00	Use of an on-chip pull-up resistor can be specified by a software setting at input port. Can be set to LCD output ^{Note 2} .
P75				KR5/SEG17/TKBO01-2	
P76				KR6/SEG18/TKBO01-1	
P77				KR7/SEG19/TKBO01-0	

Correct:

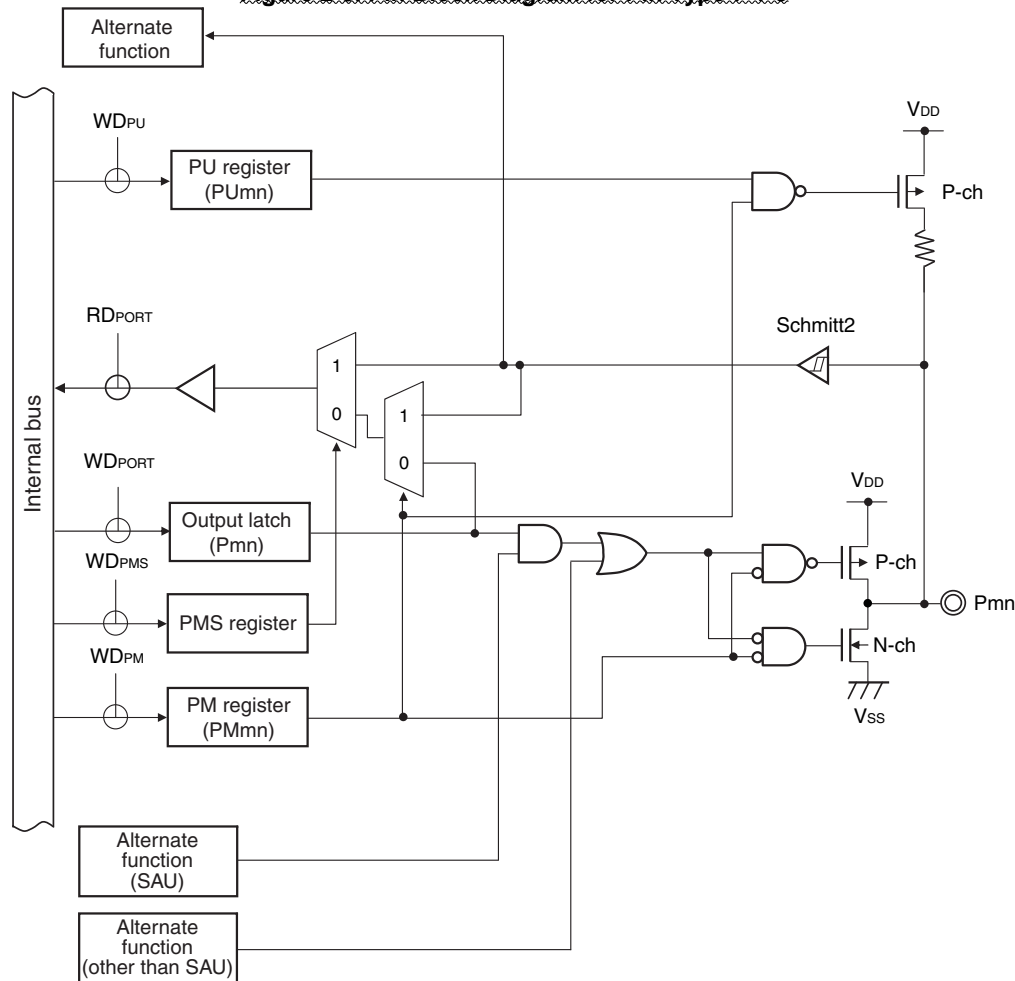
Function Name	Pin Type	I/O	After Reset	Alternate Function	Function
P60	12-1-3	I/O	Input port	SCLA0/(TI01)/(TO01)	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. N-ch open-drain output (6 V tolerance).
P61				SDAA0/(TI02)/(TO02)	
P70	7-5-4	I/O	Digital input invalid ^{Note 1}	KR0/SEG12	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units.
P71				KR1/SEG13	
P72				KR2/SEG14	
P73				KR3/SEG15	
P74	7-5-16			KR4/SEG16/TKBO00	Use of an on-chip pull-up resistor can be specified by a software setting at input port. Can be set to LCD output ^{Note 2} .
P75				KR5/SEG17/TKBO01-2	
P76				KR6/SEG18/TKBO01-1	
P77				KR7/SEG19/TKBO01-0	

19. 2.4 Block Diagrams of Pins

Figure 2-5. Pin Block Diagram for Pin Type 7-1-3 (Page 30)

Incorrect:

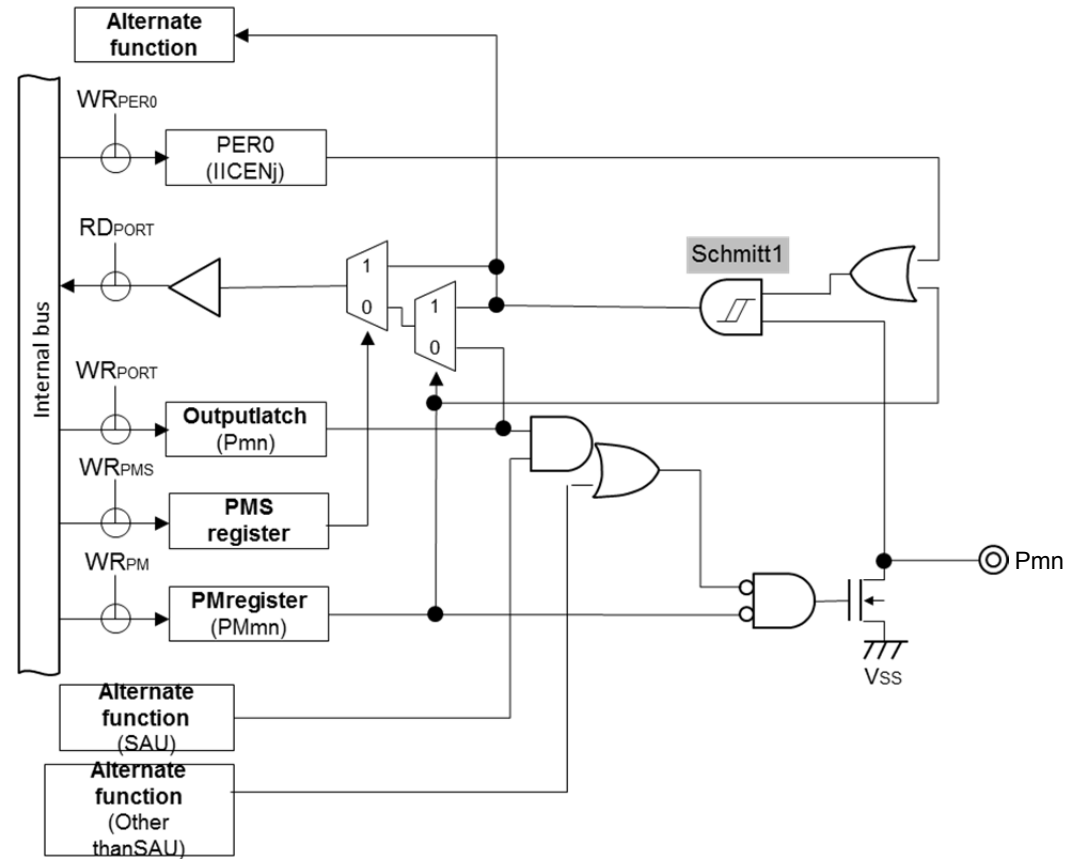
Figure 2-5. Pin Block Diagram for Pin Type 7-1-3



- Remarks**
1. For alternate functions, see 2.1 Port Function.
 2. SAU: Serial array unit

Correct:

Figure 2-5. Pin Block Diagram for Pin Type 12-1-3

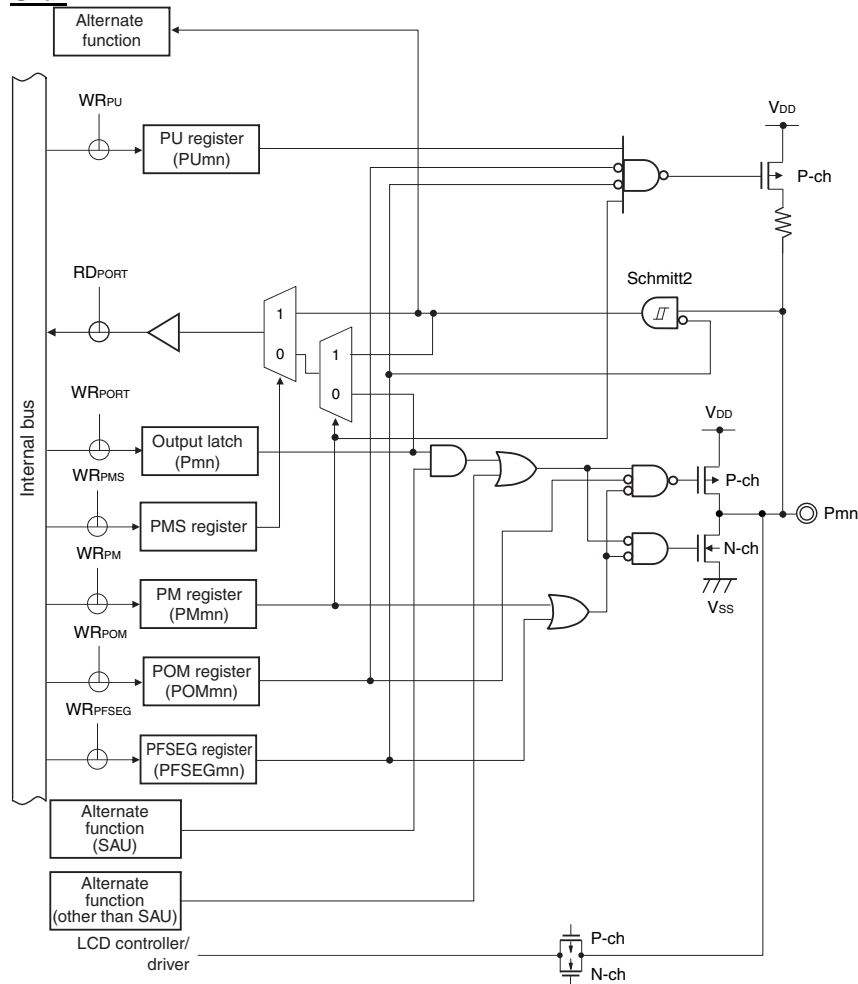


- Remarks**
1. For alternate functions, see 2.1 Port Function.
 2. SAU: Serial array unit

20. 2.4 Block Diagrams of Pins

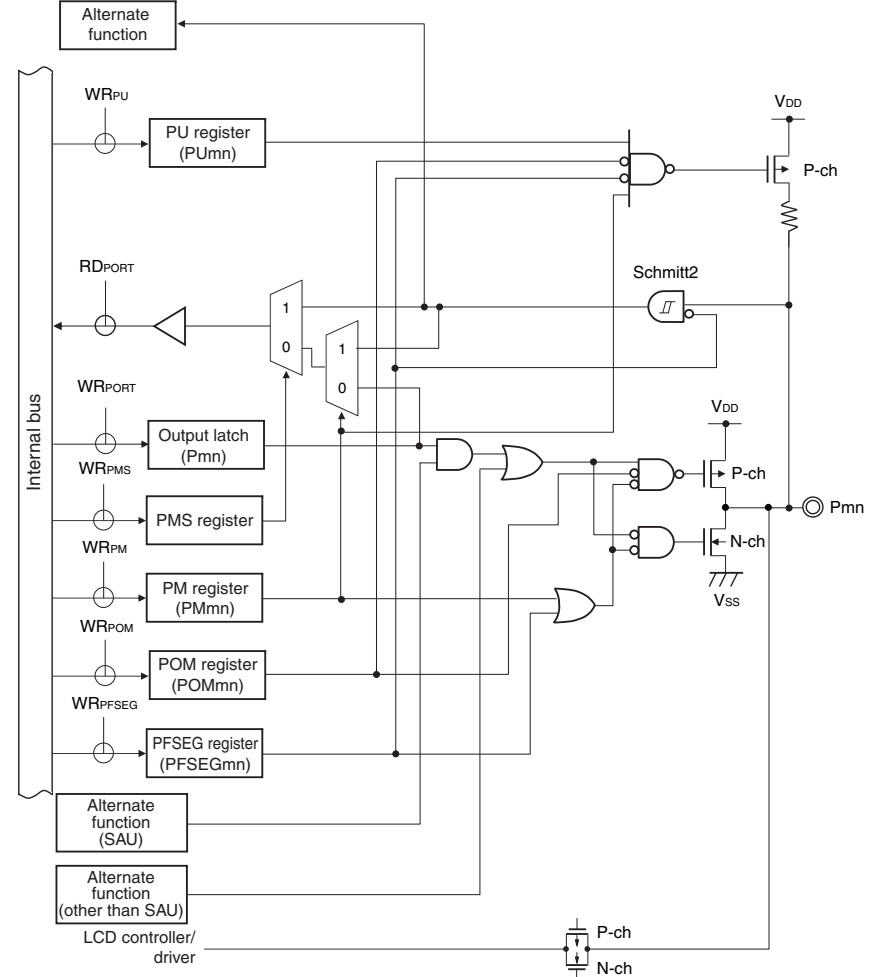
Figure 2-9. Pin Block Diagram for Pin Type 7-5-10 (Page 34)

Old:



- Remarks**
1. For alternate functions, see 2.1 Port Function.
 2. SAU: Serial array unit

New:



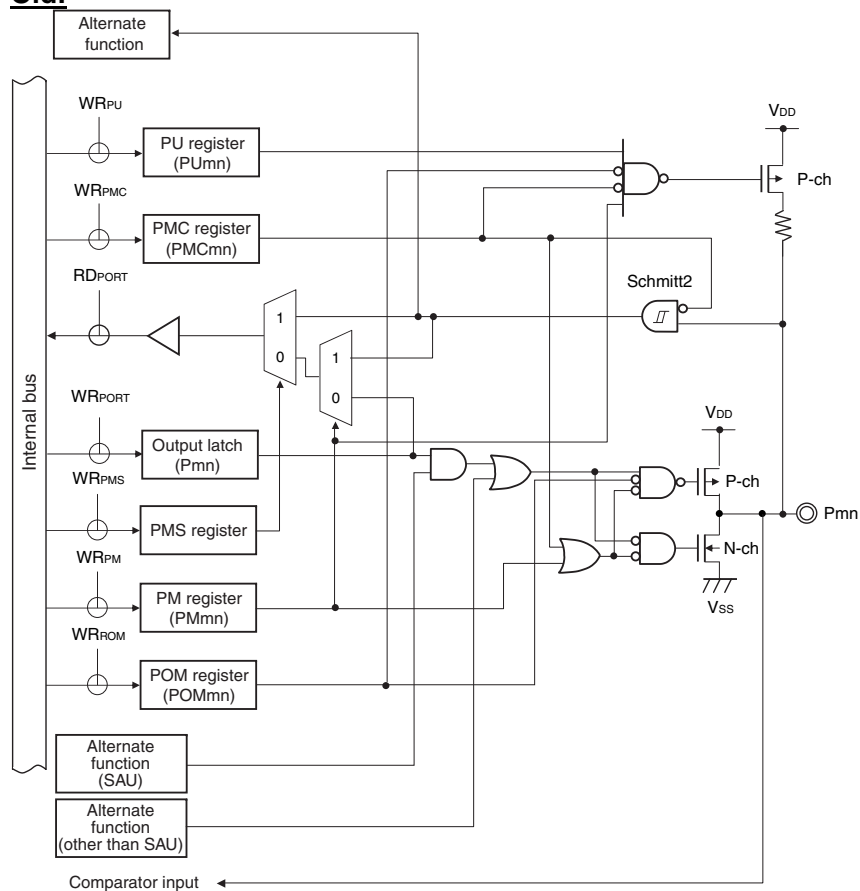
Caution A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

- Remarks**
1. For alternate functions, see 2.1 Port Function.
 2. SAU: Serial array unit

21. 2.4 Block Diagrams of Pins

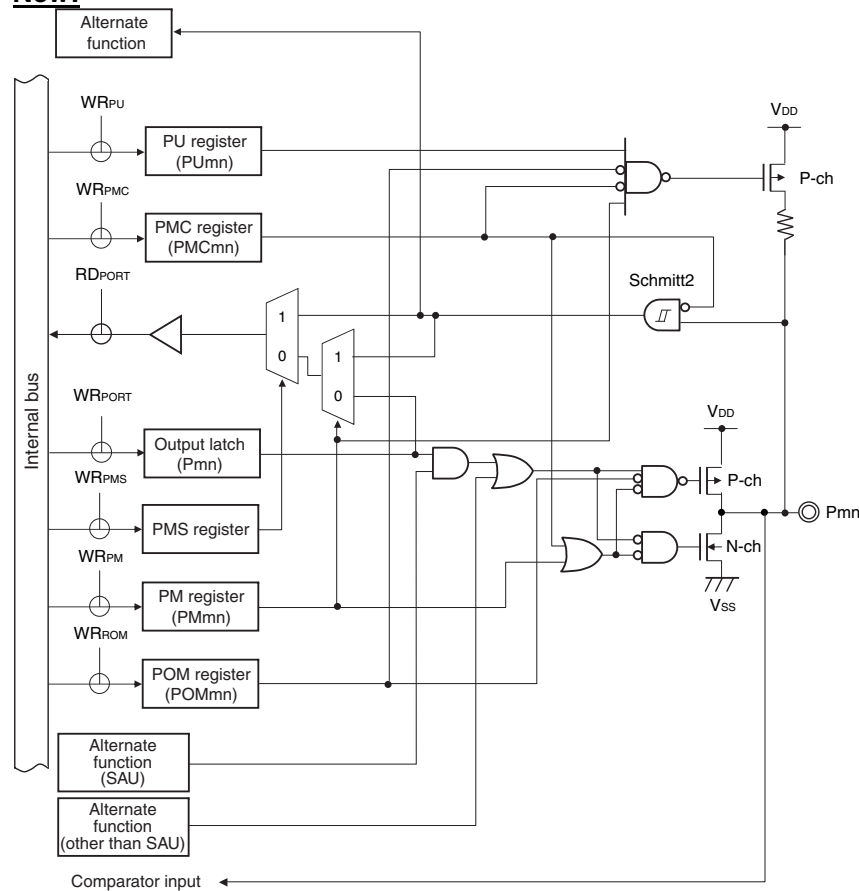
Figure 2-11. Pin Block Diagram for Pin Type 7-6-4 (Page 36)

Old:



- Remarks**
1. For alternate functions, see 2.1 Port Function.
 2. SAU: Serial array unit

New:

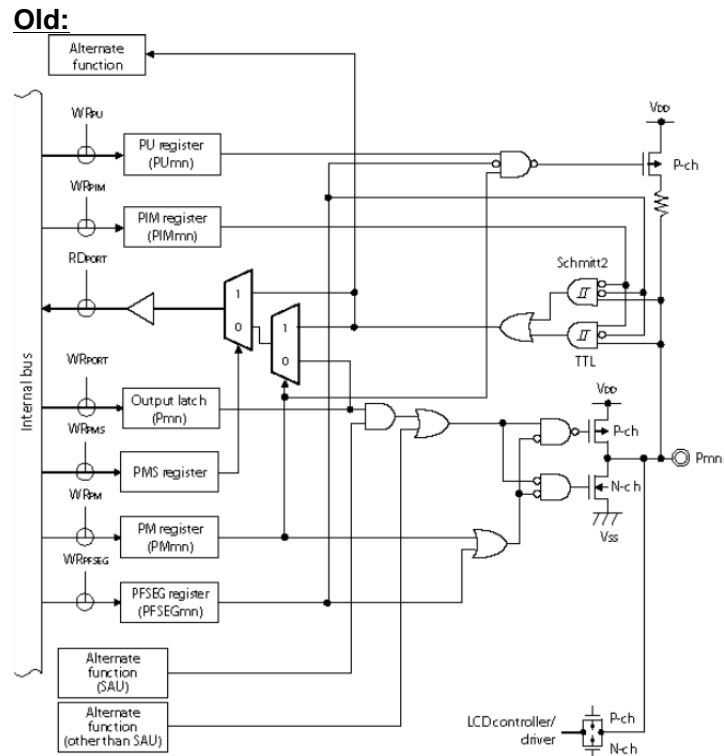


Caution A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

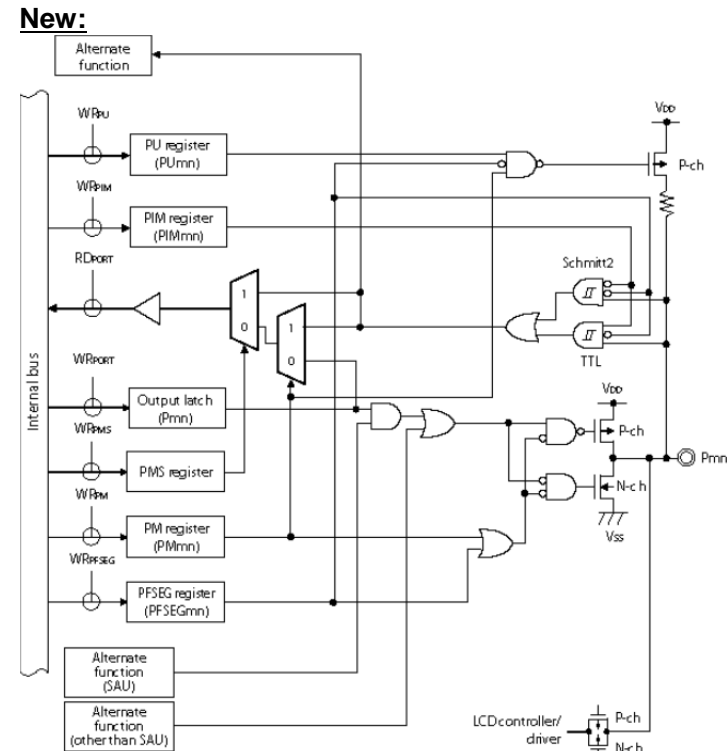
- Remarks**
1. For alternate functions, see 2.1 Port Function.
 2. SAU: Serial array unit

22. 2.4 Block Diagrams of Pins

Figure 2-14. Pin Block Diagram for Pin Type 8-5-4 (Page 39)



- Remarks**
1. For alternate functions, see 2.1 Port Function.
 2. SAU: Serial array unit



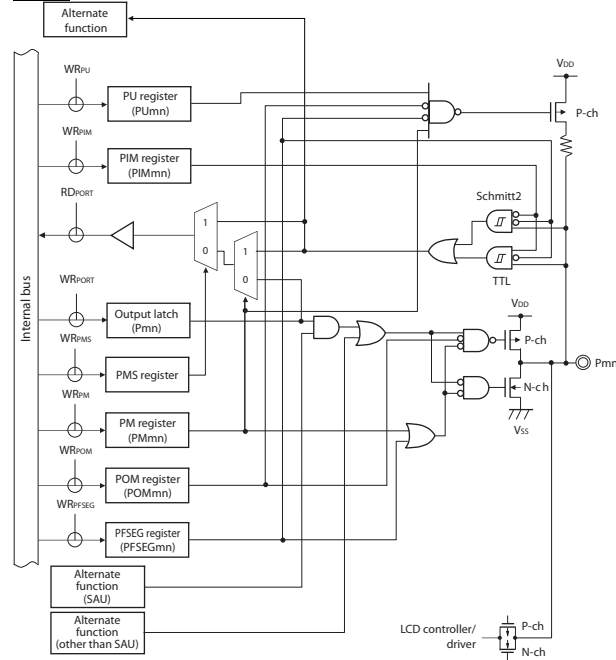
Caution Because of TTL input buffer structure, if the port input mode register (PIM_x) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

- Remarks**
1. For alternate functions, see 2.1 Port Function.
 2. SAU: Serial array unit

23. 2.4 Block Diagrams of Pins

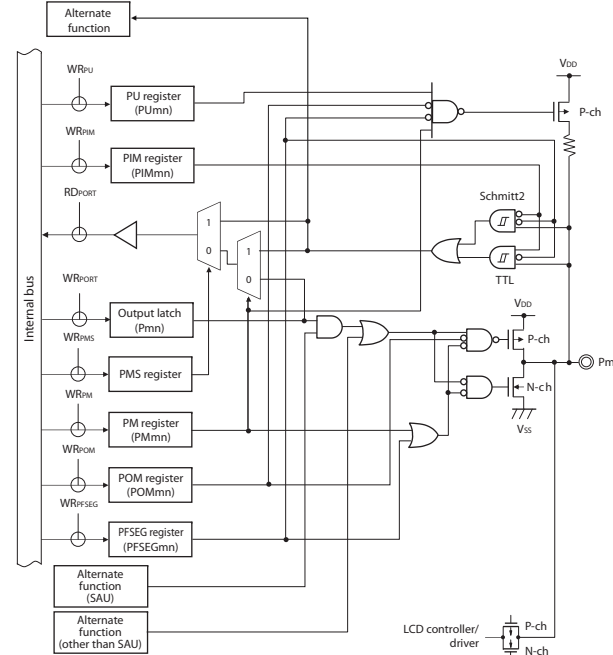
Figure 2-15. Pin Block Diagram for Pin Type 8-5-10 (Page 40)

Old:



- Remarks 1. For alternate functions, see 2.1 Port Function.
- 2. SAU: Serial array unit

New:



Caution 1. A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

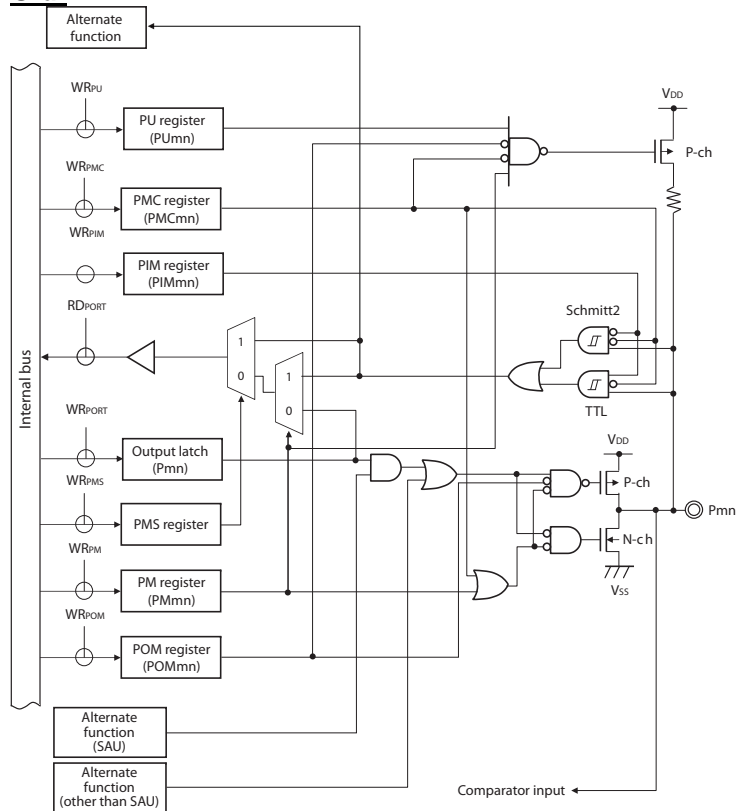
Caution 2. Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

- Remarks 1. For alternate functions, see 2.1 Port Function.
- 2. SAU: Serial array unit

24. 2.4 Block Diagrams of Pins

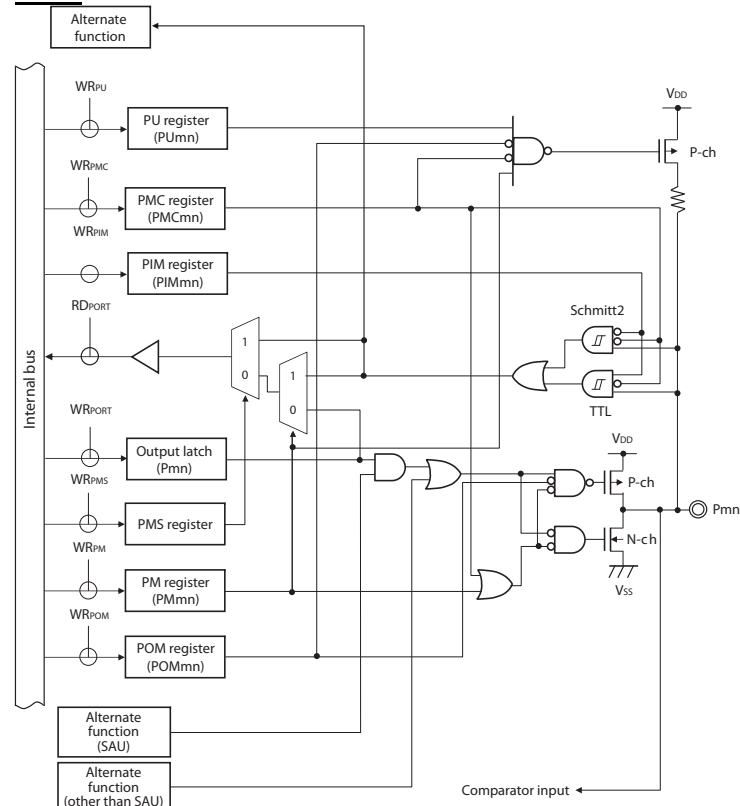
Figure 2-16. Pin Block Diagram for Pin Type 8-6-4 (Page 41)

Old:



- Remarks**
1. For alternate functions, see 2.1 Port Function.
 2. SAU: Serial array unit

New:



Caution 1. A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

Caution 2. Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

- Remarks**
1. For alternate functions, see 2.1 Port Function.
 2. SAU: Serial array unit