Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan RenesasTechn ology Corp.

Product Category	MPU&MCU		Document No.	TN-H8*-A333B/E	Rev.	2.00
Title	About the SCI3 specification change.		Information Category	Technical Notificatio	'n	
		Lot No.				
Applicable Product	Please see following description.	All	Reference Document	Please see following o	description.	
The target p	product that the following show deletes the mul	tiprocessor o	communication f	unction of SCI3 from the	e specific	ation.
< Target proc	duct manual>					
	Group Hardware Manual (REJ09B0182-0200)					
	Group Hardware Manual (REJ09B0093-0300)					
H8/38024,H8	3/38024S,H8/38024R,H8/38124 Group Hardwa	are Manual (REJ09B0042-07	700)		
H8/3887 Ser	ies Hardware Manual (ADE-602-151A)					
H8/3867 Ser	ies Hardware Manual (ADE-602-142B)					
H8/3847R G	roup H8/3847S Group H8/38347 Group H8/38	447 Group H	lardware Manua	I (REJ09B0145-0500)		
H8/3827R G	roup H8/3827S Group H8/38327 Group H8/384	127 Group H	lardware Manua	I (REJ09B0144-0500)		
H8/3802,H8/	38004,H8/38002S,H8/38104 Group Hardware	Manual (RE	J09B0024-0600)		
H8/38602R (Group Hardware Manual (REJ09B0152-0200)					
The explana	tion and the communication format etc. of	SCI3 registe	er are shown in	the following and the	er multip	rocessor
communicati	on functions are deleted from the specification	l.				
Change po	oint from Rev.1: Bit 2(MPIE) of cereal control register	(SCR)				
	Rev.1: When this bit is one, the form		communication b	ecomes possible.		
	In the case of writing 1 to this	bit, bit5 (PE)	should be writte	en with 1 all at once.		
	Please write 1 to the bit 3 of S	erial control	register (SCR) b	pefore writing 1 in this bi	t	
	Rev.2: It's a reserved bit.					
	When this bit is one, the form	at of 5 bits c	ommunication b	ecomes possible.		
	In the case of writing 1 to this	bit, bit5 (PE)	should be writte	en with 1 all at once.		
	Bit 3(MPIE) of cereal control register	(SCR)				
	Rev.1: Bit3 is reserved, this can only	be written v	with 1.			
	Rev.2: It's a reserved bit.					
() 000 0 D	ssas Technology Corp. All rights reserved				De	ae 1 of 6



Bit 7 6 5 4 3 2 1 0 Initial value 0										
Bit 7 6 5 4 3 2 1 0 Initial value Read/Write COM CHR PE PM STOP MP $CKS1$ $CKS1$ Bit RW	[Before change]									
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	Serial mode register (S	MR)								
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Bit	1								
Read/WriteR/W <td>Initial value</td> <td>J</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>· · · · · · · · · · · · · · · · · · ·</td> <td></td>	Initial value	J							· · · · · · · · · · · · · · · · · · ·	
When this bit is set to 1, the multiprocessor communication function is enabled. The PE bit and PM bit settings are invalid. In clocked synchronous mode, this bit should be cleared to 0. [after change] Serial mode register (SMR) Bit $7 6 5 4 3 2 1 0$ Initial value $0 0 0 0 0 0 0 0 0 0$ Read/Write R/W		-	-	-	-	-		-	-	
clocked synchronous mode, this bit should be cleared to 0, [after change] Serial mode register (SMR) $\begin{array}{c c c c c c c c c c c c c c c c c c c $	Bit 2 : Multiprocessor M	lode (MP)								
[after change] Serial mode register (SMR) $\frac{Bit}{Read/Write} \frac{7}{R/W} \frac{6}{R/W} \frac{5}{R/W} \frac{1}{R/W} \frac{3}{R/W} \frac{2}{R/W} \frac{1}{R/W} \frac$	When this bit is set to	1, the multipro	cessor co	mmunicatio	on function i	s enabled.	The PE bit a	and PM bit	settings are in	ivalid. In
Serial mode register (SMR) Bit $7 6 5 4 3 2 1 0$ Read/Write RW RW RW RW RW RW RW RW	clocked synchronous n	node, this bit sl	nould be cl	eared to 0.						
Serial mode register (SMR) Bit $7 6 5 4 3 2 1 0$ Read/Write RW RW RW RW RW RW RW RW										
Bit 7 6 5 4 3 2 1 0 Initial value 0 0 0 0 0 0 0 0 0 Bit 2: 5 bit communication (MP)When this bit is one, the format of 5 bits communication becomes possible.In the case of writing 1 to this bit, bit5 (PE) should be written with 1 all at once.(Before change]Serial mode register (SMR)Bit 7 6 5 4 3 2 1 0 Nultiprocessor Interrupt Enable (MPIE)When this bit is set to 1, receive data in which the multiprocessor bit is 0 is skipped, and setting of the RDRF, FER, and OERstatus flags in SSR is prohibited. On receiving data in which the multiprocessor bit is 1, this bit is automatically cleared and normal reception is resumed.[after change]Serial mode register (SMR)Bit 7 6 5 4 3 2 1 0 Bit 3: Multiprocessor Interrupt Enable (MPIE)When this bit is set to 1, receive data in which the multiprocessor bit is 0 is skipped, and setting of the RDRF, FER, and OERstatus flags in SSR is prohibited. On receiving data in which the multiprocessor bit is 1, this bit is automatically cleared and normal reception is resumed.Bit 7 6 5 4 3 2 1 0 Initial value 0 0 0 0 0 0 0 0 Bit 3: Reserved bitRWRWRWRWRWRWRWRWBit 3: Reserved	[after change]									
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Serial mode register (S	MR)								
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Bit	7	6	5	4	3	2	1	0	
Read/WriteR/WR/WR/WR/WR/WR/WR/WR/WR/WBit 2: 5 bit communication (MP)When this bit is one, the format of 5 bits communication becomes possible.In the case of writing 1 to this bit, bit5 (PE) should be written with 1 all at once.(Before change]Serial mode register (SMR)TIETERMPIETEIECKE1CKE0Initial value0000000Read/WriteR/WR/WR/WR/WR/WR/WR/WR/WBit 3: Multiprocessor Interrupt Enable (MPIE)When this bit is set to 1, receive data in which the multiprocessor bit is 0 is skipped, and setting of the RDRF, FER, and OERstatus flags in SSR is prohibited. On receiving data in which the multiprocessor bit is 1, this bit is automatically cleared and normal reception is resumed.Alter change]Serial mode register (SMR)Bit 7 6 5 4 3 2 1 0ITIE RIE TE MPIE TEIE CKE1 CKE0Initial value0000000ON O O O O O O O O O O O O O O O O O O			CHR	PE	PM	STOP				
Bit 2 : 5 bit communication (MP) When this bit is one, the format of 5 bits communication becomes possible. In the case of writing 1 to this bit, bit5 (PE) should be written with 1 all at once. [Before change] Serial mode register (SMR) Bit 7 6 5 4 3 2 1 0 Initial value 0 0 0 0 0 0 0 0 0 0 Read/Write R/W R/W R/W R/W R/W R/W R/W R/W R/W Bit 3 : Multiprocessor Interrupt Enable (MPIE) When this bit is set to 1, receive data in which the multiprocessor bit is 0 is skipped, and setting of the RDRF, FER, and OER status flags in SSR is prohibited. On receiving data in which the multiprocessor bit is 1, this bit is automatically cleared and normal reception is resumed. Iafter change] Serial mode register (SMR) Bit 7 6 5 4 3 2 1 0 Initial value 0 0 0 0 0 0 0 0 0 Bit 7 6 5 4 3 2 1 0 Initial value 0 0 0 0 0 0 0 0 0 0 Bit 7 6 5 4 3 2 1 0 Initial value 0 0 0 0 0 0 0 0 0 Bit 7 6 5 4 3 2 1 0 Initial value 0 0 0 0 0 0 0 0 0 Bit 7 6 5 4 3 2 1 0 Initial value 0 0 0 0 0 0 0 0 0 Read/Write R/W		-	-		-	-			-	
When this bit is one, the format of 5 bits communication becomes possible. In the case of writing 1 to this bit, bit5 (PE) should be written with 1 all at once. (Before change] Serial mode register (SMR) $\begin{array}{c c c c c c c c c c c c c c c c c c c $			R/W	R/W	R/W	R/W	R/VV	R/W	R/W	
In the case of writing 1 to this bit, bit5 (PE) should be written with 1 all at once. [Before change] Serial mode register (SMR) $\begin{array}{c c c c c c c c c c c c c c c c c c c $										
[Before change] Serial mode register (SMR) $\begin{array}{c c c c c c c c c c c c c c c c c c c $					•					
Serial mode register (SMR) Bit 7 6 5 4 3 2 1 0 Initial value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	In the case of writing 1	to this bit, bit5	(PE) shoul	d be writte	n with 1 all a	at once.				
Serial mode register (SMR) Bit 7 6 5 4 3 2 1 0 Initial value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0										
Bit 7 6543210Initial value Read/Write00000000Bit 3 : Multiprocessor Interrupt Enable (MPIE)When this bit is set to 1, receive data in which the multiprocessor bit is 0 is skipped, and setting of the RDRF, FER, and OER status flags in SSR is prohibited. On receiving data in which the multiprocessor bit is 1, this bit is automatically cleared and normal reception is resumed.[after change]Serial mode register (SMR)Bit 7 6 5 4 3 2 1 0 Initial value Read/Write00000 0 0 0 0 0 Bit 3 : Reserved bit	[Before change]									
TIE RIE TE RE MPIE TEIE CKE1 CKE0 Initial value 0 0 0 0 0 0 0 0 Read/Write R/W R/W R/W R/W R/W R/W R/W R/W R/W Bit 3 : Multiprocessor Interrupt Enable (MPIE) When this bit is set to 1, receive data in which the multiprocessor bit is 0 is skipped, and setting of the RDRF, FER, and OER status flags in SSR is prohibited. On receiving data in which the multiprocessor bit is 1, this bit is automatically cleared and normal reception is resumed. [after change] Serial mode register (SMR) Bit 7 6 5 4 3 2 1 0 Initial value 0 0 0 0 0 0 0 0 Initial value R/W R/W R/W R/W R/W R/W R/W R/W Bit 3 : Reserved bit R/W R/W R/W R/W R/W R/W R/W R/W	Serial mode register (S	MR)								
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Read/Write R/W R/W R/W R/W R/W R/W R/W R/W R/W Bit 3 : Multiprocessor Interrupt Enable (MPIE) When this bit is set to 1, receive data in which the multiprocessor bit is 0 is skipped, and setting of the RDRF, FER, and OER status flags in SSR is prohibited. On receiving data in which the multiprocessor bit is 1, this bit is automatically cleared and normal reception is resumed. [after change] Serial mode register (SMR) Bit 7 6 5 4 3 2 1 0 Initial value 0 0 0 0 0 0 0 0 Bit 3 : Reserved bit R/W R/W R/W R/W R/W R/W R/W R/W	2									
Bit 3 : Multiprocessor Interrupt Enable (MPIE) When this bit is set to 1, receive data in which the multiprocessor bit is 0 is skipped, and setting of the RDRF, FER, and OER status flags in SSR is prohibited. On receiving data in which the multiprocessor bit is 1, this bit is automatically cleared and normal reception is resumed. [after change] Serial mode register (SMR) $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		-	-	-	-			-	-	
When this bit is set to 1, receive data in which the multiprocessor bit is 0 is skipped, and setting of the RDRF, FER, and OER status flags in SSR is prohibited. On receiving data in which the multiprocessor bit is 1, this bit is automatically cleared and normal reception is resumed. [after change] Serial mode register (SMR) Bit 7 6 5 4 3 2 1 0 Initial value 0 0 0 0 0 0 0 Bit 7 6 5 4 3 2 1 0 Initial value 0 0 0 0 0 0 0 0 0 Bit 3 : Reserved bit River R/W R/W R/W R/W R/W R/W				R/W	R/W	K/VV	R/W	R/W	R/W	
status flags in SSR is prohibited. On receiving data in which the multiprocessor bit is 1, this bit is automatically cleared and normal reception is resumed. [after change] Serial mode register (SMR) Bit 7 6 5 4 3 2 1 0 Initial value 0 0 0 0 0 0 0 Read/Write R/W R/W R/W R/W R/W R/W R/W		•	, ,							
normal reception is resumed. [after change] Serial mode register (SMR) Bit 7 6 5 4 3 2 1 0 Initial value 0 0 0 0 0 0 0 Initial value 0 0 0 0 0 0 0 Read/Write R/W R/W R/W R/W R/W R/W R/W										
[after change] Serial mode register (SMR) Bit 7 6 5 4 3 2 1 0 TIE RIE TE RE MPIE TEIE CKE1 CKE0 Initial value 0 0 0 0 0 0 0 0 0 Read/Write R/W R/W R/W R/W R/W R/W R/W R/W Bit 3 : Reserved bit			receiving	data in wh	nich the mu	ltiprocessor	bit is 1, this	s bit is auto	omatically clea	ired and
Serial mode register (SMR) Bit 7 6 5 4 3 2 1 0 TIE RIE TE RE MPIE TEIE CKE1 CKE0 Initial value 0 0 0 0 0 0 0 0 Read/Write R/W R/W R/W R/W R/W R/W R/W R/W Bit 3 : Reserved bit Exerved bit	normal reception is res	umed.								
Serial mode register (SMR) Bit 7 6 5 4 3 2 1 0 TIE RIE TE RE MPIE TEIE CKE1 CKE0 Initial value 0 0 0 0 0 0 0 0 Read/Write R/W R/W R/W R/W R/W R/W R/W R/W Bit 3 : Reserved bit Exerved bit										
Bit 7 6 5 4 3 2 1 0 Initial value Read/Write RIE TE RE MPIE TEIE CKE1 CKE0 Initial value Read/Write 0 0 0 0 0 0 0 Bit 3 : Reserved bit Feserved bit Feserved bit Feserved bit Feserved bit Feserved bit	[after change]									
TIE RIE TE RE MPIE TEIE CKE1 CKE0 Initial value 0 <t< td=""><td>Serial mode register (S</td><td>MR)</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></t<>	Serial mode register (S	MR)								
Initial value 0 <	Bit									
Read/Write R/W	Initial value								· · · · · · · · · · · · · · · · · · ·	
Bit 3 : Reserved bit										
	Bit 3 : Reserved bit									

[Before change]								
Serial Status Register	r (SSR)							
Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	OER	FER	PER	TEND	MPBR	MPBT
Initial value Read/Write	1 R/(W)*	0 R/(W)*	0 R/(W)*	0 R/(W)*	0 R/(W)*	1 R	0 R	0 R/W
Bit 1 : Multiprocessor	Bit Receive (MF	PBR)						
MPBR stores the mu	Itiprocessor bit i	in the rece	ive characte	er data. Wh	en the RE b	oit in SCR i	s cleared to	Q its previous
etained.								
Bit 0 : Multiprocessor	Bit Transfer (MF	PBT)						
MPBT stores the mul	tiprocessor bit to	be added	to the trans	smit charact	er data.			
after change]								
Serial Status Registe	r (SSR)							
Bit	7	6	5	4	3	2	1	0
Initial value	TDRE 1	RDRF 0	OER	FER 0	PER	TEND	MPBR	MPBT
Read/Write	ı R/(W)*	0 R/(W)*	0 R/(W)*	0 R/(W)*	0 R/(W)*	1 R	- R	0 R/W
Bit 1 : Reserve bit		()	()	()				
t's a reserved read-o	nly bit.							
Bit 0 : Reserve bit								
The write value shoul	d always be 0							
	a always be 0.							



[Before change]

Data Transfer Formats (Asynchronous Mode)

	SN	/IR		Serial Data Transfer Format and Frame Length											
CHR	PE	MP	STOP	1	2	3	4	5	6	7	8	9	10	11	12
0	0	0	0	S				8-bit	data				STOP	I	
0	0	0	1	S				8-bit	data				STOP	STOP	[
0	0	1	0	s				8-bit	data				MPB	STOP	
0	0	1	1	S				8-bit	data				MPB	STOP	STOP
0	1	0	0	S				8-bit	data				Р	STOP	[
0	1	0	1	S				8-bit	data				Р	STOP	STOP
0	1	1	0	S			5-bit data	а		STOP					
0	1	1	1	S			5-bit data	а		STOP	STOP				
1	0	0	0	S			7	7-bit dat	а			STOP	ĺ		
1	0	0	1	S			7	7-bit dat	a			STOP	STOP		
1	0	1	0	S			7	7-bit dat	a			MPB	STOP	I	
1	0	1	1	S			7	7-bit dat	a			MPB	STOP	STOP	
1	1	0	0	S							STOP				
1	1	0	1	S			1	7-bit dat	a			Р	STOP	STOP	
1	1	1	0	S			5-bit data	a		Р	STOP				
1	1	1	1	S			5-bit data	a		Р	STOP	STOP			



[after change]

Data Transfer Formats (Asynchronous Mode)

	SN	/IR			Serial Data Transfer Format and Frame Length										
CHR	PE	MP	STOP	1	2	3	4	5	6	7	8	9	10	11	12
0	0	0	0	S				8-bit	data				STOP	1	
0	0	0	1	s				8-bit	data				STOP	STOP	[
0	0	1	0					:	Setting p	orohibite	d				
0	0	1	1					:	Setting p	orohibite	d				
0	1	0	0	s				8-bit	data				Р	STOP	
0	1	0	1	s				8-bit	data				Р	STOP	STOP
0	1	1	0	S			5-bit data	а		STOP					
0	1	1	1	s		5-bit data STOP STOP									
1	0	0	0	s			7	7-bit dat	а			STOP	I		
1	0	0	1	s			7	7-bit dat	а			STOP	STOP	I	
1	0	1	0					:	Setting p	orohibite	d				
1	0	1	1					:	Setting p	orohibite	d				
1	1	0	0	s			7	7-bit dat	а			Р	STOP	1	
1	1	0	1	S	7-bit data P					Ρ	STOP	STOP			
1	1	1	0	S			5-bit data	а		Р	STOP				
1	1	1	1	S			5-bit data	a		Р	STOP	STOP	Ι		



[Before change]

SMR Settings and Corresponding Data Transfer Formats

		SMR							
Bit 7	Bit 6	Bit 2	Bit 5	Bit 3	_	Data	Multiprocessor	Parity	Stop Bit
COM	CHR	MP	PE	STOP	Mode	Length	Bit	Bit	Length
0	0	0	0	0	Asynchronous	8-bit data	No	No	1 bit
					mode				2 bits
			1	0	_			Yes	1 bit
				1	_		_		2 bits
	1		0	0	_	7-bit data		No	1 bit
				1	_				2 bits
			1	0				Yes	1 bit
				1	_				2 bits
	0	1	0	0		8-bit data	Yes	No	<u>1bit</u>
				1					2 bits
			1	0	_	5-bit data	No		1bit
				1	_			_	2 bits
	1		0	0	_	7-bit data	Yes		1bit
				1	_				2 bits
			1	0	_	5-bit data	No	Yes	1bit
				1					2 bits
1	*	0	*	*	Clocked	8-bit data	No	No	No
					synchronous				
					mode				

[Legend] *: Don't care

[After change]

SMR Settings and Corresponding Data Transfer Formats

Bit 7 COM	Bit 6 CHR	Bit 2 MP	Bit 5 PE	Bit 3 STOP	Mode	Data Length	Multiprocessor Bit	Parity Bit	Stop Bit Length
0	0	0	0	0	Asynchronous	8-bit data	No	No	1 bit
					_mode				2 bits
			1	0	-			Yes	1 bit
				1	_				2 bits
	1		0	0		7-bit data		No	<u>1 bit</u>
				1	_				2 bits
			1	0	_			Yes	1 bit
				1					2 bits
	0	1	0	0	_		Setting prohibited		
				1			County promotion		
			1	0	_	5-bit data	No		1bit
				1					2 bits
	1		0	0	_		Setting prohibited		
				1			eeting promotion		
			1	0	_	5-bit data	No	Yes	1bit
				1					2 bits
1	*	0	*	*	Clocked synchronous	8-bit data	No	No	No
					mode				

[Legend] *: Don't care

