User Manual

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RH850 Evaluation Platform

RH850/P1M(-E) – 144QFP PiggyBack board V2

Y-RH850-P1X-144PIN-PB-T1-V2

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Chapter 1 Introduction

The RH850/P1M(-E) Application Board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics 32-bit RH850/P1M and RH850/P1M-E microcontrollers in 144pin QFP package with 0.4mm pin pitch. The PiggyBack board (Y-RH850-P1X-144PIN-PB-T1-V2) can be used as a standalone board, or can be mated with a mainboard (e.g. Y-RH850-X1X-MB-T1-V1) for extended functionality.

Main features:

- Socket for mounting of device
- Standalone operation of the board
- Direct supply of device voltage (typ. 3.3V, 5.0V and 1.25V) enabling single power supply (eVR) and dual power supply (DPS)
- Device programming capability
- Device debugging capability
- Pin headers for direct access to each device pin
- Reset switch
- MainOSC circuitry
- Connectors to MainBoard
- Operating temperature from 0°C to +40°C

This document describes the functionality provided by the PiggyBack board and guides the user through its operation.

For details regarding the operation of the microcontroller, refer to the corresponding user's manual.

This manual describes the following board revision:

- Y-RH850-P1X-144PIN-PB-T1-V2

For differences to the Y-RH850-P1X-144PIN-PB-T1-V1 board see **Chapter 12 'Revision History'**.

Note: Low active signals are highlighted with attached 'Z' to the pin or signal name in this document. E.g. the reset pin is named RESETZ. Please note that the corresponding pin or signal name is represented with an overline in the user documentation.

Chapter 2 Overview

2.1 Overview

Figures 1 and 2 provide a schematic view of the PiggyBack board.

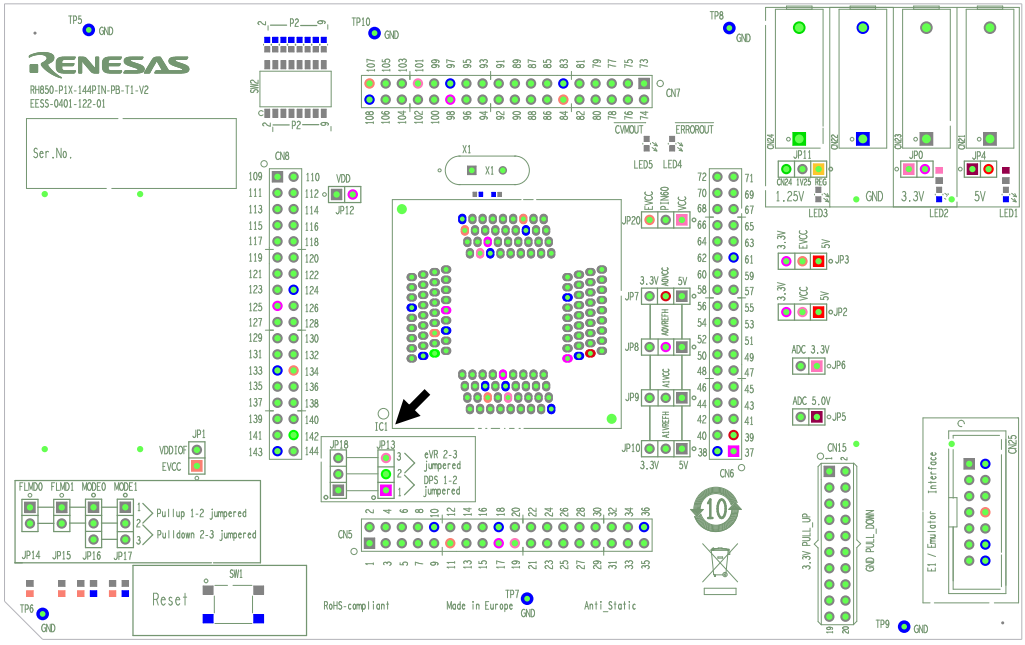


Figure 1 PiggyBack Board Schematic Top View

The black arrow denotes the position of socket pin #1.

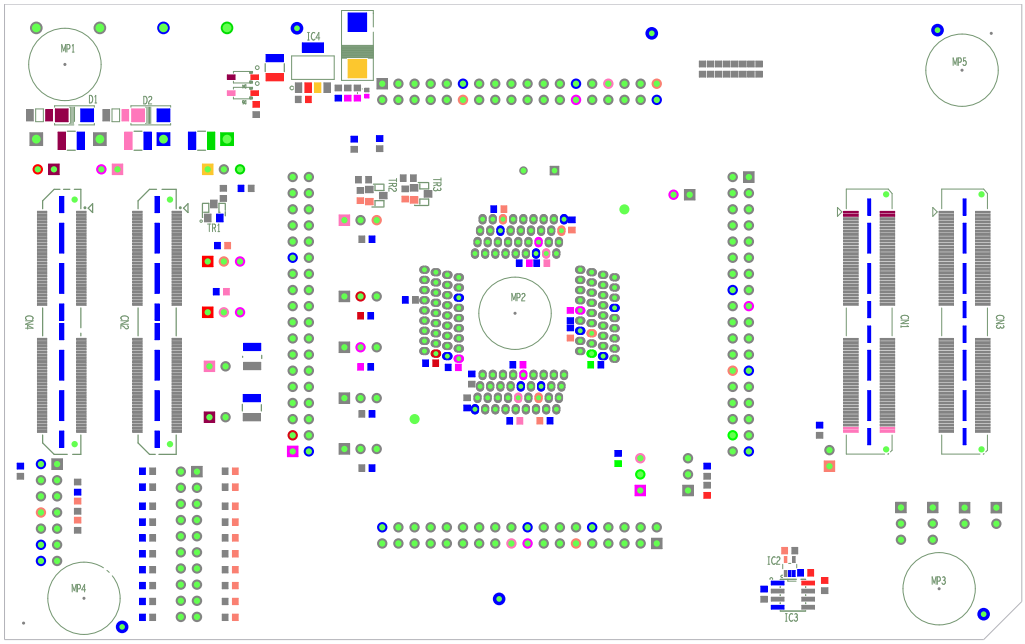


Figure 2 PiggyBack Board Schematic Bottom View

2.2 Mounting of the device

The board is designed for use with the following device:

- RH850/P1M in 144pin QFP package with 0.4mm pin pitch
- RH850/P1M-E in 144pin QFP package with 0.4mm pin pitch

The device must be placed inside the socket IC1. To insert the device, press down the lid of the socket, align the #1 pin of the device to the #1 pin of the socket, insert the device into the socket and release the lid.

Chapter 3 Power supply

3.1 Board power connection

For operation of the device, a supply voltage must be connected to the board. There are several possibilities to power the device.

Within this document the following voltages are considered as ‘typical’ connections:

Voltage1 = 5.0V

Voltage2 = 3.3V

Voltage3 = 1.25V

Direct voltage supply

Three different voltages can be supplied to the board.

The following connectors are available to supply those voltages directly:

- Four 4mm ‘banana-type’ connectors:
  - Three red connectors for voltages Voltage1 (CN21), Voltage2 (CN23) and Voltage3 (CN24).
  - A black connector for ground (GND) connection (CN22).
  Note: The three connectors are supplied with the board but not assembled.

For details about voltage distribution, refer to **Chapter 3.2 ‘Voltage distribution’**.

Supply by E1 emulator

The E1 emulator that is used for debug purposes and flash programming can also supply a single operating voltage (‘Dbg_Voltage’). This voltage is connected via EVCC to the board.

See the documentation of the E1 and **Chapter 5 ‘Debug and Programming interface’** for details.

Supply by MainBoard

In case the PiggyBack board is mounted on a MainBoard, Voltage1 and Voltage2 are supplied by the on-board regulators of the MainBoard.

CAUTION: *Do not supply Voltage1 or Voltage2 directly to the PiggyBack board in case it is mounted on the MainBoard.*

For each of the voltages, Voltage1, Voltage2 and Voltage3 a green LED is available to signal that the related voltage is available on the PiggyBack board. The corresponding LEDs are placed directly beneath the connectors of the related voltage.

- Voltage1 is signalled by LED1
- Voltage2 is signalled by LED2
- Voltage3 is signalled by LED3

3.2 Voltage distribution

The table shows the required device power supply pins. For detailed explanation of their function, please refer to the user documentation of the corresponding device:

Device Supply Pins
VCC
EVCC
AnVCC (n = 0, 1)
AnVREFH (n = 0, 1)
VDD (VCL)

Additional one power supply for the MainBoard can be selected:

Supply voltage	Function
VDDIOF	IO supply voltage for components located on a connected mainboard.

The following figure shows the configurable voltage distribution on the PiggyBack board.

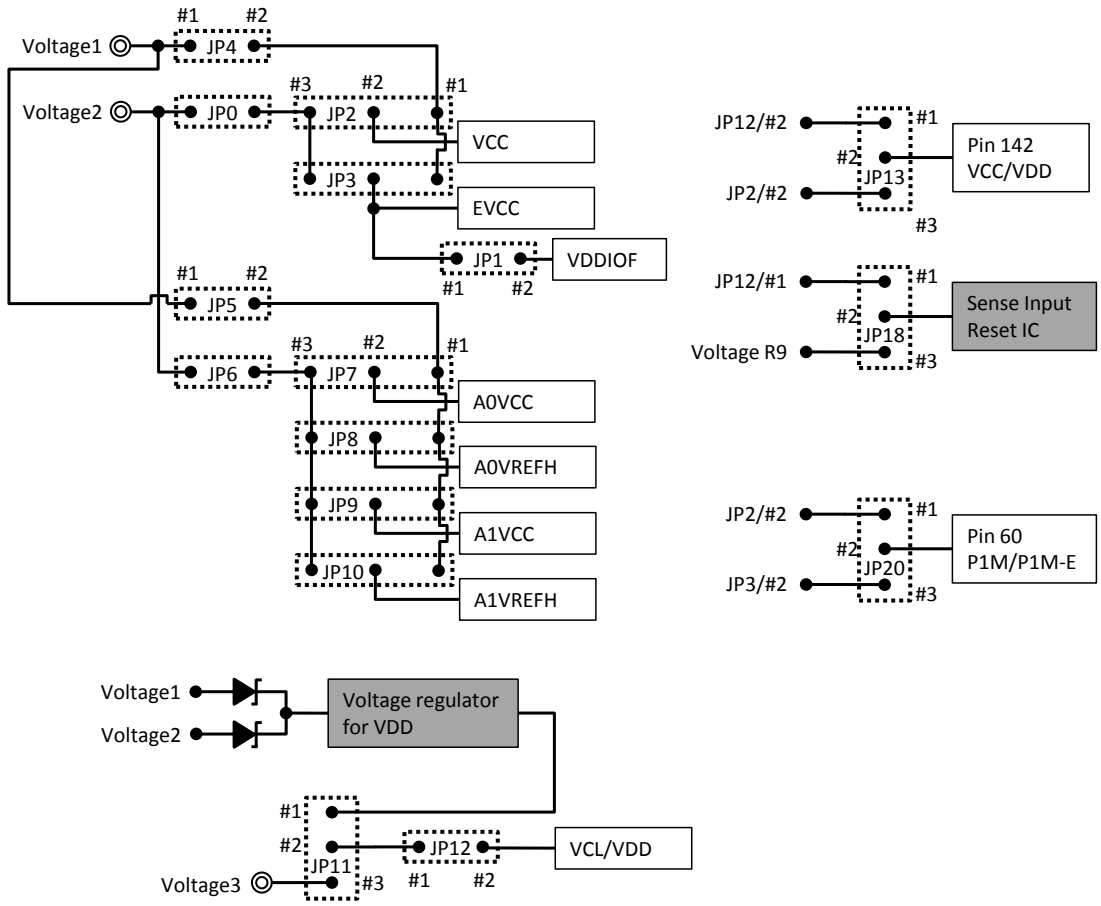


Figure 3 Voltage Distribution on the PiggyBack Board

- All power supply lines can be interrupted by jumpers. This provides the possibility to measure the current consumption of each individual power domain of the device.
- The IO supply voltage for the Mainboard (VDDIOF) can be connected via jumper JP1 to EVCC, if the PiggyBack board is mounted on a MainBoard.
- In case of a DPS device, VDD can be powered either directly from the 'banana-type' connector (Voltage3 – CN24) or by an on-board voltage regulator. Thereby even a DPS device can be operated with one single voltage supply (Voltage1 or Voltage2).
- The source for VDD is selectable by the jumper JP11. The jumper JP12 connects the voltage, configured by JP11 with the VDD pins.

CAUTION: *Jumper JP12 must not be connected in case of an eVR device. In this case the connected pins function as VCL pins and must not be supplied with a voltage.*

- Jumpers JP13 and JP18 are used to configure basic power supply type of the used microcontroller, i.e. eVR or DPS. Jumper JP13 configures voltage supplied to the pin #142. The mandatory voltage for the sense input of the on-board Reset IC is selected via jumper JP18.
- Jumper JP20 configures the voltage supplied to the pin #60 of the device

For more details, please refer to **Chapter 11 'Schematic'**. For typical configuration of the jumpers, please refer to **Chapter 8 'Jumper Configuration'**.

Chapter 4 Clock sources

One external crystal oscillator for the device clock supply is provided with the board.

4.1 MainOsc

A crystal or ceramic resonator can be mounted on socket X1.

A 16Mhz oscillator is supplied with the board.

Chapter 5 Debug and Programming interface

For connection of the microcontroller debug and flash programming tools, the connector CN25 with fourteen pins is provided.

The signal connection of the connector CN25 is shown in the table below:

CN25 Pin	Device Port	Device Signal
1	JP0_2	FLSCI3SCKI (FPCK) / DCUTCK / LPDCLK
2	GND	GND
3	JP0_4	DCUTRSTZ
4	FLMD0	FLMD0
5	JP0_1	FLSCI3TXD (FPDT) / DCUTDO / LPDO
6	-	-
7	JP0_0	FLSCI3RXD (FPDR) / FLSCI3TXD (FPDT), DCUTDI / LPDI / LPDIO
8	‘Dbg_Voltage’	EVCC
9	JP0_3	DCUTMS
10	-	-
11	JP0_5	DCURDYZ / LPDCLKOUT
12	GND	-
13	RESETZ	RESETZ
14	GND	-

Chapter 6 Connectors for ports of device

Connection to each pin of the devices is possible via the connectors CN5 to CN8. Please refer to the corresponding user's manual for available pins on the used device.

CAUTION: *The pin headers are directly connected to the pins of the device, therefore special care must be taken to avoid any (e.g. electrostatic) damage to the device.*

6.1 Push button for RESET

In order to issue a RESET to the device, the push-button SW1 is available.

For a correct start-up of the device the type (DPS or eVR) must be configured correctly via JP18. Please refer to **Chapter 8 Jumper Configuration**.

6.2 Mode Selection

The PiggyBack Board gives the possibility to configure the following mode pins

- FLMD0 via jumper JP14
- FLMD1 via jumper JP15
- MODE0 via jumper JP16
- MODE1 via jumper JP17

To apply "High" or "Low" to the mode pins, the pins 1 and 2, or the pins 2 and 3 (if available) of the corresponding jumper must be shorted, respectively.

Note: Pin 1 of all jumpers is marked by a small circle.

CAUTION: *Be careful in configuration of mode related pins, as wrong configuration can cause irregular behaviour of the devices. Be sure to check the corresponding user's manual, for details, which modes are specified for the used device.*

6.3 Connectors to MainBoard

Four connectors (CN1 to CN4) are available to connect the PiggyBack board to a MainBoard.

The signal connection of each connector is described in the following tables.

6.3.1 Connector CN1

Regarding detailed explanation on the MainBoard's function, please refer to the corresponding user's manual of supported MainBoards.

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
1	-	-		2	-	-
3	-	-		4	-	-
5	RESET	RESET		6	NMI	P3_14
7	WAKE	-		8	-	-
9	INT0	P3_4		10	INT1	P2_5
11	INT2	P3_7		12	INT3	P3_12
13	-	-		14	-	-
15	UART0TX	-		16	UART1TX	-

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
17	UART0RX	-		18	UART1RX	-
19	LIN0TX	P3_5		20	LIN1TX	P2_4
21	LIN0RX	P3_4		22	LIN1RX	P2_5
23	IIC0SDL	-		24	IIC1SDL	-
25	IIC0SDA	-		26	IIC1SDA	-
27	CAN0TX	P2_1		28	CAN1TX	P3_13
29	CAN0RX	P2_0		30	CAN1RX	P3_12
31	SENT0IN	P5_14		32	SENT1IN	P0_1
33	SENT0OUT	P0_0		34	SENT1OUT	P3_11
35	PSI50Rx	P5_14		36	PSI51Rx	P5_9
37	PSI50Tx	P0_0		38	PSI51Tx	P5_10
39	PSI50Snyc	-		40	PSI51Sync	-
41	FLX0TX	P4_0		42	FLX0EN	P4_1
43	FLX0RX	P4_2		44	FLXSTPWT	P4_4
45	FLX1TX	P4_5		46	FLX1EN	P4_6
47	FLX1RX	P4_3		48	FLX reserved	P3_14
49	-	-		50	-	-
51	ETH0MDIO	-		52	ETH0MDC	-
53	ETH0RXD0	-		54	EH0TXD0	-
55	ETH0RXD1	-		56	EH0TXD1	-
57	ETH0RXD2	-		58	EH0TXD2	-
59	ETH0RXD3	-		60	EH0TXD3	-
61	ETH0RXDCLK	-		62	ETH0TXCLK	-
63	ETH0RXER	-		64	ETH0TXER	-
65	ETH0CRSDV	-		66	ETH0TXEN	-
67	ETH0RXDV	-		68	ETH0COL	-
69	ETH0RESET	-		70	ETH0LINK	-
71	-	-		72	-	-
73	-	-		74	-	-
75	-	-		76	-	-
77	-	-		78	-	-
79	-	-		80	-	-
81	-	-		82	-	-
83	-	-		84	-	-
85	DIGIO_0	P5_8		86	DIGIO_1	P0_2
87	DIGIO_2	P0_13		88	DIGIO_3	P1_1
89	DIGIO_4	P1_2		90	DIGIO_5	P1_3
91	DIGIO_6	P1_4		92	DIGIO_7	P2_3
93	DIGIO_8	P2_6		94	DIGIO_9	P2_7
95	DIGIO_10	P2_8		96	DIGIO_11	P2_9
97	DIGIO_12	P3_3		98	DIGIO_13	P3_6
99	DIGIO_14	P3_9		100	DIGIO_15	P3_10
101	-	-		102	-	-

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
103	MUX0	-		104	MUX1	-
105	MUX2	-		106	-	-
107	ADC0	ADCx0I7		108	ADC1	ADCx0I6
109	ADC2	ADCx0I5		110	ADC3	ADCx0I4
111	ADC4	ADCx0I3		112	ADC5	ADCx0I2
113	ADC6	ADCx0I1		114	ADC7	ADCx0I0
115	VDDIOF	-		116	VDDIOF	-
117	*Voltage1*	-		118	*Voltage1*	-
119	*Voltage1*	-		120	*Voltage1*	-

Note: 'x' is a placeholder in above ADC related pin names. The name of ADC pins differ depending on the device. For the corresponding pin name, please refer to the user's manual of the used device.

6.3.2 Connector CN2

Regarding detailed explanation on the MainBoard's function, please refer to the corresponding user's manual of supported MainBoards.

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
1	CAN2TX	P5_5		2	-	-
3	CAN2RX	P5_6		4	-	-
5	-	-		6	-	-
7	-	-		8	-	-
9	-	-		10	-	-
11	-	-		12	-	-
13	-	-		14	-	-
15	-	-		16	-	-
17	-	-		18	-	-
19	-	-		20	-	-
21	-	-		22	-	-
23	-	-		24	-	-
25	-	-		26	-	-
27	-	-		28	-	-
29	-	-		30	-	-
31	-	-		32	-	-
33	-	-		34	-	-
35	-	-		36	-	-
37	-	-		38	-	-
39	-	-		40	-	-
41	-	-		42	-	-
43	-	-		44	-	-
45	-	-		46	-	-
47	-	-		48	-	-

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
49	-	-		50	-	-
51	-	-		52	-	-
53	-	-		54	-	-
55	-	-		56	-	-
57	-	-		58	-	-
59	-	-		60	-	-
61	-	-		62	-	-
63	-	-		64	-	-
65	-	-		66	-	-
67	-	-		68	-	-
69	-	-		70	-	-
71	-	-		72	-	-
73	-	-		74	-	-
75	-	-		76	-	-
77	-	-		78	-	-
79	-	-		80	-	-
81	-	-		82	-	-
83	-	-		84	-	-
85	-	-		86	-	-
87	-	-		88	-	-
89	-	-		90	-	-
91	-	-		92	-	-
93	-	-		94	-	-
95	-	-		96	-	-
97	-	-		98	-	-
99	-	-		100	-	-
101	-	-		102	-	-
103	-	-		104	-	-
105	-	-		106	-	-
107	-	-		108	-	-
109	-	-		110	-	-
111	-	-		112	-	-
113	-	-		114	-	-
115	-	-		116	-	-
117	-	-		118	-	-
119	-	-		120	-	-

6.3.3 Connector CN3

Regarding detailed explanation on the MainBoard's function, please refer to the corresponding user's manual of supported MainBoards.

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
1	-	-		2	-	-
3	-	-		4	-	-
5	-	-		6	-	-
7	-	-		8	-	-
9	-	-		10	CSIH2CSS0	P1_1
11	-	-		12	-	-
13	-	-		14	-	-
15	-	-		16	-	-
17	-	-		18	-	-
19	-	-		20	-	-
21	CSIH2CSS1	P3_3		22	CSIH2CSS7	P3_9
23	-	-		24	-	-
25	-	-		26	DIGIO	P0_0
27	-	-		28	CSIH2SO	P1_3
29	CSIH2SC	P1_4		30	CSIH2SI	P1_2
31	-	-		32	-	-
33	-	-		34	-	-
35	-	-		36	-	-
37	-	-		38	-	-
39	DIGIO	P0_1		40	-	-
41	-	-		42	-	-
43	-	-		44	-	-
45	-	-		46	-	-
47	-	-		48	-	-
49	-	-		50	-	-
51	-	-		52	-	-
53	-	-		54	-	-
55	-	-		56	-	-
57	-	-		58	-	-
59	-	-		60	-	-
61	-	-		62	-	-
63	-	-		64	-	-
65	-	-		66	-	-
67	-	-		68	-	-
69	-	-		70	-	-
71	-	-		72	-	-
73	-	-		74	-	-
75	-	-		76	-	-
77	-	-		78	-	-

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
79	-	-		80	-	-
81	-	-		82	-	-
83	-	-		84	-	-
85	-	-		86	-	-
87	-	-		88	-	-
89	-	-		90	-	-
91	-	-		92	-	-
93	-	-		94	-	-
95	-	-		96	-	-
97	-	-		98	-	-
99	-	-		100	-	-
101	-	-		102	-	-
103	-	-		104	-	-
105	-	-		106	-	-
107	-	-		108	-	-
109	-	-		110	-	-
111	-	-		112	-	-
113	-	-		114	-	-
115	-	-		116	-	-
117	-	-		118	-	-
119	-	-		120	-	-

6.3.4 Connector CN4

The here described functions are not available on any of the currently available Mainboards. They are only reserved for a potential future update.

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
1	-	-		2	-	-
3	-	-		4	-	-
5	ERROROUT	ERROROUT		6	CVMOUT	CVMOUT
7	-	-		8	-	-
9	ENC0 A	P4_0		10	ENC0 B	P4_1
11	ENC0 Z	P4_2		12	ENC1 A	P4_4
13	ENC1 B	P4_5		14	ENC1 Z	P4_6
15	Hi-Z control 0	P3_14		16	Hi-Z control 1	P0_2
17	-	-		18	-	-
19	TAUD0ch0	P3_5		20	TAUD0ch1	P5_0
21	TAUD0ch2/3	P5_1		22	TAUD0ch4/5	P5_4
23	TAUD0ch6/7	P5_5		24	TAUD0ch8/9	P5_6
25	TAUD0ch10/11	P5_7		26	TAUD0ch12/13	P5_8
27	TAUD0ch14/15	P5_9		28	-	-

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
29	TAUD1ch0/1	P2_11		30	TAUD1ch2/3	P2_12
31	TAUD1ch4/5	P2_13		32	TAUD1ch6/7	P2_14
33	TAUD1ch8/9	P2_15		34	TAUD1ch10/11	P3_0
35	TAUD1ch12/13	P3_1		36	TAUD1ch14/15	P3_2
37	-	-		38	-	-
39	-	-		40	-	-
41	-	-		42	-	-
43	TSG30STOut	P2_2		44	TSG30PWMOut1	P2_3
45	TSG30PWMOut2	P2_5		46	TSG30PWMOut3	P2_6
47	TSG30PWMOut4	P2_7		48	TSG30PWMOut5	P2_8
49	TSG30PWMOut6	P2_9		50	TSG30HSensIn0	P4_0
51	TSG30HsensIn1	P4_1		52	TSG30HsensIn2	P4_2
53	TSG31STOut	P3_6		54	TSG31PWMOut1	P3_7
55	TSG31PWMOut2	P3_8		56	TSG31PWMOut3	P3_9
57	TSG31PWMOut4	P3_10		58	TSG31PWMOut5	P3_12
59	TSG31PWMOut6	P3_13		60	TSG31HsensIn0	P4_4
61	TSG31HsensIn1	P4_5		62	TSG31HsensIn2	P4_6
63	-	-		64	-	-
65	TPBOut	P2_2		66	-	-
67	-	-		68	-	-
69	CSIH0SI	P2_4		70	CSH0CLK	P2_6
71	CSIH0SO	P2_5		72	CSIH0CSS0	P2_7
73	CSIH0CSS1	P2_8		74	-	-
75	CSIH1SI	P2_7		76	CSIH1CLK	P2_9
77	CSIH1SO	P2_8		78	-	-
79	-	-		80	-	-
81	ADC1-0	ADCx1I0		82	ADC1-1	ADCx1I1
83	ADC1-2	ADCx1I2		84	ADC1-3	ADCx1I3
85	ADC1-4	ADCx1I4		86	ADC1-5	ADCx1I5
87	ADC1-6	ADCx1I6		88	ADC1-7	ADCx1I7
89	ADC1-8	ADCx1I8		90	ADC1-9	ADCx1I9
91	ADC1-10	ADCx1I10		92	ADC1-11	ADCx1I11
93	-	-		94	-	-
95	-	-		96	-	-
97	-	-		98	-	-
99	-	-		100	-	-
101	-	-		102	-	-
103	-	-		104	-	-
105	-	-		106	-	-
107	-	-		108	-	-
109	-	-		110	-	-
111	-	-		112	-	-
113	-	-		114	-	-

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
115	-	-		116	-	-
117	-	-		118	-	-
119	-	-		120	-	-

Note: ‘x’ is a placeholder in above ADC related pin names. The name of ADC pins differ depending on the device. For the corresponding pin name, please refer to the user’s manual of the used device.

Chapter 7 Other circuitry

7.1 Signalling for CVMOUTZ and ERROROUTZ

Two red LEDs, LED5 and LED4 are available two indicate a “low” output signal from CVMOUTZ and ERROROUTZ, respectively.

7.2 Pin Headers for Pull-Down and Pull-Up

A connector CN15 is available to enable easy connection to EVCC or GND via pull-up or pull-down resistances, respectively.

Hereby uneven pins from 1 to 19 (in total ten) are configured as pull-up pin headers, while the even numbers from 2 to 20 (in total ten) can be used for pull-down.

By connecting device port pins from CN5 – 8 to CN9 it is therefore possible to pull a desired port pin to “Low” or “High”.

7.3 Signalling LEDs

Eight LEDs are provided to allow visual observation of the output state of device pins P2_2 to P2_9. The LEDs can be individually connected to the corresponding pins via the dip-switch SW2.

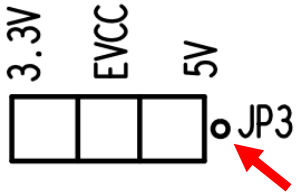
Chapter 8 Jumper Configuration

The function of the board can be configured via jumpers. This chapter describes the standard configuration, i.e. jumper setting for the intended devices. For the supported function of the used device (e.g. eVR or DPS), please refer to the corresponding HW user's manual.

The table has the following meaning:

- o: Jumper must be connected; valid for 2-pin jumpers (e.g. JP0)
- -: Jumper must not be connected
- #x-#y: Connect the pins #x and #y; valid for 3-pin jumpers (e.g. JP2)

The pin #1 can be identified by a small circle in the vicinity of the jumper



In this example (JP3), the pin #1 is on the right side. The marking circle is highlighted by the red arrow.

	Device											
	RH850/P1M						RH850/P1M-E					
	eVR		DPS				eVR		DPS			
			VDD from Board		VDD from external (CN24)				VDD from Board		VDD from external (CN24)	
Jumper #	3.3V	5.0V	3.3V	5.0V	3.3V	5.0V	3.3V	5.0V	3.3V	5.0V	3.3V	5.0V
0	o	-	o	-	o	-	o	-	o	-	o	-
1	*1											
2	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2
3	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2
4	-	o	-	o	-	o	-	o	-	o	-	o
5	-	o	-	o	-	o	-	o	-	o	-	o
6	o	-	o	-	o	-	o	-	o	-	o	-
7	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2
8	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2
9	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2
10	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2	#2-#3	#1-#2
11	-	-	#1-#2	#1-#2	#2-#3	#2-#3	-	-	#1-#2	#1-#2	#2-#3	#2-#3
12	-	-	o	o	o	o	-	-	o	o	o	o
13	#2-#3	#2-#3	#1-#2	#1-#2	#1-#2	#1-#2	#2-#3	#2-#3	#1-#2	#1-#2	#1-#2	#1-#2
14	*2											
15												
16												
17												
18	#2-#3	#2-#3	#1-#2	#1-#2	#1-#2	#1-#2	#2-#3	#2-#3	#1-#2	#1-#2	#1-#2	#1-#2
20	#2-#3	#2-#3	#2-#3	#2-#3	#2-#3	#2-#3	#1-#2	#1-#2	#1-#2	#1-#2	#1-#2	#1-#2

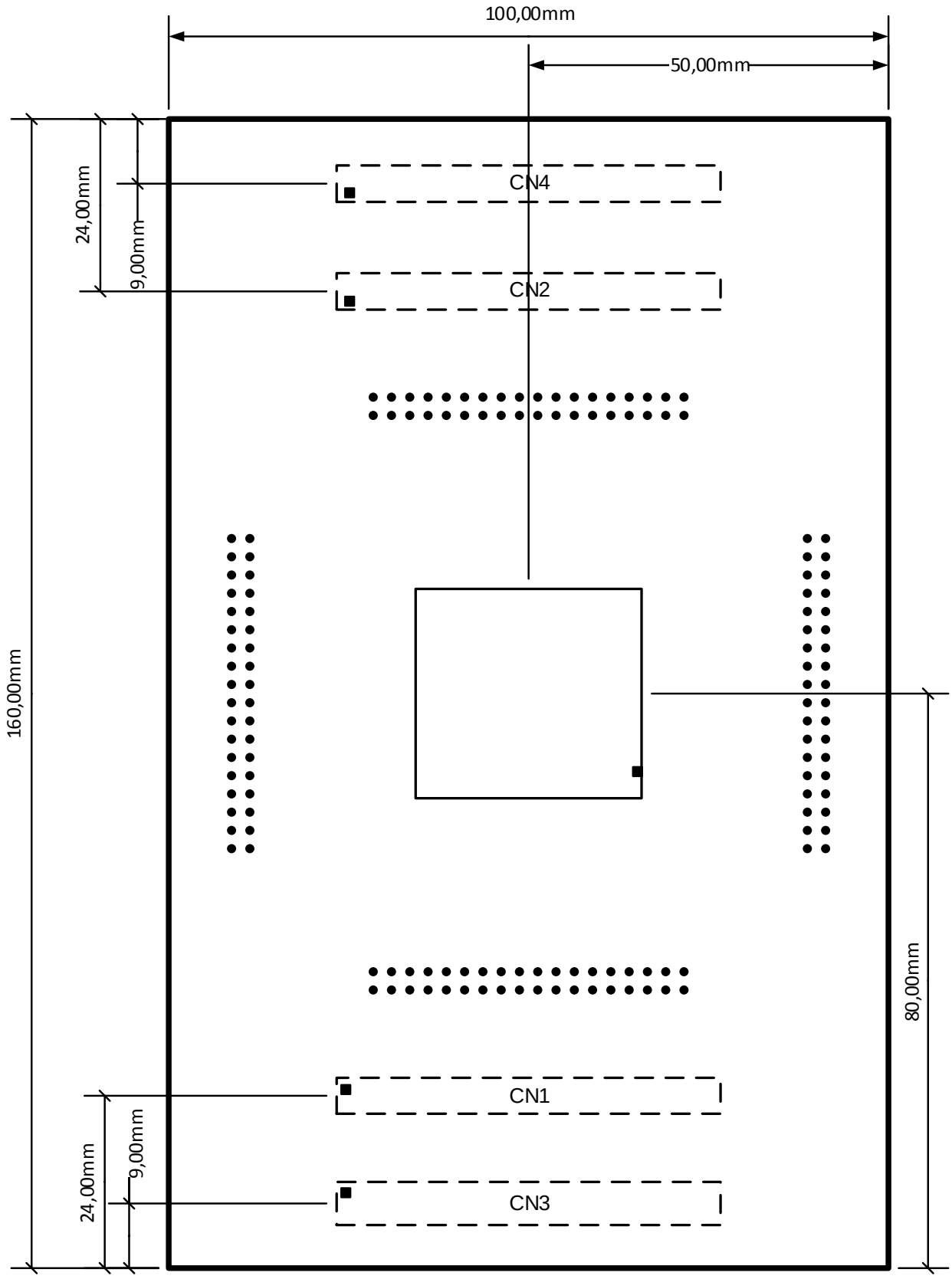
Note *1: Jumper JP1 must be connected, if the board is mounted on a mainboard.

Note *2: These jumpers shall not be connected for normal usage of the device. With these jumpers the device mode can be manipulated. Please make sure to check the corresponding HW user's manual of the used device for supported modes. Wrong configuration and operation of the device outside of its specification can cause irregular behaviour of the device and long term damage cannot be excluded.

Chapter 9 Precautions

There are no known limitations for this board.

Chapter 10 Mechanical dimensions

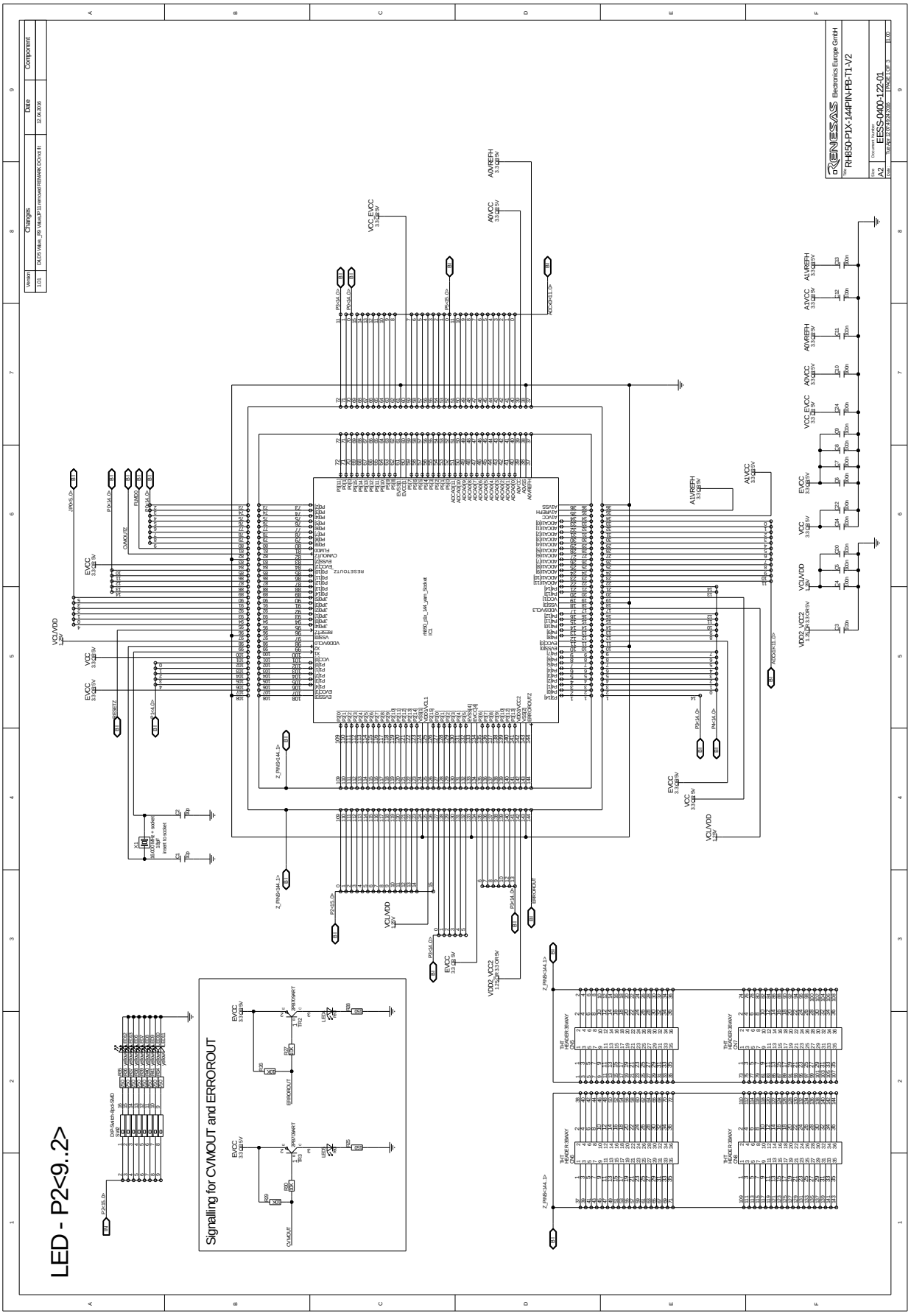


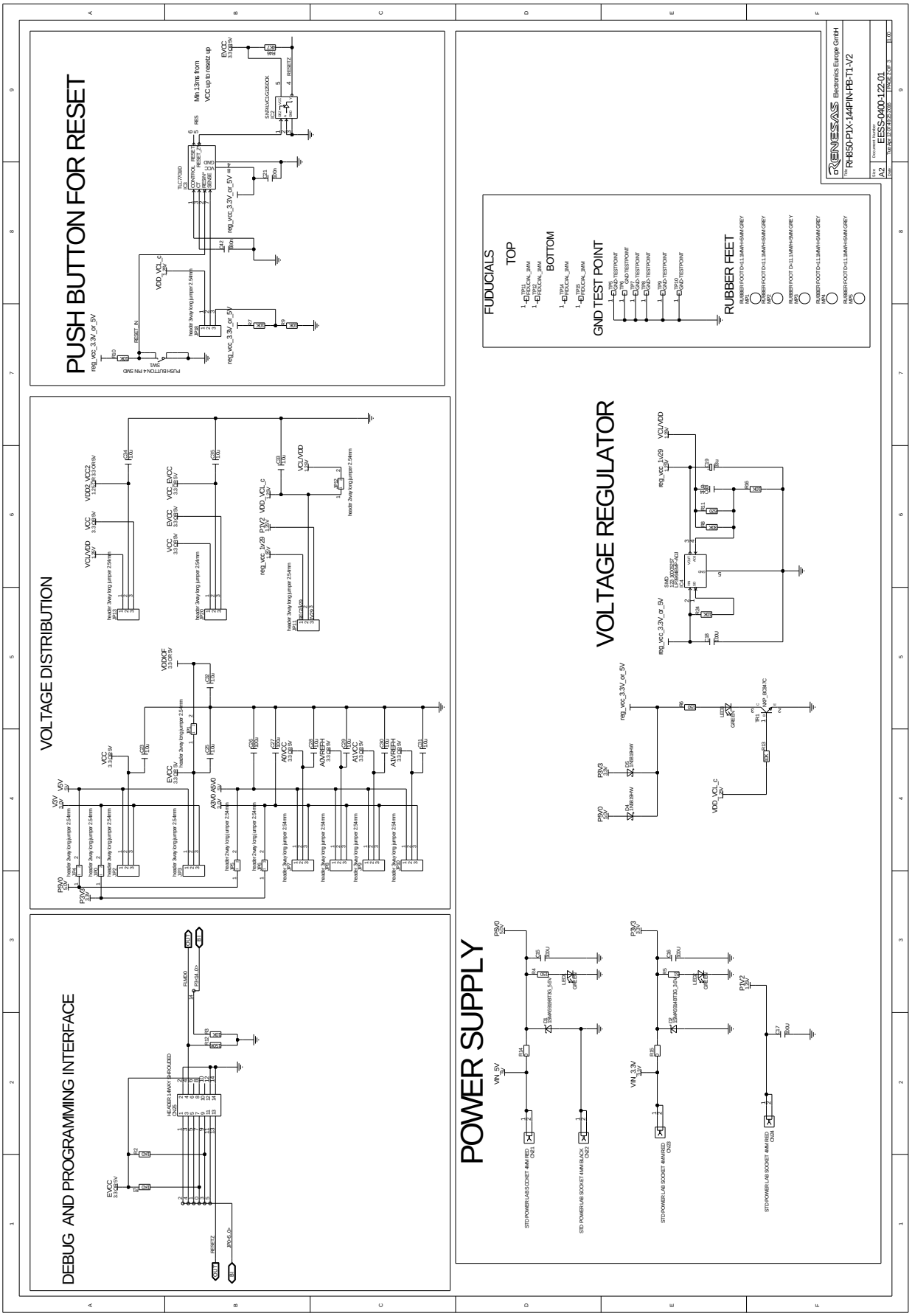
Chapter 11 Schematic

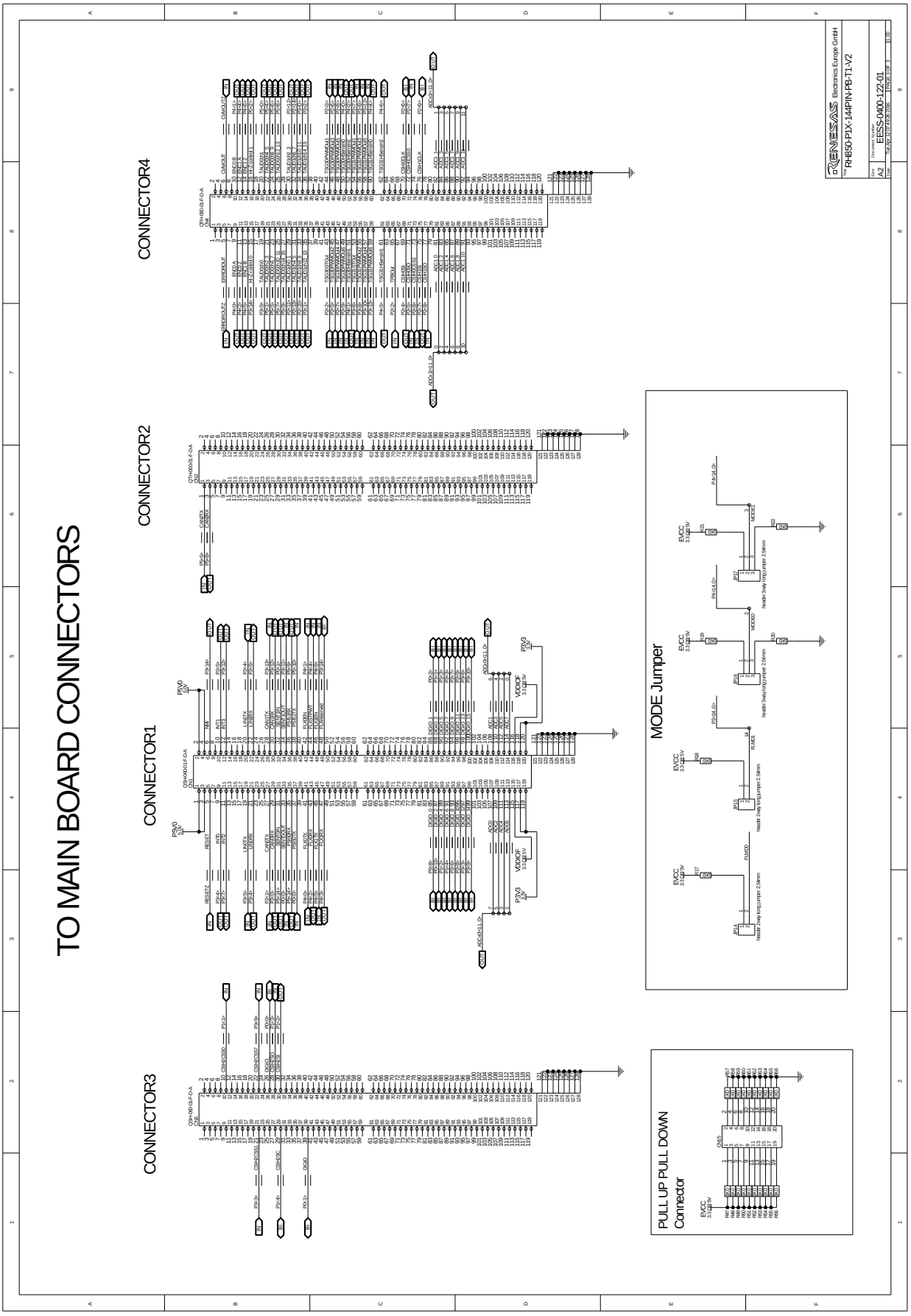
***CAUTION**: The schematic shown in this document is not intended to be used as a reference for mass production. Any usage in an application design is in sole responsibility of the customer.*

The following components described in the schematic are provided with but not mounted on the board:

- Standard 4mm power lab sockets
  - CN21
  - CN22
  - CN23
  - CN24


LED - P2<9..2>
Signalling for CVMOUT and ERROROUT
RH850-PIX-144PIN-PB-T1-V2
EESS-0400-122-01


PUSH BUTTON FOR RESET
VOLTAGE DISTRIBUTION
DEBUG AND PROGRAMMING INTERFACE
POWER SUPPLY
VOLTAGE REGULATOR
FUDUCIALS
TOP
BOTTOM
GND TEST POINT
RUBBER FEET
RENESAS Electronics Europe GmbH
RH850-P1X-144PIN-PB-T1-V2
EESS-0400-122-01


TO MAIN BOARD CONNECTORS
CONNECTOR4
CONNECTOR2
CONNECTOR1
CONNECTOR3
MODE Jumper
PULL UP PULL DOWN
Connector
RENESAS Electronics Europe GmbH
RH850-P1X-144PIN-PB-T1-V2
EESS-0400-122-01

Chapter 12 Revision History

The table provides information about the major changes of the document versions.

Date	Version	Description
2016-05-25	1.0	Initial release

Differences to the Y-RH850-P1X-144PIN-PB-T1-V1

- Support of RH850/P1M-E devices (configured via JP20)
- Enhanced Reset circuit
- Error signalling (ERROROUT -> LED4, CVMOUT -> LED5)
- GPIO signal LEDs for P2_2 to P2_9 (LED6 – 13)
- Pin header (CN15) with pull-down and pull-up supporting easy setting of “Low” and ”High” to device pins
- Support of functions on new mainboards (touchpad, additional com I/F) by adding functions to CN2 and CN3
- Jumper for every voltage domain, to support individual current measurement
- Jumper JP14 – JP17 for mode setting
- Changed pull-down resistance (R12) at FLMD0

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