NEC

K0 Family

8-Bit Single-Chip Microcontrollers

Programmer's Reference Manual

μPD78014/14Y Subseries
μPD78014H Subseries
μPD78018F/18FY Subseries
μPD780208 Subseries
μPD780024/24Y Subseries
μPD780034/34Y Subseries
μPD78044F Subseries
μPD78044H Subseries
μPD78054/54Y Subseries
μPD78058F/58FY Subseries
μPD780058/58Y Subseries
μPD78064/64Y Subseries
μPD78064B Subseries
μPD780308/308Y Subseries
μPD78078/78Y Subseries
μPD78075B/75BY Subseries
μPD78070A/70AY Subseries
μPD78083 Subseries

Document No. U13838EU1V0UM00 (1st edition)
Date Published January 1999 N

© 1999 NEC Electronics Inc. All rights reserved. Printed in U.S.A.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

A strong electric field to which a MOS device is exposed can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible and dissipate it at once when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static-shielding bag, or conductive material. All test and measurement tools, as well as the work bench and floor, should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for PW boards with semiconductor devices on them.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

Nonconnection for CMOS device inputs can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently from bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and according to the specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define the initial status of a MOS device. The production process of MOS does not define the initial operational status of the device. Immediately after the power source is turned ON, devices with a reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings, or the contents of registers. A device is not initialized until the reset signal is received. The reset operation must be executed immediately after power-on for devices having a reset function.

FIP and IEBus are trademarks of NEC Corporation.

Caution: The following products are provided with an I²C bus interface circuit:
μPD78014Y Subseries, μPD78018FY Subseries, μPD780024Y Subseries, μPD780034Y Subseries, μPD78054Y Subseries, μPD78058FY Subseries, μPD780058Y Subseries, μPD78064Y Subseries, μPD78078Y Subseries, μPD78075BY Subseries, μPD78070AY Subseries, μPD780308Y Subseries

Purchase of NEC I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

In North America: No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Electronics Inc. (NECEL). The information in this document is subject to change without notice. ALL DEVICES SOLD BY NECEL ARE COVERED BY THE PROVISIONS APPEARING IN NECEL TERMS AND CONDITIONS OF SALES ONLY, INCLUDING THE LIMITATION OF LIABILITY, WARRANTY, AND PATENT PROVISIONS. NECEL makes no warranty, express, statutory, implied, or by description, regarding information set forth herein or regarding the freedom of the described devices from patent infringement. NECEL assumes no responsibility for any errors that may appear in this document. NECEL makes no commitments to update or to keep current information contained in this document. The devices listed in this document are not suitable for use in applications such as, but not limited to, aircraft control systems, aerospace equipment, submarine cables, nuclear reactor control systems, and life-support systems. “Standard” quality grade devices are recommended for computers, office equipment, communication equipment, test and measurement equipment, machine tools, industrial robots, audio and visual equipment, and other consumer products. For automotive and transportation equipment, traffic control systems, and anti-disaster and anti-crime systems, it is recommended that the customer contact the responsible NECEL salesperson to determine the reliability requirements for any such application and any cost adder. NECEL does not recommend or approve use of any of its products in life-support devices or systems or in any application where failure could result in injury or death. If customers wish to use NECEL devices in applications not intended by NECEL, customers must contact the responsible NECEL salespeople to determine NECEL's willingness to support a given application.

No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors that may appear in this document. NEC Corporation does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied, or otherwise, is granted under any patents, copyrights, or other intellectual property rights of NEC Corporation or others. Although NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features. NEC devices are classified into the following three quality grades: “Standard,” “Special,” and “Specific.” The Specific quality grade applies only to devices developed based on a customer-designated “quality assurance program” for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers may check the quality grade of each device before using it in a particular application. Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment, and industrial robots. Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, and safety equipment (not specifically designed for life support). Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, and life-support systems or medical equipment for life support, etc. The quality grade of NEC devices is “Standard” unless otherwise specified in NEC’s data sheets or data books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, pIease contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.1.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

NEC Electronics (France) S.A.
Spain Office
Madrid, Spain
Tel: 01-504-2787
Fax: 01-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore 1130
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-719-2377
Fax: 02-719-5951

NEC do Brasil S.A.
Cumbica-Guarulhos-SP, Brasil
Tel: 011-6465-6810
Fax: 011-6465-6829

J98. 2

[MEMO]

CONTENTS

INTRODUCTION 19

CHAPTER 1 K0 PRODUCT SELECTION GUIDE 21

CHAPTER 2 ADDRESSING MODES 23
2.1 Data Memory Addressing 23
2.2 Instruction Address Addressing 25
2.2.1 Relative Addressing 25
2.2.2 Immediate Addressing 26
2.2.3 Table Indirect Addressing 27
2.2.4 Register Addressing 28
2.3 Operand Address Addressing 29
2.3.1 Implied Addressing 29
2.3.2 Register Addressing 30
2.3.3 Direct Addressing 31
2.3.4 Short Direct Addressing 32
2.3.5 Special Function Register (SFR) Addressing 33
2.3.6 Register Indirect Addressing 34
2.3.7 Based Addressing 34
2.3.8 Based Indexed Addressing 35
2.3.9 Stack Addressing 35

CHAPTER 3 REGISTERS AND STACK OPERATION 37
3.1 General Purpose Registers 37
3.2 Processor Registers 38
3.2.1 Control Registers 38
(1) Program counter (PC) 38
(2) Program status word (PSW) 38
(3) Stack pointer (SP) 39
3.3 Stack Operation 39

CHAPTER 4 INSTRUCTION SET 41
4.1 Operand Descriptions 41
4.1.1 Description of “Flag” Column 42
4.2 Instruction Set Table 43
4.3 Instructions Listed by Addressing Type 51
4.3.1 8-Bit Instructions 51
4.3.2 16-Bit Instructions 53
4.3.3 Bit Manipulation Instructions 53
4.3.4 Call Instructions/Branch Instructions 54
4.3.5 Other Instructions 54

CHAPTER 5 SAMPLE PROGRAM 55
5.1 Test.asm 56
5.2 Test.bat 58
5.3 Test.prn 59
5.4 Test.p 62

CHAPTER 6 DEVICE MEMORY MAP AND SPECIAL FUNCTION REGISTERS 65
6.1 μPD78014, 78014H, and 78018F Subseries 66
6.1.1 Documentation Reference Information 66
6.1.2 Device Series Differences 66
6.1.3 Memory Address Space 67
6.1.4 Special Function Registers (SFRs) 74
(1) Registers controlling port functions 77
(2) Register controlling clock generator 79
(3) Registers controlling 16-bit timer/event counter 80
(4) Registers controlling 8-bit timer/event counter 85
(5) Registers controlling watch timer 89
(6) Registers controlling watchdog timer 91
(7) Registers controlling clock output function 93
(8) Registers controlling buzzer output function 94
(9) Registers controlling A/D converter 95
(10) Registers controlling serial interface channel 0 (Non-Y subseries) 97
(11) Registers controlling serial interface channel 0 (Y subseries) 103
(12) Registers controlling serial interface channel 1 110
(13) Registers controlling interrupt function 115
(14) Registers controlling test function 120
(15) Registers controlling external device expansion function 122
(16) Register controlling standby function 124
(17) Reset function 128
(18) Registers controlling ROM correction (mask ROM versions of μPD78018F/18FY subseries only) 131
(19) Register controlling internal memory capacity 132
(20) Register controlling internal expansion RAM capacity 134
6.2 μPD780208 Subseries 135
6.2.1 Documentation Reference Information 135
6.2.2 Memory Address Space 136
6.2.3 Special Function Registers (SFRs) 140
(1) Registers controlling port functions 142
(2) Registers controlling clock generator 144
(3) Registers controlling 16-bit timer/event counter 148
(4) Registers controlling 8-bit timer/event counter 152
(5) Registers controlling watch timer 156
(6) Registers controlling watchdog timer 158
(7) Registers controlling clock output function 160
(8) Registers controlling buzzer output function 161
(9) Registers controlling A/D converter 162
(10) Registers controlling serial interface channel 0 165
(11) Registers controlling serial interface channel 1 170

(12) Registers controlling FIP controller 175
(13) Registers controlling interrupt function 179
(14) Registers controlling test function 184
(15) Register controlling standby function 185
(16) Reset function 188
(17) Register controlling internal memory capacity 191
(18) Register controlling internal expansion RAM capacity 192
6.3 μPD780024 and 780034 Subseries 193
6.3.1 Documentation Reference Information 193
6.3.2 Device Series Differences 193
6.3.3 Memory Address Space 194
6.3.4 Special Function Registers (SFRs) 198
(1) Registers controlling port functions 201
(2) Register controlling clock generator 203
(3) Registers controlling 16-bit timer/event counter 204
(4) Registers controlling 8-bit timer/event counter 208
(5) Register controlling watch timer 211
(6) Registers controlling watchdog timer 212
(7) Registers controlling clock output function 214
(8) Registers controlling A/D converter 215
(9) Registers controlling serial interface (UART0) 217
(10) Register controlling serial interface (SIO3) 221
(11) Registers controlling serial interface (I^2C) 222
(12) Registers controlling interrupt function 231
(13) Registers controlling external device expansion function 237
(14) Register controlling standby function 238
(15) Reset function 241
(16) Register controlling internal memory capacity 244
6.4 μPD78044F and 78044H Subseries 245
6.4.1 Documentation Reference Information 245
6.4.2 Device Series Differences 245
6.4.3 Memory Address Space 246
6.4.4 Special Function Registers (SFRs) 254
(1) Registers controlling port functions 257
(2) Registers controlling clock generator 260
(3) Registers controlling 16-bit timer/event counter 263
(4) Registers controlling 8-bit timer/event counter 266
(5) Registers controlling watch timer 270
(6) Registers controlling watchdog timer 272
(7) Register controlling 6-bit up/down counter 274
(8) Registers controlling clock output function 275
(9) Registers controlling buzzer output function 276
(10) Registers controlling A/D converter 277
(11) Registers controlling serial interface channel 0 (μPD78044F Subseries only) 280
(12) Registers controlling serial interface channel 1 285
(13) Registers controlling FIP controller 292
(14) Registers controlling interrupt function 294
(15) Registers controlling test function 302
(16) Register controlling standby function 303

(17) Reset function 308
(18) Register controlling internal memory capacity 311
(19) Register controlling internal expansion RAM capacity 313
6.5 μPD78054, 78058F, and 780058 Subseries 315
6.5.1 Documentation Reference Information 315
6.5.2 Device Series Differences 315
6.5.3 Memory Address Space 316
6.5.4 Special Function Registers (SFRs) 322
(1) Registers controlling port functions 325
(2) Registers controlling clock generator 329
(3) Registers controlling 16-bit timer/event counter 331
(4) Registers controlling 8-bit timer/event counter 335
(5) Registers controlling watch timer 339
(6) Registers controlling watchdog timer 341
(7) Registers controlling clock output function 343
(8) Registers controlling buzzer output function 345
(9) Registers controlling A/D converter 346
(10) Register controlling D/A converter 349
(11) Registers controlling serial interface channel 0 (Non-Y Subseries) 350
(12) Registers controlling serial interface channel 0 (Y Subseries) 357
(13) Registers controlling serial interface channel 1 364
(14) Registers controlling serial interface channel 2 372
(15) Registers controlling real-time output port 379
(16) Registers controlling interrupt function 380
(17) Registers controlling test function 390
(18) Registers controlling external device expansion function 392
(19) Register controlling standby function 394
(20) Reset function 397
(21) Registers controlling ROM correction (μPD78058/58Y, 78058F/58FY, and 780058/58Y only) 400
(22) Register controlling internal memory capacity 401
(23) Register controlling internal expansion RAM capacity 406
6.6 μPD78064, 78064B, and 780308 Subseries 407
6.6.1 Documentation Reference Information 407
6.6.2 Device Series Differences 407
6.6.3 Memory Address Space 408
6.6.4 Special Function Registers (SFRs) 413
(1) Registers controlling port functions 416
(2) Registers controlling clock generator 419
(3) Registers controlling 16-bit timer/event counter 422
(4) Registers controlling 8-bit timer/event counters 1 and 2 427
(5) Registers controlling watch timer 431
(6) Registers controlling watchdog timer 433
(7) Registers controlling clock output function 435
(8) Registers controlling buzzer output function 437
(9) Registers controlling A/D converter 438
(10) Registers controlling serial interface channel 0 (Non-Y Subseries) 441
(11) Registers controlling serial interface channel 0 (Y Subseries) 448

(12) Registers controlling serial interface channel 2 455
(13) Registers controlling serial interface channel 3 (μPD780308/308Y Subseries only) 460
(14) Registers controlling LCD controller/driver 462
(15) Registers controlling interrupt function 465
(16) Registers controlling test function 473
(17) Register controlling standby function 475
(18) Reset function 478
(19) Register controlling internal memory capacity 481
(20) Register controlling internal expansion RAM capacity (μPD780308/308Y Subseries only) 484

6.7 μPD78078, 78075B, and 78070A Subseries 485

6.7.1 Documentation Reference Information 485
6.7.2 Device Series Differences 485
6.7.3 Memory Address Space 486
6.7.4 Special Function Registers (SFRs) 491
(1) Registers controlling port functions 495
(2) Registers controlling clock generator 499
(3) Registers controlling 16-bit timer/event counter 502
(4) Registers controlling 8-bit timer/event counters 1 and 2 507
(5) Registers controlling 8-bit timer/event counters 5 and 6 511
(6) Registers controlling watch timer 515
(7) Registers controlling watchdog timer 517
(8) Registers controlling clock output function 519
(9) Registers controlling buzzer output function 521
(10) Registers controlling A/D converter 522
(11) Register controlling D/A converter 525
(12) Registers controlling serial interface channel 0 (Non-Y Subseries) 526
(13) Registers controlling serial interface channel 0 (Y Subseries) 532
(14) Registers controlling serial interface channel 1 539
(15) Registers controlling serial interface channel 2 546
(16) Registers controlling real-time output port 551
(17) Registers controlling interrupt function 552
(18) Registers controlling test function 558
(19) Registers controlling external device expansion function 560
(20) Register controlling standby function 564
(21) Reset function 567
(22) Registers controlling ROM correction (μPD78078/78Y Subseries only) 571
(23) Register controlling internal memory capacity 572
(24) Register controlling internal expansion RAM capacity 573

6.8 μPD78083 Subseries 575

6.8.1 Documentation Reference Information 575
6.8.2 Memory Address Space 576
6.8.3 Special Function Registers (SFRs) 579
(1) Registers controlling port functions 581
(2) Registers controlling clock generator 583
(3) Registers controlling 8-bit timer/event counters 5 and 6 585

(4) Registers controlling watchdog timer 587
(5) Registers controlling clock output function 589
(6) Registers controlling buzzer output function 590
(7) Registers controlling A/D converter 591
(8) Registers controlling serial interface channel 2 594
(9) Registers controlling interrupt function 599
(10) Register controlling standby function 605
(11) Reset function 607
(12) Register controlling internal memory capacity 609

APPENDIX A INDEX (ARCHITECTURE) 611

APPENDIX B REGISTER INDEX 613
B.1 μPD78014/14Y, 78014H, and 78018F/18FY Subseries 613
B.2 μPD780208 Subseries 616
B.3 μPD780024/24Y and 780034/34Y Subseries 619
B.4 μPD78044F and 78044H Subseries 622
B.5 μPD78054/54Y, 78058F/58FY, 780058/58Y Subseries 625
B.6 μPD78064/64Y, 78064B, and 780308/308Y Subseries 629
B.7 μPD78078/78Y, 78075B/75BY, and 78070A/70AY Subseries 632
B.8 μPD78083 Subseries 636

LIST OF FIGURES (1/2)

Figure No.	Title	Page
2-1	Example of Data Memory Addressing (μPD780306, 780306Y)	23
2-2	Example of Data Memory Addressing (μPD780308, 780308Y)	24
3-1	Configuration of General Purpose Registers	37
3-2	Format of Program Counter	38
3-3	Format of Program Status Word	38
3-4	Format of Stack Pointer	39
3-5	Data To Be Saved on the Stack	39
3-6	Data To Be Restored from the Stack	40
6-1	Memory Map (μPD78011B/11BY, 11F/11FY, 11H)	67
6-2	Memory Map (μPD78012B/12BY, 12F/12FY, 12H)	68
6-3	Memory Map (μPD78013/13Y, 13F/13FY, 13H)	69
6-4	Memory Map (μPD78014/14Y, 78P014/14Y, 78014F/14FY, 14H)	70
6-5	Memory Map (μPD78015F/15FY)	71
6-6	Memory Map (μPD78016F/16FY)	72
6-7	Memory Map (μPD78018F/18FY, 78P018F/18FY)	73
6-8	Memory Map (μPD780204)	136
6-9	Memory Map (μPD780205)	137
6-10	Memory Map (μPD780206)	138
6-11	Memory Map (μPD780208, 78P0208)	139
6-12	Memory Map (μPD780021/21Y, 780031/31Y)	194
6-13	Memory Map (μPD780022/22Y, 780032/32Y)	195
6-14	Memory Map (μPD780023/23Y, 780033/33Y)	196
6-15	Memory Map (μPD780024/24Y, 780034/34Y, 78F0034/34Y)	197
6-16	Memory Map (μPD78042F)	246
6-17	Memory Map (μPD78043F)	247
6-18	Memory Map (μPD78044F)	248
6-19	Memory Map (μPD78044H)	249
6-20	Memory Map (μPD78045F)	250
6-21	Memory Map (μPD78045H)	251
6-22	Memory Map (μPD78046H)	252
6-23	Memory Map (μPD78P048A, 78P048B)	253
6-24	Memory Map (μPD78052/52Y)	316
6-25	Memory Map (μPD78053/53Y, 780053/53Y)	317
6-26	Memory Map (μPD78054/54Y, 78P054, 780054/54Y)	318
6-27	Memory Map (μPD78055/55Y, 780055/55Y)	319
6-28	Memory Map (μPD78056/56Y, 78056F/56FY, 780056/56Y)	320
6-29	Memory Map (μPD78058/58Y, 78P058/58Y, 78058F/58FY, 78P058F/58FY, 780058/58Y, 78F0058/58Y)	321
6-30	Memory Map (μPD78062/62Y)	408
6-31	Memory Map (μPD78063/63Y)	409
6-32	Memory Map (μPD78064/64Y/64B, 78P064/64Y/64B)	410
6-33	Memory Map (μPD780306/306Y)	411

LIST OF FIGURES (2/2)

Figure No.	Title	Page
6-34	Memory Map (μPD780308/308Y, 78P0308/308Y)	412
6-35	Memory Map (μPD78070A/70AY)	486
6-36	Memory Map (μPD78074B/74BY)	487
6-37	Memory Map (μPD78075B/75BY)	488
6-38	Memory Map (μPD78076/76Y)	489
6-39	Memory Map (μPD78078/78Y, 78P078/78Y)	490
6-40	Memory Map (μPD78081)	576
6-41	Memory Map (μPD78082)	577
6-42	Memory Map (μPD78P083)	578

LIST OF TABLES (1/1)

Table No.	Title	Page
1-1	K0 Microcontroller Subseries Product Guide	21
4-1	Operand Descriptions	41
4-2	Instruction Set	43
4-3	8-Bit Instructions Listed by Operand Type	52
4-4	16-Bit Instructions Listed by Operand Type	53
4-5	Bit Manipulations Listed by Operand Type	53
4-6	Call and Branch Instructions Listed by Operand Type	54
6-1	Special Function Register List (μPD78014/14Y, 78014H, and 78018F/18FY Subseries)	74
6-2	Interrupt Source List	115
6-3	Interrupt Sources and Flags	116
6-4	Hardware Status After Reset	129
6-5	Special Function Register List (μPD780208 Subseries)	140
6-6	Interrupt Source List	179
6-7	Interrupt Sources and Flags	180
6-8	Hardware Status After Reset	189
6-9	Special Function Register List (μPD780024/24Y and 780034/34Y Subseries)	198
6-10	Interrupt Source List	231
6-11	Interrupt Sources and Flags	232
6-12	Hardware Status After Reset	242
6-13	Special Function Register List (μPD78044F and 78044H Subseries)	254
6-14	Interrupt Source List	294
6-15	Interrupt Source List	295
6-16	Interrupt Sources and Flags	296
6-17	Hardware Status After Reset	309
6-18	Special Function Register List (μPD78054/54Y, 78058F/58FY, and 780058/58Y Subseries)	322
6-19	Interrupt Source List	380
6-20	Interrupt Source List	381
6-21	Interrupt Sources and Flags	382
6-22	Hardware Status After Reset	398
6-23	Special Function Register List (μPD78064/64Y, 78064B, and 780308/308Y Subseries)	413
6-24	Interrupt Source List	465
6-25	Interrupt Sources and Flags	466
6-26	Hardware Status After Reset	479
6-27	Special Function Register List (μPD78078/78Y, 78075B/75BY, and 78070A/70AY Subseries)	491
6-28	Interrupt Source List	552
6-29	Interrupt Sources and Flags	553
6-30	Hardware Status After Reset	568
6-31	Special Function Register List (μPD78083 Subseries)	579
6-32	Interrupt Source List	599
6-33	Interrupt Sources and Flags	600
6-34	Hardware Status After Reset	608

[MEMO]

DEVICES COVERED IN THIS MANUAL

K0 Series products included in this document

- μPD78014 Subseries: μPD78011B, 78012B, 78013, 78014, 78P014
- μPD78014Y Subseries: μPD78011BY, 78012BY, 78013Y, 78014Y, 78P014Y
- μPD78014H Subseries: μPD78011H, 78012H, 78013H, 78014H
- μPD78018F Subseries: μPD78011F, 78012F, 78013F, 78014F, 78015F, 78016F, 78018F, 78P018F
- μPD78018FY Subseries: μPD78011FY, 78012FY, 78013FY, 78014FY, 78015FY, 78016FY, 78018FY, 78P018FY
- μPD780208 Subseries: μPD780204, 780205, 780206, 780208, 78P0208
- μPD780024 Subseries: μPD780021, 780022, 780023, 780024
- μPD780024Y Subseries: μPD780021Y, 780022Y, 780023Y, 780024Y
- μPD780034 Subseries: μPD780031, 780032, 780033, 780034, 78F0034
- μPD780034Y Subseries: μPD780031Y, 780032Y, 780033Y, 780034Y, 78F0034Y
- μPD78044F Subseries: μPD78042F, 78043F, 78044F, 78045F, 78P048A
- μPD78044H Subseries: μPD78044H, 78045H, 78046H, 78P048B
- μPD78054 Subseries: μPD78052, 78053, 78054, 78P054, 78055, 78056, 78058, 78P058
- μPD78054Y Subseries: μPD78052Y, 78053Y, 78054Y, 78P054Y, 78055Y, 78056Y, 78058Y, 78P058Y
- μPD78058F Subseries: μPD78056F, 78058F, 78P058F
- μPD78058FY Subseries: μPD78056FY, 78058FY, 78P058FY
- μPD780058 Subseries: μPD780053, 780054, 780055, 780056, 780058, 78F0058
- μPD780058Y Subseries: μPD780053Y, 780054Y, 780055Y, 780056Y, 780058Y, 78F0058Y
- μPD78064 Subseries: μPD78062, 78063, 78064, 78P064
- μPD78064Y Subseries: μPD78062Y, 78063Y, 78064Y, 78P064Y
- μPD78064B Subseries: μPD78064B, 78P064B
- μPD780308 Subseries: μPD780306, 780308, 78P0308
- μPD780308Y Subseries: μPD780306Y, 780308Y, 78P0308Y
- μPD78078 Subseries: μPD78076, 78078, 78P078
- μPD78078Y Subseries: μPD78076Y, 78078Y, 78P078Y
- μPD78075B Subseries: μPD78074B, 78075B
- μPD78075BY Subseries: μPD78074BY, 78075BY
- μPD78070A Subseries: μPD78070A
- μPD78070AY Subseries: μPD78070AY
- μPD78083 Subseries: μPD78081, 78082, 78P083

[MEMO]

INTRODUCTION

This reference manual is intended for software and firmware engineers already familiar with the K0 device they are using. They can obtain programming data about the microcontroller without having to refer to the user's manuals for their device. The document describes the K0 architecture, addressing modes, registers, instruction set, stack operation, and special function registers (SFRs).

Contents Overview

Chapter 1: Product selection guide

Chapter 2: K0 memory map and addressing modes

Chapter 3: K0 registers and stack operations

Chapter 4: Contains two tables describing the instruction set, and a description of all keywords and operands. The first table lists all the instructions, their operands, and a description of the operation of each instruction. The second table is a matrix that the user can look up the first and second operands, and find a list of all instructions that use both operands

Chapter 5: Example K0 program module and associated listings generated by the assembler

Chapter 6: User Manual document numbers, memory maps, SFR information, status information during halt and stop modes, and SFR values after a reset for each K0 subseries:

a. μPD78014, μPD014H, and μPD78018F
b. μPD780208
c. μPD780024 and μPD0034
d. μP78044F and μPD78044H
e. μP78054, μPD78058F, and μPD780058
f. μPD78064, μPD78064B and μPD780308
g. μPD78070A, μPD78075B and μPD78078
h. μPD78083

Appendix A: Architecture index for Chapters 2-5

Appendix B: Register index for Chapter 6

Additional Information

Please consult the relevant data sheet and user's manual for specific information about individual devices. For information about the instruction set, refer to the *78K0 Instruction Set User's Manual*. The most current and up-to-date information can be obtained by calling 1-800-366-9782 or visiting our web site at www.necel.com.

[MEMO]

CHAPTER 1 K0 PRODUCT SELECTION GUIDE

The following table shows major differences among K0 subseries products.

Table 1-1. K0 Microcontroller Subseries Product Guide

Application	Subseries (**Notes 1, 2**)	ROM Capacity (K)	Timers			10-bit ADC	8-bit ADC	8-bit DAC	FIP/ LCD	Serial Interface			I/O pin	PKG pin
			8-bit	16-bit	RTC					I^2C	UART	Sync		
General Control with UART	μPD780024	8–32	2 ch	1 ch	1 ch	–	8 ch	–	–	Y	1 ch	2 ch	51	64
	μPD780034	8–32				8 ch	–	–					51	64
	μPD780058	24–60				–	8 ch	2 ch					68	80
	μPD78054	16–60											69	80
	μPD78058F	48–60											69	80
	μPD78070A	–	4 ch										61	100
	μPD78078	32–60	4 ch										88	100
	μPD78083	8–16	2 ch		–			–		–		1 ch	33	44
FIP Controller Driver	μPD780208	32–60	2 ch	1 ch	1 ch	–	8 ch	–	40 × 16	–	–	1 ch	74	100
	μPD780228	48-60							32 × 16			2 ch	72	100
	μPD78044F	16–40							24 × 16			2 ch	68	80
	μPD78044H	32–48							24 × 16			1 ch	68	80
LCD Driver	μPD780308	48–60	2 ch	1 ch	1 ch	–	8 ch	–	40 × 4	Y	1 ch	3 ch	57	100
	μPD78064	16–32	2 ch	1 ch	1 ch	–	8 ch	–	40 × 4	Y	1 ch	2 ch	57	100
IEBus	μPD78098	32–60	2 ch	–	–	–	8 ch	–	–	–	1 ch	3 ch	69	80
Motor Invertor Controller	μPD780988	24–60	3 ch	2 ch	–	8 ch	–	–	–	–	2 ch	–	47	64
Dash board	μPD780973	24	3 ch	1 ch	1 ch	–	5 ch	–	20 × 4	–	1 ch	1 ch	56	80
CAN	μPD780948	60	2 ch	2 ch	1 ch	–	8 ch	–	20 × 4	–	1 ch	1 ch	79	100

Notes: 1. Each subseries refers to the entire series of parts with various ROM/RAM sizes.

2. Parts are available in plastic QFP, TQFP, and SDIP packages, and some in ceramic SDIP and WQFN packages.

[MEMO]

2.1 Data Memory Addressing

Addressing is to specify the address of the instruction to be executed next or the address of a register or memory to be manipulated when an instruction is executed.

The address of the instruction to be executed next is specified by the program counter.

Figure 2-1. Example of Data Memory Addressing (μPD780306, 780306Y)

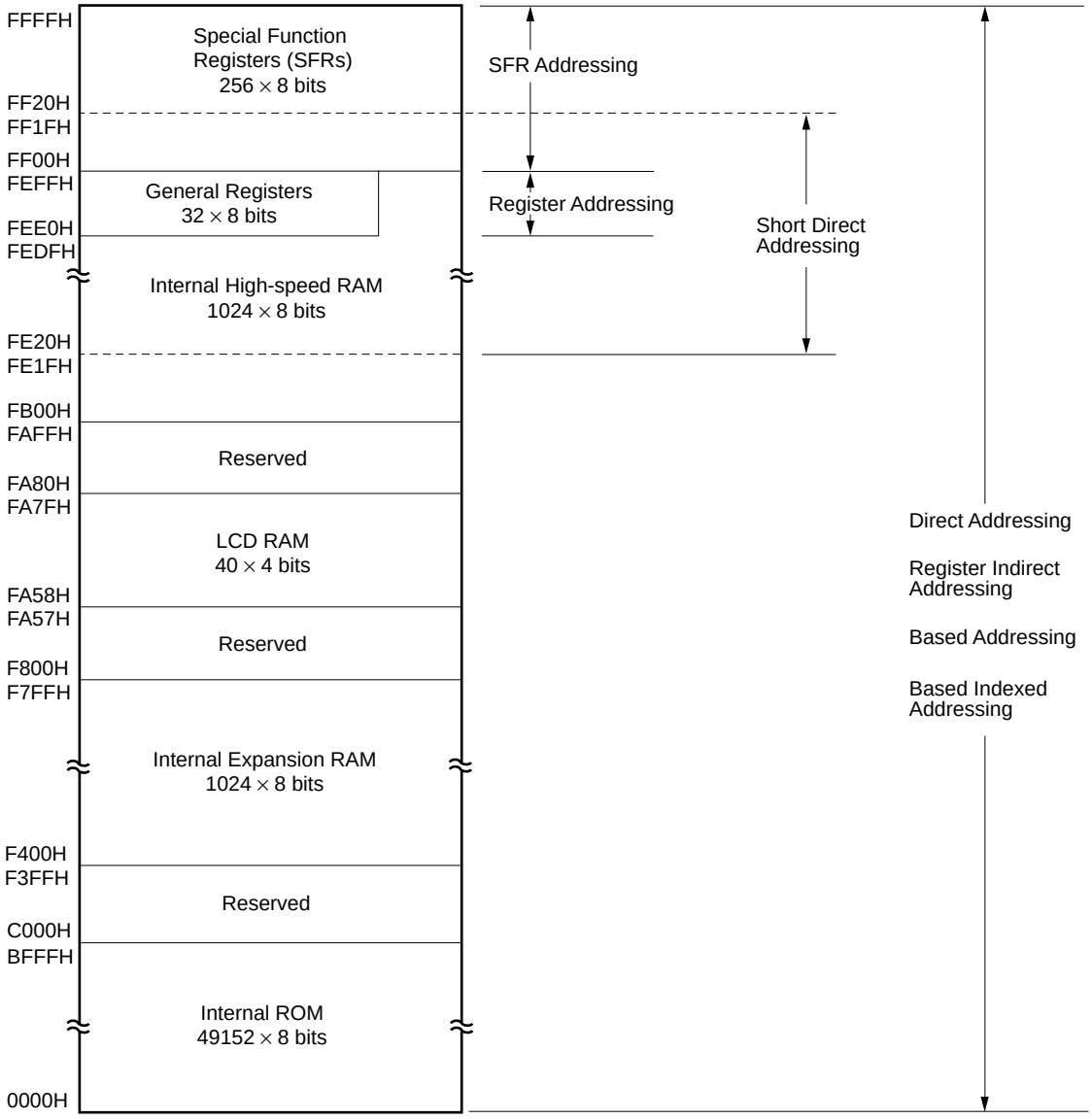
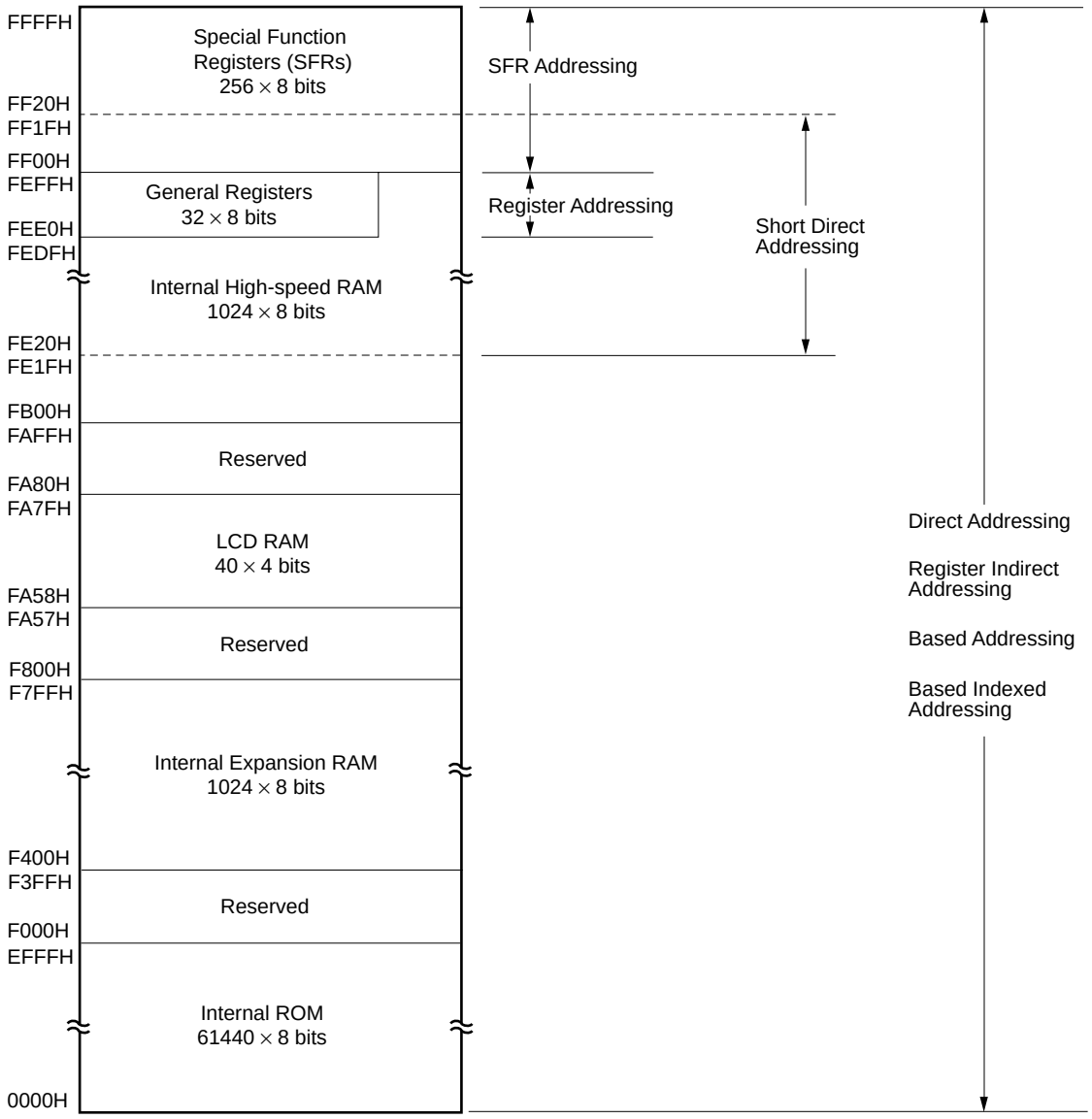


Figure 2-2. Example of Data Memory Addressing (μPD780308, 780308Y)



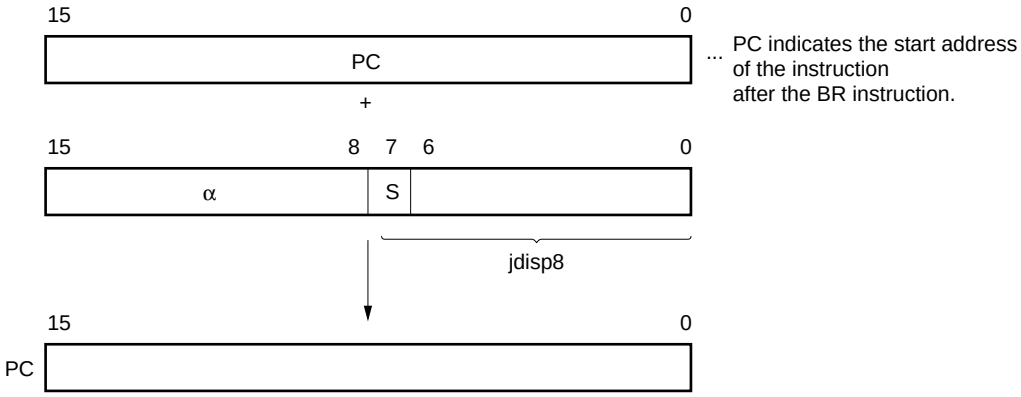
2.2 Instruction Address Addressing

An instruction address is determined by program counter (PC) contents and is normally incremented (+1 for each byte) automatically according to the number of bytes of an instruction to be fetched each time another instruction is executed. When a Branch instruction is executed, the branch destination information is set to the PC and branched by the following types of addressing.

2.2.1 Relative Addressing

The value obtained by adding 8-bit immediate data (displacement value: jdisp8) of an instruction code to the start address of the following instruction is transferred to the program counter (PC) and branched. The displacement value is treated as signed two's-complement data (–128 to +127) and bit 7 becomes a sign bit. In other words, relative addressing consists of relative branching from the start address of the following instruction to the –128 to +127 range.

This function is used when the BR $addr16 instruction or a Conditional Branch instruction is executed.



When S = 0, all bits of α are 0.
When S = 1, all bits of α are 1.

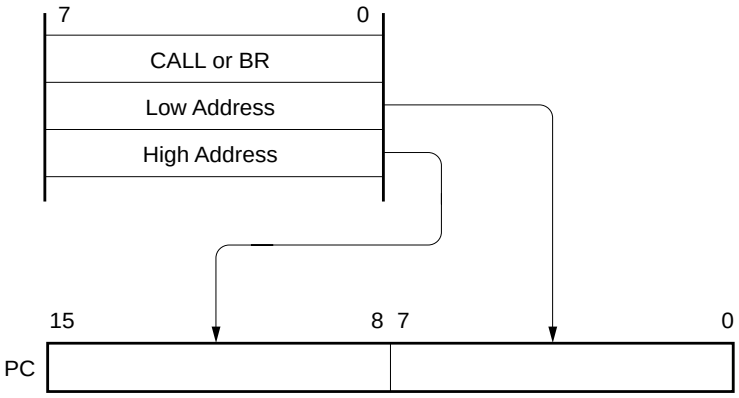
2.2.2 Immediate Addressing

Immediate data in the instruction word is transferred to the program counter (PC) and branched.

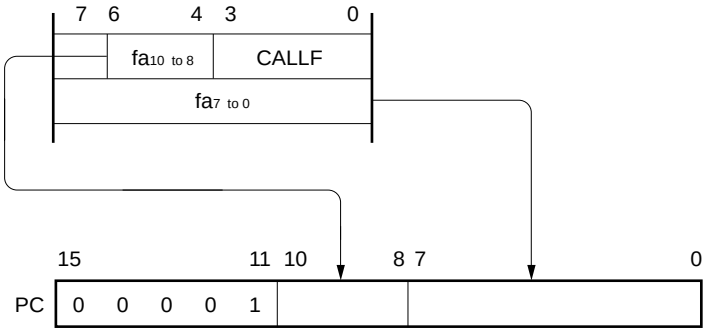
This function is used when the CALL !addr16 or BR !addr16 or CALLF !addr11 instruction is executed.

CALL !addr16 and BR !addr16 instructions can be branched to the entire memory space. The CALLF !addr11 instruction is branched to the 0800H to 0FFFH area.

In the CALL !addr16 and BR !addr16 instructions



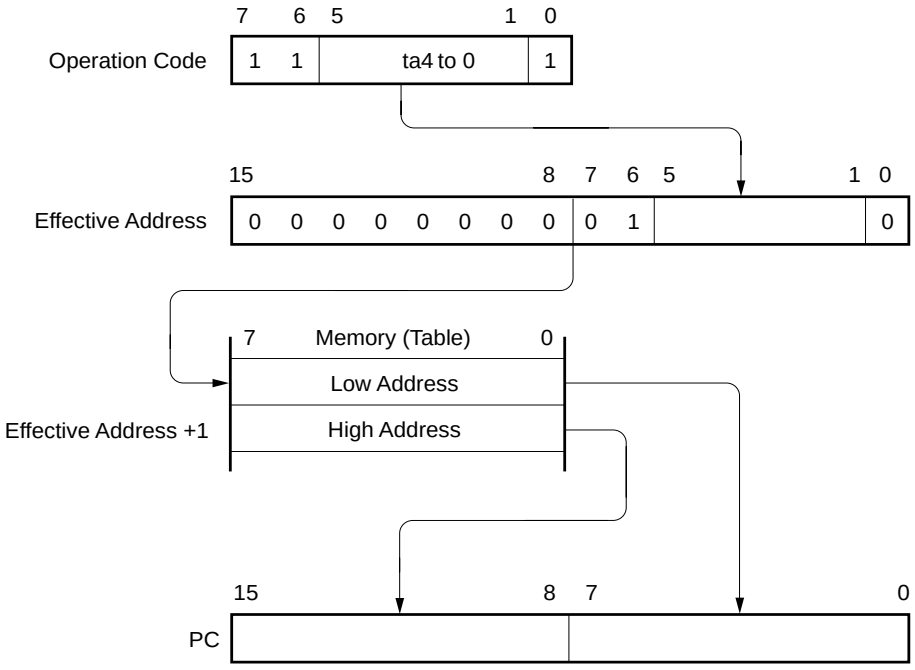
In the CALLF !addr11 instruction



2.2.3 Table Indirect Addressing

Table contents (branch destination address) of the particular location are addressed (by bits 1 to 5 of the immediate data of the opcode) and transferred to the program counter (PC), and the program branches. Table indirect addressing is used when the CALLT [addr5] instruction is executed.

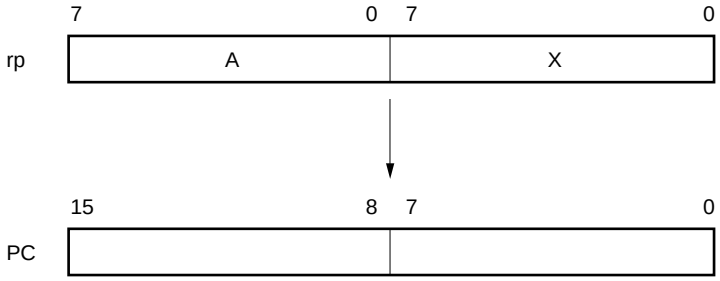
This instruction references the address stored in the memory table from 40H to 7FH, and allows branching to the entire memory space.



2.2.4 Register Addressing

Register pair (AX) contents are transferred to the program counter (PC) and the program branches.

This function is used when the BR AX instruction is executed.



2.3 Operand Address Addressing

The following methods are available to specify the register and memory (addressing) that are manipulated during instruction execution.

2.3.1 Implied Addressing

The register, which functions as an accumulator (A and AX) in the general register, is automatically addressed.

Instruction	Register To Be Specified by Implied Addressing
MULU	A register for multiplicand and AX register for product storage
DIVUW	AX register for dividend and quotient storage
ADJBA/ADJBS	A register for storage of numeric values, which become decimal correction targets
ROR4/ROL4	A register for storage of digit data, which undergoes digit rotation

Operand format

Because implied addressing can be automatically employed with an instruction, no particular operand format is necessary.

Example

In the MULU X

With an 8-bit x 8-bit Multiply instruction, the product of A register and X register is stored in AX. In this example, the A and AX registers are specified by implied addressing.

2.3.2 Register Addressing

The general register to be specified is accessed as an operand with the register bank select flags (RBS0 and RBS1) and with the register specify codes (Rn and RPn) in an operation code.

This addressing can be used when an instruction with the following operand format is executed. When an 8-bit register is specified, one of the eight registers is specified with 3 bits in the operation code.

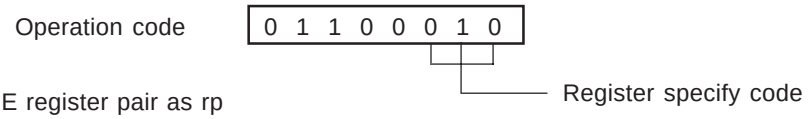
Operand format

Identifier	Description
r	X, A, C, B, E, D, L, H
rp	AX, BC, DE, HL

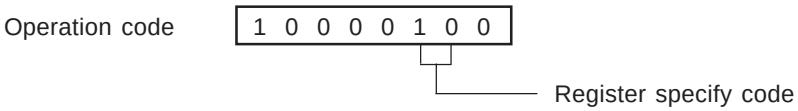
'r' and 'rp' can be described with function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL) as well as absolute names (R0 to R7 and RP0 to RP3).

Example

MOV A, C; when selecting C register as r



INCW DE; when selecting DE register pair as rp



2.3.3 Direct Addressing

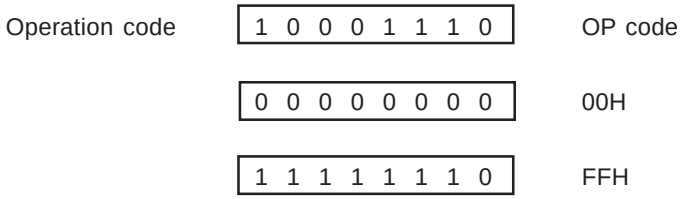
This addressing is to directly address the memory indicated by the immediate data in the instruction word.

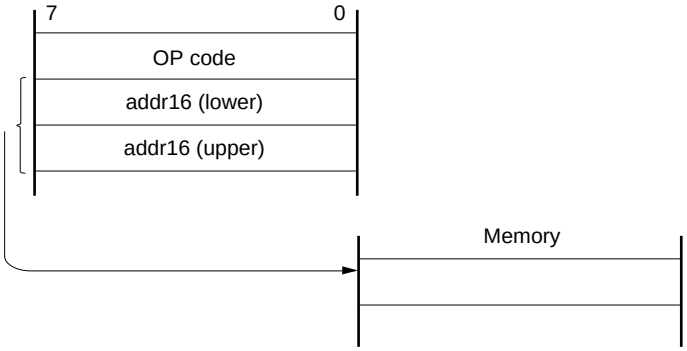
Operand format

Identifier	Description
addr16	Label or 16-bit immediate data

Example

MOV A, !FE00H; when setting !addr16 to FE00H





2.3.4 Short Direct Addressing

The memory to be manipulated in the fixed space is directly addressed with 8-bit data in an instruction word.

This addressing is applied to a fixed 256-byte space of FE20H through FF1FH. An internal high-speed RAM and a special function register (SFR) are mapped at FE20H to FEFFH and FF00H to FF1FH, respectively.

The SFR area (FF00H through FF1FH) to which short direct addressing is applied is part of the entire SFR area. Ports frequently accessed in a program, *Compare* registers, and *Capture* registers of timers/event counters are mapped to this area and these SFRs can be manipulated with a small number of bytes and clocks.

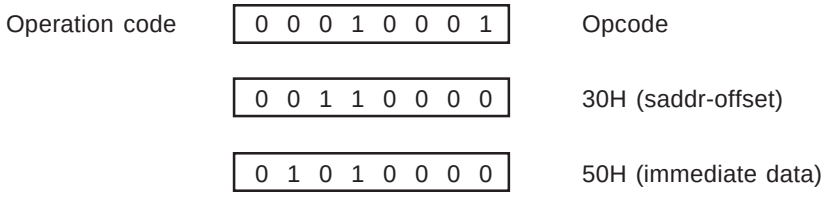
When 8-bit immediate data is at 20H to FFH, bit 8 of an effective address is set to 0. When it is at 00H to 1FH, bit 8 is set to 1.

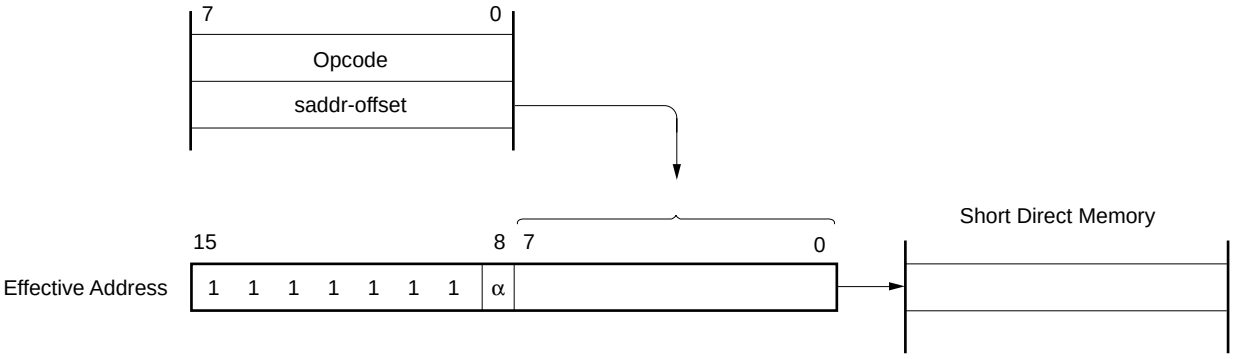
Operand format

Identifier	Description
saddr	Label of FE20H to FF1FH immediate data
saddrp	Label of FE20H to FF1FH immediate data (even address only)

Example

MOV 0FE30H, #50H; when using saddr FE30H and immediate data 50H





When 8-bit saddr-offset data is 20H to FFH, $\alpha = 0$

When 8-bit saddr-offset data is 00H to 1FH, $\alpha = 1$

2.3.5 Special Function Register (SFR) Addressing

The memory-mapped special function register (SFR) is addressed with 8-bit immediate data in an instruction word.

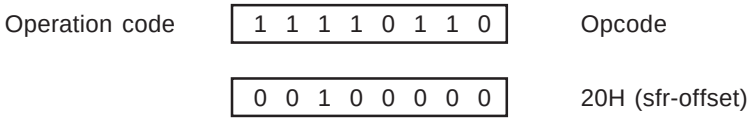
This addressing is applied to the 240-byte spaces FF00H to FFCFH and FFE0H to FFFFH. The SFR mapped at FF00H to FF1FH can also be accessed with short direct addressing.

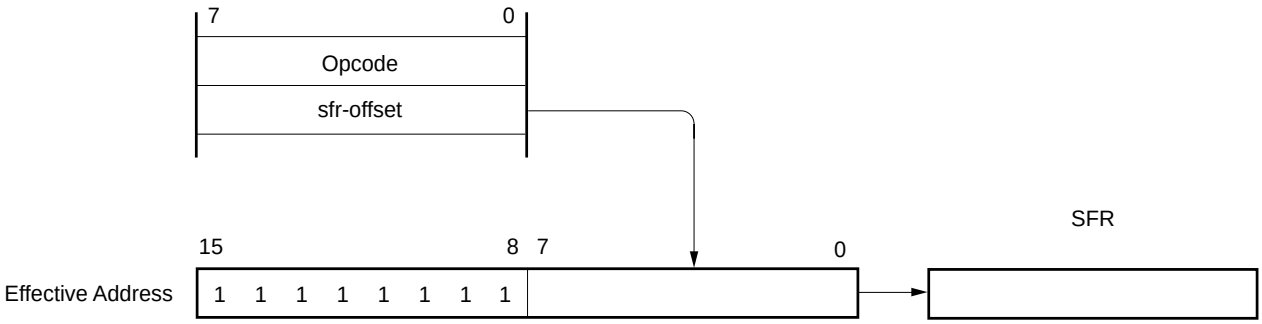
Operand format

Identifier	Description
sfr	Special function register name
sfrp	16-bit manipulatable special function register name (even address only)

Example

MOV PM0, A; when selecting PM0 (FF20H) as sfr





2.3.6 Register Indirect Addressing

This addressing is to address a memory area to be manipulated by using the contents of a register pair (specified by the register bank select flags RBS0 and RBS1) and the register pair specification code in the operation code.

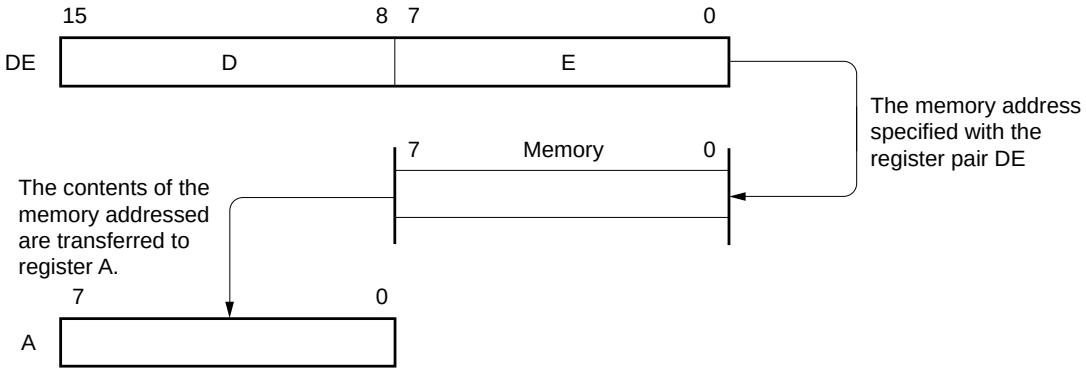
Operand format

Identifier	Description
—	[DE], [HL]

Example

MOV A, [DE]; when selecting [DE] as the register pair

Operation code | 1 0 0 0 0 1 0 1 |



2.3.7 Based Addressing

This addressing addresses memory by using the sum of the 8-bit immediate data to the contents of register pair HL (used as a base register). The HL register pair to be accessed is in the register bank specified with the register bank select flags (RBS0 and RBS1). Addition is performed by expanding the offset data as a positive number to 16 bits. A carry from the 16th bit is ignored. This addressing can be used for the entire memory space.

Operand format

Identifier	Description
—	[HL + byte]

Example

MOV A, [HL + 10H]; when setting byte to 10H

Operation code | 1 0 1 0 1 1 1 0 |

| 0 0 0 1 0 0 0 0 |

2.3.8 Based Indexed Addressing

This addressing addresses memory by using the result of adding the contents of the B or C register (specified in the instruction word) to the contents of the HL register that is used as a base register. The H, B, and C registers accessed are in the register bank specified by the register bank select registers (RBS0 and RBS1). The addition is executed with the contents of the B or C register extended to 16 bits as a positive number. A carry from the 16th bit is ignored. This addressing can be used for the entire memory space.

Operand format

Identifier	Description
—	[HL + B], [HL + C]

Example

In the MOV A, [HL + B]

Operation code | 1 0 1 0 1 0 1 1 |

2.3.9 Stack Addressing

The stack area is indirectly addressed with the stack pointer (SP) contents.

This addressing method is automatically employed when the PUSH, POP, Subroutine CALL, and RETURN instructions are executed or the register is saved or restored upon generation of an Interrupt request.

Stack addressing addresses the internal high-speed RAM area only.

Example

PUSH DE

Operation code | 1 0 1 1 0 1 0 1 |

[MEMO]

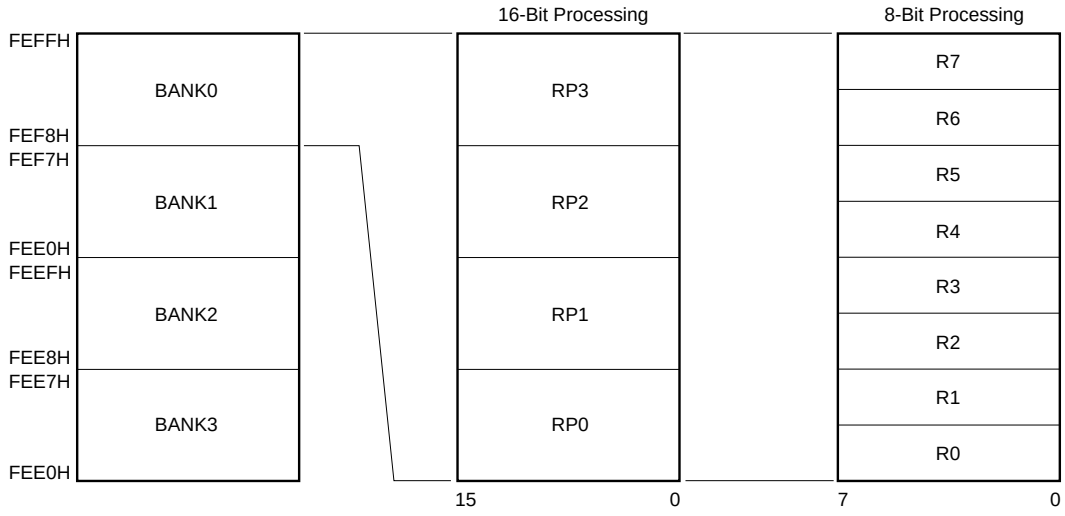
CHAPTER 3 REGISTERS AND STACK OPERATION

3.1 General Purpose Registers

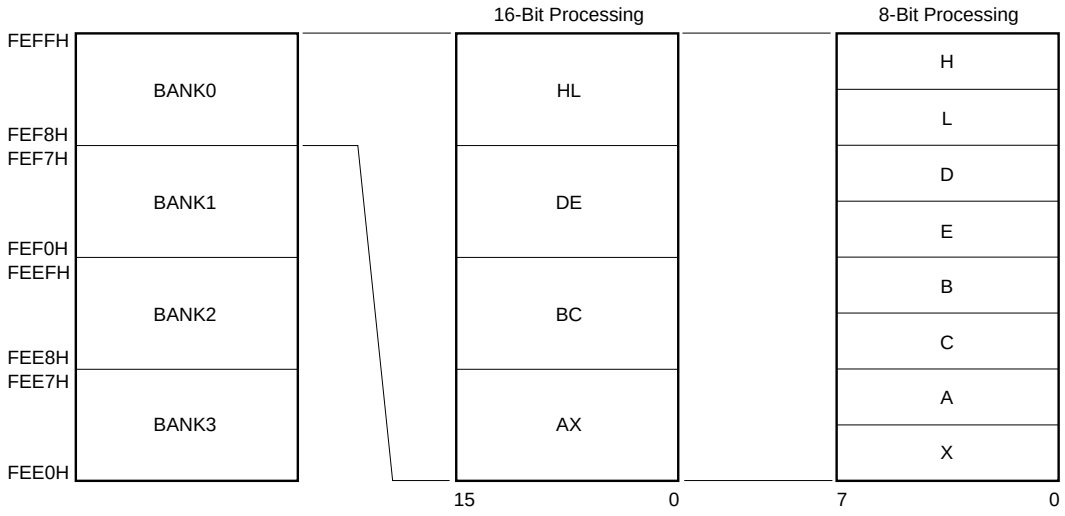
General purpose registers are mapped at addresses (FEE0H to FEFFH) of the internal high-speed RAM. There are four register banks; each bank consists of eight 8-bit registers (X, A, C, B, E, D, L, and H). Each register can be used as an 8-bit register, or two 8-bit registers can be used in pairs as a 16-bit register (AX, BC, DE, and HL). They can be described in function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL) and absolute names (R0 to R7 and RP0 to RP3). The register bank to be used for instruction execution is set with the CPU control instruction SEL RBn. Because of the 4-register bank configuration, context switching can be created by switching between the current register and a register bank for various tasks.

Figure 3-1. Configuration of General Purpose Registers

(a) Absolute Name



(b) Function Name



3.2 Processor Registers

3.2.1 Control Registers

The control registers control the program sequence, statuses, and stack memory. The control registers consist of a program counter (PC), a program status word (PSW), and a stack pointer (SP).

(1) Program counter (PC)

The program counter is a 16-bit register that holds the address of the next program to be executed.

In normal operation, the PC is automatically incremented by the number of bytes of the current instruction. When a Branch instruction is executed, immediate data and register contents are set.

$\overline{\text{RESET}}$ sets the Reset vector table values at addresses 0000H and 0001H to the program counter.

Figure 3-2. Format of Program Counter

	15															0
PC	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

(2) Program status word (PSW)

The program status word is an 8-bit register consisting of various flags to be set/reset by instruction execution. The program status word contents are automatically saved on the stack during Interrupt request processing or when a PUSH PSW instruction is executed. The PSW is automatically restored upon execution of the RETB, RETI, and POP PSW instructions. $\overline{\text{RESET}}$ sets the PSW to 02H.

Figure 3-3. Format of Program Status Word

	7							0
PSW	IE	Z	RBS1	AC	RBS0	0	ISP	CY

(a) Interrupt enable flag (IE)

This flag controls the Interrupt request acknowledge operations of the CPU. When IE = 0, Interrupt requests are disabled (DI), and all interrupts except the non-maskable interrupt are disabled. When IE = 1, the interrupts are enabled (EI). At this time, acknowledging Interrupt requests is controlled with an in-service priority flag (ISP), an interrupt mask flag (for each interrupt source), and a priority specification flag. This flag is reset (to 0) upon DI instruction execution or interrupt acknowledgment, and is set (to 1) upon EI instruction execution.

(b) Zero flag (Z)

When the operation result is zero, this flag is set (to 1). It is reset (to 0) in all other cases.

(c) Register bank select flags (RBS0 and RBS1)

These are 2 flag bits that select one of the four register banks. These bits indicate the register bank selected by an SEL RBn instruction.

(d) Auxiliary carry flag (AC)

If the operation result has a carry from bit 3 or a borrow at bit 3, this flag is set (to 1). It is reset (to 0) in all other cases.

(e) In-service priority flag (ISP)

This flag manages the priority of acknowledgment of maskable vectored Interrupt requests. When ISP = 0, the vectored interrupts assigned a low priority (with the priority registers PR0L, PR0H, and PR1L) are disabled. Acknowledgment of interrupts is controlled with the interrupt enable flag (IE).

(f) Carry flag (CY)

This flag stores overflow and underflow upon Add/Subtract instruction execution. It stores the shift-out value upon Rotate instruction execution and functions as a bit accumulator during Bit Manipulation instruction execution.

(3) Stack pointer (SP)

This is a 16-bit register that contains the current address of the memory stack area. Only the internal high-speed RAM area (FB00H to FEFFH) can be set as the stack area.

Figure 3-4. Format of Stack Pointer

	15															0
SP	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

3.3 Stack Operation

Each stack operation saves or restores data as shown in Figures 3-5 and 3-6.

Caution: Since $\overline{\text{RESET}}$ input makes the SP contents undefined, be sure to initialize the SP before instruction execution.

Figure 3-5. Data To Be Saved on the Stack

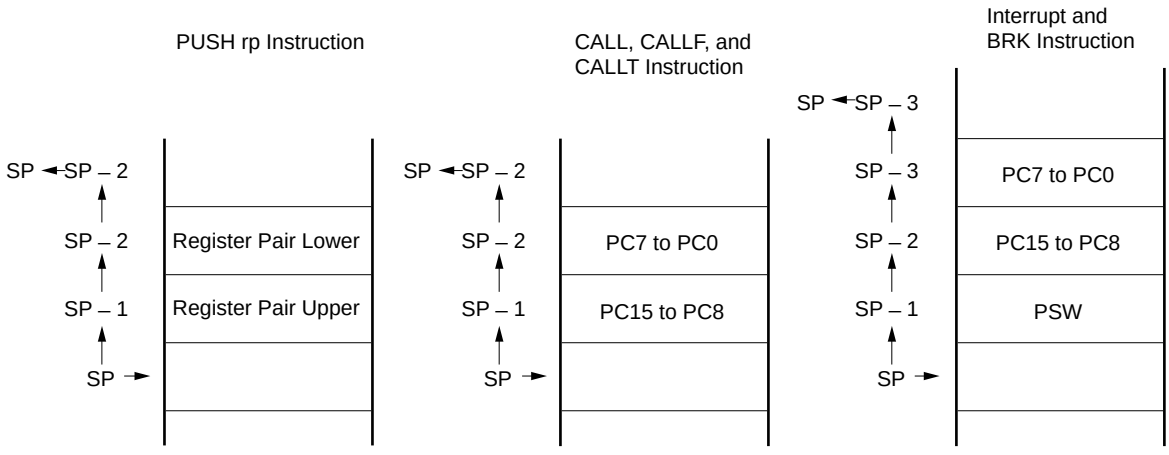
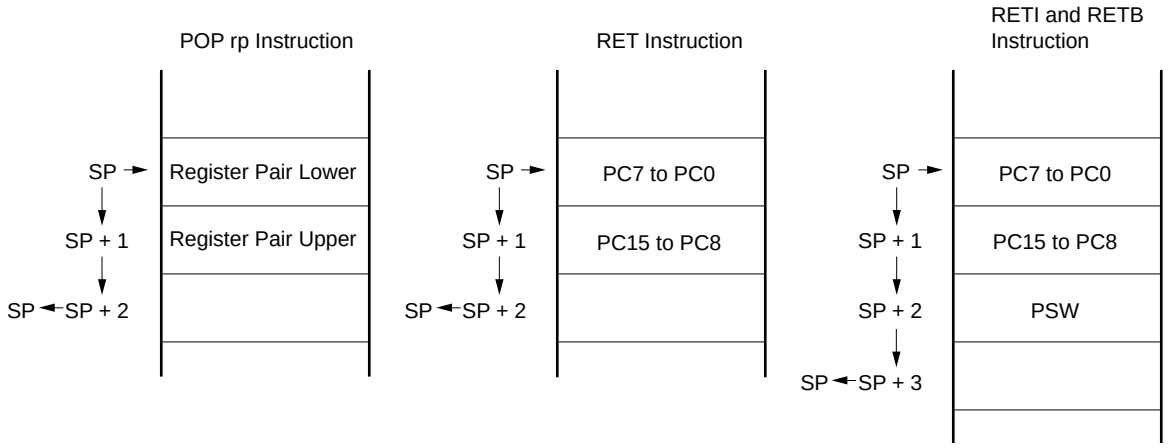


Figure 3-6. Data To Be Restored from the Stack



CHAPTER 4 INSTRUCTION SET

4.1 Operand Descriptions

Operands are described in the "Operand" column of each instruction. Alphabetic letters in capitals and the symbols #, !, $, and [ ] are key words, and each symbol has the following meaning.

- # Immediate data specification
- ! Absolute address specification
- $ Relative address specification
- [ ] Indirect address specification

In the case of immediate data (#), an appropriate numeric value or label must follow the # symbol.

For operand register identifiers r and rp, either a function name (X, A, C, etc.) or an absolute name (names in parentheses in the table below—R0, R1, R2, etc.) can be used for description.

Table 4-1. Operand Description

Identifier	Description Method
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7),
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special function register symbol **Note 1**
sfrp	Special function register symbol (16-bit manipulatable register even addresses only) **Note 1**
saddr	FE20H to FF1FH immediate data or labels
saddrp	FE20H to FF1FH immediate data or labels (even address only)
addr16	0000H to FFFFH immediate data or labels (Only even addresses for 16-bit Data Transfer instructions)
addr11	0800H to 0FFFH immediate data or labels
addr5	0040H to 007FH immediate data or labels (even address only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit **Note 2**	3-bit immediate data or label
RBn	RB0 to RB3

Notes: 1. Addresses from FFD0H to FFDFH cannot be accessed with these operands.

2. The bit identifier allows a specific bit to be addressed.
   For example, in the instruction:

   ```
   SET   A.3
   ```

   this instruction causes bit 3 of register A to be set to 1.

A	A register; 8-bit accumulator
X	X register
B	B register
C	C register
D	D register
E	E register
H	H register
L	L register
AX	AX register pair; 16-bit accumulator
BC	BC register pair
DE	DE register pair
HL	HL register pair
PC	Program counter
SP	Stack pointer
PSW	Program status word
CY	Carry flag
AC	Auxiliary carry flag
Z	Zero flag
RBS	Register bank select flag
IE	Interrupt request enable flag
NMIS	Non-maskable interrupt servicing flag
( )	Memory contents indicated by address or register contents in parentheses
$\times_H$, $\times_L$	Higher 8 bits and lower 8 bits of 16-bit register
$\wedge$	Logical product (AND)
$\vee$	Logical sum (OR)
$\veebar$	Exclusive logical sum (exclusive OR)
$\overline{\quad}$	Inverted data
addr16	16-bit immediate data or label
jdisp8	Signed 8-bit data (displacement value)

4.1.1 Description of “Flag” Column

(Blank):	Not affected
0:	Cleared to 0
1:	Set to 1
$\times$:	Set/cleared according to the result
R:	Previously saved value is restored

4.2 Instruction Set Table

Table 4-2. Instruction Set (1/8)

Instruction Group	Mnemonic	Operands	Byte	Clock		Operation	Flag
				Note 1	Note 2		Z AC CY
8-bit data transfer	MOV	r, #byte	2	4	–	r ← byte	
		saddr, #byte	3	6	7	(saddr) ← byte	
		sfr, #byte	3	–	7	sfr ← byte	
		A, r Note 3	1	2	–	A ← r	
		r, A Note 3	1	2	–	r ← A	
		A, saddr	2	4	5	A ← (saddr)	
		saddr, A	2	4	5	(saddr) ← A	
		A, sfr	2	–	5	A ← sfr	
		sfr, A	2	–	5	sfr ← A	
		A, !addr16	3	8	9	A ← (addr16)	
		!addr16, A	3	8	9	(addr16) ← A	
		PSW, #byte	3	–	7	PSW ← byte	× × ×
		A, PSW	2	–	5	A ← PSW	
		PSW, A	2	–	5	PSW ← A	× × ×
		A, [DE]	1	4	5	A ← (DE)	
		[DE], A	1	4	5	(DE) ← A	
		A, [HL]	1	4	5	A ← (HL)	
		[HL], A	1	4	5	(HL) ← A	
		A, [HL + byte]	2	8	9	A ← (HL + byte)	
		[HL + byte], A	2	8	9	(HL + byte) ← A	
		A, [HL + B]	1	6	7	A ← (HL + B)	
		[HL + B], A	1	6	7	(HL + B) ← A	
		A, [HL + C]	1	6	7	A ← (HL + C)	
		[HL + C], A	1	6	7	(HL + C) ← A	
	XCH	A, r Note 3	1	2	–	A ↔ r	
		A, saddr	2	4	6	A ↔ (saddr)	
		A, sfr	2	–	6	A ↔ sfr	
		A, !addr16	3	8	10	A ↔ (addr16)	
		A, [DE]	1	4	6	A ↔ (DE)	
		A, [HL]	1	4	6	A ↔ (HL)	
		A, [HL + byte]	2	8	10	A ↔ (HL + byte)	
		A, [HL + B]	2	8	10	A ↔ (HL + B)	
		A, [HL + C]	2	8	10	A ↔ (HL + C)	

Notes: 1. When the internal high-speed RAM area is accessed or there is an instruction with no data access
2. When any area except the internal high-speed RAM area is accessed
3. Except 'r = A'

Remark: One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control (PCC) register.

Table 4-2. Instruction Set (2/8)

Instruction Group	Mnemonic	Operands	Byte	Clock		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
16-bit data transfer	**MOVW**	rp, #word	3	6	–	rp ← word			
		saddrp, #word	4	8	10	(saddrp) ← word			
		sfrp, #word	4	–	10	sfrp ← word			
		AX, saddrp	2	6	8	AX ← (saddrp)			
		saddrp, AX	2	6	8	(saddrp) ← AX			
		AX, sfrp	2	–	8	AX ← sfrp			
		sfrp, AX	2	–	8	sfrp ← AX			
		AX, rp Note 3	1	4	–	AX ← rp			
		rp, AX Note 3	1	4	–	rp ← AX			
		AX, !addr16	3	10	12	AX ← (addr16)			
		!addr16, AX	3	10	12	(addr16) ← AX			
	XCHW	AX, rp Note 3	1	4	–	AX ↔ rp			
8-bit operation	**ADD**	A, #byte	2	4	–	A, CY ← A + byte	×	×	×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) + byte	×	×	×
		A, r Note 4	2	4	–	A, CY ← A + r	×	×	×
		r, A	2	4	–	r, CY ← r + A	×	×	×
		A, saddr	2	4	5	A, CY ← A + (saddr)	×	×	×
		A, !addr16	3	8	9	A, CY ← A + (addr16)	×	×	×
		A, [HL]	1	4	5	A, CY ← A + (HL)	×	×	×
		A, [HL + byte]	2	8	9	A, CY ← A + (HL + byte)	×	×	×
		A, [HL + B]	2	8	9	A, CY ← A + (HL + B)	×	×	×
		A, [HL + C]	2	8	9	A, CY ← A + (HL + C)	×	×	×
	ADDC	A, #byte	2	4	–	A, CY ← A + byte + CY	×	×	×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) + byte + CY	×	×	×
		A, r Note 4	2	4	–	A, CY ← A + r + CY	×	×	×
		r, A	2	4	–	r, CY ← r + A + CY	×	×	×
		A, saddr	2	4	5	A, CY ← A + (saddr) + CY	×	×	×
		A, !addr16	3	8	9	A, CY ← A + (addr16) + CY	×	×	×
		A, [HL]	1	4	5	A, CY ← A + (HL) + CY	×	×	×
		A, [HL + byte]	2	8	9	A, CY ← A + (HL + byte) + CY	×	×	×
		A, [HL + B]	2	8	9	A, CY ← A + (HL + B) + CY	×	×	×
		A, [HL + C]	2	8	9	A, CY ← A + (HL + C) + CY	×	×	×

Notes: 1. When the internal high-speed RAM area is accessed or there is an instruction with no data access
2. When any area except the internal high-speed RAM area is accessed
3. Only when rp = BC, DE or HL
4. Except ‘r = A’

Remark: One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control (PCC) register.

Table 4-2. Instruction Set (3/8)

Instruction Group	Mnemonic	Operands	Byte	Clock		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	**SUB**	A, #byte	2	4	–	A, CY ← A – byte	×	×	×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) – byte	×	×	×
		A, r Note 3	2	4	–	A, CY ← A – r	×	×	×
		r, A	2	4	–	r, CY ← r – A	×	×	×
		A, saddr	2	4	5	A, CY ← A – (saddr)	×	×	×
		A, !addr16	3	8	9	A, CY ← A – (addr16)	×	×	×
		A, [HL]	1	4	5	A, CY ← A – (HL)	×	×	×
		A, [HL + byte]	2	8	9	A, CY ← A – (HL + byte)	×	×	×
		A, [HL + B]	2	8	9	A, CY ← A – (HL + B)	×	×	×
		A, [HL + C]	2	8	9	A, CY ← A – (HL + C)	×	×	×
	SUBC	A, #byte	2	4	–	A, CY ← A – byte – CY	×	×	×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) – byte – CY	×	×	×
		A, r Note 3	2	4	–	A, CY ← A – r – CY	×	×	×
		r, A	2	4	–	r, CY ← r – A – CY	×	×	×
		A, saddr	2	4	5	A, CY ← A – (saddr) – CY	×	×	×
		A, !addr16	3	8	9	A, CY ← A – (addr16) – CY	×	×	×
		A, [HL]	1	4	5	A, CY ← A – (HL) – CY	×	×	×
		A, [HL + byte]	2	8	9	A, CY ← A – (HL + byte) – CY	×	×	×
		A, [HL + B]	2	8	9	A, CY ← A – (HL + B) – CY	×	×	×
		A, [HL + C]	2	8	9	A, CY ← A – (HL + C) – CY	×	×	×
	AND	A, #byte	2	4	–	A ← A ∧ byte	×		
		saddr, #byte	3	6	8	(saddr) ← (saddr) ∧ byte	×		
		A, r Note 3	2	4	–	A ← A ∧ r	×		
		r, A	2	4	–	r ← r ∧ A	×		
		A, saddr	2	4	5	A ← A ∧ (saddr)	×		
		A, !addr16	3	8	9	A ← A ∧ (addr16)	×		
		A, [HL]	1	4	5	A ← A ∧ (HL)	×		
		A, [HL + byte]	2	8	9	A ← A ∧ (HL + byte)	×		
		A, [HL + B]	2	8	9	A ← A ∧ (HL + B)	×		
		A, [HL + C]	2	8	9	A ← A ∧ (HL + C)	×		

Notes: 1. When the internal high-speed RAM area is accessed or there is an instruction with no data access
2. When any area except the internal high-speed RAM area is accessed
3. Except ‘r = A’

Remark: One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control (PCC) register.

Table 4-2. Instruction Set (4/8)

Instruction Group	Mnemonic	Operands	Byte	Clock		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	**OR**	A, #byte	2	4	–	A ← A ∨ byte	×		
		saddr, #byte	3	6	8	(saddr) ← (saddr) ∨ byte	×		
		A, r Note 3	2	4	–	A ← A ∨ r	×		
		r, A	2	4	–	r ← r ∨ A	×		
		A, saddr	2	4	5	A ← A ∨ (saddr)	×		
		A, !addr16	3	8	9	A ← A ∨ (addr16)	×		
		A, [HL]	1	4	5	A ← A ∨ (HL)	×		
		A, [HL + byte]	2	8	9	A ← A ∨ (HL + byte)	×		
		A, [HL + B]	2	8	9	A ← A ∨ (HL + B)	×		
		A, [HL + C]	2	8	9	A ← A ∨ (HL + C)	×		
	XOR	A, #byte	2	4	–	A ← A ⩛ byte	×		
		saddr, #byte	3	6	8	(saddr) ← (saddr) ⩛ byte	×		
		A, r Note 3	2	4	–	A ← A ⩛ r	×		
		r, A	2	4	–	r ← r ⩛ A	×		
		A, saddr	2	4	5	A ← A ⩛ (saddr)	×		
		A, !addr16	3	8	9	A ← A ⩛ (addr16)	×		
		A, [HL]	1	4	5	A ← A ⩛ (HL)	×		
		A, [HL + byte]	2	8	9	A ← A ⩛ (HL + byte)	×		
		A, [HL + B]	2	8	9	A ← A ⩛ (HL + B)	×		
		A, [HL + C]	2	8	9	A ← A ⩛ (HL + C)	×		
	CMP	A, #byte	2	4	–	A – byte	×	×	×
		saddr, #byte	3	6	8	(saddr) – byte	×	×	×
		A, r Note 3	2	4	–	A – r	×	×	×
		r, A	2	4	–	r – A	×	×	×
		A, saddr	2	4	5	A – (saddr)	×	×	×
		A, !addr16	3	8	9	A – (addr16)	×	×	×
		A, [HL]	1	4	5	A – (HL)	×	×	×
		A, [HL + byte]	2	8	9	A – (HL + byte)	×	×	×
		A, [HL + B]	2	8	9	A – (HL + B)	×	×	×
		A, [HL + C]	2	8	9	A – (HL + C)	×	×	×

Notes: 1. When the internal high-speed RAM area is accessed or there is an instruction with no data access
2. When any area except the internal high-speed RAM area is accessed
3. Except ‘r = A’

Remark: One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control (PCC) register.

Table 4-2. Instruction Set (5/8)

Instruction Group	Mnemonic	Operands	Byte	Clock		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
16-bit operation	**ADDW**	AX, #word	3	6	–	AX, CY ← AX + word	×	×	×
	SUBW	AX, #word	3	6	–	AX, CY ← AX – word	×	×	×
	CMPW	AX, #word	3	6	–	AX – word	×	×	×
Multiply/ divide	**MULU**	X	2	16	–	AX ← A × X			
	DIVUW	C	2	25	–	AX (Quotient), C (Remainder) ← AX ÷ C			
Increment/ decrement	**INC**	r	1	2	–	r ← r + 1	×	×	
		saddr	2	4	6	(saddr) ← (saddr) + 1	×	×	
	DEC	r	1	2	–	r ← r – 1	×	×	
		saddr	2	4	6	(saddr) ← (saddr) – 1	×	×	
	INCW	rp	1	4	–	rp ← rp + 1			
	DECW	rp	1	4	–	rp ← rp – 1			
Rotate	**ROR**	A, 1	1	2	–	(CY, $A_7 \leftarrow A_0$, $A_{m-1} \leftarrow A_m$) × 1 time			×
	ROL	A, 1	1	2	–	(CY, $A_0 \leftarrow A_7$, $A_{m+1} \leftarrow A_m$) × 1 time			×
	RORC	A, 1	1	2	–	(CY ← A_0, $A_7 \leftarrow$ CY, $A_{m-1} \leftarrow A_m$) × 1 time			×
	ROLC	A, 1	1	2	–	(CY ← A_7, $A_0 \leftarrow$ CY, $A_{m+1} \leftarrow A_m$) × 1 time			×
	ROR4	[HL]	2	10	12	$A_{3-0} \leftarrow (HL)_{3-0}$, $(HL)_{7-4} \leftarrow A_{3-0}$, $(HL)_{3-0} \leftarrow (HL)_{7-4}$			
	ROL4	[HL]	2	10	12	$A_{3-0} \leftarrow (HL)_{7-4}$, $(HL)_{3-0} \leftarrow A_{3-0}$, $(HL)_{7-4} \leftarrow (HL)_{3-0}$			
BCD adjust	**ADJBA**		2	4	–	Decimal Adjust Accumulator after Addition	×	×	×
	ADJBS		2	4	–	Decimal Adjust Accumulator after Subtract	×	×	×
Bit manipulate	**MOV1**	CY, saddr.bit	3	6	7	CY ← (saddr.bit)			×
		CY, sfr.bit	3	–	7	CY ← sfr.bit			×
		CY, A.bit	2	4	–	CY ← A.bit			×
		CY, PSW.bit	3	–	7	CY ← PSW.bit			×
		CY, [HL].bit	2	6	7	CY ← (HL).bit			×
		saddr.bit, CY	3	6	8	(saddr.bit) ← CY			
		sfr.bit, CY	3	–	8	sfr.bit ← CY			
		A.bit, CY	2	4	–	A.bit ← CY			
		PSW.bit, CY	3	–	8	PSW.bit ← CY	×	×	
		[HL].bit, CY	2	6	8	(HL).bit ← CY			

Notes: 1. When the internal high-speed RAM area is accessed or there is an instruction with no data access
2. When any area except the internal high-speed RAM area is accessed

Remark: One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control (PCC) register.

Table 4-2. Instruction Set (6/8)

Instruction Group	Mnemonic	Operands	Byte	Clock		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
Bit manipulate	**AND1**	CY, saddr.bit	3	6	7	CY ← CY ∧ (saddr.bit)			×
		CY, sfr.bit	3	–	7	CY ← CY ∧ sfr.bit			×
		CY, A.bit	2	4	–	CY ← CY ∧ A.bit			×
		CY, PSW.bit	3	–	7	CY ← CY ∧ PSW.bit			×
		CY, [HL].bit	2	6	7	CY ← CY ∧ (HL).bit			×
	OR1	CY, saddr.bit	3	6	7	CY ← CY ∨ (saddr.bit)			×
		CY, sfr.bit	3	–	7	CY ← CY ∨ sfr.bit			×
		CY, A.bit	2	4	–	CY ← CY ∨ A.bit			×
		CY, PSW.bit	3	–	7	CY ← CY ∨ PSW.bit			×
		CY, [HL].bit	2	6	7	CY ← CY ∨ (HL).bit			×
	XOR1	CY, saddr.bit	3	6	7	CY ← CY ⊻ (saddr.bit)			×
		CY, sfr.bit	3	–	7	CY ← CY ⊻ sfr.bit			×
		CY, A.bit	2	4	–	CY ← CY ⊻ A.bit			×
		CY, PSW.bit	3	–	7	CY ← CY ⊻ PSW.bit			×
		CY, [HL].bit	2	6	7	CY ← CY ⊻ (HL).bit			×
	SET1	saddr.bit	2	4	6	(saddr.bit) ← 1			
		sfr.bit	3	–	8	sfr.bit ← 1			
		A.bit	2	4	–	A.bit ← 1			
		PSW.bit	2	–	6	PSW.bit ← 1	×	×	×
		[HL].bit	2	6	8	(HL).bit ← 1			
	CLR1	saddr.bit	2	4	6	(saddr.bit) ← 0			
		sfr.bit	3	–	8	sfr.bit ← 0			
		A.bit	2	4	–	A.bit ← 0			
		PSW.bit	2	–	6	PSW.bit ← 0	×	×	×
		[HL].bit	2	6	8	(HL).bit ← 0			
	SET1	CY	1	2	–	CY ← 1			1
	CLR1	CY	1	2	–	CY ← 0			0
	NOT1	CY	1	2	–	CY ← $\overline{CY}$			×

Notes: 1. When the internal high-speed RAM area is accessed or there is an instruction with no data access
2. When any area except the internal high-speed RAM area is accessed

Remark: One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control (PCC) register.

Table 4-2. Instruction Set (7/8)

Instruction Group	Mnemonic	Operands	Byte	Clock		Operation	Flag
				Note 1	Note 2		Z AC CY
Call/return	**CALL**	!addr16	3	7	–	$(SP-1) \leftarrow (PC+3)_H$, $(SP-2) \leftarrow (PC+3)_L$, $PC \leftarrow$ addr16, $SP \leftarrow SP-2$	
	CALLF	!addr11	2	5	–	$(SP-1) \leftarrow (PC+2)_H$, $(SP-2) \leftarrow (PC+2)_L$, $PC_{15-11} \leftarrow 00001$, $PC_{10-0} \leftarrow$ addr11, $SP \leftarrow SP-2$	
	CALLT	[addr5]	1	6	–	$(SP-1) \leftarrow (PC+1)_H$, $(SP-2) \leftarrow (PC+1)_L$, $PC_H \leftarrow (00000000, addr5+1)$, $PC_L \leftarrow (00000000, addr5)$, $SP \leftarrow SP-2$	
	BRK		1	6	–	$(SP-1) \leftarrow PSW$, $(SP-2) \leftarrow (PC+1)_H$, $(SP-3) \leftarrow (PC+1)_L$, $PC_H \leftarrow (003FH)$, $PC_L \leftarrow (003EH)$, $SP \leftarrow SP-3$, $IE \leftarrow 0$	
	RET		1	6	–	$PC_H \leftarrow (SP+1)$, $PC_L \leftarrow (SP)$, $SP \leftarrow SP+2$	
	RETI		1	6	–	$PC_H \leftarrow (SP+1)$, $PC_L \leftarrow (SP)$, $PSW \leftarrow (SP+2)$, $SP \leftarrow SP+3$, $NMIS \leftarrow 0$	R R R
	RETB		1	6	–	$PC_H \leftarrow (SP+1)$, $PC_L \leftarrow (SP)$, $PSW \leftarrow (SP+2)$, $SP \leftarrow SP+3$	R R R
Stack manipulate	**PUSH**	PSW	1	2	–	$(SP-1) \leftarrow PSW$, $SP \leftarrow SP-1$	
		rp	1	4	–	$(SP-1) \leftarrow rp_H$, $(SP-2) \leftarrow rp_L$, $SP \leftarrow SP-2$	
	POP	PSW	1	2	–	$PSW \leftarrow (SP)$, $SP \leftarrow SP+1$	R R R
		rp	1	4	–	$rp_H \leftarrow (SP+1)$, $rp_L \leftarrow (SP)$, $SP \leftarrow SP+2$	
	MOVW	SP, #word	4	–	10	$SP \leftarrow$ word	
		SP, AX	2	–	8	$SP \leftarrow AX$	
		AX, SP	2	–	8	$AX \leftarrow SP$	
Unconditional branch	**BR**	!addr16	3	6	–	$PC \leftarrow$ addr16	
		$addr16	2	6	–	$PC \leftarrow PC+2+$ jdisp8	
		AX	2	8	–	$PC_H \leftarrow A$, $PC_L \leftarrow X$	
Conditional branch	**BC**	$addr16	2	6	–	$PC \leftarrow PC+2+$ jdisp8 if CY = 1	
	BNC	$addr16	2	6	–	$PC \leftarrow PC+2+$ jdisp8 if CY = 0	
	BZ	$addr16	2	6	–	$PC \leftarrow PC+2+$ jdisp8 if Z = 1	
	BNZ	$addr16	2	6	–	$PC \leftarrow PC+2+$ jdisp8 if Z = 0	

Notes: 1. When the internal high-speed RAM area is accessed or there is an instruction with no data access
2. When any area except the internal high-speed RAM area is accessed

Remark: One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control (PCC) register.

Table 4-2. Instruction Set (8/8)

Instruction Group	Mnemonic	Operands	Byte	Clock		Operation	Flag
				Note 1	Note 2		Z AC CY
Conditional branch	**BT**	saddr.bit, $addr16	3	8	9	PC ← PC + 3 + jdisp8 if (saddr.bit) = 1	
		sfr.bit, $addr16	4	–	11	PC ← PC + 4 + jdisp8 if sfr.bit = 1	
		A.bit, $addr16	3	8	–	PC ← PC + 3 + jdisp8 if A.bit = 1	
		PSW.bit, $addr16	3	–	9	PC ← PC + 3 + jdisp8 if PSW.bit = 1	
		[HL].bit, $addr16	3	10	11	PC ← PC + 3 + jdisp8 if (HL).bit = 1	
	BF	saddr.bit, $addr16	4	10	11	PC ← PC + 4 + jdisp8 if (saddr.bit) = 0	
		sfr.bit, $addr16	4	–	11	PC ← PC + 4 + jdisp8 if sfr.bit = 0	
		A.bit, $addr16	3	8	–	PC ← PC + 3 + jdisp8 if A.bit = 0	
		PSW.bit, $addr16	4	–	11	PC ← PC + 4 + jdisp8 if PSW.bit = 0	
		[HL].bit, $addr16	3	10	11	PC ← PC + 3 + jdisp8 if (HL).bit = 0	
	BTCLR	saddr.bit, $addr16	4	10	12	PC ← PC + 4 + jdisp8 if (saddr.bit) = 1 then reset (saddr.bit)	
		sfr.bit, $addr16	4	–	12	PC ← PC + 4 + jdisp8 if sfr.bit = 1 then reset sfr.bit	
		A.bit, $addr16	3	8	–	PC ← PC + 3 + jdisp8 if A.bit = 1 then reset A.bit	
		PSW.bit, $addr16	4	–	12	PC ← PC + 4 + jdisp8 if PSW.bit = 1 then reset PSW.bit	× × ×
		[HL].bit, $addr16	3	10	12	PC ← PC + 3 + jdisp8 if (HL).bit = 1 then reset (HL).bit	
	DBNZ	B.bit, $addr16	2	6	–	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0	
		C.bit, $addr16	2	6	–	C ← C –1, then PC ← PC + 2 + jdisp8 if C ≠ 0	
		saddr, $addr16	3	8	10	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0	
CPU control	**SEL**	RBn	2	4	–	RBS1, 0 ← n	
	NOP		1	2	–	No Operation	
	EI		2	–	6	IE ← 1 (Enable Interrupt)	
	DI		2	–	6	IE ← 0 (Disable Interrupt)	
	HALT		2	6	–	Set HALT Mode	
	STOP		2	6	–	Set STOP Mode	

Notes: 1. When the internal high-speed RAM area is accessed or there is an instruction with no data access
2. When any area except the internal high-speed RAM area is accessed

Remark: One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control (PCC) register.

4.3 Instructions Listed by Addressing Type

The following tables show which instructions can be used with various operands. For example, if the first operand is r and the second operand is A, the MOV, ADD, ADDC, SUB, SUBC, AND, OR, XOR, and CMP instructions can be used.

4.3.1 8-Bit Instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

Table 4-3. 8-Bit Instructions Listed by Operand Type

First Operand \ Second Operand	#byte	A	r [Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note: Except r = A

4.3.2 16-Bit Instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

Table 4-4. 16-Bit Instructions Listed by Operand Type

First Operand \ Second Operand	#word	AX	rp [Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW [Note]						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note: Only when rp = BC, DE, HL

4.3.3 Bit Manipulation Instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

Table 4-5. Bit Manipulations Listed by Operand Type

First Operand \ Second Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

4.3.4 Call Instructions/Branch Instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

Table 4-6. Call and Branch Instructions Listed by Operand Type

Second Operand / First Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR BC BNC BZ BNZ
Compound instruction					BT BF BTCLR DBNZ

4.3.5 Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

CHAPTER 5 SAMPLE PROGRAM

This chapter contains a sample program that shows the structure of a typical K0 program module. The text below describes the sections contained in this chapter.

5.1 This section, entitled **Test.asm**, contains the source code for a typical module.
The module starts by declaring the label **Interval_timer_2** as public. Next, it reserves 23H bytes of RAM. After that it shows how to tell the assembler how to set up the reset address, external interrupt INTP1, and an internal interrupt from 8-bit timer/event counter 2 (INTTM2 with the label Interval_timer_2).

The program starts by going through an initialization routine. Next it executes the main_loop program while waiting for interrupts from timer/event counter 2 and external interrupt INTP1. The end of this module is designated by the **end** directive at the bottom of the page.

5.2 This section, entitled **Test.bat**, contains a batch file to assemble, link, and create a hex file from the Test.asm program. The batch file also creates an absolute listing using the assembler's list converter with the command:

lcnv78k0 test -ltest

5.3 This section, entitled **Test.prn**, contains a file that is generated when the program is assembled. The addresses in this file are not absolute addresses.

5.4 The final section, entitled **Test.p**, contains a file of the program with absolute memory locations. This file is created by the list converter, which is the last task in the batch file (**lcnv78k0 test -ltest**).

5.1 Test.asm

```
;This example shows the structure of a typical K0 program.

       public Interval_timer_2

;*********************************************************
;     Short address space saddr = 0FE20h to 0FF1Fh     ***
;*********************************************************

       dseg    saddr    ;Data segment saddr
SoftCount_0:  ds   1    ;Reserve one byte in saddr
SoftCount_1:  ds   2    ;Reserves one word in saddr

;*********************************************************
;    High speed RAM Allocation area 0FB00H to 0FEFFH    ***
;*********************************************************

       dseg   IHRAM  ;IHRAM is keyword for beginning
                     ;of internal RAM (address 0FB00H)
       ds     20h    ;Reserve 20 bytes for stack
Stack:               ;Declare starting address
                     ;of stack = 0FB20H

;*********************************************************
;     Set up reset (start of program) and              ***
;     interrupt vectors for internal counter 2         ***
;     and external interrupt INTP1                     ***
;*********************************************************

Vector cseg   at 0000h      ;Set up Reset address
       dw     Start         ;beginning at Start

       org    08h           ;Set up external interrupt
       dw     INTP1         ;address for INTP1.

       org    26h                ;Set up interrupt address
       dw     Interval_timer_2   ;of 8-bit timer 2 Interrupt.


Main   cseg               ;MAIN Routine
Start: mov    OSMS,#01H   ;Set up clock to divide by 1.
       movw   SP,#Stack   ;Set stack pointer to
                          ;0B20H (IHMEM + 20H)
       mov    TMC1,#02H   ;Enable 8-bit timer 2 clock
       mov    TCL1,#070H  ;Set 8-bit counter clock = 0.8 usec
       mov    CR20,#250   ;Set time interval time to 200 usec
       mov    INTM0,#00H  ;Sets INTP1 to falling edge
```

```
      clr1  TMMK2            ;Unmask timer 2 & INTP1
      clr1  PMK1             ;Unmask INTP1
      EI                     ;Enable interrupts.
      mov   SoftCount_0,#50  ;Set 8-bit software
                             ;counter to 10 msec

main_loop:
      cmp   SoftCount_0,#0   ;Is count = 0?
      bnz   $main_loop       ;No, keep testing.
      mov   SoftCount_0,#50  ;Yes, reset count to 50.
      br    $main_loop       ;Start testing the count.

;*********************************************************
;     Interval timer 2 Interrupt routine               ***
;     If SoftCount is not equal to 0, decrement        ***
;     SoftCount by 1. If count = 0, then stop.         ***
;*********************************************************

Interval_timer_2:            ;8-bit software counter
                             ;Interrupt every 200 usec
      cmp   SoftCount_0,#0   ;Is count = 0?
      bz    $it10            ;Yes, take branch.
      dec   SoftCount_0      ;No, decrement by 1.
it10: reti  ;Return from interrupt.

;***********************************************
;     Count every negative edge on external    ***
;     interrupt INTP1 and put the value in     ***
;     the HL register                          ***
;***********************************************

INTP1:add   a,l    ;Add reg L to A.
      xch   a,l    ;Put result in reg L.
      mov   a,h    ;Move reg H to A.
      addc  a,#0   ;Add any carry to A.
      xch   a,h    ;Put in reg H.
      reti
      end
```

5.2 Test.bat

```
REM     This batch file assembles, links, and generates a
REM     HEX file. It also generates an absolute listing.


ra78k0  test.asm -c078
REM     The above command assembles the ‘test’ program.

pause
REM     The above pause command allows the user
REM     to look at the assembly result.

lk78k0 test
REM     The above command links the ‘test’ program.

pause
REM     The above pause command allows the user
REM     to look at the linking result.

oc78k0 test
REM     The above command generates a hex file.

pause
REM     Examine the result of the hex file generation.

lcnv78k0 test  -ltest

REM     The above command generates an absolute
REM     listing of the ‘test’ file.
```

5.3 Test.prn

```
78K/0 Series Assembler V3.10
Date:11 Feb 1998 Page:    1

Command: test.asm -c078
Para-file:
In-file:  TEST.ASM
Obj-file: TEST.REL
Prn-file: TEST.PRN

       Assemble list

ALNO STNO ADRS OBJECT M  I  SOURCE STATEMENT

   1    1                 ;This example shows the structure of a typical K0
                           program.
   2    2
   3    3                      public  Interval_timer_2
   4    4
   5    5                 ;*************************************************
   6    6                 ;  Short address space saddr = 0FE20h to 0FF1Fh   ***
   7    7                 ;*************************************************
   8    8
   9    9 ----                 dseg    saddr     ;Data segment saddr
  10   10 0000            SoftCount_0:  ds  1     ;Reserve one byte in saddr
  11   11 0001            SoftCount_1:  ds  2     ;Reserves one word in saddr
  12   12
  13   13                 ;*************************************************
  14   14                 ; High speed RAM Allocation area 0FB00H to 0FEFFH  ***
  15   15                 ;*************************************************
  16   16
  17   17 ----                 dseg    IHRAM     ;IHRAM is keyword for beginning
  18   18                                         ;of internal RAM (address 0FB00H)
  19   19 0000                dseg      20h      ;Reserve 20 bytes for stack
  20   20 0020            Stack:                  ;Declare starting address
  21   21                                         ;of stack = 0FB20H
  22   22
  23   23                 ;*************************************************
  24   24                 ;   Set up reset (start of program) and          ***
  25   25                 ;   interrupt vectors for internal counter 2     ***
  26   26                 ;   and external interrupt INTP1                 ***
  27   27                 ;*************************************************
  28   28
  29   29 ----            Vector cseg    at 0000h  ;Set up Reset address
  30   30 0000 R0000             dw      Start     ;beginning at Start
  31   31
  32   32 ----                   org     08h       ;Set up external interrupt
```

```
33   33 0008 R3000            dw      INTP1     ;address for INTP1.
34   34
35   35 ----                  org   26h             ;Set up interrupt address
36   36 0026 R2800            dw    Interval_timer_2 ;of 8-bit timer 2 Interrupt.
37   37
38   38
39   39 ----             Main cseg            ;MAIN Routine
40   40 0000 13F201    Start: mov  OSMS,#01H  ;Set up clock to divide by 1.
41   41 0003 REE1C2000        movw SP,#Stack  ;Set stack pointer to
42   42                                       ;0B20H (IHMEM + 20H)
43   43 0007 134902           mov  TMC1,#02H  ;Enable 8-bit timer 2 clock
44   44 000A 134170           mov  TCL1,#070H ;Set 8-bit counter clock = 0.8 usec
45   45 000D 1117FA           mov  CR20,#250  ;Set time interval time to 200 usec
46   46 0010 13EC00           mov   INTM0,#00H ;Sets INTP1 to falling edge
47   47 0013 711BE6           clr1 TMMK2      ;Unmask timer 2 & INTP1
48   48 0016 712BE4           clr1 PMK1       ;Unmask INTP1
49   49 0019 7A1E             EI              ;Enable interrupts.
50   50 001B R110032          mov  SoftCount_0,#50;Set 8-bit software
51   51                                        ;counter to 10 msec
52   52
53   53 001E             main_loop:
54   54 001E RC80000     cmp   SoftCount_0,#0  ;Is count = 0?
55   55 0021 BDFB              bnz     $main_loop      ;No, keep testing.
56   56 0023 R110032     mov   SoftCount_0,#50 ;Yes, reset count to 50.
57   57 0026 FAF6              br      $main_loop      ;Start testing the count.
58   58
59   59                  ;*************************************************
60   60                  ;   Interval timer 2 Interrupt routine            ***
61   61                  ;   If SoftCount is not equal to 0, decrement     ***
62   62                  ;   SoftCount by 1. If count = 0, then stop.      ***
63   63                  ;*************************************************
64   64
65   65 0028             Interval_timer_2:            ;8-bit software counter
66   66                                               ;Interrupt every 200 usec
67   67 0028 RC80000     cmp   SoftCount_0,#0         ;Is count = 0?
68   68 002B AD02              bz      $it10           ;Yes, take branch.
69   69 002D R9100             dec     SoftCount_0     ;No, decrement by 1.
70   70 002F 8F          it10: reti                    ;Return from interrupt.
71   71
72   72                  ;*********************************************
73   73                  ;   Count every negative edge on external    ***
74   74                  ;   interrupt INTP1 and put the value in     ***
75   75                  ;   the HL register                          ***
76   76                  ;*********************************************
```

```
  77   77
  78   78 0030 610E        INTP1: add    a,l       ;Add reg L to A.
  79   79 0032 36                 xch    a,l       ;Put result in reg L.
  80   80 0033 67                 mov    a,h       ;Move reg H to A.
  81   81 0034 2D00               addc   a,#0      ;Add any carry to A.
  82   82 0036 37                 xch    a,h       ;Put in reg H.
  83   83 0037 8F                 reti
  84   84                         end


Segment information:

ADRS LEN    NAME

0000 0003H  ?DSEGS
0000 0020H  ?DSEGIH
0000 0002H  Vector
0008 0002H  ?A000008
0026 0002H  ?A000026
0000 0038H  Main

Target chip : uPD78078
Device file : V2.01
Assembly complete,      0 error(s) and      0 warning(s) found. (     0)
```

5.4 Test.p

```
78K/0 Series Assembler V3.10
Date:11 Feb 1998 Page:    1

Command: test.asm -c078
Para-file:
In-file:  TEST.ASM
Obj-file: TEST.REL
Prn-file: TEST.PRN

       Assemble list

ALNO STNO ADRS OBJECT M  I  SOURCE STATEMENT

   1    1                 ;This example shows the structure of a typical K0
                           program.
   2    2
   3    3                      public   Interval_timer_2
   4    4
   5    5                 ;*************************************************
   6    6                 ;  Short address space saddr = 0FE20h to 0FF1Fh   ***
   7    7                 ;*************************************************
   8    8
   9    9 ----                 dseg    saddr     ;Data segment saddr
  10   10 FE20            SoftCount_0:  ds   1     ;Reserve one byte in saddr
  11   11 FE21            SoftCount_1:  ds   2     ;Reserves one word in saddr
  12   12
  13   13                 ;*************************************************
  14   14                 ; High speed RAM Allocation area 0FB00H to 0FEFFH  ***
  15   15                 ;*************************************************
  16   16
  17   17 ----                 dseg    IHRAM    ;IHRAM is keyword for beginning
  18   18                                       ;of internal RAM (address 0FB00H)
  19   19 FB00                ds      20h       ;Reserve 20 bytes for stack
  20   20 FB20            Stack:                ;Declare starting address
  21   21                                       ;of stack = 0FB20H
  22   22
  23   23                 ;*************************************************
  24   24                 ;   Set up reset (start of program) and          ***
  25   25                 ;   interrupt vectors for internal counter 2     ***
  26   26                 ;   and external interrupt INTP1                 ***
  27   27                 ;*************************************************
  28   28
  29   29 ----            Vector cseg   at 0000h  ;Set up Reset address
  30   30 0000 R8000             dw     Start     ;beginning at Start
  31   31
  32   32 ----                   org    08h       ;Set up external interrupt
```

```
33   33 0008 RB000             dw     INTP1     ;address for INTP1.
34   34
35   35 ----                   org  26h              ;Set up interrupt address
36   36 0026 RA800             dw   Interval_timer_2 ;of 8-bit timer 2 Interrupt.
37   37
38   38
39   39 ----            Main  cseg            ;MAIN Routine
40   40 0080 13F201     Start:mov  OSMS,#01H  ;Set up clock to divide by 1.
41   41 0083 REE1C20FB        movw SP,#Stack  ;Set stack pointer to
42   42                                       ;0B20H (IHMEM + 20H)
43   43 0087 134902           mov TMC1,#02H  ;Enable 8-bit timer 2 clock
44   44 008A 134170           mov TCL1,#070H ;Set 8-bit counter clock = 0.8 usec
45   45 008D 1117FA           mov CR20,#250  ;Set time interval time to 200 usec
46   46 0090 13EC00           mov INTM0,#00H ;Sets INTP1 to falling edge
47   47 0093 711BE6           clr1 TMMK2     ;Unmask timer 2 & INTP1
48   48 0096 712BE4           clr1 PMK1      ;Unmask INTP1
49   49 0099 7A1E             EI             ;Enable interrupts.
50   50 009B R112032      mov  SoftCount_0,#50      ;Set 8-bit software
51   51                                        ;counter to 10 msec
52   52
53   53 009E              main_loop:
54   54 009E RC82000      cmp   SoftCount_0,#0          ;Is count = 0?
55   55 00A1 BDFB               bnz     $main_loop      ;No, keep testing.
56   56 00A3 R112032      mov   SoftCount_0,#50         ;Yes, reset count to 50.
57   57 00A6 FAF6               br      $main_loop      ;Start testing the count.
58   58
59   59                   ;*************************************************
60   60                   ;   Interval timer 2 Interrupt routine           ***
61   61                   ;   If SoftCount is not equal to 0, decrement    ***
62   62                   ;   SoftCount by 1. If count = 0, then stop.     ***
63   63                   ;*************************************************
64   64
65   65 00A8              Interval_timer_2:             ;8-bit software counter
66   66                                                 ;Interrupt every 200 usec
67   67 00A8 RC82000      cmp   SoftCount_0,#0          ;Is count = 0?
68   68 00AB AD02               bz      $it10          ;Yes, take branch.
69   69 00AD R9120              dec     SoftCount_0    ;No, decrement by 1.
70   70 00AF 8F           it10: reti                    ;Return from interrupt.
71   71
72   72                   ;*********************************************
73   73                   ;   Count every negative edge on external    ***
74   74                   ;   interrupt INTP1 and put the value in     ***
75   75                   ;   the HL register                          ***
76   76                   ;*********************************************
```

```
  77   77
  78   78 00B0 610E        INTP1: add    a,l       ;Add reg L to A.
  79   79 00B2 36                 xch    a,l       ;Put result in reg L.
  80   80 00B3 67                 mov    a,h       ;Move reg H to A.
  81   81 00B4 2D00               addc   a,#0      ;Add any carry to A.
  82   82 00B6 37                 xch    a,h       ;Put in reg H.
  83   83 00B7 8F                 reti
  84   84                         end


Segment information:

ADRS LEN    NAME

FE00 0003H  ?DSEGS
FB00 0020H  ?DSEGIH
0000 0002H  Vector
0008 0002H  ?A000008
0026 0002H  ?A000026
0080 0038H  Main

Target chip : uPD78078
Device file : V2.01
Assembly complete,      0 error(s) and      0 warning(s) found. (     0)
```

CHAPTER 6 DEVICE MEMORY MAP AND SPECIAL FUNCTION REGISTERS

This chapter describes the memory maps and special function registers (SFRs) of each K0 Series device. They are categorized by subseries and shown in each section, as follows:

6.1 μPD78014, 78014H, and 78018F Subseries
6.2 μPD780208 Subseries
6.3 μPD780024 and 780034 Subseries
6.4 μPD78044F and 78044H Subseries
6.5 μPD78054, 78058F, and 780058 Subseries
6.6 μPD78064, 78064B, and 780308 Subseries
6.7 μPD78078, 78075B, and 78070A Subseries
6.8 μPD78083 Subseries

6.1 μPD78014, 78014H, and 78018F Subseries

6.1.1 Documentation Reference Information

Device Series Number	User's Manual Number	Date Published
μPD78014/14Y	U10085EJ7V0UM00	October 1997
μPD78014H	U12220EJ1V0UM00	May 1997
μPD78018F/18FY	U10659EJ4V0UM00	June 1997

Caution: The user should check the current User's Manual with the information in this section to be sure of having the most up-to-date information.

6.1.2 Device Series Differences

Device Series Number	ROM and RAM Differences		Number of Serial Channels
	ROM Size	RAM Size	
μPD78014, 78014Y	8 K/16 K/24 K/32 K	512/1 K	2
μPD78014H	8 K/16 K/24 K/32 K/60 K		
μPD78018F, 78018FY	8 K/16 K/24 K/32 K/40 K/48 K/60 K		

General Programmer's Note

The NEC C-compiler and the NEC Assembler are capable of recognizing certain symbolic SFR bit names. These special bit names are identified in the user manual in one of the four ways shown below:

1. <7>
2. (7)
3. ⑦
4. [7]

Example:

	<7>	<6>	<5>	<4>	3	2	1	0
PCC	MCC	FRC	CLS	CSS	0	PCC2	PCC1	PCC0

If a bit number has one of the four symbols around it, the NEC software will recognize the associated symbolic bit name. For example to set bit 7, the user can write the code in two ways:

```
1.    SET1    MCC
2.    SET1    PCC.7
```

Alternatively since bit 2 does not have any of the four symbols around it, the user can only set this bit as follows:

```
1.    SET1    PCC.2
```

Note: The attempt to employ a symbolic name of bit-2 (PCC2) will return an error. Thus the use of instruction

```
SET1    PCC2
```

is improper since neither the NEC C-compiler nor the NEC Assembler recognizes this symbolic name and will generate an error.

6.1.3 Memory Address Space

Each model in the μPD78014/14Y, 78014H, and 78018F/18FY Subseries can access a memory space of 64K. Figures 6-1 through 6-7 show memory maps of the respective models.

Figure 6-1. Memory Map (μPD78011B/11BY, 11F/11FY, 11H)

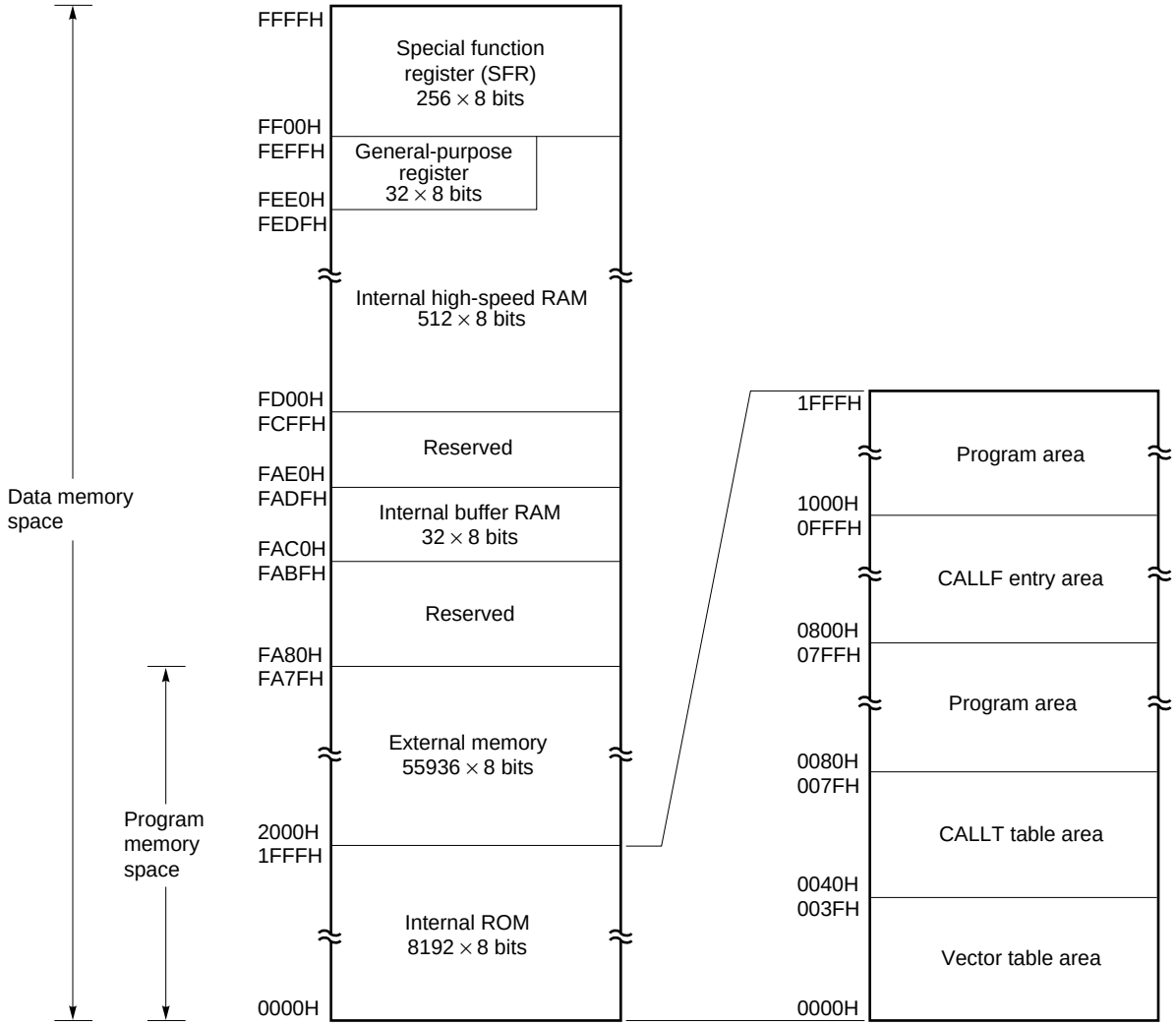


Figure 6-2. Memory Map (μPD78012B/12BY, 12F/12FY, 12H)

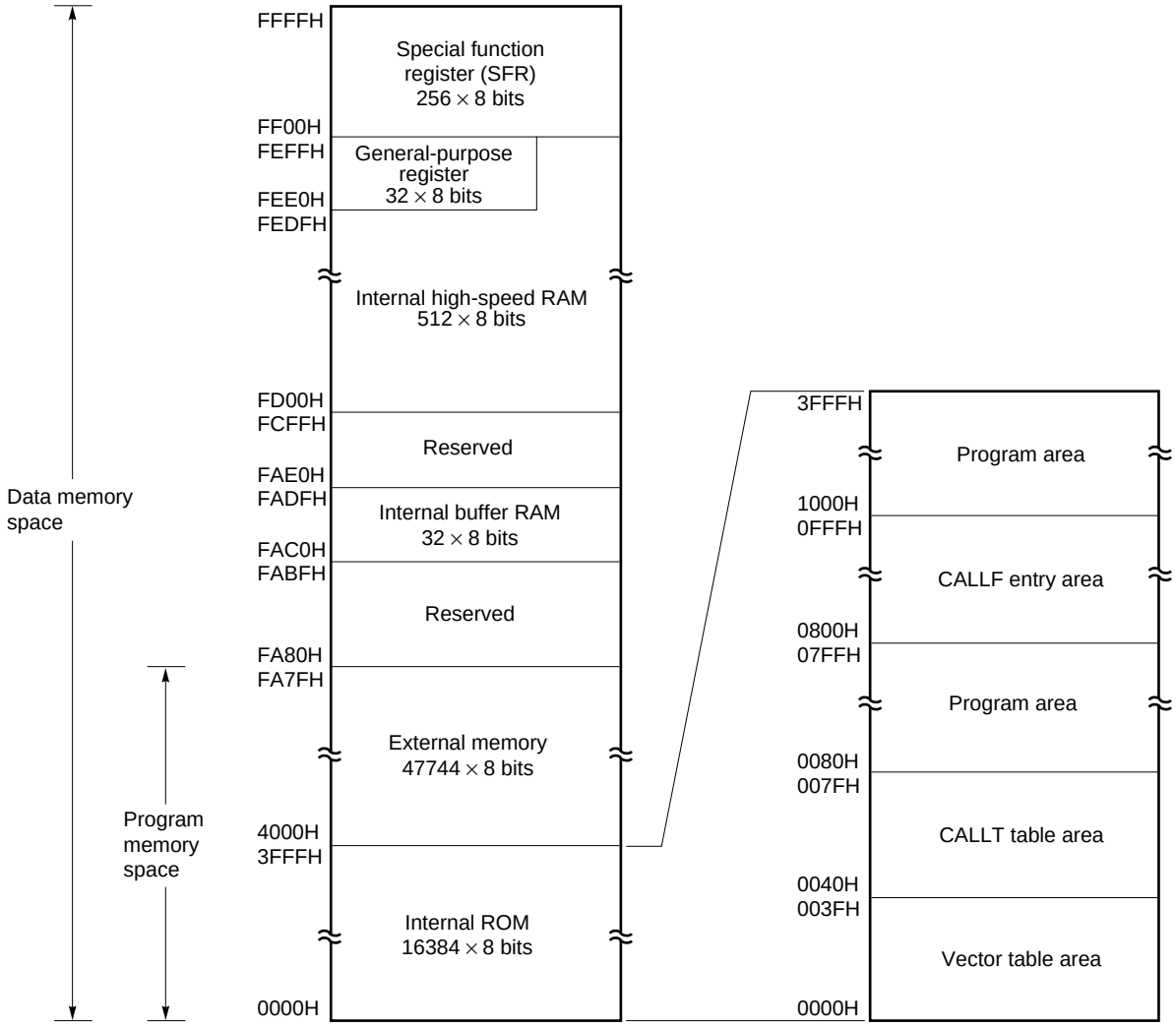


Figure 6-3. Memory Map (μPD78013/13Y, 13F/13FY, 13H)

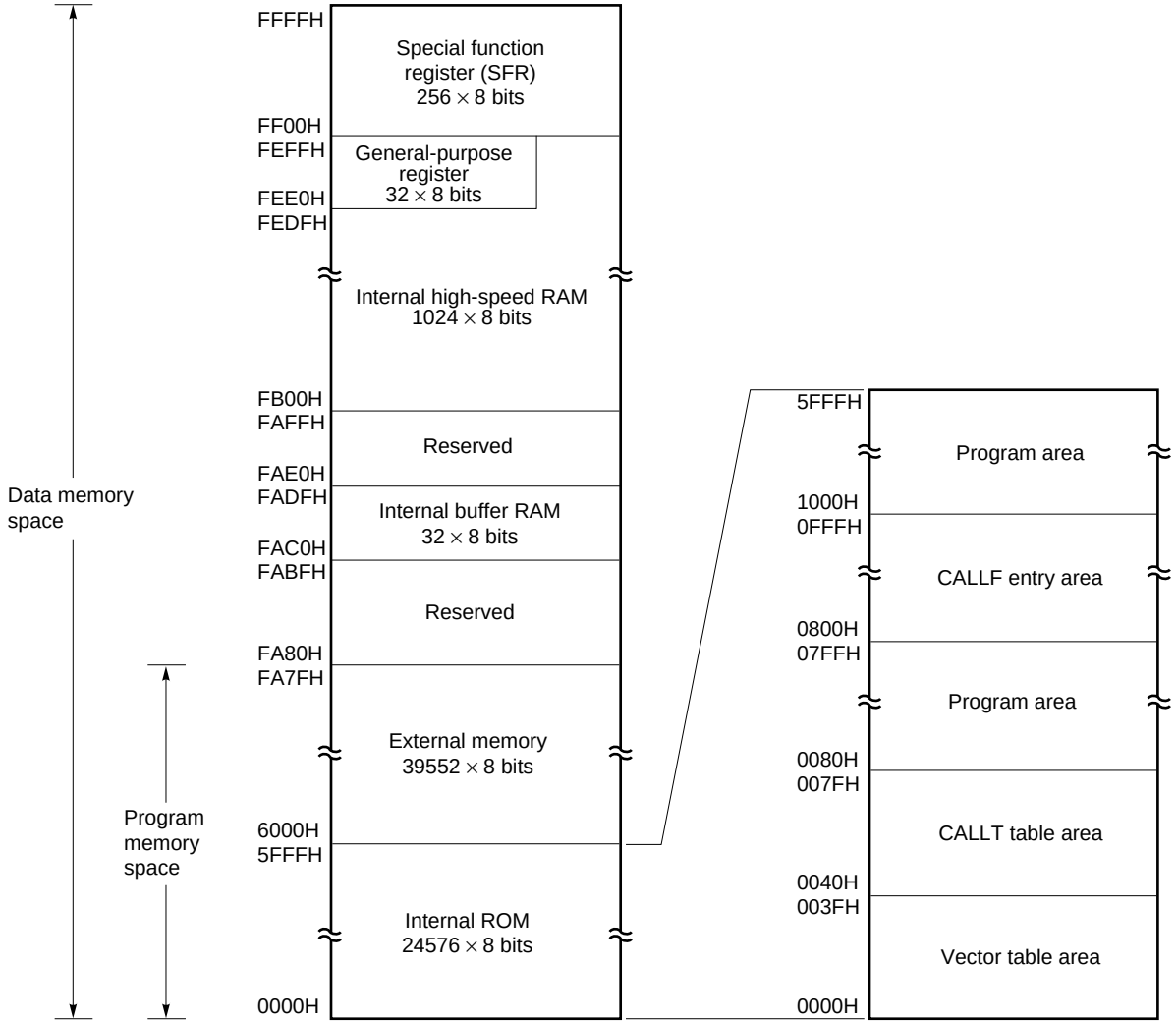


Figure 6-4. Memory Map (μPD78014/14Y, 78P014/14Y, 78014F/14FY, 14H)

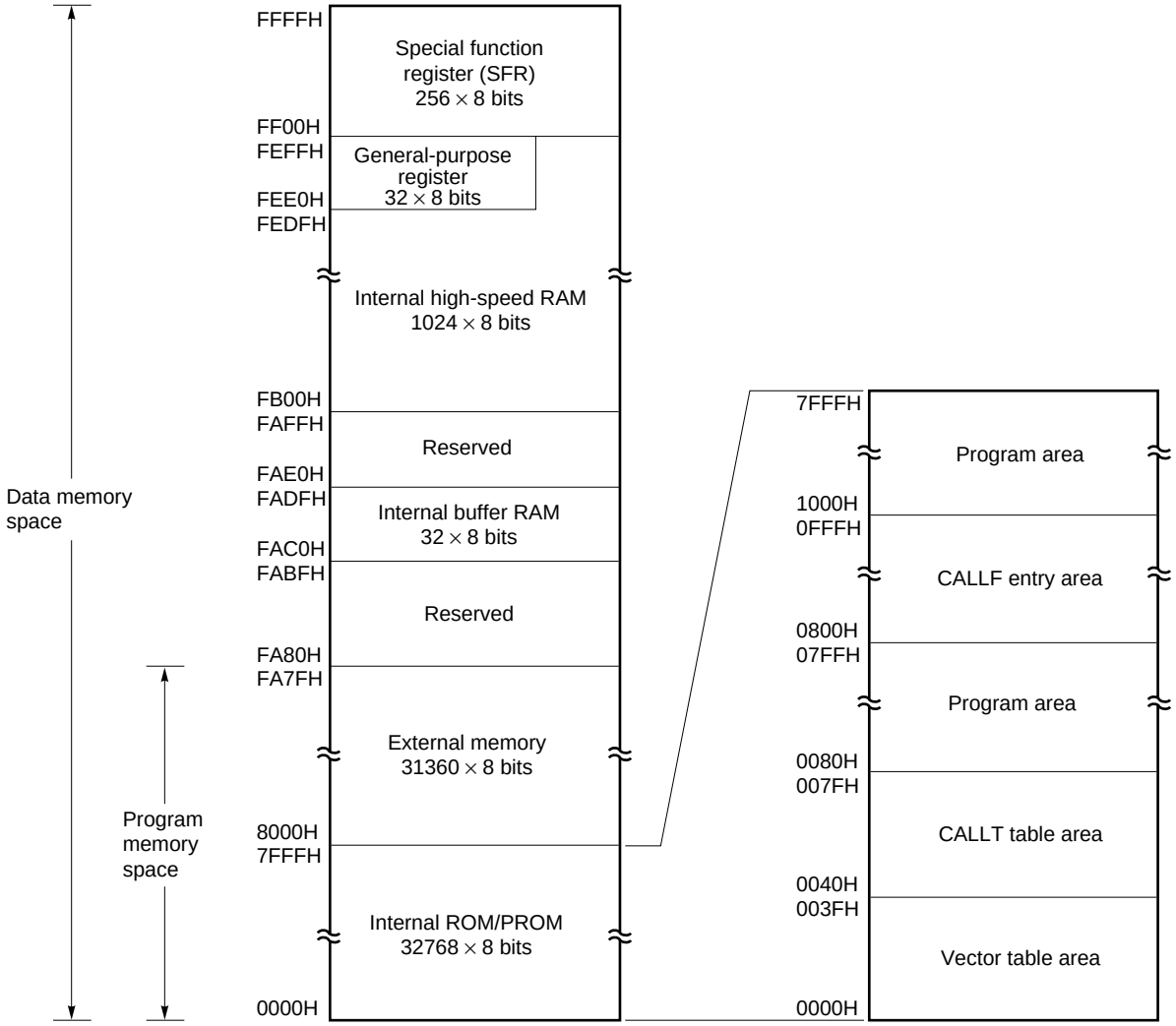


Figure 6-5. Memory Map (μPD78015F/15FY)

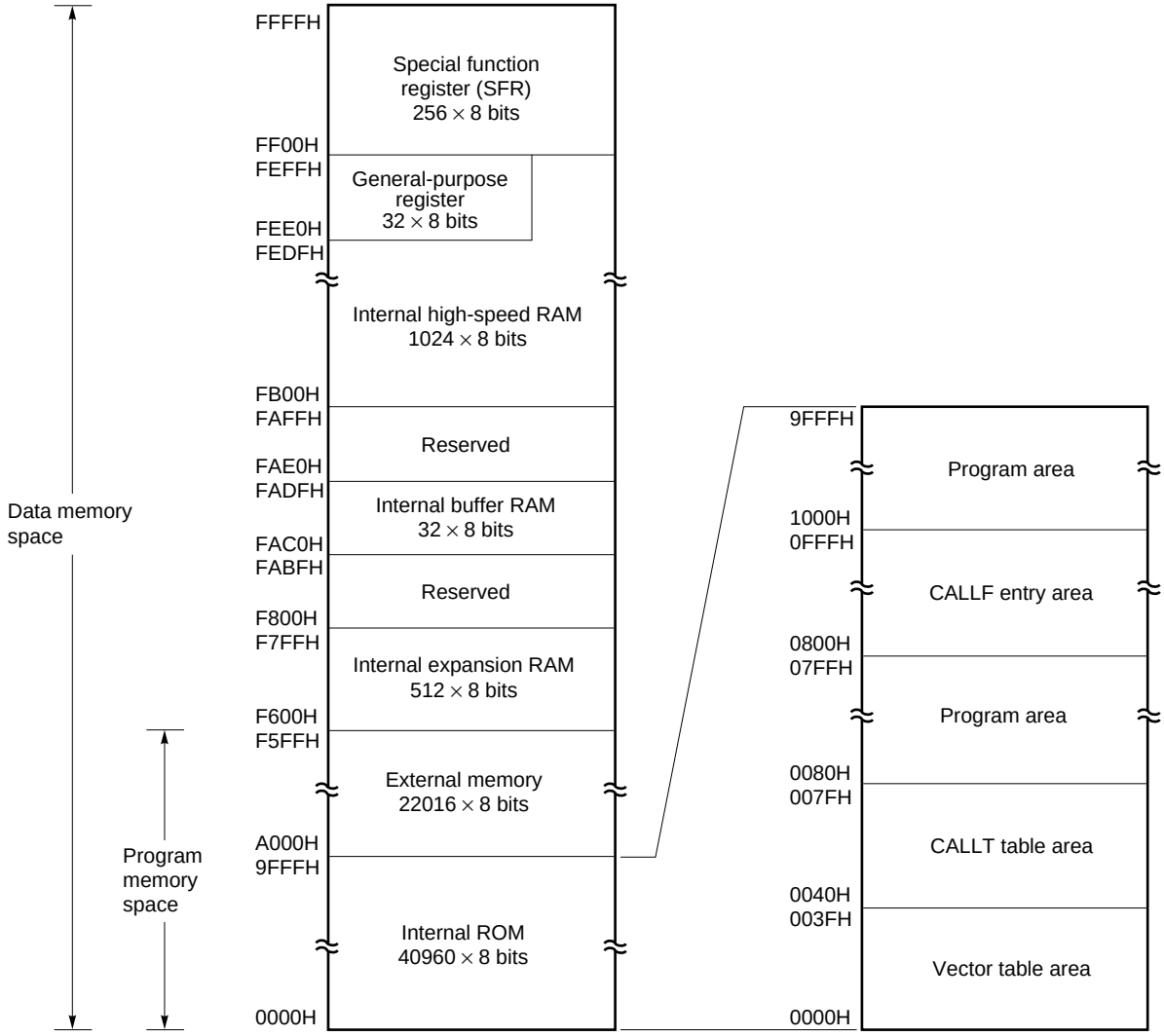


Figure 6-6. Memory Map (μPD78016F/16FY)

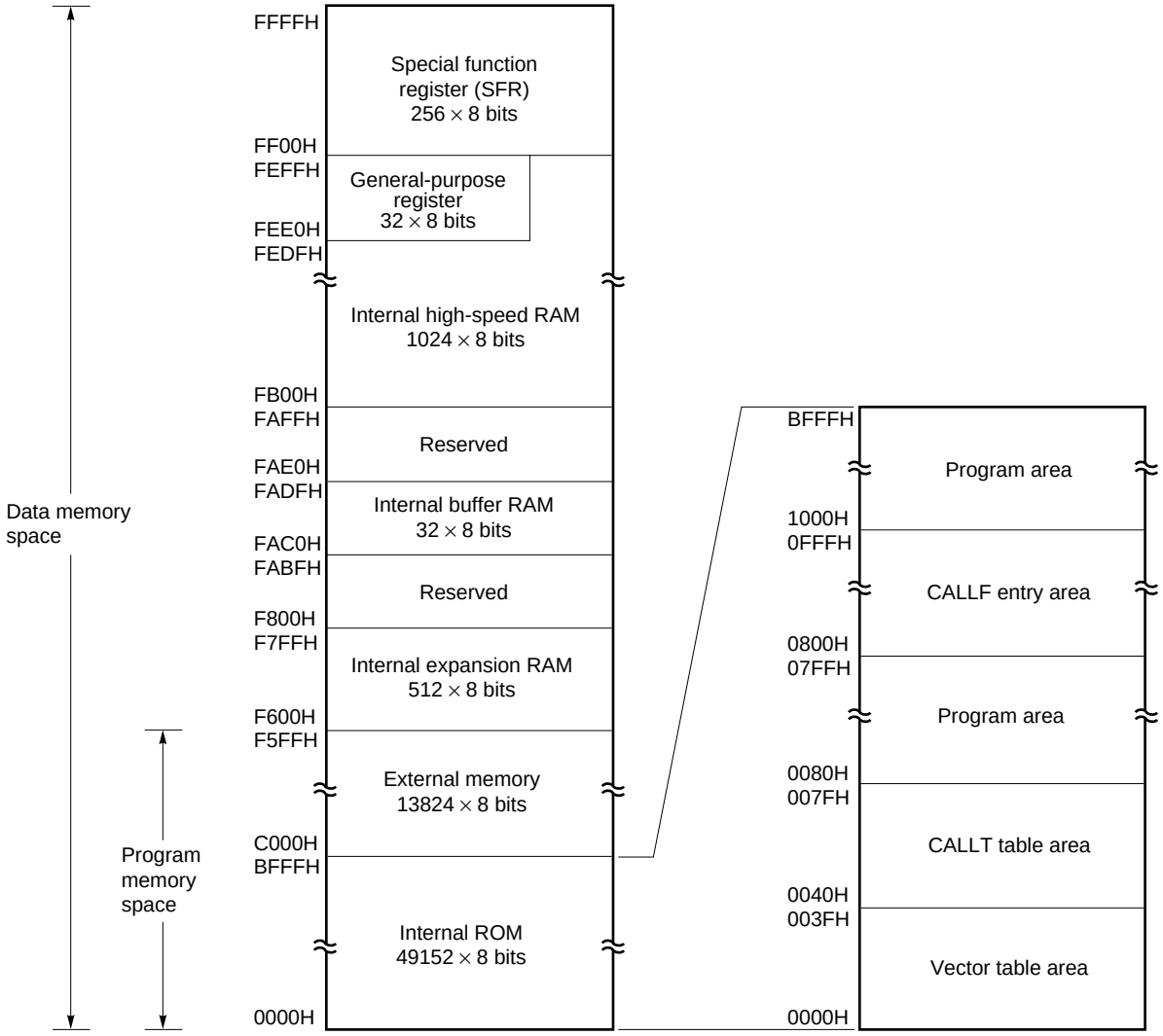
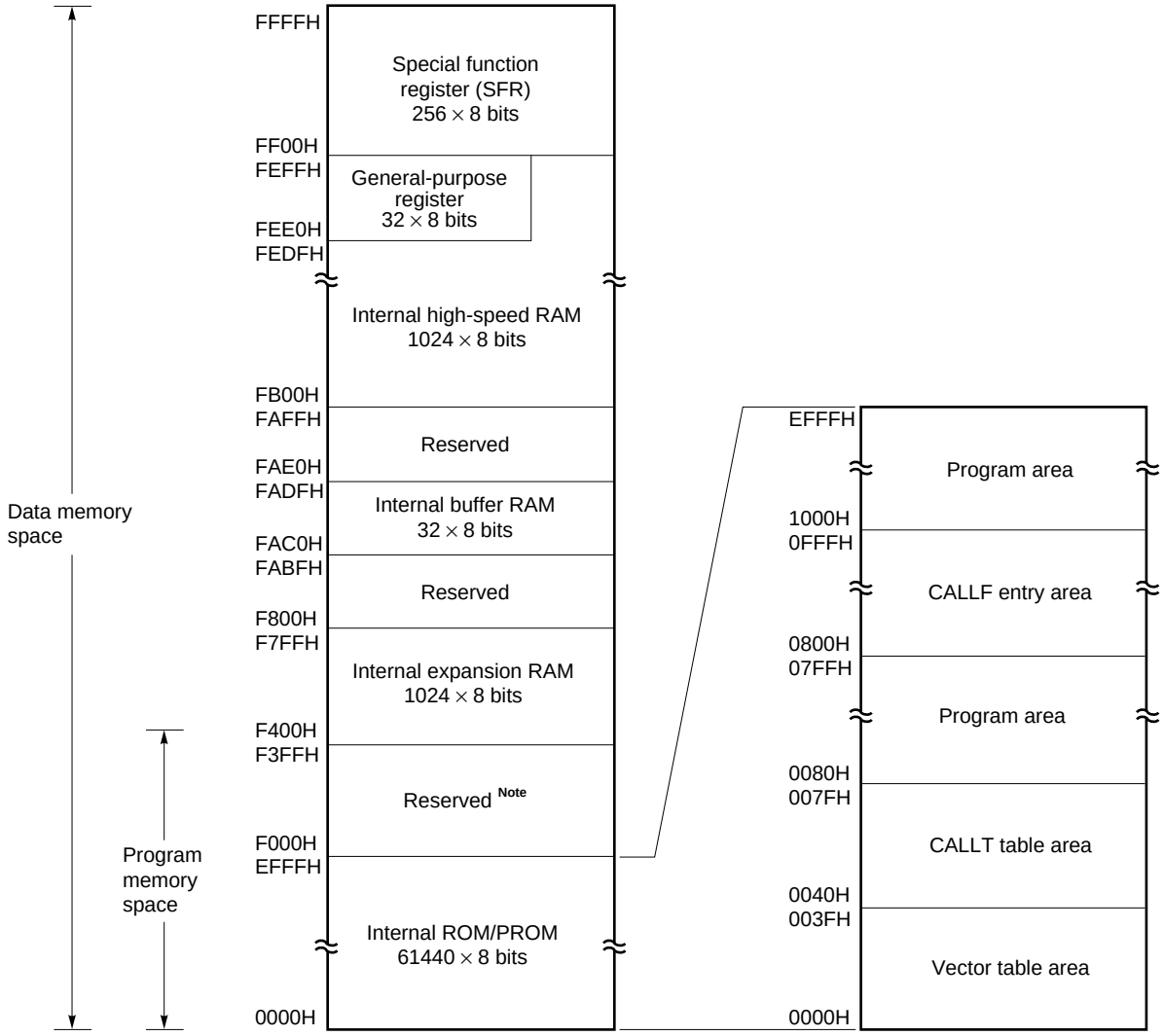


Figure 6-7. Memory Map (μPD78018F/18FY, 78P018F/18FY)



Note: When the internal ROM or internal PROM capacity is 60K, the area of F000H–F3FFH cannot be used. The area of F000H–F3FFH can be used as an external memory by setting the internal ROM capacity to 56K or less with the internal memory size switching register (IMS).

6.1.4 Special Function Registers (SFRs)

Table 6-1. Special Function Register List (μPD78014/14Y, 78014H, and 78018F/18FY Subseries) (1/2)

Address	Special Function Register (SFR) Name	Symbol	R/W	Access Unit			After Reset
				1 bit	8 bits	16 bits	
FF00H	Port 0	P0	R/W	√	√	–	00H
FF01H	Port 1	P1		√	√	–	
FF02H	Port 2	P2		√	√	–	
FF03H	Port 3	P3		√	√	–	
FF04H	Port 4	P4		√	√	–	Undefined
FF05H	Port 5	P5		√	√	–	
FF06H	Port 6	P6		√	√	–	
FF10H FF11H	16-bit compare register	CR00		–	–	√	
FF12H FF13H	16-bit capture register	CR01	R	–	–	√	
FF14H FF15H	16-bit timer register	TM0		–	–	√	0000H
FF16H	8-bit compare register	CR10	R/W	–	√	–	Undefined
FF17H	8-bit compare register	CR20		–	√	–	
FF18H	8-bit timer register 1	TMS TM1	R	–	√	√	00H
FF19H	8-bit timer register 2	TM2		–	√		
FF1AH	Serial I/O shift register 0	SIO0	R/W	–	√	–	Undefined
FF1BH	Serial I/O shift register 1	SIO1		–	√	–	
FF1FH	A/D conversion result register	ADCR	R	–	√	–	
FF20H	Port mode register 0	PM0	R/W	√	√	–	1FH
FF21H	Port mode register 1	PM1		√	√	–	FFH
FF22H	Port mode register 2	PM2		√	√	–	
FF23H	Port mode register 3	PM3		√	√	–	
FF25H	Port mode register 5	PM5		√	√	–	
FF26H	Port mode register 6	PM6		√	√	–	
FF38H FF39H	Collection address register 0 Note 1	CORAD0		–	–	√	0000H
FF3AH FF3BH	Collection address register 1 Note 1	CORAD1		–	–	√	
FF40H	Timer clock select register 0	TCL0		√	√	–	00H
FF41H	Timer clock select register 1	TCL1		–	√	–	
FF42H	Timer clock select register 2	TCL2		–	√	–	
FF43H	Timer clock select register 3	TCL3		–	√	–	88H
FF47H	Sampling clock select register	SCS		–	√	–	00H
FF48H	16-bit timer mode control register	TMC0		√	√	–	
FF49H	8-bit timer mode control register	TMC1		√	√	–	
FF4AH	Watch timer mode control register	TMC2		√	√	–	
FF4EH	16-bit timer output control register	TOC0		√	√	–	

Table 6-1. Special Function Register List (μPD78014/14Y, 78014H, and 78018F/18FY Subseries) (2/2)

Address	Special Function Register (SFR) Name	Symbol		R/W	Access Unit			After Reset
					1 bit	8 bits	16 bits	
FF4FH	8-bit timer output control register	TOC1		R/W	√	√	–	00H
FF60H	Serial operation mode register 0	CSIM0			√	√	–	
FF61H	Serial bus interface control register	SBIC			√	√	–	
FF62H	Slave address register	SVA			–	√	–	Undefined
FF63H	Interrupt timing specification register	SINT			√	√	–	00H
FF68H	Serial operation mode register 1	CSIM1			√	√	–	
FF69H	Automatic data transmit/receive control register	ADTC			√	√	–	
FF6AH	Automatic data transmit/receive address pointer	ADTP			–	√	–	
FF6BH	Automatic transmit/receive interval specification register Note 1	ADTI			√	√	–	
FF80H	A/D converter mode register	ADM			√	√	–	01H
FF84H	A/D converter input select register	ADIS			–	√	–	00H
FF8AH	Collection control register Note 1	CORCN			√	√	–	
FFD0H to FFDFH	External access area Note 2				√	√	–	Undefined
FFE0H	Interrupt request flag register 0L	IF0	IF0L		√	√	√	00H
FFE1H	Interrupt request flag register 0H		IF0H		√	√		
FFE4H	Interrupt mask flag register 0L	MK0	MK0L		√	√	√	FFH
FFE5H	Interrupt mask flag register 0H		MK0H		√	√		
FFE8H	Priority specification flag register 0L	PR0	PR0L		√	√	√	
FFE9H	Priority specification flag register 0H		PR0H		√	√		
FFECH	External interrupt mode register	INTM0			–	√	–	00H
FFF0H	Internal memory size switching register	IMS		W	–	√	–	**Note 3**
FFF4H	Internal expansion RAM size switching register	IXS			–	√	–	**Note 4**
FFF6H	Key return mode register	KRM		R/W	√	√	–	02H
FFF7H	Pull-up resistor option register	PUO			√	√	–	00H
FFF8H	Memory expansion mode register	MM			√	√	–	10H
FFF9H	Watchdog timer mode register	WDTM			√	√	–	00H
FFFAH	Oscillation stabilization time select register	OSTS			–	√	–	04H
FFFBH	Processor clock control register	PCC			√	√	–	

Notes: 1. Provided to some products of the μPD78018F Subseries only:
μPD78015F/FY, 78016F/FY, 78018F/FY, and 78P018F/FY.

2. The external access area cannot be accessed by SFR addressing. Access this area by means of direct addressing.

3. The value after reset differs depending on the product, as follows:

	μPD78011B/BY μPD78011F/FY μPD78011H	μPD78012B/BY μPD78012F/FY μPD78012H	μPD78013/Y μPD78013F/FY μPD78013H	μPD78014/Y μPD78P014F/FY μPD78014F/FY μPD78014H	μPD78015F/FY	μPD78016F/FY	μPD78018F/FY μPD78P018F/FY
IMS	42H	44H	C6H	C8H	CAH	CCH	CFH

To use a mask ROM version, do not set to IMS a value other than that after reset, except when the external device expansion function is used with the μPD78018F/FY.

4. Provided to μPD78011F/FY, 78012F/FY, 78013F/FY, 78014F/FY, 78015F/FY, 78016F/FY, 78018F/FY, and 78P018F/FY (μPD78018F, 78018FY Subseries) only.
The value after reset differs depending on the product, as follows:

	μPD78011F/FY	μPD78012F/FY	μPD78013F/FY	μPD78014F/FY	μPD78015F/FY	μPD78016F/FY	μPD78018F/FY μPD78P018F/FY
IXS	0CH				0BH		0AH

To use a mask ROM version, do not set to IXS a value other than that after reset, except when the external device expansion function is used with the μPD78018F/FY.

(1) Registers controlling port functions

The following four types of registers control the ports:

- Port mode registers (PM0, PM1, PM2, PM3, PM5, PM6)
- Pull-up resistor option register (PUO)

Format of Port Mode Registers

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PM0	0	0	0	1	PM03	PM02	PM01	1	FF20H	1FH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W
PM3	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	FF23H	FFH	R/W
PM5	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	FF25H	FFH	R/W
PM6	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	FF26H	FFH	R/W

PMmn	Selects I/O mode of Pmn pin (m = 0, 1, 2, 3, 5, 6 : n = 0 to 7)
0	Output mode (output buffer ON)
1	Input mode (output buffer OFF)

Cautions: 1. Pins P00 and P04 are input-only pins.

2. I/O specification of pins P40 to P47 is set by using the memory expansion mode register (MM).

3. As port 0 has an alternate function as external interrupt request input, when the port function output mode is specified and the output level is changed, the interrupt request flag is set. When the output mode is used, therefore, the interrupt mask flag should be set to 1 beforehand.

Format of Pull-up Resistor Option Register

Symbol	7	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
PUO	0	PUO6	PUO5	PUO4	PUO3	PUO2	PUO1	PUO0	FFF7H	00H	R/W

PUOm	Selects internal pull-up resistor of Pm (m = 0, 1, 2, 3, 4, 5, 6)
0	Internal pull-up resistor is not used
1	Internal pull-up resistor is used

Cautions: 1. The P00 and P04 pins do not incorporate a pull-up resistor.

2. When ports 1, 4, and 5 and the P64 to P67 pins are used as alternate function pins, an on-chip pull-up resistor cannot be used even if 1 is set in PUOm (m = 1, 4 to 6).

3. The PU06 bit of PUO register controls pull-up resistors of only P64 through P67 in both mask and OTP devices. The pull-up resistors of P60 through P63 are only available as mask option in 1-bit inputs and cannot be selected in OTP devices.

(2) Register controlling clock generator

The following register controls the clock generator:

- Processor clock control (PCC) register

Format of Processor Clock Control Register

Symbol	<7>	<6>	<5>	<4>	3	2	1	0	Address	After Reset	R/W
PCC	MCC	FRC	CLS	CSS	0	PCC2	PCC1	PCC0	FFFBH	04H	R/W Note 1

R/W

CSS	PCC2	PCC1	PCC0	Selects CPU clock (f_{CPU})
0	0	0	0	f_X (0.4 μs)
	0	0	1	$f_X/2$ (0.8 μs)
	0	1	0	$f_X/2^2$ (1.6 μs)
	0	1	1	$f_X/2^3$ (3.2 μs)
	1	0	0	$f_X/2^4$ (6.4 μs)
1	0	0	0	f_{XT} (122 μs)
	0	0	1	
	0	1	0	
	0	1	1	
	1	0	0	
Settings other than above are prohibited				

R

CLS	Status of CPU clock
0	Main system clock
1	Subsystem clock

R/W

FRC	Selects feedback resistor of subsystem clock
0	Uses internal feedback resistor
1	Does not use internal feedback resistor

R/W

MCC	Controls oscillation of main system clock Note 2
0	Enables oscillation
1	Stops oscillation

Notes: 1. Bit 5 is a read-only bit.

2. To stop oscillation of the main system clock while the CPU operates on the subsystem clock, use MCC. Do not use the STOP instruction.

Caution: Be sure to clear bit 3 to 0.

Remarks: f_X: Main system clock oscillation frequency

f_{XT}: Subsystem clock oscillation frequency

( ): Minimum instruction execution time at f_X = 10.0 MHz or f_{XT} = 32.768 kHz: $4/f_{CPU}$

(3) Registers controlling 16-bit timer/event counter

The following six registers control the 16-bit timer/event counter:

- Timer clock select register 0 (TCL0)
- 16-bit timer mode control register (TMC0)
- 16-bit timer output control register (TOC0)
- Port mode register 3 (PM3)
  - Refer to section (1) for the register format.
- External interrupt mode register (INTM0)
  - Refer to section (13) for the register format.
- Sampling clock select register (SCS)
  - Refer to section (13) for the register format.

Format of Timer Clock Select Register 0

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL0	CLOE	TCL06	TCL05	TCL04	TCL03	TCL02	TCL01	TCL00	FF40H	00H	R/W

This section controls the clock output circuit.
Refer to **(7) Registers controlling clock output function** or **Chapter 12** of *μPD78014, 78014Y Subseries User's Manual*, **Chapter 10** of *μPD78014H Subseries User's Manual*, or **Chapter 12** of *μPD78018F, 78018FY Subseries User's Manual* for detailed information.

TCL06	TCL05	TCL04	Selects count clock of 16-bit timer register
0	0	0	TI0 (valid edge can be specified)
0	1	0	$f_X/2$ (5.0 MHz)
0	1	1	$f_X/2^2$ (2.5 MHz)
1	0	0	$f_X/2^3$ (1.25 MHz)
Settings other than above are prohibited			

Cautions: 1. Setting of the TI0/INTP0 pin valid edge is performed by the external interrupt mode register and selection of the sampling clock frequency is performed by the sampling clock select register.

2. To read the count value when TI0 has been specified as the TM0 count clock, the value should be read from TM0, not from the 16-bit capture register (CR01).

3. To write data other than that already written to TCL0, stop the timer operation once.

Remarks: f_X: Main system clock oscillation frequency
TI0: Input pin of 16-bit timer/event counter
TM0: 16-bit timer register
( ): At f_X = 10.0 MHz operation

This register is also used to set the clock for PCL output, in addition to the function of setting the count clock of the 16-bit timer register.

Format of 16-Bit Timer Mode Control Register

Symbol	7	6	5	4	3	2	1	<0>	Address	After Reset	R/W
TMC0	0	0	0	0	TMC03	TMC02	TMC01	OVF0	FF48H	00H	R/W

OVF0	Detects overflow in 16-bit timer register
0	Overflow does not occur
1	Overflow occurs

TMC03	TMC02	TMC01	Selects operation mode or clear mode	Selects timing of TO0 output	Generates interrupt
0	0	0	Stops operation (TM0 is cleared to 0)	Not affected	Not generated
0	0	1	PWM mode (free running)	PWM pulse output	Generated when TM0 coincides with CR00
0	1	0	Free-running mode	Coincidence between TM0 and CR00	
0	1	1		Coincidence between TM0 and CR00 or valid edge of TI0	
1	0	0	Clear and start at valid edge of TI0	Coincidence between TM0 and CR00	
1	0	1		Coincidence between TM0 and CR00 or valid edge of TI0	
1	1	0	Clear and start at coincidence between TM0 and CR00	Coincidence between TM0 and CR00	
1	1	1		Coincidence between TM0 and CR00 or valid edge of TI0	

Cautions: 1. The 16-bit timer register (TM0) starts operation when a value other than 0, 0, 0 is set to TMC01 to TMC03 (Operation Stop mode). To stop the operation, set TMC01 to TMC03 to 0, 0, 0.

2. Before changing the mode of operation and/or output timing, stop the timer (set TMC01 through TMC03 to 0, 0, 0).

3. The valid edge of the TI0/INTP0 pin is set by the external Interrupt mode register. The frequency of the sampling clock is selected by the sampling clock select register.

4. When using the PWM mode, set the PWM mode and then set data to CR00.

5. When a mode in which the 16-bit timer is cleared and started on coincidence between TM0 and CR00 is selected, the OVF0 flag is set to 1 when the value of TM0 changes from FFFFH to 0000H, with FFFFH set to CR00.

Remarks: TO0: Output pin of 16-bit timer/event counter
TI0: Input pin of 16-bit timer/event counter
TM0: 16-bit timer register
CR00: 16-bit compare register

Format of 16-Bit Timer Output Control Register

Symbol	7	6	5	4	<3>	<2>	1	<0>	Address	After Reset	R/W
TOC0	0	0	0	0	LVS0	LVR0	TOC01	TOE0	FF4EH	00H	R/W

TOE0	Controls output of 16-bit timer/event counter
0	Disables output (Port mode)
1	Enables output

TOC01	PWM mode	Other than PWM mode
	Selects active level	Controls timer output F/F
0	High active	Disables inversion
1	Low active	Enables inversion

LVS0	LVR0	Sets status of timer output F/F of 16-bit timer/event counter
0	0	Not affected
0	1	Resets timer output F/F to 0
1	0	Sets timer output F/F to 1
1	1	Setting prohibited

Cautions: 1. Be sure to stop the timer operation before setting TOC0.

2. 0 is read from LVS0 and LVR0 after data has been set to these bits.

Format of External Interrupt Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
INTM0	ES31	ES30	ES21	ES20	ES11	ES10	0	0	FFECH	00H	R/W

ES11	ES10	Selects valid edge of INTP0
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

ES21	ES20	Selects valid edge of INTP1
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

ES31	ES30	Selects valid edge of INTP2
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

Caution: Before setting the valid edge of the INP0/TI0/P00 pin, stop the timer operation by clearing bits 1 through 3 (TMC01 through TMC03) of the 16-bit timer mode control register (TMC0) to 0, 0, 0.

Remarks: The INTP0 pin also functions as TI0/P00.
The valid edge of INTP3 is fixed at the falling edge.

Format of Sampling Clock Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
SCS	0	0	0	0	0	0	SCS1	SCS0	FF47H	00H	R/W

SCS1	SCS0	Selects sampling clock of INTP0
0	0	$f_X/2^{N+1}$
0	1	Setting prohibited
1	0	$f_X/2^6$ (156 kHz)
1	1	$f_X/2^7$ (78.1 kHz)

Caution: $f_X/2^{N+1}$ is the clock supplied to the CPU, and $f_X/2^6$ and $f_X/2^7$ are the clocks supplied to the hardware. $f_X/2^{N+1}$ is stopped in the HALT mode.

Remarks: N: Value (N = 0 to 4) set to bits 0 to 2 (PCC0 to PCC2) of the processor clock control register
f_X: Main system clock oscillation frequency
( ): At f_X = 10.0 MHz operation

(4) Registers controlling 8-bit timer/event counter

The following four registers control the 8-bit timer/event counters:

- Timer clock select register 1 (TCL1)
- 8-bit timer mode control register (TMC1)
- 8-bit timer output control register (TOC1)
- Port mode register 3 (PM3)
  - Refer to section (1) for register format.

Format of Timer Clock Select Register 1

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL1	TCL17	TCL16	TCL15	TCL14	TCL13	TCL12	TCL11	TCL10	FF41H	00H	R/W

TCL13	TCL12	TCL11	TCL10	Selects count clock of 8-bit timer register 1
0	0	0	0	Falling edge of TI1
0	0	0	1	Rising edge of TI1
0	1	1	0	$f_X/2^2$ (2.5 MHz)
0	1	1	1	$f_X/2^3$ (1.25 MHz)
1	0	0	0	$f_X/2^4$ (625 kHz)
1	0	0	1	$f_X/2^5$ (313 kHz)
1	0	1	0	$f_X/2^6$ (156 kHz)
1	0	1	1	$f_X/2^7$ (78.1 kHz)
1	1	0	0	$f_X/2^8$ (39.1 kHz)
1	1	0	1	$f_X/2^9$ (19.5 kHz)
1	1	1	0	$f_X/2^{10}$ (9.8 kHz)
1	1	1	1	$f_X/2^{12}$ (2.4 kHz)
Settings other than above are prohibited				

TCL17	TCL16	TCL15	TCL14	Selects count clock of 8-bit timer register 2
0	0	0	0	Falling edge of TI2
0	0	0	1	Rising edge of TI2
0	1	1	0	$f_X/2^2$ (2.5 MHz)
0	1	1	1	$f_X/2^3$ (1.25 MHz)
1	0	0	0	$f_X/2^4$ (625 kHz)
1	0	0	1	$f_X/2^5$ (313 kHz)
1	0	1	0	$f_X/2^6$ (156 kHz)
1	0	1	1	$f_X/2^7$ (78.1 kHz)
1	1	0	0	$f_X/2^8$ (39.1 kHz)
1	1	0	1	$f_X/2^9$ (19.5 kHz)
1	1	1	0	$f_X/2^{10}$ (9.8 kHz)
1	1	1	1	$f_X/2^{12}$ (2.4 kHz)
Settings other than above are prohibited				

Caution: To write data other than that already written to TCL1, stop the timer operation once.

Remarks: f_X: Main system clock oscillation frequency
TI1: Input pin of 8-bit timer register 1
TI2: Input pin of 8-bit timer register 2
( ): At f_X = 10.0 MHz operation

Format of 8-Bit Timer Mode Control Register

Symbol	7	6	5	4	3	2	<1>	<0>	Address	After Reset	R/W
TMC1	0	0	0	0	0	TMC12	TCE2	TCE1	FF49H	00H	R/W

TCE1	Controls operation of 8-bit timer register 1
0	Stops operation (TM1 is cleared to 0)
1	Enables operation

TCE2	Controls operation of 8-bit timer register 2
0	Stops operation (TM2 is cleared to 0)
1	Enables operation

TMC12	Selects operation mode
0	8-bit timer register × 2 channel mode (TM1 , TM2)
1	16-bit timer register × 1 channel mode (TMS)

Cautions: 1. Before changing the operation mode, stop the timer operations.

2. When TM1 and TM2 are used together as a 16-bit timer register (TMS), set enable or disable of the operation by using the TCE1 bit of the 8-bit timer mode control register (TMC1).

Format of 8-Bit Timer Output Control Register

Symbol	<7>	<6>	5	<4>	<3>	<2>	1	<0>	Address	After Reset	R/W
TOC1	LVS2	LVR2	TOC15	TOE2	LVS1	LVR1	TOC11	TOE1	FF4FH	00H	R/W

TOE1	Controls output of 8-bit timer/event counter 1
0	Disables output (Port mode)
1	Enables output

TOC11	Controls timer output F/F of 8-bit timer/event counter 1
0	Disables inversion
1	Enables inversion

LVS1	LVR1	Sets status of timer output F/F of 8-bit timer/event counter 1
0	0	Not affected
0	1	Resets timer output F/F to 0
1	0	Sets timer output F/F to 1
1	1	Setting prohibited

TOE2	Controls output of 8-bit timer/event counter 2
0	Disables output (Port mode)
1	Enables output

TOC15	Controls timer output F/F of 8-bit timer/event counter 2
0	Disables inversion
1	Enables inversion

LVS2	LVR2	Sets status of timer output F/F of 8-bit timer/event counter 2
0	0	Not affected
0	1	Resets timer output F/F to 0
1	0	Sets timer output F/F to 1
1	1	Setting prohibited

Cautions: 1. Be sure to stop the timer operation before setting TOC1.

2. 0 is read from LVS1, LVS2, LVR1, and LVR2 after data has been set to these bits.

(5) Registers controlling watch timer

The following two registers control the watch timer:

- Timer clock select register 2 (TCL2)
- Watch timer mode control register (TMC2)

Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL2	TCL27	TCL26	TCL25	TCL24	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

This section controls the watchdog timer.
Refer to **(6) Registers controlling watchdog timer** or **Chapter 11** of *μPD78014, 78014Y Subseries User's Manual*, **Chapter 9** of *μPD78014H Subseries User's Manual*, or **Chapter 11** of *μPD78018F, 78018FY Subseries User's Manual* for detailed information.

TCL24	Selects count clock of watch timer
0	$f_X/2^8$ (39.1 kHz)
1	f_{XT} (32.768 kHz)

This section controls the buzzer output function.
Refer to **(8) Registers controlling buzzer output function** or **Chapter 13** of *μPD78014, 78014Y Subseries User's Manual*, **Chapter 11** of *μPD78014H Subseries User's Manual*, or **Chapter 13** of *μPD78018F, 78018FY Subseries User's Manual* for detailed information.

Caution: To write new data to TCL2, stop the timer operation once.

Remarks: f_X: Main system clock oscillation frequency
f_{XT}: Subsystem clock oscillation frequency
( ): At f_X = 10.0 MHz or f_{XT} = 32.768 kHz operation
This register is also used to control the watchdog timer and the buzzer.

Format of Watch Timer Mode Control Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TMC2	0	TMC26	TMC25	TMC24	TMC23	TMC22	TMC21	TMC20	FF4AH	00H	R/W

TMC23	TMC20	Selects set time of watch flag
0	0	$2^{14}/f_W$ (0.5 s)
1	0	$2^{13}/f_W$ (0.25 s)
0	1	$2^5/f_W$ (977 μs)
1	1	$2^4/f_W$ (488 μs)

TMC21	Controls prescaler operation Note
0	Clears after operation stopped
1	Enables operation

TMC22	Controls 5-bit counter operation
0	Clears after operation stopped
1	Enables operation

TMC26	TMC25	TMC24	Selects interval time of prescaler
0	0	0	$2^4/f_W$ (488 μs)
0	0	1	$2^5/f_W$ (977 μs)
0	1	0	$2^6/f_W$ (1.95 ms)
0	1	1	$2^7/f_W$ (3.91 ms)
1	0	0	$2^8/f_W$ (7.81 ms)
1	0	1	$2^9/f_W$ (15.6 ms)
Settings other than above are prohibited			

Note: Do not clear the prescaler frequently when using the watch timer.

Remarks: f_W: Watch timer clock frequency ($f_X/2^8$ or f_{XT})
( ): At f_W = 32.768 kHz operation

A 0.5 or 0.25 second interval can be generated either with an 8.38 MHz main system clock or a 32.768 KHz subsystem clock.

(6) Registers controlling watchdog timer

The following two registers control the watchdog timer:

- Timer clock select register 2 (TCL2)
- Watchdog timer mode register (WDTM)

Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL2	TCL27	TCL26	TCL25	TCL24	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

TCL22	TCL21	TCL20	Selects count clock of watchdog timer
0	0	0	$f_X/2^4$ (625 kHz)
0	0	1	$f_X/2^5$ (313 kHz)
0	1	0	$f_X/2^6$ (156 kHz)
0	1	1	$f_X/2^7$ (78.1 kHz)
1	0	0	$f_X/2^8$ (39.1 kHz)
1	0	1	$f_X/2^9$ (19.5 kHz)
1	1	0	$f_X/2^{10}$ (9.8 kHz)
1	1	1	$f_X/2^{12}$ (2.4 kHz)

This section controls the watch timer.
Refer to **(5) Registers controlling watch timer** or **Chapter 10** of *μPD78014, 78014Y Subseries User's Manual*, **Chapter 8** of *μPD78014H Subseries User's Manual*, or **Chapter 10** of *μPD78018F, 78018FY Subseries User's Manual* for detailed information.

This section controls the buzzer output function.
Refer to **(8) Registers controlling buzzer output function** or **Chapter 13** of *μPD78014, 78014Y Subseries User's Manual*, **Chapter 11** of *μPD78014H Subseries User's Manual*, or **Chapter 13** of *μPD78018F, 78018FY Subseries User's Manual* for detailed information.

Caution: To write new data to TCL2, stop the timer operation once.

Remarks: f_X: Main system clock oscillation frequency
( ): At f_X = 10.0 MHz operation

Format of Watchdog Timer Mode Register

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
WDTM	RUN	0	0	WDTM4	WDTM3	0	0	0	FFF9H	00H	R/W

WDTM4	WDTM3	Selects operation mode of watchdog timer Note 1
0	×	Interval timer mode Note 2 (overflow and maskable interrupt occur)
1	0	Watchdog timer mode 1 (overflow and non-maskable interrupt occur)
1	1	Watchdog timer mode 2 (overflow occurs and reset operation started)

RUN	Selects operation of watchdog timer Note 3
0	Stops counting
1	Clears counter and starts counting

Notes: 1. Once WDTM3 and WDTM4 have been set to 1, they cannot be cleared to 0 by software.

2. The watchdog timer starts operating as an interval timer as soon as the RUN bit has been set to 1.

3. Once RUN has been set to 1, it cannot be cleared to 0 by software. Therefore, when counting is started, it cannot be stopped by any means other than $\overline{\text{RESET}}$ input.

Cautions: 1. When the watchdog timer is cleared by setting 1 to RUN, the actual overflow time is up to 0.5% shorter than the time set by the timer clock select register 2.

2. To use watchdog timer modes 1 and 2, set the WDTM4 bit to 1 after confirming that the interrupt request flag (TMIF4) is 0.

If WDTM4 is set when TMIF4 is 1, a Non-Maskable Interrupt request is generated regardless of the contents of WDTM3.

Remark: ×: Don't care

(7) Registers controlling clock output function

The following two registers control the clock output function:

- Timer clock select register 0 (TCL0)
- Port mode register 3 (PM3)
  - Refer to section (1) for register format.

Format of Timer Clock Select Register 0

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL0	CLOE	TCL06	TCL05	TCL04	TCL03	TCL02	TCL01	TCL00	FF40H	00H	R/W

TCL03	TCL02	TCL01	TCL00	Selects clock of PCL output
0	0	0	0	f_{XT} (32.768 kHz)
0	1	1	1	$f_X/2^3$ (1.25 MHz)
1	0	0	0	$f_X/2^4$ (625 kHz)
1	0	0	1	$f_X/2^5$ (313 kHz)
1	0	1	0	$f_X/2^6$ (156 kHz)
1	0	1	1	$f_X/2^7$ (78.1 kHz)
1	1	0	0	$f_X/2^8$ (39.1 kHz)
Settings other than above are prohibited				

This section controls the 16-bit timer.
Refer to **(3) Registers controlling 16-bit timer/event counter** or **Chapter 8** of *μPD78014, 78014Y Subseries User's Manual*, **Chapter 6** of *μPD78014H Subseries User's Manual*, or **Chapter 8** of *μPD78018F, 78018FY Subseries User's Manual* for detailed information.

CLOE	PCL output clock
0	Output disable
1	Output enable

Cautions: 1. To enable PCL output, set TCL00 through TCL03, and then set CLOE to 1 by using a 1-bit memory manipulation instruction.

2. To write data other than that already written to TCL0, stop the timer operation once.

Remarks: f_X: Main system clock oscillation frequency

f_{XT}: Subsystem clock oscillation frequency

( ): At f_X = 10.0 MHz or f_{XT} = 32.768 kHz operation

(8) Registers controlling buzzer output function

The following two registers control the buzzer output function:

- Timer clock select register 2 (TCL2)
- Port mode register 3 (PM3)
  - Refer to section (1) for register format.

Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL2	TCL27	TCL26	TCL25	TCL24	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

This section controls the watchdog timer.
Refer to **(6) Registers controlling watchdog timer** or **Chapter 11** of *μPD78014, 78014Y Subseries User's Manual*, **Chapter 9** of *μPD78014H Subseries User's Manual*, or **Chapter 11** of *μPD78018F, 78018FY Subseries User's Manual* for detailed information.

This section controls the watch timer.
Refer to **(5) Registers controlling watch timer** or **Chapter 10** of *μPD78014, 78014Y Subseries User's Manual*, **Chapter 8** of *μPD78014H Subseries User's Manual*, or **Chapter 10** of *μPD78018F, 78018FY Subseries User's Manual* for detailed information.

TCL27	TCL26	TCL25	Selects frequency of buzzer output
0	×	×	Buzzer output disabled
1	0	0	$f_X/2^{10}$ (9.8 kHz)
1	0	1	$f_X/2^{11}$ (4.9 kHz)
1	1	0	$f_X/2^{12}$ (2.4 kHz)
1	1	1	Setting prohibited

Caution: To write data other than that already written to TCL2, stop the timer operation once.

Remarks: f_X: Main system clock oscillation frequency
×: Don't care
( ): At f_X = 10.0 MHz operation

(9) Registers controlling A/D converter

The following two registers control the A/D converter:

- A/D converter mode register (ADM)
- A/D converter input select register (ADIS)

Format of A/D Converter Mode Register

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After Reset	R/W
ADM	CS	TRG	FR1	FR0	ADM3	ADM2	ADM1	HSC	FF80H	01H	R/W

ADM3	ADM2	ADM1	Selects analog input channel
0	0	0	ANI0
0	0	1	ANI1
0	1	0	ANI2
0	1	1	ANI3
1	0	0	ANI4
1	0	1	ANI5
1	1	0	ANI6
1	1	1	ANI7

FR1	FR0	HSC	Selects A/D conversion time Note1				
				At f_X = 10.0 MHz	At f_X = 8.38 MHz	At f_X = 5.0 MHz	At f_X = 4.19 MHz
0	0	1	160/f_X	Setting prohibited Note2	19.1 μs	32.0 μs	38.1 μs
0	1	1	80/f_X	Setting prohibited Note2	Setting prohibited Note2	Setting prohibited Note2	19.1 μs
1	0	0	100/f_X	Setting prohibited Note2	Setting prohibited Note2	20.0 μs	23.9 μs
1	0	1	200/f_X	20.0 μs	23.9 μs	40.0 μs	47.7 μs
Settings other than above are prohibited							

TRG	Selects external trigger
0	No external trigger (software start mode)
1	Conversion started by external trigger (hardware start mode)

CS	Controls A/D conversion operation
0	Stops operation
1	Starts operation

Notes: 1. Set these bits so that the A/D conversion time is 19.1 μs or more.
2. This setting is prohibited because the A/D conversion time is less than 19.1 μs.

Cautions: 1. To reduce the power consumption of the A/D converter in the Standby mode, clear bit 7 (CS) to 0 to stop A/D conversion, and then execute the HALT or STOP instruction.
2. To resume A/D conversion that has been stopped, clear the interrupt request flag (ADIF) to 0 and then start the A/D conversion.

Remark: f_X: Main system clock oscillation frequency

Format of A/D Converter Input Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADIS	0	0	0	0	ADIS3	ADIS2	ADIS1	ADIS0	FF84H	00H	R/W

ADIS3	ADIS2	ADIS1	ADIS0	Selects number of analog input channels
0	0	0	0	None (P10 to P17)
0	0	0	1	1 channel (ANI0, P11 to P17)
0	0	1	0	2 channels (ANI0, ANI1, P12 to P17)
0	0	1	1	3 channels (ANI0 to ANI2, P13 to P17)
0	1	0	0	4 channels (ANI0 to ANI3, P14 to P17)
0	1	0	1	5 channels (ANI0 to ANI4, P15 to P17)
0	1	1	0	6 channels (ANI0 to ANI5, P16 to P17)
0	1	1	1	7 channels (ANI0 to ANI6, P17)
1	0	0	0	8 channels (ANI0 to ANI7)
Settings other than above are prohibited				

(10) Registers controlling serial interface channel 0 (Non-Y subseries)

The μPD78014, 78014H, and 78018F Subseries are provided with two channels of clocked serial interfaces. The differences between channels 0 and 1 are as indicated in the table below.

Differences Between Channels 0 and 1

Serial Transfer Mode		Channel 0	Channel 1
3-wire serial I/O	Clock selection	$f_X/2^2$ Note, $f_X/2^3$, $f_X/2^4$, $f_X/2^5$, $f_X/2^6$, $f_X/2^7$, $f_X/2^8$, $f_X/2^9$, external clock, TO2 output	
	Transfer method	MSB first/LSB first switchable	MSB/LSB first switchable Automatic transmission/reception function
	Transfer end flag	Serial interface channel 0 transfer end interrupt request flag (CSIIF0)	Serial interface channel 1 transfer end interrupt request flag (CSIIF1 and TRF)
SBI (serial bus interface)		Available	Not available
2-wire serial I/O			

Note: Can be set only when the main system clock oscillates at 4.19 MHz or less.

The following four registers control serial interface channel 0:

- Timer clock select register 3 (TCL3)
- Serial operation mode register 0 (CSIM0)
- Serial bus interface control register (SBIC)
- Interrupt timing specification register (SINT)

Format of Timer Clock Select Register 3

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL3	TCL37	TCL36	TCL35	TCL34	TCL33	TCL32	TCL31	TCL30	FF43H	88H	R/W

This section controls the serial interface channel 1.
Refer to **(12) Registers controlling serial interface channel 1** or **Chapter 17** of *μPD78014, 78014Y Subseries User's Manual*, **Chapter 14** of *μPD78014H Subseries User's Manual*, or **Chapter 17** of *μPD78018F, 78018FY Subseries User's Manual* for detailed information.

TCL33	TCL32	TCL31	TCL30	Selects serial clock of serial interface channel 0
0	1	1	0	$f_X/2^2$ **Note**
0	1	1	1	$f_X/2^3$ (1.25 MHz)
1	0	0	0	$f_X/2^4$ (625 kHz)
1	0	0	1	$f_X/2^5$ (313 kHz)
1	0	1	0	$f_X/2^6$ (156 kHz)
1	0	1	1	$f_X/2^7$ (78.1 kHz)
1	1	0	0	$f_X/2^8$ (39.1 kHz)
1	1	0	1	$f_X/2^9$ (19.5 kHz)
Settings other than above are prohibited				

Note: Can be set only when the main system clock oscillates at 4.19 MHz or less.

Caution: To write data other than that already written to TCL3, stop the serial transfer once.

Remarks: f_X : Main system clock oscillation frequency
( ): At f_X = 10.0 MHz operation

Format of Serial Operation Mode Register 0

Symbol	<7>	<6>	<5>	4	3	2	1	0	Address	After Reset	R/W
CSIM0	CSIE0	COI	WUP	CSIM04	CSIM03	CSIM02	CSIM01	CSIM00	FF60H	00H	R/W Note 1

R/W

CSIM01	CSIM00	Selects clock of serial interface channel 0
0	×	Clock externally input to $\overline{\text{SCK0}}$ pin
1	0	Output of 8-bit timer register 2 (TM2)
1	1	Clock specified by bits 0—3 of timer clock select register 3 (TCL3)

R/W

CSIM 04	CSIM 03	CSIM 02	PM25	P25	PM26	P26	PM27	P27	Operation mode	First bit	SI0/SB0/P25 pin function	SO0/SB1/P26 pin function	$\overline{\text{SCK0}}$/P27 pin function
0	×	0	1	×	0	0	0	1	3-wire serial I/O mode	MSB	SI0 Note 2 (input)	SO0 (CMOS output)	$\overline{\text{SCK0}}$ (CMOS I/O)
		1								LSB			
1	0	0	Note 3 ×	Note 3 ×	0	0	0	1	SBI mode	MSB	P25 (CMOS I/O)	SB1 (N-ch open drain I/O)	$\overline{\text{SCK0}}$ (CMOS I/O)
		1	0	0	Note 3 ×	Note 3 ×	0	1			SB0 (N-ch open drain I/O)	P26 (CMOS I/O)	
1	1	0	Note 3 ×	Note 3 ×	0	0	0	1	2-wire serial I/O mode	MSB	P25 (CMOS I/O)	SB1 (N-ch open drain I/O)	$\overline{\text{SCK0}}$ (N-ch open drain I/O)
		1	0	0	Note 3 ×	Note 3 ×	0	1			SB0 (N-ch open drain I/O)	P26 (CMOS I/O)	

R/W

WUP	Controls wake-up function Note 4
0	Generates interrupt request signal in all modes each time serial transfer is executed
1	Generates interrupt request signal when address received after bus has been released in SBI mode (when CMDD = RELD = 1) coincides with data of slave address register

R

COI	Slave address comparison result flag Note 5
0	Data of slave address register does not coincide with data of serial I/O shift register 0
1	Data of slave address register coincides with data of serial I/O shift register 0

R/W

CSIE0	Controls operation of serial interface channel 0
0	Stops operation
1	Enables operation

Notes: 1. Bit 6 (COI) is a read-only bit.
2. This pin can be used as P25 (CMOS input) when serial channel used only for transmission.
3. This pin can be freely used for port function if input or output function is not used by serial channel.
4. Clear bit 5 (SIC) of the interrupt timing specification register (SINT) to 0 when using the wake-up function (WUP = 1).
5. COI is 0 when CSIE0 = 0.

Caution: Do not change the operation mode (3-wire serial I/O, 2-wire serial I/O, or SBI) while the operation of serial interface channel 0 is enabled. Stop the serial operation before changing the operation mode.

Remark: ×: Don't care
PM××: Port mode register
P××: Output latch of port

Format of Serial Bus Interface Control Register (1/2)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
SBIC	BSYE	ACKD	ACKE	ACKT	CMDD	RELD	CMDT	RELT	FF61H	00H	R/W Note

R/W

RELT	Used to output bus release signal. SO0 latch is set to 1 when RELT = 1 . After setting SO0 latch, RELT is automatically cleared to 0. This bit is also cleared to 0 when CSIE0 = 0.

R/W

CMDT	Used to output command signal. SO0 latch is cleared to 0 when CMDT = 1. After clearing SO0 latch, CMDT is automatically cleared to 0. This bit is also cleared to 0 when CSIE0 = 0.

R

RELD	Bus release detection	
Clear conditions (RELD = 0)		Set condition (RELD = 1)
• When transfer start instruction is executed • When values of SIO0 and SVA do not coincide when address is received • When $\overline{\text{CSIE0}}$ = 0 • When $\overline{\text{RESET}}$ is input		• When bus release signal (REL) is detected

R

CMDD	Command detection	
Clearing conditions (CMDD = 0)		Setting condition (CMDD = 1)
• When transfer start instruction is executed • When bus release signal (REL) is detected • When $\overline{\text{CSIE0}}$ = 0 • When $\overline{\text{RESET}}$ is input		• When command signal (CMD) is detected

Note: Bits 2, 3, and 6 (RELD, CMDD, and ACKD) are read-only bits.

Remark: CSIE0: Bit 7 of the serial operation mode register 0

Format of Serial Bus Interface Control Register (2/2)

R/W

ACKT	Outputs acknowledge signal in synchronization with falling edge of clock of $\overline{SCK0}$ immediately after instruction that sets this bit to 1 has been executed. After acknowledge signal has been output, this bit is automatically cleared to 0. This bit is also cleared to 0 when transfer of serial interface is started or when CSIE0 = 0.

R/W

ACKE	Acknowledge signal output control	
0	Disables automatic output of acknowledge signal (output by ACKT is enabled)	
1	Before completion of transfer	Outputs acknowledge signal in synchronization with falling edge of 9th clock of $\overline{SCK0}$ (automatically outputs when ACKE = 1)
	After completion of transfer	Outputs acknowledge signal in synchronization with falling edge of clock of $\overline{SCK0}$ immediately after instruction that sets this bit to 1 has been executed (automatically output when ACKE = 1). However, this bit is not automatically cleared to 0 after acknowledge signal has been output.

R

ACKD	Acknowledge detection	
Clearing conditions (ACKD = 0)		Setting condition (ACKD = 1)
• At falling edge of clock of $\overline{SCK0}$ immediately after busy mode is released after transfer start instruction has been executed • When CSIE0 = 0 • When $\overline{RESET}$ is input		• When acknowledge signal ($\overline{ACK}$) is detected at rising edge of clock of $\overline{SCK0}$ after completion of transfer

R/W

BSYE Note	Synchronous busy signal output control
0	Disables output of busy signal in synchronization with falling edge of clock of $\overline{SCK0}$ immediately after instruction that clears this bit to 0 has been executed
1	Outputs busy signal from falling edge of clock of $\overline{SCK0}$ following acknowledge signal

Note: The Busy mode can be released when transfer by the serial interface has been started. However, the BSYE flag is not cleared to 0.

Remarks: Bits 0, 1, and 4 (RELT, CMDT, and ACKT) are 0 when they are read after data has been set.
CSIE0: Bit 7 of the serial operation mode register 0 (CSIM0)

Format of Interrupt Timing Specification Register

Symbol	7	<6>	<5>	<4>	3	2	1	0	Address	After Reset	R/W
SINT	0	CLD	SIC	SVAM	0	0	0	0	FF63H	00H	R/W Note 1

R/W

SVAM	Bits of SVA used as slave address
0	Bits 0 to 7
1	Bits 1 to 7

R/W

SIC	Selects interrupt source of INTCSI0 Note 2
0	Sets CSIIF0 at end of transfer by serial interface channel 0
1	Sets CSIIF0 at end of transfer by serial interface channel 0 or on detection of bus release signal

R

CLD	Level of $\overline{SCK0}$/P27 pin Note 3
0	Low level
1	High level

Notes: 1. Bit 6 (CLD) is a read-only bit.
2. Set SIC to 0 when using the wake-up function in SBI mode.
3. CLD is 0 when CSIE0 = 0.

Caution: Be sure to set bits 0 through 3 to 0.

Remarks: SVA: Slave address register
CSIIF0: Interrupt request flag corresponding to INTCSI0
CSIE0: Bit 7 of the serial operation mode register 0 (CSIM0)

(11) Registers controlling serial interface channel 0 (Y subseries)

The μPD78014Y and 78018FY Subseries are provided with two channels of clocked serial interfaces. The differences between channels 0 and 1 are as indicated in the table below.

Differences Between Channels 0 and 1

Serial Transfer Mode		Channel 0	Channel 1
3-wire serial I/O	Clock selection	$f_X/2^2$ Note 1, $f_X/2^3$, $f_X/2^4$, $f_X/2^5$, $f_X/2^6$, $f_X/2^7$, $f_X/2^8$, $f_X/2^9$, external clock, TO2 output	
	Transfer method	MSB first/LSB first switchable	MSB/LSB first switchable Automatic transmission/reception function
	Transfer end flag	Serial interface channel 0 transfer end interrupt request flag (CSIIF0)	Serial interface channel 1 transfer end interrupt request flag (CSIIF1 and TRF)
SBI (serial bus interface) Note 2		Available	Not available
2-wire serial I/O			
I^2C bus (inter-IC bus)			

Notes: 1. Can be set only when the main system clock oscillates at 4.19 MHz or less.
2. Provided to μPD78014Y Subseries only.

The following four registers control serial interface channel 0:

- Timer clock select register 3 (TCL3)
- Serial operation mode register 0 (CSIM0)
- Serial bus interface control register (SBIC)
- Interrupt timing specification register (SINT)

Format of Timer Clock Select Register 3

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL3	TCL37	TCL36	TCL35	TCL34	TCL33	TCL32	TCL31	TCL30	FF43H	88H	R/W

This section controls the serial interface channel 1.
Refer to **(12) Registers controlling serial interface channel 1** or **Chapter 17** of *μPD78014, 78014Y Subseries User's Manual*, **Chapter 14** of *μPD78014H Subseries User's Manual*, or **Chapter 17** of *μPD78018F, 78018FY Subseries User's Manual* for detailed information.

TCL33	TCL32	TCL31	TCL30	Selects serial clock of serial interface channel 0	
				Serial clock in I^2C bus mode	Serial clock in 3-wire serial I/O mode or 2-wire serial I/O mode
0	1	1	0	$f_X/2^6$ (156 kHz)	$f_X/2^2$ **Note**
0	1	1	1	$f_X/2^7$ (78.1 kHz)	$f_X/2^3$ (1.25 MHz)
1	0	0	0	$f_X/2^8$ (39.1 kHz)	$f_X/2^4$ (625 kHz)
1	0	0	1	$f_X/2^9$ (19.5 kHz)	$f_X/2^5$ (313 kHz)
1	0	1	0	$f_X/2^{10}$ (9.8 kHz)	$f_X/2^6$ (156 kHz)
1	0	1	1	$f_X/2^{11}$ (4.9 kHz)	$f_X/2^7$ (78.1 kHz)
1	1	0	0	$f_X/2^{12}$ (2.4 kHz)	$f_X/2^8$ (39.1 kHz)
1	1	0	1	$f_X/2^{13}$ (1.2 kHz)	$f_X/2^9$ (19.5 kHz)
Settings other than above are prohibited					

Note: Can be set only when the main system clock oscillates at 4.19 MHz or less.

Caution: To write data other than that already written to TCL3, stop the serial transfer once.

Remarks: f_X : Main system clock oscillation frequency
( ): At f_X = 10.0 MHz operation

Format of Serial Operation Mode Register 0

Symbol	<7>	<6>	<5>	4	3	2	1	0	Address	After Reset	R/W
CSIM0	CSIE0	COI	WUP	CSIM04	CSIM03	CSIM02	CSIM01	CSIM00	FF60H	00H	R/W Note 1

R/W

CSIM01	CSIM00	Selects clock of serial interface channel 0
0	×	Clock externally input to $\overline{\text{SCK0}}$/SCL pin
1	0	Output of 8-bit timer register 2 (TM2) Note 2
1	1	Clock specified by bits 0 to 3 of timer clock select register 3 (TCL3)

R/W

CSIM 04	CSIM 03	CSIM 02	PM25	P25	PM26	P26	PM27	P27	Operating mode	Start bit	SI0/SB0/SDA0/ P25 pin function	SO0/SB1/SDA1/ P26 pin function	$\overline{\text{SCK0}}$/SCL/P27 pin function
0	×	0	1	×	0	0	0	1	3-wire serial I/O mode	MSB	SI0 Note 3 (input)	SO0 (CMOS output)	$\overline{\text{SCK0}}$ (CMOS I/O)
		1								LSB			
1 Note 7	0	0	Note 4 ×	Note 4 ×	0	0	0	1	SBI mode	MSB	P25 (CMOS I/O)	SB1/SDA1 (N-ch open drain I/O)	$\overline{\text{SCK0}}$ (CMOS I/O)
		1	0	0	Note 4 ×	Note 4 ×	0	1			SB0/SDA0 (N-ch open-drain I/O)	P26 (CMOS I/O)	
1	1	0	Note 4 ×	Note 4 ×	0	0	0	1	2-wire serial I/O mode or I^2C bus mode	MSB	P25 (CMOS I/O)	SB1/SDA1 (N-ch open-drain I/O)	$\overline{\text{SCK0}}$/SCL (N-ch open-drain I/O)
		1	0	0	Note 4 ×	Note 4 ×	0	1			SB0/SDA0 (N-ch open-drain I/O)	P26 (CMOS I/O)	

R/W

WUP	Controls wake-up function Note 5
0	Generates interrupt request signal in all modes each time serial transfer is executed
1	Generates interrupt request signal when address received after start condition is detected in I^2C bus mode (when CMDD = 1) coincides with data of slave address register

R

COI	Slave address comparison result flag Note 6
0	Data of slave address register does not coincide with data of serial I/O shift register 0
1	Data of slave address register coincides with data of serial I/O shift register 0

R/W

CSIE0	Controls operation of serial interface channel 0
0	Stops operation
1	Enables operation

Notes: 1. Bit 6 (COI) is a read-only bit.
2. The clock frequency is 1/16 of the frequency output by TO2 in the I^2C bus mode.
3. This pin can be used as P25 (CMOS input) when used only for transmission.
4. This pin can be freely used for port function.
5. Clear bit 5 (SIC) of the interrupt timing specification register (SINT) to 1 when using the wake-up function. Do not execute an instruction that writes the serial I/O shift register 0 (SIO0) while WUP = 1.
6. COI is 0 when CSIE0 = 0.
7. SBI mode is only valid for μPD78014, μPD78014Y.

Caution: Do not change the operation mode (3-wire serial I/O, 2-wire serial I/O, or I^2C bus) while the operation of serial interface channel 0 is enabled. Stop the serial operation before changing the operation mode.

Remark: ×: Don't care
PM××: Port mode register
P××: Output latch of port

Format of Serial Bus Interface Control Register (1/2)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
SBIC	BSYE	ACKD	ACKE	ACKT	CMDD	RELD	CMDT	RELT	FF61H	00H	R/W Note

R/W

RELT	Used to output stop condition in I^2C bus mode. SO0 latch is set to 1 when RELT = 1 . After setting the SO0 latch, RELT is automatically cleared to 0. This bit is also cleared to 0 when CSIE0 = 0.

R/W

CMDT	Used to output start condition in I^2C bus mode. SO0 latch is cleared to 0 when CMDT = 1. After clearing the SO0 latch, CMDT is automatically cleared to 0. This bit is also cleared to 0 when CSIE0 = 0.

R

RELD	Stop condition detection	
	Clearing conditions (RELD = 0)	Setting condition (RELD = 1)
	• When transfer start instruction is executed • When values of SIO0 and SVA do not coincide when address is received • When $\overline{CSIE0}$ = 0 • When $\overline{RESET}$ is input	• When stop condition is detected in I^2C mode

R

CMDD	Start condition detection	
	Clearing conditions (CMDD = 0)	Setting condition (CMDD = 1)
	• When transfer start instruction is executed • When stop condition is detected in I^2C mode • When $\overline{CSIE0}$ = 0 • When $\overline{RESET}$ is input	• When start condition is detected in I^2C bus mode

Note: Bits 2, 3, and 6 (RELD, CMDD, and ACKD) are read-only bits.

Remark: CSIE0: Bit 7 of the serial operation mode register 0 (CSIM0)

Format of Serial Bus Interface Control Register (2/2)

R/W

ACKT	Makes SDA0 (SDA1) low immediately after execution of setting instruction (ACKT = 1) until falling edge of next SCL. Used to generate $\overline{ACK}$ signal by software when 8-clock wait is selected. This bit is cleared to 0 when transfer of serial interface is started or when CSIE0 = 0.

R/W

ACKE	Acknowledge signal automatic output control Note 1
0	Disables automatic output of acknowledge signal (output by ACKT is enabled). Used for transmission, or reception with 8-clock wait selected. Note 2
1	Enables automatic output of acknowledge signal. Outputs acknowledge signal in synchronization with falling edge of 9th clock of SCL (automatically outputs when $\overline{ACKE}$ = 1). This bit is not automatically cleared to 0 after acknowledge signal has been output. Used for reception with 9-clock wait selected.

R

ACKD	Acknowledge detection	
Clearing conditions (ACKD = 0)		Setting condition (ACKD = 1)
• When transfer start instruction is executed • When $\overline{CSIE0}$ = 0 • When $\overline{RESET}$ is input		• When acknowledge signal is detected at rising edge of clock of SCL after completion of transfer

R/W

BSYE Note 3	Controls N-ch open-drain output for transmission in I^2C bus mode Note 4
0	Enables output (transmission)
1	Disables output (reception)

Notes: 1. Set this bit before starting transfer.
2. Output the acknowledge signal during reception by using ACKT when an 8-clock wait is selected.
3. The wait mode can be released when transfer by the serial interface has been started when an address signal has been received. However, the BSYE flag is not cleared to 0.
4. Be sure to set BSYE to 1 when using the wake-up function.

Remark: CSIE0: Bit 7 of the serial operation mode register 0 (CSIM0)

Format of Interrupt Timing Specification Register (1/2)

Symbol	7	<6>	<5>	<4>	<3>	<2>	1	0	Address	After Reset	R/W
SINT	0	CLD	SIC	SVAM	CLC	WREL	WAT1	WAT0	FF63H	00H	R/W Note 1

R/W	WAT1	WAT0	Controls wait and interrupt
	0	0	Generates interrupt processing request at rising edge of 8th clock of $\overline{SCK0}$ (clock output goes to high-impedance state)
	0	1	Setting prohibited
	1	0	Used in I^2C bus mode (8-clock wait). Generates interrupt processing request at rising edge of 8th clock of SCL (master makes SCL output low and waits after outputting 8 clocks. Slave makes SCL pin low and requests for wait after inputting 8 clocks).
	1	1	Used in I^2C bus mode (9-clock wait). Generates interrupt processing request at rising edge of 9th clock of SCL (master makes SCL output low and waits after outputting 9 clocks. Slave makes SCL pin low land requests for wait after inputting 9 clocks).

R/W	WREL	Controls clearing wait
	0	Wait clear status
	1	Clears wait status. This bit is automatically cleared to 0 after wait status has been cleared (used to clear wait status set by WAT0, WAT1)

R/W	CLC	Controls clock level Note 2
	0	Used in I^2C bus mode. Makes output level of SCL pin low when serial transfer is not executed.
	1	Used in I^2C bus mode. Puts output level of SCL pin in high-impedance state when serial transfer is not executed (the clock line is high). Master uses this setting to make SCL high to generate start/stop condition.

Notes: 1. Bit 6 (CLD) is a read-only bit.

2. Set CLC to 0 when the I^2C bus mode is not used.

Format of Interrupt Timing Specification Register (2/2)

R/W	SVAM	Bits of SVA used as slave address
	0	Bits 0 to 7
	1	Bits 1 to 7

R/W	SIC	Selects interrupt source of INTCSI0 Note 1
	0	Sets CSIIF0 to 1 at end of transfer by serial interface channel 0.
	1	Sets CSIIF0 to 1 at end of transfer by serial interface channel 0 or on detection of stop condition in I^2C bus mode.

R	CLD	Level of $\overline{SCK0}$/SCL pin Note 2
	0	Low level
	1	High level

Notes: 1. Set SIC to 1 when using wake-up function in the I^2C bus mode.
2. CLD is 0 when CSIE = 0.

Remarks: SVA: Slave address register
CSIIF0: Interrupt request flag corresponding to INTCSI0
CSIE0: Bit 7 of the serial operation mode register 0 (CSIM0)

(12) Registers controlling serial interface channel 1

The following four registers control serial interface channel 1:

- Timer clock select register 3 (TCL3)
- Serial operation mode register 1 (CSIM1)
- Automatic data transmit/receive control register (ADTC)
- Automatic data transmit/receive time interval specification register (ADTI)
  - This register is not present in μPD78014, μPD78014Y subseries devices.

Format of Timer Clock Select Register 3

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL3	TCL37	TCL36	TCL35	TCL34	TCL33	TCL32	TCL31	TCL30	FF43H	88H	R/W

This section controls the serial interface channel 0.
Refer to **(10) Registers controlling serial interface channel 0 (Non-Y subseries)**, **(11) Registers controlling serial interface channel 0 (Y subseries),** or
Chapters 15 and 16 of *μPD78014, 78014Y Subseries User's Manual*,
Chapter 13 of *μPD78014H Subseries User's Manual*, or
Chapters 15 and 16 of *μPD78018F, 78018FY Subseries User's Manual*
for detailed information.

TCL37	TCL36	TCL35	TCL34	Selects serial clock of serial interface channel 1
0	1	1	0	$f_X/2^2$ **Note**
0	1	1	1	$f_X/2^3$ (1.25 MHz)
1	0	0	0	$f_X/2^4$ (625 kHz)
1	0	0	1	$f_X/2^5$ (313 kHz)
1	0	1	0	$f_X/2^6$ (156 kHz)
1	0	1	1	$f_X/2^7$ (78.1 kHz)
1	1	0	0	$f_X/2^8$ (39.1 kHz)
1	1	0	1	$f_X/2^9$ (19.5 kHz)
Settings other than above are prohibited				

Note: Can be set only when the main system clock oscillates at 4.19 MHz or less.

Caution: To write data other than that already written to TCL3, stop the serial transfer once.

Remarks: f_X : Main system clock oscillation frequency
( ): At f_X = 10.0 MHz operation

Format of Serial Operation Mode Register 1

Symbol	<7>	6	<5>	4	3	2	1	0	Address	After Reset	R/W
CSIM1	CSIE1	DIR	ATE	0	0	0	CSIM11	CSIM10	FF68H	00H	R/W

CSIM11	CSIM10	Selects clock of serial interface channel 1
0	×	Clock externally input to $\overline{\text{SCK1}}$ pin Note 1
1	0	Output of 8-bit timer register 2 (TM2)
1	1	Clock specified by bits 4 to 7 of timer clock select register 3 (TCL3)

ATE	Selects operation mode of serial interface channel 1
0	3-wire serial I/O mode
1	3-wire serial I/O mode with automatic transmission/reception function

DIR	First bit	SI1 pin function	SO1 pin function
0	MSB	SI1/P20 (input)	SO1 (CMOS output)
1	LSB		

CSIE1	CSIM 11	PM20	P20	PM21	P21	PM22	P22	Shift register 1 operation	Serial clock count operation control	SI1/P20 pin function	SO1/P21 pin function	$\overline{\text{SCK1}}$/P22 pin function
0	×	Note 2 ×	Note 2 ×	Note 2 ×	Note 2 ×	Note 2 ×	Note 2 ×	Operation disabled	Clear	P20 (CMOS I/O)	P21 (CMOS I/O)	P22 (CMOS I/O)
1	0	Note 3 1	Note 3 ×	0	0	1	×	Operation enabled	Count operation	SI1 Note 3 (input)	SO1 (CMOS output)	$\overline{\text{SCK1}}$ (input)
	1					0	1					$\overline{\text{SCK1}}$ (CMOS output)

Notes: 1. When external clock input is selected by setting CSIM11 to 0, set bit 1 (BUSY1) and bit 2 (STRB) of the automatic data transmission/reception control register (ADTC) to 0, 0.

2. These pins can be used freely as port pins if not used as IN/OUT pins for serial channel.

3. When data is only transmitted, this pin can be used as P20 (CMOS I/O) (set bit 7 (RE) of ADTC to 0).

Remarks: ×: Don't care

PM××: Port mode register

P××: Output latch of port

Format of Automatic Data Transmit/Receive Control Register

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
ADTC	RE	ARLD	ERCE	ERR	TRF	STRB	BUSY1	BUSY0	FF69H	00H	R/W Note 1

R/W

BUSY1	BUSY0	Controls busy input
0	×	Does not use busy input
1	0	Enables busy input (high active)
1	1	Enables busy input (low active)

R/W

STRB	Controls strobe output
0	Disables strobe output
1	Enables strobe output

R

TRF	Status of automatic transmission/reception function Note 2
0	Detects end of automatic transmission/reception (set to 0 when automatic transmission/reception is aborted, or when ARLD = 0)
1	Automatic transmission/reception is in progress (set to 1 when this bit is written to SIO1)

R

ERR	Error detection of automatic transmission/reception function
0	No error during automatic transmission/reception (set to 0 when this bit is written to SIO1)
1	Error during automatic transmission/reception

R/W

ERCE	Controls error check of automatic transmission/ reception function
0	Disables error check during automatic transmission/ reception
1	Enables error check during automatic transmission/ reception (only when BUSY1 = 1)

R/W

ARLD	Selects operation mode of automatic transmission/ reception function
0	Single mode
1	Repeated mode

R/W

RE	Controls reception of automatic transmission/ reception function
0	Disables reception
1	Enables reception

Notes: 1. Bits 3 and 4 (TRF and ERR) are read-only bits.

2. The completion of automatic transmission/reception should be determined with TRF instead of CSIIF1 (interrupt request flag).

Caution: Set STRB and BUSY1 of ADTC to 0, 0 when external clock input is selected by setting bit 1 (CSIM11) of the serial operation mode register 1 (CSIM1) to 0.

Remark: ×: Don't care

Format of Automatic Data Transmit/Receive Interval Time Specification Register (1/2)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADTI	ADTI7	0	0	ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	FF6BH	00H	R/W

ADTI7	Controls interval time of data transfer
0	Interval time not controlled by ADTI[Note 1]
1	Interval time controlled by ADTI (ADTI0 to ADTI4)

ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	Specifies interval time of data transfer (f_X = 10.0 MHz operation)	
					Minimum value[Note 2]	Maximum value[Note 2]
0	0	0	0	0	18.4 μs + 0.5/f_{SCK}	20.0 μs + 1.5/f_{SCK}
0	0	0	0	1	31.2 μs + 0.5/f_{SCK}	32.8 μs + 1.5/f_{SCK}
0	0	0	1	0	44.0 μs + 0.5/f_{SCK}	45.6 μs + 1.5/f_{SCK}
0	0	0	1	1	56.8 μs + 0.5/f_{SCK}	58.4 μs + 1.5/f_{SCK}
0	0	1	0	0	69.6 μs + 0.5/f_{SCK}	71.2 μs + 1.5/f_{SCK}
0	0	1	0	1	82.4 μs + 0.5/f_{SCK}	84.0 μs + 1.5/f_{SCK}
0	0	1	1	0	95.2 μs + 0.5/f_{SCK}	96.8 μs + 1.5/f_{SCK}
0	0	1	1	1	108.0 μs + 0.5/f_{SCK}	109.6 μs + 1.5/f_{SCK}
0	1	0	0	0	120.8 μs + 0.5/f_{SCK}	122.4 μs + 1.5/f_{SCK}
0	1	0	0	1	133.6 μs + 0.5/f_{SCK}	135.2 μs + 1.5/f_{SCK}
0	1	0	1	0	146.4 μs + 0.5/f_{SCK}	148.0 μs + 1.5/f_{SCK}
0	1	0	1	1	159.2 μs + 0.5/f_{SCK}	160.8 μs + 1.5/f_{SCK}
0	1	1	0	0	172.0 μs + 0.5/f_{SCK}	173.6 μs + 1.5/f_{SCK}
0	1	1	0	1	184.8 μs + 0.5/f_{SCK}	186.4 μs + 1.5/f_{SCK}
0	1	1	1	0	197.6 μs + 0.5/f_{SCK}	199.2 μs + 1.5/f_{SCK}
0	1	1	1	1	210.4 μs + 0.5/f_{SCK}	212.0 μs + 1.5/f_{SCK}

Notes: 1. The interval time is dependent on the CPU processing only.

2. The interval time for data transfer is variable. The minimum and maximum values of the interval time for transferring each data can be calculated by the following expressions (n: value placed in ADTI0 through ADTI4). If the minimum value calculated by the following expression is less than 2/f_{SCK}, however, the minimum interval time is assumed to be 2/f_{SCK}.

$$\text{Minimum value} = (n + 1) \times \frac{2^7}{f_X} + \frac{56}{f_X} + \frac{0.5}{f_{SCK}}$$

$$\text{Maximum value} = (n + 1) \times \frac{2^7}{f_X} + \frac{72}{f_X} + \frac{1.5}{f_{SCK}}$$

Cautions: 1. Do not write data to ADTI during operation of the automatic data transmit/receive function.

2. Be sure to set bits 5 and 6 to 0.

3. While ADTI is used to control the interval time for data transfer by the automatic data transmit/receive function, busy control is invalid.

Remarks: f_X: Main system clock oscillation frequency

f_{SCK}: Serial clock frequency

Format of Automatic Data Transmit/Receive Interval Time Specification Register (2/2)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADTI	ADTI7	0	0	ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	FF6BH	00H	R/W

ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	Specifies interval time for data transfer (f_X = 10.0 MHz operation)	
					Minimum value[Note]	Maximum value[Note]
1	0	0	0	0	223.2 μs + 0.5/f_{SCK}	224.8 μs + 1.5/f_{SCK}
1	0	0	0	1	236.0 μs + 0.5/f_{SCK}	237.6 μs + 1.5/f_{SCK}
1	0	0	1	0	248.8 μs + 0.5/f_{SCK}	250.4 μs + 1.5/f_{SCK}
1	0	0	1	1	261.6 μs + 0.5/f_{SCK}	263.2 μs + 1.5/f_{SCK}
1	0	1	0	0	274.4 μs + 0.5/f_{SCK}	276.0 μs + 1.5/f_{SCK}
1	0	1	0	1	287.2 μs + 0.5/f_{SCK}	288.8 μs + 1.5/f_{SCK}
1	0	1	1	0	300.0 μs + 0.5/f_{SCK}	301.6 μs + 1.5/f_{SCK}
1	0	1	1	1	312.8 μs + 0.5/f_{SCK}	314.4 μs + 1.5/f_{SCK}
1	1	0	0	0	325.6 μs + 0.5/f_{SCK}	327.2 μs + 1.5/f_{SCK}
1	1	0	0	1	338.4 μs + 0.5/f_{SCK}	340.0 μs + 1.5/f_{SCK}
1	1	0	1	0	351.2 μs + 0.5/f_{SCK}	352.8 μs + 1.5/f_{SCK}
1	1	0	1	1	364.0 μs + 0.5/f_{SCK}	365.6 μs + 1.5/f_{SCK}
1	1	1	0	0	376.8 μs + 0.5/f_{SCK}	378.4 μs + 1.5/f_{SCK}
1	1	1	0	1	389.6 μs + 0.5/f_{SCK}	391.2 μs + 1.5/f_{SCK}
1	1	1	1	0	402.4 μs + 0.5/f_{SCK}	404.0 μs + 1.5/f_{SCK}
1	1	1	1	1	415.2 μs + 0.5/f_{SCK}	416.8 μs + 1.5/f_{SCK}

Note: The interval time for data transfer is variable. The minimum and maximum values of the interval time for transferring each data can be calculated by the following expressions (n: value placed in ADTI0 through ADTI4). If the minimum value calculated by the following expression is less than 2/f_{SCK}, however, the minimum interval time is assumed to be 2/f_{SCK}.

$$\text{Minimum value} = (n + 1) \times \frac{2^7}{f_X} + \frac{56}{f_X} + \frac{0.5}{f_{SCK}}$$

$$\text{Maximum value} = (n + 1) \times \frac{2^7}{f_X} + \frac{72}{f_X} + \frac{1.5}{f_{SCK}}$$

Cautions: 1. Do not write data to ADTI during operation of the automatic data transmit/receive function.

2. Be sure to set bits 5 and 6 to 0.

3. While ADTI is used to control the interval time for data transfer by the automatic data transmit/receive function, busy control is invalid.

Remarks: f_X: Main system clock oscillation frequency

f_{SCK}: Serial clock frequency

(13) Registers controlling interrupt function

A total of 14 interrupt sources are provided for the μPD78014/14Y, 78014H, and 78018F/18FY Subseries, including reset, non-maskable, maskable, and software interrupts.

Table 6-2. Interrupt Source List

Interrupt Type	Default Priority Note	Interrupt Source		Internal/ External	Vector Table Address
		Name	Trigger		
Reset	—	RESET	RESET pin input	External	0000H
Non-maskable	—	INTWDT	Overflow of watchdog timer (when watchdog timer mode 1 is selected)	Internal	0004H
Maskable	0	INTWDT	Overflow of watchdog timer (when interval timer mode is selected)		
	1	INTP0	Pin input edge detection	External	0006H
	2	INTP1			0008H
	3	INTP2			000AH
	4	INTP3			000CH
	5	INTCSI0	End of transfer of serial interface channel 0	Internal	000EH
	6	INTCSI1	End of transfer of serial interface channel 1		0010H
	7	INTTM3	Reference time interval signal from watch timer		0012H
	8	INTTM0	Generation of coincidence signal from16-bit timer/ event counter		0014H
	9	INTTM1	Generation of coincidence signal from 8-bit timer/ event counter 1		0016H
	10	INTTM2	Generation of coincidence signal from 8-bit timer/ event counter 2		0018H
	11	INTAD	End of conversion of A/D converter		001AH
Software	—	BRK	Execution of BRK instruction	—	003EH

Note: The default priority is used when two or more Maskable Interrupt requests occur at the same time. 0 is the highest and 11 is the lowest priority.

The following table gives a listing of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 6-3. Interrupt Sources and Flags

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
		Register		Register		Register
INTWDT	TMIF4	IF0L	TMMK4	MK0L	TMPR4	PR0L
INTP0	PIF0		PMK0		PPR0	
INTP1	PIF1		PMK1		PPR1	
INTP2	PIF2		PMK2		PPR2	
INTP3	PIF3		PMK3		PPR3	
INTCSI0	CSIIF0		CSIMK0		CSIPR0	
INTCSI1	CSIIF1		CSIMK1		CSIPR1	
INTTM3	TMIF3		TMMK3		TMPR3	
INTTM0	TMIF0	IF0H	TMMK0	MK0H	TMPR0	PR0H
INTTM1	TMIF1		TMMK1		TMPR1	
INTTM2	TMIF2		TMMK2		TMPR2	
INTAD	ADIF		ADMK		ADPR	

The following six types of registers control the interrupt function:

- Interrupt request flag registers (IF0L, IF0H)
- Interrupt mask flag registers (MK0L, MK0H)
- Priority specification flag registers (PR0L, PR0H)
- External interrupt mode register (INTM0)
- Sampling clock select register (SCS)
- Program status word (PSW)

Format of Interrupt Request Flag Registers

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
IF0L	TMIF3	CSIIF1	CSIIF0	PIF3	PIF2	PIF1	PIF0	TMIF4	FFE0H	00H	R/W

	7	6	<5>	4	<3>	<2>	<1>	<0>			
IF0H	0	0	Note WTIF	0	ADIF	TMIF2	TMIF1	TMIF0	FFE1H	00H	R/W

××IF	Interrupt request flag
0	Interrupt request signal is not generated
1	Interrupt request signal is generated and interrupt is requested

Note: The WTIF is a test input flag and does not generate a vectored Interrupt request.

Cautions: 1. The TMIF4 flag can be read/written only when the watchdog timer is used as an interval timer. Clear the TMIF4 flag to 0 when the watchdog timer mode 1 is used.

2. Be sure to set bits 4, 6, and 7 of IF0H to 0.

Format of Interrupt Mask Flag Registers

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
MK0L	TMMK 3	CSIMK 1	CSIMK 0	PMK3	PMK2	PMK1	PMK0	TMMK 4	FFE4H	FFH	R/W

	7	6	<5>	4	<3>	<2>	<1>	<0>			
MK0H	1	1	Note WTMK	1	ADMK	TMMK 2	TMMK 1	TMMK 0	FFE5H	FFH	R/W

××MK	Controls interrupt servicing
0	Enables interrupt servicing
1	Disables interrupt servicing

Note: The WTMK controls enabling/disabling the release of the Standby mode. It does not control the interrupt function.

Cautions: 1. The TMMK4 flag is undefined when it is read while the watchdog timer is used in the watchdog timer mode 1.

2. Because port 0 is shared with external Interrupt request inputs, the corresponding Interrupt request flag is set when the output mode is specified and the output level of a port pin is changed. To use the port in the output mode, therefore, set the corresponding interrupt mask flag to 1 in advance.

3. Be sure to set bits 4, 6, and 7 of MK0H to 1.

Format of Priority Specification Flag Registers

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
PR0L	TMPR3	CSIPR1	CSIPR0	PPR3	PPR2	PPR1	PPR0	TMPR4	FFE8H	FFH	R/W

	7	6	5	4	<3>	<2>	<1>	<0>			
PR0H	1	1	1	1	ADPR	TMPR2	TMPR1	TMPR0	FFE9H	FFH	R/W

××PR	Selects priority level
0	High priority level
1	Low priority level

Cautions: 1. Set the TMPR4 flag to 1 when using the watchdog timer in the watchdog timer mode 1.

2. Be sure to set bits 4 through 7 of PR0H to 1.

Format of External Interrupt Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
INTM0	ES31	ES30	ES21	ES20	ES11	ES10	0	0	FFECH	00H	R/W

ES11	ES10	Selects valid edge of INTP0
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

ES21	ES20	Selects valid edge of INTP1
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

ES31	ES30	Selects valid edge of INTP2
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

Caution: Before setting the valid edges of the INTP0/TI0/P00 pins, stop the timer operation by clearing bits 1 to 3 (TMC01 to TMC03) of the 16-bit timer mode control register (TMC0) to 0, 0, 0.

Remark: INTP0 pin also functions as TI0/P00.

Format of Sampling Clock Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
SCS	0	0	0	0	0	0	SCS1	SCS0	FF47H	00H	R/W

SCS1	SCS0	Selects sampling clock of INTP0
0	0	$f_X/2^{N+1}$
0	1	Setting prohibited
1	0	$f_X/2^6$ (156 kHz)
1	1	$f_X/2^7$ (78.1 kHz)

Caution: $f_X/2^{N+1}$ is the clock supplied to the CPU; $f_X/2^6$ and $f_X/2^7$ are the clocks supplied to the peripheral hardware. $f_X/2^{N+1}$ is stopped in the HALT mode.

Remarks: N: Value (N = 0 to 4) set to bits 0 to 2 (PCC0 to PCC2) of processor clock control register
f_X: Main system clock oscillation frequency
( ): At f_X = 10.0 MHz operation

Format of Program Status Word

Symbol	7	6	5	4	3	2	1	0	After Reset
PSW	IE	Z	RBS1	AC	RBS0	0	ISP	CY	02H

→ Used when normal instruction is executed

ISP	Priority of interrupt currently serviced
0	Interrupt with higher priority is serviced (interrupt with lower priority is disabled)
1	Interrupt is not accepted, or interrupt with lower priority is serviced (all maskable interrupts are enabled)

IE	Enables/disables accepting Interrupt request
0	Disables
1	Enables

(14) Registers controlling test function

The names of the test input flag and test mask flag corresponding to the test input signal name are as follows.

Test Input Sources

Test Input		Test Input Flag	Test Mask Flag	Internal/
Name	Trigger			External
INTWT	Watch timer overflow	WTIF	WTMK	Internal
INTPT4	Falling edge detection at port 4	KRIF	KRMK	External

The following three types of registers control the test function:

- Interrupt request flag register 0H (IF0H)
- Interrupt mask flag register 0H (MK0H)
- Key return mode register (KRM)

Format of Interrupt Request Flag Register 0H

Symbol	7	6	<5>	4	<3>	<2>	<1>	<0>	Address	After Reset	R/W
IF0H	0	0	WTIF	0	ADIF	TMIF2	TMIF1	TMIF0	FFE1H	00H	R/W

WTIF	Watch timer overflow detection flag
0	Not detected
1	Detected

Caution: Be sure to clear bits 4, 6, and 7 to 0.

Format of Interrupt Mask Flag Register 0H

Symbol	7	6	<5>	4	<3>	<2>	<1>	<0>	Address	After Reset	R/W
MK0H	1	1	WTMK	1	ADMK	TMMK2	TMMK1	TMMK0	FFE5H	FFH	R/W

WTMK	Standby mode control by watch timer
0	Enables releasing Standby mode.
1	Disables releasing Standby mode.

Caution: Be sure to set bits 4, 6, and 7 to 1.

Format of Key Return Mode Register

Symbol	7	6	5	4	3	2	<1>	<0>	Address	After Reset	R/W
KRM	0	0	0	0	0	0	KRMK	KRIF	FFF6H	02H	R/W

KRIF	Key return signal detection flag
0	Not detected
1	Detected (port 4 falling edge detection)

KRMK	Standby mode control by key return signal
0	Enables releasing Standby mode
1	Disables releasing Standby mode

Caution: When port 4 falling edge detection is used, be sure to clear KRIF to 0 (it is not cleared automatically).

(15) Registers controlling external device expansion function

The following two registers control the external device expansion function:

- Memory expansion mode register (MM)
- Internal memory size switching register (IMS)

Format of Memory Expansion Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
MM	0	0	PW1	PW0	0	MM2	MM1	MM0	FFF8H	10H	R/W

MM2	MM1	MM0	Selects single-chip/ memory expansion mode		Status of P40 to P47, P50 to P57, P64 to P67 pins				
					P40 to P47		P50 to P53	P54, P55	P56, P57	P64 to P67
0	0	0	Single-chip mode		Port mode	Input	Port mode			
0	0	1				Output				
0	1	1	Memory expansion mode	256-byte mode	AD0 to AD7		Port mode			P64 = $\overline{RD}$ P65 = $\overline{WR}$ P66 = $\overline{WAIT}$ P67 = ASTB
1	0	0		4K mode			A8 to A11	Port mode		
1	0	1		16K mode				A12, A13	Port mode	
1	1	1		Full[Note] address mode					A14, A15	
Other than above			Setting prohibited							

PW1	PW0	Controls wait state
0	0	No wait
0	1	Wait (1 wait state is inserted)
1	0	Setting prohibited
1	1	Wait control by external wait pin

Note: The Full Address mode is a mode in which the entire area of the 64K address space, except the internal ROM, RAM, SFR, and unused areas, can be externally expanded.

Remark: The P60 to P63 pins can be used in the Port mode, regardless of the single-chip mode and memory expansion mode.

Format of Internal Memory Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	**Note 1**	W

ROM3	ROM2	ROM1	ROM0	Selects internal ROM capacity
0	0	1	0	8K
0	1	0	0	16K
0	1	1	0	24K
1	0	0	0	32K
1	0	1	0	40K **Note 2**
1	1	0	0	48K **Note 2**
1	1	1	0	56K **Notes 2, 3**
1	1	1	1	60K **Note 2**
Settings other than above are prohibited				

RAM2	RAM1	RAM0	Selects internal high-speed RAM capacity
0	1	0	512 bytes
1	1	0	1024 bytes
Settings other than above are prohibited			

Notes: 1. The value of this register after reset differs depending on the product (refer to the table below).
2. Setting prohibited for the μPD78014/14Y and 78014H Subseries.
3. When the external device expansion function of the μPD78018F/18FY is used, set the internal ROM capacity to 56K or less.

Value of Internal Memory Size Switching Register After Reset

Part Number	Value After Reset
μPD78011B/11BY/11F/11FY/11H	42H
μPD78012B/12BY/12F/12FY/12H	44H
μPD78013/13Y/13F/13FY/13H	C6H
μPD78014/14Y/P014/P014Y/14F/14FY/14H	C8H
μPD78015F/15FY	CAH
μPD78016F/16FY	CCH
μPD78018F/18FY/P018F/P018FY	CFH

(16) Register controlling standby function

The standby function is intended to decrease the power consumption of the system. The following two modes are available: HALT and STOP.

When MCU is released from the STOP mode, a wait time is required for the crystal to resume oscillations. The wait time is controlled by the following register:

- Oscillation stabilization time select register (OSTS)

Format of Oscillation Stabilization Time Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0	FFFAH	04H	R/W

OSTS2	OSTS1	OSTS0	Selects oscillation stabilization time when releasing STOP mode
0	0	0	$2^{13}/f_X$ (819 μs)
0	0	1	$2^{15}/f_X$ (3.28 ms)
0	1	0	$2^{16}/f_X$ (6.55 ms)
0	1	1	$2^{17}/f_X$ (13.1 ms)
1	0	0	$2^{18}/f_X$ (26.2 ms)
Settings other than above are prohibited			

Remarks f_X: Main system clock oscillation frequency

Values in parentheses apply to operation with f_X = 10.0 MHz.

The operation status in the HALT mode is described below.

HALT Mode Operating Status

(a) When HALT instruction is executed while system operates on main system clock

Setting of HALT Mode / Item		Without Subsystem Clock Note 1	With Subsystem Clock Note 2
Clock generator		Both main system clock and subsystem clock can oscillate. Supply of clock to CPU is stopped.	
CPU		Stops operation	
Port (output latch)		Retains previous status before setting HALT mode	
16-bit timer/event counter		Operable	
8-bit timer/event counter			
Watchdog timer			
A/D converter			
Watch timer		Operable when $fx/2^8$ is selected as count clock	Operable
Serial interface	Other than automatic transmission/reception function	Operable	
	Automatic transmission/reception function	Stops operation	
External interrupt	INTP0	Operable when clock to peripheral hardware ($fx/2^6$, $fx/2^7$) is selected as sampling clock	
	INTP1 to INTP3	Operable	
Externally extended bus line	AD0 to AD7	High impedance	
	A8 to A15	Retains previous status before setting HALT mode	
	ASTB	Low level	
	$\overline{WR}$, $\overline{RD}$	High level	
	$\overline{WAIT}$	High impedance	

Notes: 1. Includes the case in which an external clock is not supplied as the subsystem clock.
2. Includes the case in which an external clock is supplied as the subsystem clock.

(b) When HALT instruction is executed while system operates on subsystem clock

Item \ Setting of HALT Mode		When Main System Clock Oscillation Continues	When Main System Clock Oscillation Stops
Clock generator		Both main system clock and subsystem clock can oscillate. Supply of clock to CPU is stopped.	
CPU		Stops operation	
Port (output latch)		Retains previous status before setting HALT mode	
16-bit timer/event counter		Operable	Stops operation
8-bit timer/event counter			Operable when TI1 or TI2 is selected as count clock
Watchdog timer		Stops operation	
A/D converter		Operable	Stops operation
Watch timer			Operable when f_{XT} is selected as count clock
Serial interface	Other than automatic transmission/reception function	Operable	Operable when external clock is selected
	Automatic transmission/ reception function	Stops operation	
External interrupt	INTP0	Operable when clock to peripheral hardware ($f_X/2^6$, $f_X/2^7$) is selected as sampling clock	Stops operation
	INTP1 to INTP3	Operable	
Externally extended bus line	AD0 to AD7	High impedance	
	A8 to A15	Retains previous status before setting HALT mode	
	ASTB	Low level	
	$\overline{WR}$, $\overline{RD}$	High level	
	$\overline{WAIT}$	High impedance	

The operation status in the STOP mode is described below.

STOP Mode Operating Status

Item \ Setting of STOP Mode		When Subsystem Clock Is Used	When Subsystem Clock Is Not Used
Clock generator		Only main system clock stops oscillation	
CPU		Stops operation	
Output port (output latch)		Retains previous status immediately before STOP instruction execution	
16-bit timer/event counter		Stops operation	
8-bit timer/event counter		Operable only when TI1 or TI2 is selected as count clock	
Watchdog timer		Stops operation	
A/D converter			
Watch timer		Operable only when f_{XT} is selected as count clock	Stops operation as count clock
Serial interface	Other than automatic transmission/reception function	Operable only when external input clock is selected as serial clock	
	Automatic transmission/reception function	Stops operation	
External interrupt	INTP0	Cannot operate	
	INTP1 to INTP3	Operable	
Externally expanded bus line	AD0 to AD7	High impedance	
	A8 to A15	Retains previous status immediately before STOP instruction execution	
	ASTB	Low level	
	$\overline{WR}$, $\overline{RD}$	High level	
	$\overline{WAIT}$	High impedance	

Cautions: 1. When the STOP mode is set, the X2 pin is internally connected to V_{DD} via a pull-up resistor to minimize the leakage current at the crystal oscillator. Thus, do not use the STOP mode in a system in which an external clock is used for the main system clock.

2. Because the interrupt request signal is used to release the Standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the Standby mode is immediately released if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction. After the wait set using the oscillation stabilization time select register (OSTS), the operating mode is set.

(17) Reset function

The following two operations can be used to generate a reset signal:

- External reset input via the $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer in the Watchdog Timer mode

Table 6-4. Hardware Status After Reset (1/2)

Hardware		Status After Reset
Program counter (PC) Note 1		Contents of reset vector tables (0000H, 0001H) are set
Stack pointer (SP)		Undefined
Program status word (PSW)		02H
RAM	Data memory	Undefined Note 2
	General-purpose register	Undefined Note 2
Port (output latch)	Ports 0 to 3 (P0 to P3)	00H
	Ports 4 to 6 (P4 to P6)	Undefined
Port mode registers	(PM0)	1FH
	(PM1, PM2, PM3, PM5, PM6)	FFH
Pull-up resistor option register (PUO)		00H
Processor clock control register (PCC)		04H
Memory expansion mode register (MM)		10H
Internal memory size switching register (IMS)		**Note 3**
Internal expansion RAM size switching register (IXS)		**Note 4**
Oscillation stabilization time select register (OSTS)		04H
16-bit timer/event counter	Timer register (TM0)	0000H
	Compare register (CR00)	Undefined
	Capture register (CR01)	Undefined
	Clock select register (TCL0)	00H
	Mode control register (TMC0)	00H
	Output control register (TOC0)	00H
8-bit timer/event counter	Timer registers (TM1, TM2)	00H
	Compare registers (CR10, CR20)	Undefined
	Clock select register (TCL1)	00H
	Mode control register (TMC1)	00H
	Output control register (TOC1)	00H
Watch timer	Mode control register (TMC2)	00H
	Clock select register (TCL2)	
Watchdog timer	Mode register (WDTM)	00H
Serial interface	Clock select register (TCL3)	88H
	Shift registers (SIO0, SIO1)	Undefined
	Mode registers (CSIM0, CSIM1)	00H
	Serial bus interface control register (SBIC)	00H
	Slave address register (SVA)	Undefined
	Automatic data transmit/receive control register (ADTC)	00H
	Automatic data transmit/receive interval specification register (ADTI) Note 5	00H
	Automatic data transmit/receive address pointer (ADTP)	00H
	Interrupt timing specification register (SINT)	00H

Table 6-4. Hardware Status After Reset (2/2)

Hardware		Status After Reset
A/D converter	Mode register (ADM)	01H
	Conversion result register (ADCR)	Undefined
	Input select register (ADIS)	00H
ROM correction	Correction address registers (CORAD0, CORAD1)Note 6	0000H
	Correction control register (CORCN)Note 6	00H
Interrupt	Request flag registers (IF0L, IF0H)	00H
	Mask flag registers (MK0L, MK0H)	FFH
	Priority specification flag registers (PR0L, PR0H)	FFH
	External interrupt mode register (INTM0)	00H
	Key return mode register (KRM)	02H
	Sampling clock select register (SCS)	00H

Notes: 1. Only the contents of the PC among hardware become undefined during reset input and oscillation stabilization time wait. The other status is not different from that after reset as above.

2. The status before reset is retained in Standby mode.

3. The value after reset differs depending on the product, as follows:

	μPD78011B/BY μPD78011F/FY μPD78011H	μPD78012B/BY μPD78012F/FY μPD78012H	μPD78013/Y μPD78013F/FY μPD78013H	μPD78014/Y μPD78P014F/FY μPD78014F/FY μPD78014H	μPD78015F/FY	μPD78016F/FY	μPD78018F/FY μPD78P018F/FY
IMS	42H	44H	C6H	C8H	CAH	CCH	CFH

To use a mask ROM version, do not set IMS to a value other than that after reset, except, however, when the external device expansion function is used with the μPD78018F/FY.

4. Provided to the μPD78011F/FY, 78012F/FY, 78013F/FY, 78014F/FY, 78015F/FY, 78016F/FY, 78018F/FY, and 78P018F/FY (μPD78018F, 78018FY Subseries) only.
The value after reset differs depending on the product, as follows:

	μPD78011F/FY	μPD78012F/FY	μPD78013F/FY	μPD78014F/FY	μPD78015F/FY	μPD78016F/FY	μPD78018F/FY μPD78P018F/FY
IXS	0CH				0BH		0AH

To use a mask ROM version, do not set IXS to a value other than that after reset, except, however, when the external device expansion function is used with the μPD78018F/FY.

5. Provided to the μPD78014H and 78018F Subseries only.

6. Provided to some products of the μPD78018F Subseries only:
μPD78015F/FY, 78016F/FY, 78018F/FY, and 78P018F/FY.

(18) Registers controlling ROM correction (mask ROM versions of μPD78018F/18FY subseries only)

The following two types of registers control the ROM correction:

- Correction address registers 0 and 1 (CORAD0 and CORAD1)
- Correction control register (CORCN)

Format of Correction Address Registers 0 and 1

Symbol	15	0	Address	After Reset	R/W
CORAD0			FF38H/FF39H	0000H	R/W
CORAD1			FF3AH/FF3BH	0000H	R/W

Cautions: 1. Set CORAD0 and CORAD1 when bits 1 (COREN0) and 3 (COREN1) of the correction control register (CORCN; refer to the figure below) are 0.

2. Only addresses where operation codes are stored can be set in CORAD0 and CORAD1.

3. Do not set the following addresses to CORAD0 and CORAD1:

- **Address value in table area of table reference instruction (CALLT instruction): 0040H to 007FH**
- **Address value in vector table area: 0000H to 003FH**

Format of Correction Control Register

Symbol	7	6	5	4	<3>	<2>	<1>	<0>	Address	After Reset	R/W
CORCN	0	0	0	0	COREN1	CORST1	COREN0	CORST0	FF8AH	00H	R/W Note

CORST0	Flag detecting coincidence between correction address register 0 and fetch address
0	Coincidence not detected
1	Coincidence detected

COREN0	Controls detection of coincidence between correction address register 0 and fetch address
0	Detection disabled
1	Detection enabled

CORST1	Flag detecting coincidence between correction address register 1 and fetch address
0	Coincidence not detected
1	Coincidence detected

COREN1	Controls detection of coincidence between correction address register 1 and fetch address
0	Detection disabled
1	Detection enabled

Note: Bits 0 and 2 are read-only bits.

(19) Register controlling internal memory capacity

The μPD78P014/14Y and μPD78P018F/18FY (PROM versions) allow users to select the internal memory capacity. The following register is used to control the internal memory capacity:

- Internal memory size switching register (IMS)

(a) μPD78P014/14Y (for μPD78014/14Y subseries only)

To map the memory of the μPD78P014 or 78P014Y identically to that of a mask ROM version, the value at the time the mask ROM version is reset must be set.

For the mask ROM version, IMS does not need to be set.

Format of Internal Memory Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	C8H	W

ROM3	ROM2	ROM1	ROM0	Selects internal ROM capacity
0	0	0	1	4K
0	0	1	0	8K
0	1	0	0	16K
0	1	1	0	24K
1	0	0	0	32K
Settings other than above are prohibited				

RAM2	RAM1	RAM0	Selects internal high-speed RAM capacity
0	0	0	768 bytes
0	0	1	640 bytes
0	1	0	512 bytes
0	1	1	384 bytes
1	0	0	256 bytes
1	0	1	Setting prohibited
1	1	0	1024 bytes
1	1	1	896 bytes

The following table shows the set value of IMS to map the memory of the μPD78P014 or 78P014Y identically to that of a mask ROM version.

Set Value of Internal Memory Size Switching Register

Target Mask ROM Version	Set Value of IMS
μPD78001B/001BY	82H
μPD78002B/002BY	64H
μPD78011B/11BY	42H
μPD78012B/12BY	44H
μPD78013/13Y	C6H
μPD78014/14Y	C8H

Caution: When using a mask ROM version, do not set a value other than those shown in the above table to IMS.

(20) Register controlling internal expansion RAM capacity

The μPD78P018F/18FY (PROM versions) allow users to select the internal expansion RAM capacity. The following register is used to control the internal expansion RAM capacity:

- Internal expansion RAM size switching register (IXS)

Format of Internal Expansion RAM Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IXS	0	0	0	0	IX RAM3	IX RAM2	IX RAM1	IX RAM0	FFF4H	0AH	W

IX RAM3	IX RAM2	IX RAM1	IX RAM0	Selects internal expansion RAM capacity
1	0	1	0	1024 bytes (F400H to F7FFH)
1	0	1	1	512 bytes (F600H to F7FFH)
1	1	0	0	0 bytes
Settings other than above are prohibited				

The following table shows the set value of IXS at which to map the internal expansion RAM of the μPD78P018F or 78P018FY identically to that of a mask ROM version.

Set Value of Internal Expansion RAM Size Switching Register

Target Mask ROM Version	Set Value of IXS
μPD78011F/11FY	0CH
μPD78012F/12FY	
μPD78013F/13FY	
μPD78014F/14FY	
μPD78015F/15FY	0BH
μPD78016F/16FY	
μPD78018F/18FY	0AH

Cautions: 1. The μPD78014/14Y and μPD78014H Subseries do not provide IXS.

2. For the mask ROM version, IXS does not need to be set.

3. When using a mask ROM version, do not set a value other than those shown in the above table to IXS.

6.2 μPD780208 Subseries

6.2.1 Documentation Reference Information

Device Series Number	User's Manual Number	Date Published
μPD780208	U11302EJ3V0UM00	October 1997

Caution: The user should check the current User's Manual with the information in this section to be sure of having the most up-to-date information.

General Programmer's Note

The NEC C-compiler and the NEC Assembler are capable of recognizing certain symbolic SFR bit names. These special bit names are identified in the user manual in one of the four ways shown below:

1. <7>
2. (7)
3. ⑦
4. 7

Example:

	<7>	<6>	<5>	<4>	3	2	1	0
PCC	MCC	FRC	CLS	CSS	0	PCC2	PCC1	PCC0

If a bit number has one of the four symbols around it, the NEC software will recognize the associated symbolic bit name. For example to set bit 7, the user can write the code in two ways:

```
1.    SET1    MCC
2.    SET1    PCC.7
```

Alternatively since bit 2 does not have any of the four symbols around it, the user can only set this bit as follows:

```
1.    SET1    PCC.2
```

Note: The attempt to employ a symbolic name of bit-2 (PCC2) will return an error. Thus the use of instruction

```
SET1    PCC2
```

is improper since neither the NEC C-compiler nor the NEC Assembler recognizes this symbolic name and will generate an error.

6.2.2 Memory Address Space

Each model in the μPD780208 Subseries can access a memory space of 64K. Figures 6-8 through 6-11 show memory maps of the respective models.

Figure 6-8. Memory Map (μPD780204)

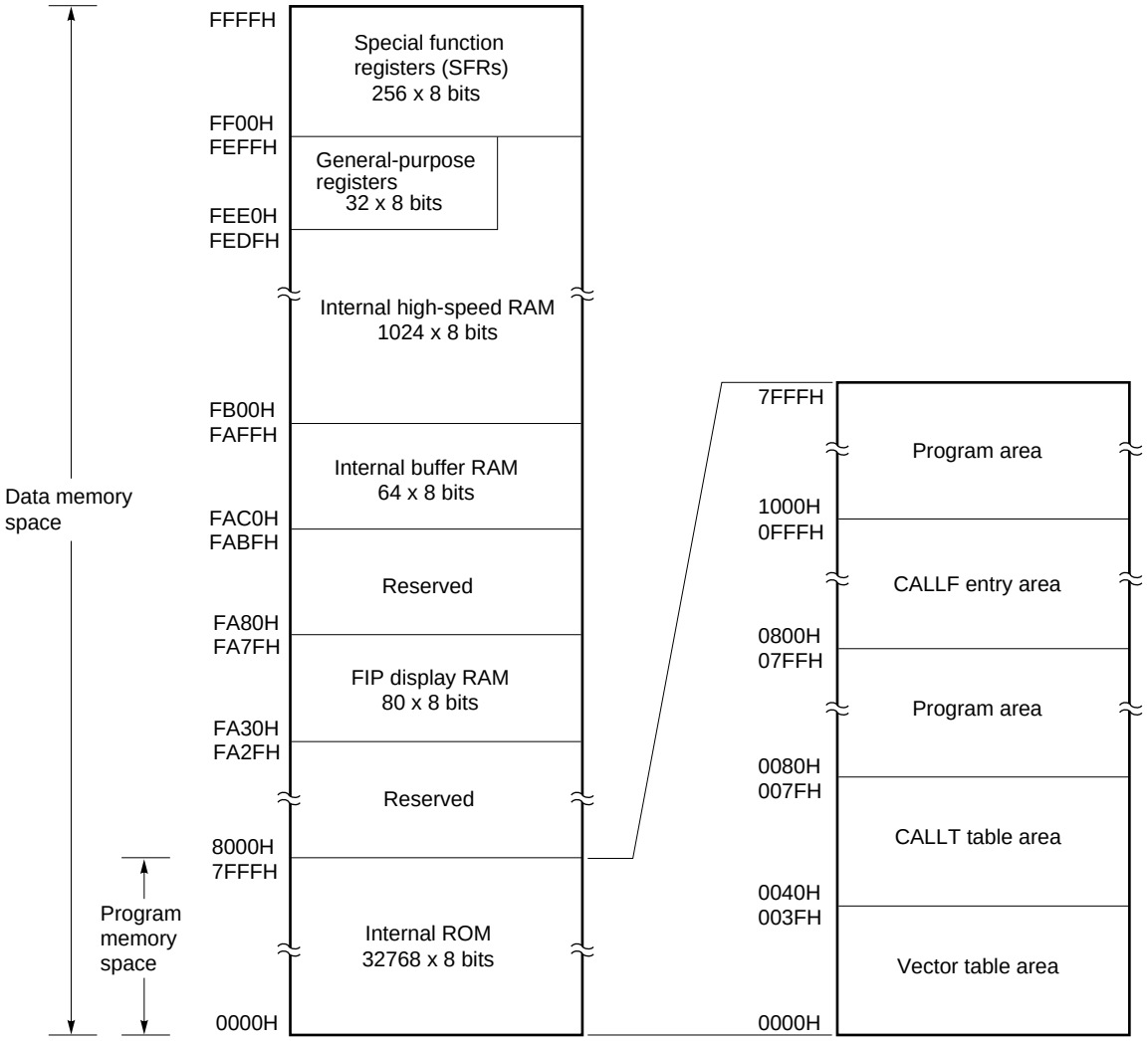


Figure 6-9. Memory Map (μPD780205)

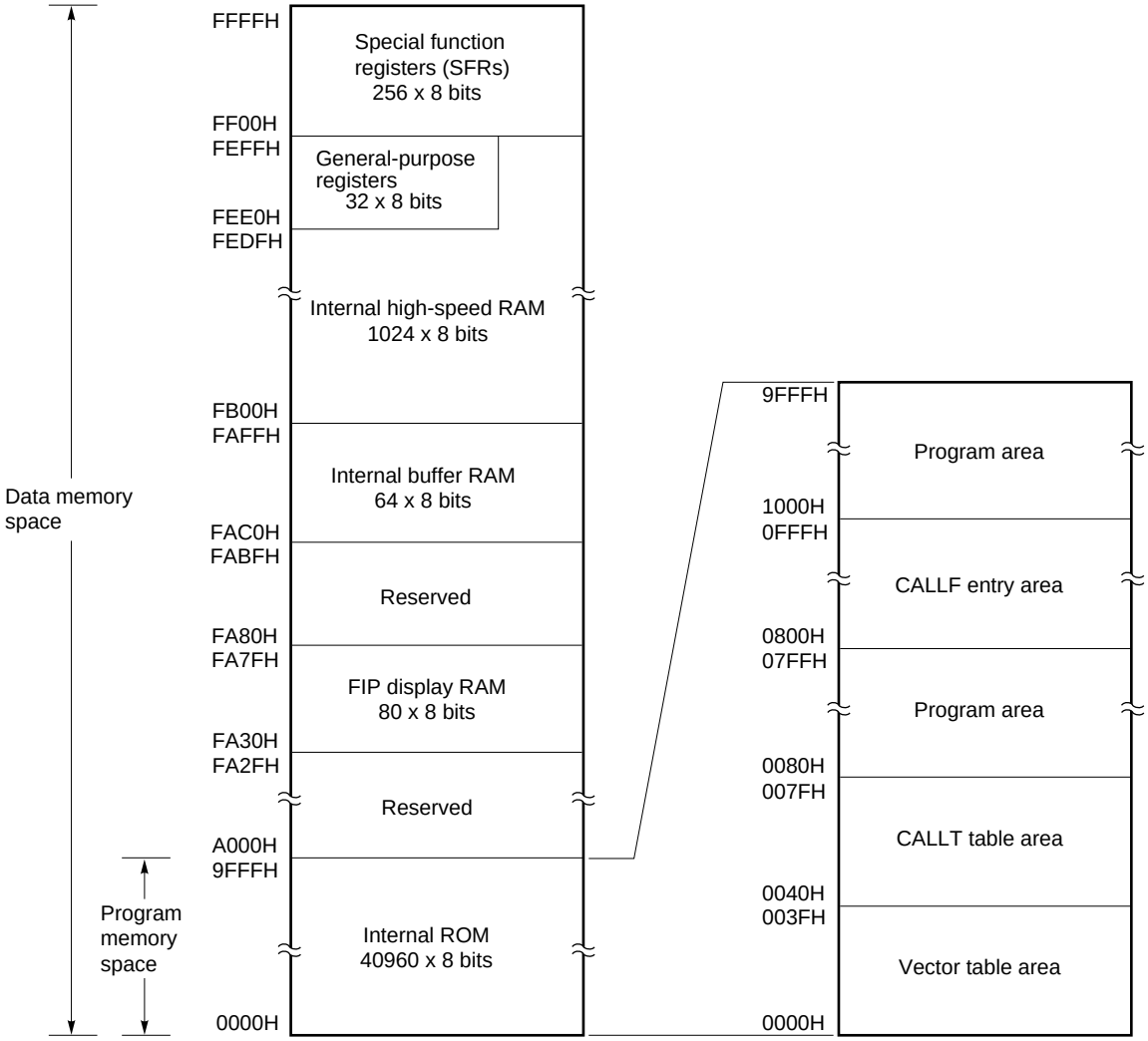


Figure 6-10. Memory Map (μPD780206)

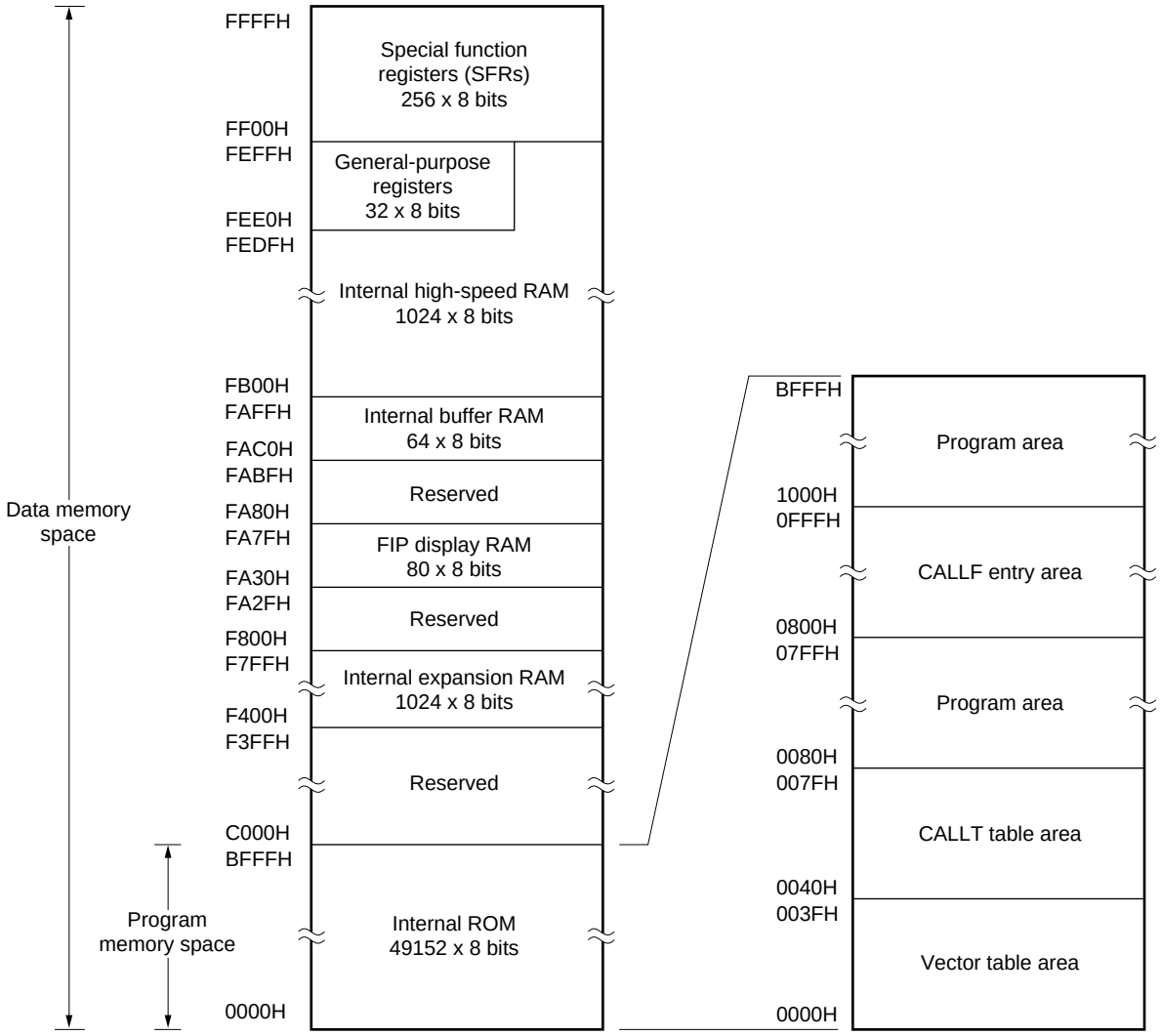
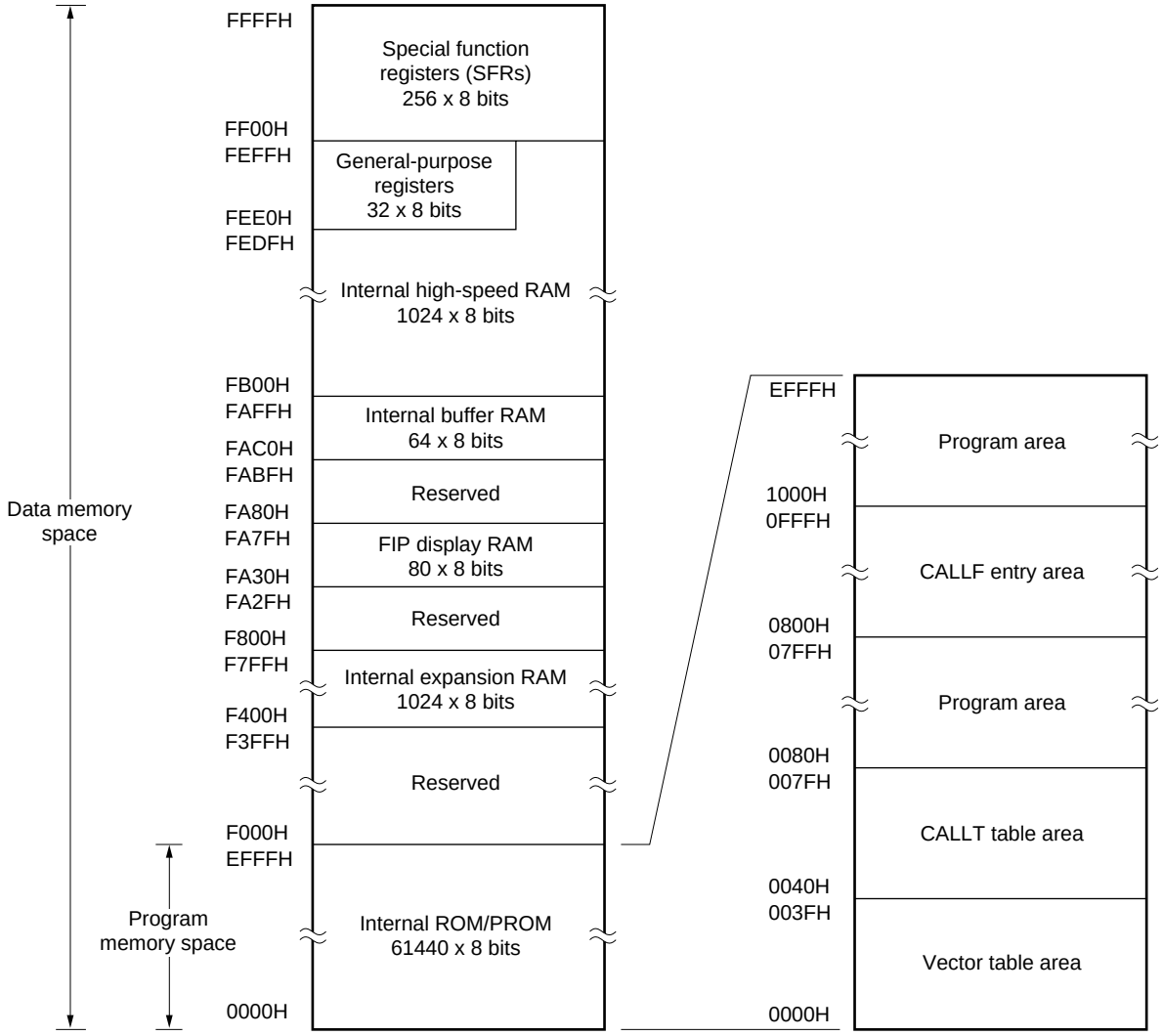


Figure 6-11. Memory Map (μPD780208, 78P0208)



6.2.3 Special Function Registers (SFRs)

Table 6-5. Special Function Register List (μPD780208 Subseries) (1/2)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulatable Bit Unit			After Reset
				1 Bit	8 Bits	16 Bits	
FF00H	Port 0	P0	R/W	√	√	–	00H
FF01H	Port 1	P1		√	√	–	
FF02H	Port 2	P2		√	√	–	
FF03H	Port 3	P3		√	√	–	
FF07H	Port 7	P7	W	√	√	–	
FF08H	Port 8	P8		√	√	–	
FF09H	Port 9	P9		√	√	–	
FF0AH	Port 10	P10	R/W	√	√	–	
FF0BH	Port 11	P11		√	√	–	
FF0CH	Port 12	P12		√	√	–	
FF10H FF11H	16-bit compare register	CR00		–	–	√	Undefined
FF12H FF13H	16-bit capture register	CR01	R	–	–	√	
FF14H FF15H	16-bit timer register	TM0		–	–	√	0000H
FF16H	8-bit compare register 10	CR10	R/W	–	√	–	Undefined
FF17H	8-bit compare register 20	CR20		–	√	–	
FF18H	8-bit timer register 1	TMS TM1	R	–	√	√	00H
FF19H	8-bit timer register 2	TM2		–	√		
FF1AH	Serial I/O shift register 0	SIO0	R/W	–	√	–	Undefined
FF1BH	Serial I/O shift register 1	SIO1		–	√	–	
FF1FH	A/D conversion result register	ADCR	R	–	√	–	
FF20H	Port mode register 0	PM0	R/W	√	√	–	1FH
FF21H	Port mode register 1	PM1		√	√	–	FFH
FF22H	Port mode register 2	PM2		√	√	–	
FF23H	Port mode register 3	PM3		√	√	–	
FF27H	Port mode register 7	PM7		√	√	–	1FH
FF2AH	Port mode register 10	PM10		√	√	–	FFH
FF2BH	Port mode register 11	PM11		√	√	–	
FF2CH	Port mode register 12	PM12		√	√	–	
FF40H	Timer clock select register 0	TCL0		√	√	–	00H
FF41H	Timer clock select register 1	TCL1		–	√	–	
FF42H	Timer clock select register 2	TCL2		–	√	–	
FF43H	Timer clock select register 3	TCL3		–	√	–	88H
FF47H	Sampling clock select register	SCS		–	√	–	00H
FF48H	16-bit timer mode control register	TMC0		√	√	–	
FF49H	8-bit timer mode control register	TMC1		√	√	–	
FF4AH	Watch timer mode control register	TMC2		√	√	–	

Table 6-5. Special Function Register List (μPD780208 Subseries) (2/2)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulatable Bit Unit			After Reset
					1 Bit	8 Bits	16 Bits	
FF4EH	16-bit timer output control register	TOC0		R/W	√	√	–	00H
FF4FH	8-bit timer output control register	TOC1			√	√	–	
FF60H	Serial operation mode register 0	CSIM0			√	√	–	
FF61H	Serial bus interface control register	SBIC			√	√	–	
FF62H	Slave address register	SVA			–	√	–	Undefined
FF63H	Interrupt timing specification register	SINT			√	√	–	00H
FF68H	Serial operation mode register 1	CSIM1			√	√	–	
FF69H	Automatic data transmit/receive control register	ADTC			√	√	–	
FF6AH	Automatic data transmit/receive address pointer	ADTP			–	√	–	
FF6BH	Automatic data transmit/receive interval specification register	ADTI			√	√	–	
FF80H	A/D converter mode register	ADM			√	√	–	01H
FF84H	A/D converter input select register	ADIS			–	√	–	00H
FFA0H	Display mode register 0	DSPM0			Δ Note 1	√	–	
FFA1H	Display mode register 1	DSPM1			–	√	–	
FFA2H	Display mode register 2	DSPM2			–	√	–	
FFE0H	Interrupt request flag register 0L	IF0	IF0L		√	√	√	
FFE1H	Interrupt request flag register 0H		IF0H		√	√		
FFE4H	Interrupt mask flag register 0L	MK0	MK0L		√	√	√	FFH
FFE5H	Interrupt mask flag register 0H		MK0H		√	√		
FFE8H	Priority order specification flag register 0L	PR0	PR0L		√	√	√	
FFE9H	Priority order specification flag register 0H		PR0H		√	√		
FFECH	External interrupt mode register	INTM0			–	√	–	00H
FFF0H	Internal memory size switching register	IMS			–	√	–	**Note 2**
FFF4H	Internal expansion RAM size switching register	IXS		W	–	√	–	**Note 2**
FFF7H	Pull-up resistor option register	PUO		R/W	√	√	–	00H
FFF9H	Watchdog timer mode register	WDTM			√	√	–	
FFFAH	Oscillation stabilization time select register	OSTS			–	√	–	04H
FFFBH	Processor clock control register	PCC			√	√	–	

Notes: 1. Only bit 7 enables for read-only operation.

2. The value after resetting the internal memory size switching register (IMS) and internal expansion RAM size switching register (IXS) differs depending on the product.
   If using the mask ROM version, do not set any value other than that of IMS and IXS after reset, as shown in the table below.

	μPD780204	μPD780205	μPD780206	μPD780208	μPD78P0208
IMS	C8H	CAH	CCH	CFH	
IXS	None		0AH		

(1) Registers controlling port functions

The following two types of registers control the ports:

- Port mode registers (PM0 to PM3, PM7, PM10 to PM12)
- Pull-up resistor option register (PUO)

Format of Port Mode Registers

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PM0	0	0	0	1	PM03	PM02	PM01	1	FF20H	1FH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W
PM3	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	FF23H	FFH	R/W
PM7	0	0	0	PM74	PM73	PM72	PM71	PM70	FF27H	1FH	R/W
PM10	PM107	PM106	PM105	PM104	PM103	PM102	PM101	PM100	FF2AH	FFH	R/W
PM11	PM117	PM116	PM115	PM114	PM113	PM112	PM111	PM110	FF2BH	FFH	R/W
PM12	PM127	PM126	PM125	PM124	PM123	PM122	PM121	PM120	FF2CH	FFH	R/W

PMmn	Selects I/O mode of Pmn pin (m = 0, 1, 2, 3, 7, 10, 11, 12 : n = 0 to 7)
0	Output mode (output buffer ON)
1	Input mode (output buffer OFF)

Format of Pull-up Resistor Option Register

Symbol	7	6	5	4	<3>	<2>	<1>	<0>	Address	After Reset	R/W
PUO	0	0	0	0	PUO3	PUO2	PUO1	PUO0	FFF7H	00H	R/W

PUOm	Selects internal pull-up resistor of Pm (m = 0, 1, 2, 3)
0	Internal pull-up resistor not used
1	Internal pull-up resistor used

Cautions: 1. P00 and P04 pins do not incorporate a pull-up resistor (Port 0).

2. When port 1 is used as analog input for an A/D converter, an on-chip pull-up resistor cannot be used even if 1 is set in PUO1.

(2) Registers controlling clock generator

The following three registers control the clock generator:

- Processor clock control register (PCC)
- Display mode register 0 (DSPM0)
- Display mode register 1 (DSPM1)

Format of Processor Clock Control Register

Symbol	<7>	<6>	<5>	<4>	3	2	1	0	Address	After Reset	R/W
PCC	MCC	FRC	CLS	CSS	0	PCC2	PCC1	PCC0	FFFBH	04H	R/W Note 1

R/W

CSS	PCC2	PCC1	PCC0	Selects CPU clock (f_{CPU})
0	0	0	0	f_X
	0	0	1	$f_X/2$
	0	1	0	$f_X/2^2$
	0	1	1	$f_X/2^3$
	1	0	0	$f_X/2^4$
1	0	0	0	$f_{XT}/2$
	0	0	1	
	0	1	0	
	0	1	1	
	1	0	0	
Settings other than above are prohibited				

R

CLS	Status of CPU clock
0	Main system clock
1	Subsystem clock

R/W

FRC	Selects feedback resistor of subsystem clock
0	Uses internal feedback resistor
1	Does not use internal feedback resistor

R/W

MCC	Controls oscillation of main system clock Note 2
0	Enables oscillation
1	Stops oscillation

Notes: 1. Bit 5 is a read-only bit.

2. When the CPU is operating from the subsystem clock, MCC should be used to stop the main system clock oscillation. A STOP instruction should not be used.

Cautions: 1. Bit 3 must be set to 0.

2. Do not set MCC while an external clock is being input. This is because the X2 pin is pulled up to V_{DD}.

Remarks: f_X: Main system clock oscillation frequency

f_{XT}: Subsystem clock oscillation frequency

Format of Display Mode Register 0 (1/2)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
DSPM0	KSF	DSPM06	DSPM05	SEGS4	SEGS3	SEGS2	SEGS1	SEGS0	FFA0H	00H	R/W

R/W

SEGS4	SEGS3	SEGS2	SEGS1	SEGS0	Display segment (Display mode 1)	Display output total (Display mode 2)
0	0	0	0	0	9	9
0	0	0	0	1	10	10
0	0	0	1	0	11	11
0	0	0	1	1	12	12
0	0	1	0	0	13	13
0	0	1	0	1	14	14
0	0	1	1	0	15	15
0	0	1	1	1	16	16
0	1	0	0	0	17	17
0	1	0	0	1	18	18
0	1	0	1	0	19	19
0	1	0	1	1	20	20
0	1	1	0	0	21	21
0	1	1	0	1	22	22
0	1	1	1	0	23	23
0	1	1	1	1	24	24
1	0	0	0	0	25	25
1	0	0	0	1	26	26
1	0	0	1	0	27	27
1	0	0	1	1	28	28
1	0	1	0	0	29	29
1	0	1	0	1	30	30
1	0	1	1	0	31	31
1	0	1	1	1	32	32
1	1	0	0	0	33	33
1	1	0	0	1	34	34
1	1	0	1	0	35	35
1	1	0	1	1	36	36
1	1	1	0	0	37	37
1	1	1	0	1	38 Note	38
1	1	1	1	0	39 Note	39
1	1	1	1	1	40 Note	40

Note: When the sum of digits and segments is over 53, specification of the number of digits has the priority.

Format of Display Mode Register 0 (2/2)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
DSPM0	KSF	DSPM06	DSPM05	SEGS4	SEGS3	SEGS2	SEGS1	SEGS0	FFA0H	00H	R/W Note 1

R/W	DSPM05	Display mode setting
	0	Display mode 1 (Segment/character type)
	1	Display mode 2 (Type in which a segment spans two or more grids)

R/W	DSPM06	Mode of noise elimination circuit for subsystem clock Note 2
	0	2.5 MHz < f_X ≤ 5.0 MHz
	1	1.25 MHz ≤ f_X ≤ 2.5 MHz Note 3

R	KSF	Timing status
	0	Display timing
	1	Key scan timing

Notes: 1. Bit 7 (KSF) is a read-only bit.

2. Set this bit according to the main system clock oscillation frequency (f_X) selected. Noise elimination circuit is effective during FIP display operation.

3. When f_X is used between 1.25 MHz and 2.5 MHz, set bit 6 (DSPM06) to 1 prior to FIP display.

Caution: When the main system clock frequency selected is below 1.25 MHz and the FIP controller/driver is enabled, make sure to use the main clock for watch timer counting by setting TCL24 to 0.

Format of Display Mode Register 1

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
DSPM1	DIGS3	DIGS2	DIGS1	DIGS0	DIMS3	DIMS2	DIMS1	DIMS0	FFA1H	00H	R/W

DIMS0	Display mode cycle setting
0	1024/f_X is 1 display cycle (1 display cycle = 204.8 μs: @ 5.0-MHz operation)
1	2048/f_X is 1 display cycle (1 display cycle = 409.6 μs: @ 5.0-MHz operation)

DIMS3	DIMS2	DIMS1	FIP output signal cut width
0	0	0	1/16
0	0	1	2/16
0	1	0	4/16
0	1	1	6/16
1	0	0	8/16
1	0	1	10/16
1	1	0	12/16
1	1	1	14/16

DIGS3	DIGS2	DIGS1	DIGS0	Display digit (Display mode 1) DSPM05 = 0	Display pattern (Display mode 2) DSPM05 = 1
0	0	0	0	Display stopped (static display) Note	Display stopped (static display) Note
0	0	0	1	2 digits	2 patterns
0	0	1	0	3 digits	3 patterns
0	0	1	1	4 digits	4 patterns
0	1	0	0	5 digits	5 patterns
0	1	0	1	6 digits	6 patterns
0	1	1	0	7 digits	7 patterns
0	1	1	1	8 digits	8 patterns
1	0	0	0	9 digits	9 patterns
1	0	0	1	10 digits	10 patterns
1	0	1	0	11 digits	11 patterns
1	0	1	1	12 digits	12 patterns
1	1	0	0	13 digits	13 patterns
1	1	0	1	14 digits	14 patterns
1	1	1	0	15 digits	15 patterns
1	1	1	1	16 digits	16 patterns

Note: When setting to display stopped, static display can be set by operating the port output latch.

Remarks: f_X: Main system clock oscillation frequency
DSPM05: Bit 5 of display mode register 0 (DSPM0)

(3) Registers controlling 16-bit timer/event counter

The following six registers control the 16-bit timer/event counter:

- Timer clock select register 0 (TCL0)
- 16-bit timer mode control register (TMC0)
- 16-bit timer output control register (TOC0)
- Port mode register 3 (PM3)
  - Refer to section (1) for the register format.
- External interrupt mode register (INTM0)
  - Refer to section (13) for the register format.
- Sampling clock select register (SCS)
  - Refer to section (13) for the register format.

Format of Timer Clock Select Register 0

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL0	CLOE	TCL06	TCL05	TCL04	TCL03	TCL02	TCL01	TCL00	FF40H	00H	R/W

This section controls the clock output circuit.
Refer to **(7) Registers controlling clock output function** or **Chapter 10** of *μPD780208 Subseries User's Manual* for detailed information.

TCL06	TCL05	TCL04	16-bit timer register count clock selection
0	0	0	TI0 (Valid edge specifiable)
0	0	1	f_X (5.0 MHz)
0	1	0	$f_X/2$ (2.5 MHz)
0	1	1	$f_X/2^2$ (1.25 MHz)
1	0	0	$f_X/2^3$ (625 kHz)
Settings other than above are prohibited			

Cautions: 1. Setting of the TI0/INTP0 pin valid edge is performed by the external interrupt mode register (INTM0), and selection of the sampling clock frequency is performed by the sampling clock select register (SCS).

2. To read the count value when TI0 has been specified as the TM0 count clock, the value should be read from TM0, not from the 16-bit capture register (CR01).

3. To write data other than that already written to TCL0, stop the timer operation once.

Remarks: f_X: Main system clock oscillation frequency

TI0 : 16-bit timer/event counter input pin

TM0: 16-bit timer register

Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of 16-Bit Timer Mode Control Register

Symbol	7	6	5	4	3	2	1	<0>	Address	After Reset	R/W
TMC0	0	0	0	0	TMC03	TMC02	TMC01	OVF00	FF48H	00H	R/W

OVF0	16-bit timer register overflow detection
0	Overflow not detected
1	Overflow detected

TMC03	TMC02	TMC01	Operating mode and clear mode selection	TO0 output timing selection	Interrupt request generation
0	0	0	Operation stop (TM0 cleared to 0)	No change	Not generated
0	0	1	PWM mode (free running)	PWM pulse output	Generated on match between TM0 and CR00
0	1	0	Free-running mode	Match between TM0 and CR00	
0	1	1		Match between TM0 and CR00 or TI0 valid edge	
1	0	0	Clear and start on TI0 valid edge	Match between TM0 and CR00	
1	0	1		Match between TM0 and CR00 or TI0 valid edge	
1	1	0	Clear and start on match between TM0 and CR00	Match between TM0 and CR00	
1	1	1		Match between TM0 and CR00 or TI0 valid edge	

Cautions: 1. The 16-bit timer register (TM0) starts operation when a value other than 0, 0, 0 is set to TMC01 to TMC03 (operation stop mode). To stop the operation, set TMC01 to TMC03 to 0, 0, 0.

2. Switch the clear mode and the TO0 output timing after stopping the timer operation (by setting TMC01 to TMC03 to 0, 0, 0).

3. Setting of the TI0/INTP0 pin valid edge is performed by the external interrupt mode register (INTM0), and selection of the sampling clock frequency is performed by the sampling clock select register (SCS).

4. When using the PWM mode, set the PWM and then set data to CR00.

Remarks: TO0: Output pin of 16-bit timer/event counter
TI0: Input pin of 16-bit timer/event counter
TM0: 16-bit timer register
CR00: 16-bit compare register

Format of 16-Bit Timer Output Control Register

Symbol	7	6	5	4	<3>	<2>	1	<0>	Address	After Reset	R/W
TOC0	0	0	0	0	LVS0	LVR0	TOC01	TOE0	FF4EH	00H	R/W

TOE0	16-bit timer/event counter output control
0	Output disabled (Port mode)
1	Output enabled

TOC01	In PWM mode	In other modes
	Active level selection	Timer output F/F control
0	Active high	Inversion operation disabled
1	Active low	Inversion operation enabled

LVS0	LVR0	16-bit timer/event counter timer output F/F status setting
0	0	No change
0	1	Timer output F/F reset (0)
1	0	Timer output F/F set (1)
1	1	Setting prohibited

Cautions: 1. Timer operation must be stopped before setting TOC0.

2. If LVS0 and LVR0 are read after data is set, they will be 0.

(4) Registers controlling 8-bit timer/event counter

The following four registers control the 8-bit timer/event counters:

- Timer clock select register 1 (TCL1)
- 8-bit timer mode control register (TMC1)
- 8-bit timer output control register (TOC1)
- Port mode register 3 (PM3)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 1

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL1	TCL17	TCL16	TCL15	TCL14	TCL13	TCL12	TCL11	TCL10	FF41H	00H	R/W

TCL13	TCL12	TCL11	TCL10	8-bit timer register 1 count clock selection
0	0	0	0	TI1 falling edge
0	0	0	1	TI1 rising edge
0	1	0	1	$f_X/2$ (2.5 MHz)
0	1	1	0	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_X/2^9$ (9.8 kHz)
1	1	1	0	$f_X/2^{10}$ (4.9 kHz)
1	1	1	1	$f_X/2^{12}$ (1.2 kHz)
Settings other than above are prohibited				

TCL17	TCL16	TCL15	TCL14	8-bit timer register 2 count clock selection
0	0	0	0	TI2 falling edge
0	0	0	1	TI2 rising edge
0	1	0	1	$f_X/2$ (2.5 MHz)
0	1	1	0	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_X/2^9$ (9.8 kHz)
1	1	1	0	$f_X/2^{10}$ (4.9 kHz)
1	1	1	1	$f_X/2^{12}$ (1.2 kHz)
Settings other than above are prohibited				

Caution: If TCL1 is to be rewritten in data other than identical data, the timer operation must be stopped first.

Remarks: f_X: Main system clock frequency

TI1: 8-bit timer register 1 input pin

TI2: 8-bit timer register 2 input pin

Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of 8-Bit Timer Mode Control Register

Symbol	7	6	5	4	3	2	<1>	<0>	Address	After Reset	R/W
TMC1	0	0	0	0	0	TMC12	TCE2	TCE1	FF49H	00H	R/W

TCE1	8-bit timer register 1 operation control
0	Operation stop (TM1 clear to 0)
1	Operation enable

TCE2	8-bit timer register 2 operation control
0	Operation stop (TM2 clear to 0)
1	Operation enable

TMC12	Operating mode selection
0	8-bit timer register x 2-channel mode (TM1, TM2)
1	16-bit timer register x 1-channel mode (TMS)

Cautions: 1. Switch the operation mode after stopping timer operation.

2. When used as a 16-bit timer register (TMS), TCE1 should be used for operation enable/stop.

Format of 8-Bit Timer Output Control Register

Symbol	<7>	<6>	5	<4>	<3>	<2>	1	<0>	Address	After Reset	R/W
TOC1	LVS2	LVR2	TOC15	TOE2	LVS1	LVR1	TOC11	TOE1	FF4FH	00H	R/W

TOE1	8-bit timer/event counter 1 output control
0	Output disable (Port mode)
1	Output enable

TOC11	8-bit timer/event counter 1 timer output F/F control
0	Inverted operation disable
1	Inverted operation enable

LVS1	LVR1	8-bit timer/event counter 1 timer output F/F status set
0	0	Unchanged
0	1	Timer output F/F reset (0)
1	0	Timer output F/F set (1)
1	1	Setting prohibited

TOE2	8-bit timer/event counter 2 output control
0	Output disable (Port mode)
1	Output enable

TOC15	8-bit timer/event counter 2 timer output F/F control
0	Inverted operation disable
1	Inverted operation enable

LVS2	LVR2	8-bit timer/event counter 2 timer output F/F status set
0	0	Unchanged
0	1	Timer output F/F reset (0)
1	0	Timer output F/F set (1)
1	1	Setting prohibited

Cautions: 1. Be sure to set TOC1 after stopping timer operation.

2. After data setting, 0 can be read from LVS1, LVS2, LVR1, and LVR2.

(5) Registers controlling watch timer

The following two registers control the watch timer:

- Timer clock select register 2 (TCL2)
- Watch timer mode control register (TMC2)

Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL2	TCL27	TCL26	TCL25	TCL24	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

This section controls the watchdog timer.
Refer to **(6) Registers controlling watchdog timer** or **Chapter 9** of *μPD780208 Subseries User's Manual* for detailed information.

TCL24	Watch timer count clock selection [Note]
0	$f_X/2^8$ (19.5 kHz)
1	f_{XT} (32.768 kHz)

This section controls the buzzer output function.
Refer to **(8) Registers controlling buzzer output function** or **Chapter 11** of *μPD780208 Subseries User's Manual* for detailed information.

Note: When using a main system clock of 1.25 MHz or less and a FIP controller/driver, select $f_X/2^8$ as the counter clock for the watch timer.

Caution: To write data other than that already written to TCL2, first stop the timer operation.

Remarks: f_X: Main system clock frequency
f_{XT}: Subsystem clock oscillation frequency
Values in parentheses apply to operation with f_X = 5.0 MHz or f_{XT} = 32.768 kHz.
This register is also used to control the watchdog timer and the buzzer output function.

Format of Watch Timer Mode Control Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TMC2	0	TMC26	TMC25	TMC24	TMC23	TMC22	TMC21	TMC20	FF4AH	00H	R/W

TMC23	TMC20	Watch flag set time selection
0	0	$2^{14}/f_W$ (0.5 s)
1		$2^{13}/f_W$ (0.25 s)
0	1	$2^5/f_W$ (977 μs)
1		$2^4/f_W$ (488 μs)

TMC21	Prescaler operation control[Note]
0	Clear after operation stops
1	Operation enable

TMC22	5-bit counter operation control
0	Clear after operation stops
1	Operation enable

TMC26	TMC25	TMC24	Prescaler interval time selection
0	0	0	$2^4/f_W$ (488 μs)
0	0	1	$2^5/f_W$ (977 μs)
0	1	0	$2^6/f_W$ (1.95 ms)
0	1	1	$2^7/f_W$ (3.91 ms)
1	0	0	$2^8/f_W$ (7.81 ms)
1	0	1	$2^9/f_W$ (15.6 ms)
Settings other than above are prohibited			

Note: Do not frequently clear the prescaler when using the watch timer.

Remarks: f_W: Watch timer clock frequency ($f_X/2^8$ or f_{XT})

Values in parentheses apply to operation with f_W = 32.768 kHz.

A 1 second or 0.5 second interval can be generated with a 4.19304 MHz main system clock.

A 0.5 second or 0.25 second interval can be generated with the 32.768 kHz subsystem clock.

(6) Registers controlling watchdog timer

The following two registers control the watchdog timer:

- Timer clock select register 2 (TCL2)
- Watchdog timer mode register (WDTM)

Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL2	TCL27	TCL26	TCL25	TCL24	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

TCL22	TCL21	TCL20	Count clock selection	
			Watchdog Timer mode	Interval Timer mode
0	0	0	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
0	0	1	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
0	1	0	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
0	1	1	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	0	0	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	0	1	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
1	1	0	$f_X/2^9$ (9.8k Hz)	$f_X/2^{10}$ (4.9 kHz)
1	1	1	$f_X/2^{11}$ (2.4 kHz)	$f_X/2^{12}$ (1.2 kHz)

This section controls the watch timer.
Refer to **(5) Registers controlling watch timer** or **Chapter 8** of *μPD780208 Subseries User's Manual* for detailed information.

This section controls the buzzer output function.
Refer to **(8) Registers controlling buzzer output function** or **Chapter 11** of *μPD780208 Subseries User's Manual* for detailed information.

Caution: To write data other than that already written to TCL2, first stop the timer operation.

Remarks: f_X: Main system clock frequency
f_{XT}: Subsystem clock oscillation frequency
Values in parentheses apply to operation with f_X = 5.0 MHz.
This register is also used to control the watch timer and the buzzer output function.

Format of Watchdog Timer Mode Register

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
WDTM	RUN	0	0	WDTM4	WDTM3	0	0	0	FFF9H	00H	R/W

WDTM4	WDTM3	Watchdog timer operating mode selection[Note 1]
0	x	Interval timer mode[Note 2] (Maskable interrupt request occurs upon generation of an overflow.)
1	0	Watchdog timer mode 1 (Non-maskable interrupt request occurs upon generation of an overflow.)
1	1	Watchdog timer mode 2 (Reset operation is activated upon generation of an overflow.)

RUN	Watchdog timer operation selection[Note 3]
0	Count stop
1	Counter is cleared and counting starts

Notes: 1. Once set to 1, WDTM3 and WDTM4 cannot be cleared to 0 by software.
2. Starts operation as an interval timer as soon as RUN is set to 1.
3. Once set to 1, RUN cannot be cleared to 0 by software. Thus, once counting starts, it can only be stopped by $\overline{\text{RESET}}$ input.

Cautions: 1. When 1 is set in RUN so that the watchdog timer is cleared, the actual overflow time is up to 0.5% shorter than the time set by timer clock select register 2 (TCL2).
2. When using the watchdog timer mode 1 and 2, make sure that the interrupt request flag (TMIF4) is set to 0 before setting WDTM4 to 1. If WDTM4 is set to 1 while TMIF4 is 1, a non-maskable interrupt request occurs regardless of the contents of WDTM3.

Remark: ×: Don't care

(7) Registers controlling clock output function

The following two registers control the clock output function:

- Timer clock select register 0 (TCL0)
- Port mode register 3 (PM3)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 0

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL0	CLOE	TCL06	TCL05	TCL04	TCL03	TCL02	TCL01	TCL00	FF40H	00H	R/W

TCL03	TCL02	TCL01	TCL00	PCL output clock selection
0	0	0	0	f_{XT} (32.768 kHz)
0	1	1	1	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_X/2^8$ (19.5 kHz)
Settings other than above are prohibited				

This section controls the 16-bit timer.
Refer to **(3) Registers controlling 16-bit timer/event counter** or **Chapter 6** of *μPD780208 Subseries User's Manual* for detailed information.

CLOE	PCL output control
0	Output disable
1	Output enable

Cautions: 1. When enabling PCL output, set TCL00 to TCL03, then set 1 in CLOE with a 1-bit memory manipulation instruction.

2. To write data other than that already written to TCL0, first stop the timer operation.

Remarks: f_X: Main system clock frequency

f_{XT}: Subsystem clock oscillation frequency

Values in parentheses apply to operation with f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

(8) Registers controlling buzzer output function

The following two registers control the buzzer output function:

- Timer clock select register 2 (TCL2)
- Port mode register 3 (PM3)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL2	TCL27	TCL26	TCL25	TCL24	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

This section controls the watchdog timer.
Refer to **(6) Registers controlling watchdog timer** or **Chapter 9** of *μPD780208 Subseries User's Manual* for detailed information.

This section controls the watch timer.
Refer to **(5) Registers controlling watch timer** or **Chapter 8** of *μPD780208 Subseries User's Manual* for detailed information.

TCL27	TCL26	TCL25	Buzzer output frequency selection
0	x	x	Buzzer output disable
1	0	0	$f_X/2^{10}$ (4.9 kHz)
1	0	1	$f_X/2^{11}$ (2.4 kHz)
1	1	0	$f_X/2^{12}$ (1.2 kHz)
1	1	1	Setting prohibited

Caution: To write data other than that already written to TCL2, stop the timer operation once.

Remarks: f_X: Main system clock frequency
×: Don't care
Values in parentheses apply to operation with f_X = 5.0 MHz.

(9) Registers controlling A/D converter

The following two registers control the A/D converter:

- A/D converter mode register (ADM)
- A/D converter input select register (ADIS)

Format of A/D Converter Mode Register

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After Reset	R/W
ADM	CS	TRG	FR1	FR0	ADM3	ADM2	ADM1	1	FF80H	01H	R/W

ADM3	ADM2	ADM1	Analog input channel selection
0	0	0	ANI0
0	0	1	ANI1
0	1	0	ANI2
0	1	1	ANI3
1	0	0	ANI4
1	0	1	ANI5
1	1	0	ANI6
1	1	1	ANI7

FR1	FR0	A/D conversion time selection[Note 1]	
		When operated at f_X = 5.0 MHz	When operated at f_X = 4.19 MHz
0	0	160/f_X (32.0 μs)	160/f_X (38.1 μs)
0	1	80/f_X (Setting prohibited[Note 2])	80/f_X (19.1 μs)
1	0	200/f_X (40.0 μs)	200/f_X (47.7 μs)
1	1	Setting prohibited	

TRG	External trigger selection
0	No external trigger (software starts mode)
1	Conversion started by external trigger (hardware starts mode)

CS	A/D conversion operation control
0	Operation stop
1	Operation start

Notes: 1. Set so that the A/D conversion time is 19.1 μs or more.
2. Setting prohibited because the A/D conversion time is less than 19.1 μs.

Cautions:
1. In consideration of power consumption reduction at the A/D converter when the standby function is working, clear bit 7 (CS) of this register to 0 to stop the A/D conversion operation before executing a HALT or STOP instruction.
2. When restarting the stopped A/D conversion operation, start the A/D conversion operation after clearing the interrupt request flag (ADIF) to 0.

Remark: f_X: Main system clock frequency

Format of A/D Converter Input Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADIS	0	0	0	0	ADIS3	ADIS2	ADIS1	ADIS0	FF84H	00H	R/W

ADIS3	ADIS2	ADIS1	ADIS0	Number of analog input channel selection
0	0	0	0	No analog input channel (P10 to P17)
0	0	0	1	1 channel (ANI0, P11 to P17)
0	0	1	0	2 channels (ANI0, ANI1, P12 to P17)
0	0	1	1	3 channels (ANI0 to ANI2, P13 to P17)
0	1	0	0	4 channels (ANI0 to ANI3, P14 to P17)
0	1	0	1	5 channels (ANI0 to ANI4, P15 to P17)
0	1	1	0	6 channels (ANI0 to ANI5, P16, P17)
0	1	1	1	7 channels (ANI0 to ANI6, P17)
1	0	0	0	8 channels (ANI0 to ANI7)
Settings other than above are prohibited				

Cautions: 1. Set the analog input channel in the following order:

a. Set the number of analog input channels with ADIS.

b. Using A/D converter mode register (ADM), select one channel to undergo A/D conversion among the channels that are set for analog input with ADIS.

2. No internal pull-up resistor can be connected to the channels set for analog input with ADIS, irrespective of the value of bit 1 (PUO1) of the pull-up resistor option register (PUO).

(10) Registers controlling serial interface channel 0

The following four registers control serial interface channel 0:

- Timer clock select register 3 (TCL3)
- Serial operation mode register 0 (CSIM0)
- Serial bus interface control register (SBIC)
- Interrupt timing specification register (SINT)

Format of Timer Clock Select Register 3

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL3	TCL37	TCL36	TCL35	TCL34	TCL33	TCL32	TCL31	TCL30	FF43H	88H	R/W

TCL33	TCL32	TCL31	TCL30	Serial interface channel 0 serial clock selection
0	1	1	0	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_X/2^9$ (9.8 kHz)
Settings other than above are prohibited				

This section controls the serial interface channel 1.
Refer to **(11) Registers controlling serial interface channel 1** or **Chapter 14** of *μPD780208 Subseries User's Manual* for detailed information.

Caution: If a value that is not the same as the previous value must be written to TCL3, stop the serial transfer before writing the value.

Remarks: fx: Main system clock frequency
Values in parentheses apply to operation with fx = 5.0 MHz.

Format of Serial Operation Mode Register 0

Symbol	<7>	<6>	<5>	4	3	2	1	0	Address	After Reset	R/W
CSIM0	CSIE0	COI	WUP	CSIM 04	CSIM 03	CSIM 02	CSIM 01	CSIM 00	FF60H	00H	R/W Note 1

R/W

CSIM 01	CSIM 00	Serial interface channel 0 clock selection
0	×	Input clock to $\overline{\text{SCK0}}$ pin from off-chip
1	0	8-bit timer register 2 (TM2) output
1	1	Clock specified with bits 0 to 3 of timer clock select register 3 (TCL3)

R/W

CSIM 04	CSIM 03	CSIM 02	PM25	P25	PM26	P26	PM27	P27	Operating Mode	Start Bit	SI0/P25 Pin Function	SO0/P26 Pin Function	$\overline{\text{SCK0}}$/P27 Pin Function
0	×	0	1	×	0	0	0	1	3-wire serial I/O mode	MSB	SI0 Note 2 (Input)	SO0 (CMOS output)	$\overline{\text{SCK0}}$ (CMOS input/output)
		1								LSB			
1	0	0	Note 3 ×	Note 3 ×	0	0	0	1	SBI mode	MSB	P25 (CMOS input/output)	SB1 (N-ch open-drain input/output)	$\overline{\text{SCK0}}$ (CMOS input/output)
		1	0	0	Note 3 ×	Note 3 ×	0	1			SB0 (N-ch open-drain input/output)	P26 (CMOS input/ output)	
1	1	0	Note 3 ×	Note 3 ×	0	0	0	1	2-wire serial I/O mode	MSB	P25 (CMOS input/output)	SB1 (N-ch open-drain input/output)	$\overline{\text{SCK0}}$ (N-ch open-drain input/ output)
		1	0	0	Note 3 ×	Note 3 ×	0	1			SB0 (N-ch open-drain input/output)	P26 (CMOS input/output)	

R/W

WUP	Wake-up function control Note 4
0	Interrupt request signal generation with each serial transfer in any mode
1	Interrupt request signal generation when the address received after bus release (when CMDD = RELD = 1) matches the slave address register (SVA) in SBI mode

R

COI	Slave address comparison result flag Note 5
0	Slave address register (SVA) not equal to serial I/O shift register 0 (SIO0) data
1	Slave address register (SVA) equal to serial I/O shift register 0 (SIO0) data

R/W

CSIE0	Serial interface channel 0 operation control
0	Operation stopped
1	Operation enable

Notes: 1. Bit 6 (COI) is a read-only bit.
2. Can be used as P25 (CMOS input) when serial channel is used only for transmission.
3. Can be used freely as a port function when not used in SBI or 2-wire mode.
4. To use the wake-up function (WUP = 1), clear bit 5 (SIC) of the interrupt timing specify register (SINT) to 0.
5. COI becomes 0 when CSIE0 = 0.

Caution: Do not change the operation mode (3-wire serial I/O, 2-wire serial I/O, or SBI) while the operation of serial interface channel 0 is enabled. Stop the serial operation before changing the operation mode.

Remarks: ×: Don't care
PM××: Port mode register
P××: Port output latch

Format of Serial Bus Interface Control Register (1/2)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
SBIC	BSYE	ACKD	ACKE	ACKT	CMDD	RELD	CMDT	RELT	FF61H	00H	R/W[Note]

R/W		
R/W	RELT	Use for bus release signal output. When RELT = 1, SO latch is set to 1. After SO latch setting, automatically cleared to 0. Also cleared to 0 when CSIE0 = 0.

R/W		
R/W	CMDT	Use for command signal output. When CMDT = 1, SO latch is cleared to (0). After SO latch clearance, automatically cleared to (0). Also cleared to (0) when CSIE0 = 0.

R	RELD	Bus release detection	
	Clear Conditions (RELD = 0)		Set Condition (RELD = 1)
	• When transfer start instruction is executed • If SIO0 and SVA values do not match in address reception • When CSIE0 = 0 • When $\overline{\text{RESET}}$ input is applied		• When bus release signal (REL) is detected

R	CMDD	Command detection	
	Clear Conditions (CMDD = 0)		Set Condition (CMDD = 1)
	• When transfer start instruction is executed • When bus release signal (REL) is detected • When CSIE0 = 0 • When $\overline{\text{RESET}}$ input is applied		• When command signal (CMD) is detected

R/W		
R/W	ACKT	Acknowledge signal is output in synchronization with the falling-edge clock of $\overline{\text{SCK0}}$ just after execution of the instruction to be set to 1, and after acknowledge signal output, automatically cleared to 0. Also cleared to 0 upon start of serial interface transfer or when CSIE0 = 0.

Note: Bits 2, 3, and 6 (RELD, CMDD, and ACKD) are read-only bits.

Remark: CSIE0: Bit 7 of the serial operating mode register 0 (CSIM0)

Format of Serial Bus Interface Control Register (2/2)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
SBIC	BSYE	ACKD	ACKE	ACKT	CMDD	RELD	CMDT	RELT	FF61H	00H	R/W[Note]

R/W

ACKE	Acknowledge signal output control	
0	Acknowledge signal automatic output disable (output with ACKT enable)	
1	Before completion of transfer	Acknowledge signal is output in synchronization with the 9th clock falling edge of $\overline{SCK0}$ (automatically output when ACKE = 1).
	After completion of transfer	Acknowledge signal is output in synchronization with the falling edge of $\overline{SCK0}$ just after execution of the instruction to be set to 1 (automatically output when ACKE = 1). However, it is not automatically cleared to 0 after acknowledge signal output.

R

ACKD	Acknowledge detection	
Clear Conditions (ACKD = 0)		Set Condition (ACKD = 1)
• At the falling edge of $\overline{SCK0}$ immediately after the busy mode has been released when a transfer start instruction is executed • When $\overline{CSIE0}$ = 0 • When $\overline{RESET}$ input is applied		• When acknowledge signal ($\overline{ACK}$) is detected at the rising edge of $\overline{SCK0}$ clock after completion of transfer

R/W

BSYE[Note]	Synchronizing busy signal output control
0	Disables busy signal, which is output in synchronization with the falling edge of $\overline{SCK0}$ clock just after execution of the instruction to be cleared to 0.
1	Outputs busy signal at the falling edge of $\overline{SCK0}$ clock following the acknowledge signal.

Note: Busy mode can be cleared by starting a serial interface transfer. However, the BSYE flag is not cleared to 0.

Remarks: Bits 0, 1, and 4 (RELT, CMDT, and ACKT) are 0 when read after data setting.
CSIE0: Bit 7 of the serial operating mode register 0 (CSIM0)

Format of Interrupt Timing Specification Register

Symbol	7	<6>	<5>	<4>	3	2	1	0	Address	After Reset	R/W
SINT	0	CLD	SIC	SVAM	0	0	0	0	FF63H	00H	R/W[Note 1]

R/W

SVAM	SVA bit to be used as slave address
0	Bits 0 to 7
1	Bits 1 to 7

R/W

SIC	INTCSI0 interrupt factor selection[Note 2]
0	CSIIF0 is set upon termination of a serial interface channel 0 transfer
1	CSIIF0 is set upon bus release detection or termination of a serial interface channel 0 transfer

R

CLD	$\overline{\text{SCK0}}$ pin level[Note 3]
0	Low level
1	High level

Notes: 1. Bit 6 (CLD) is a read-only bit.
2. When using the wake-up function, set SIC to 0.
3. When CSIE = 0, CLD becomes 0.

Caution: Be sure to set bits 0 through 3 to 0.

Remarks: SVA: Slave address register
CSIIF0: Interrupt request flag for INTCSI0
CSIE0: Bit 7 of serial operation mode register 0 (CSIM0)

(11) Registers controlling serial interface channel 1

The following four registers control serial interface channel 1:

- Timer clock select register 3 (TCL3)
- Serial operation mode register 1 (CSIM1)
- Automatic data transmit/receive control register (ADTC)
- Automatic data transmit/receive interval specification register (ADTI)

Format of Timer Clock Select Register 3

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL3	TCL37	TCL36	TCL35	TCL34	TCL33	TCL32	TCL31	TCL30	FF43H	88H	R/W

This section controls the serial interface channel 0.
Refer to **(10) Registers controlling serial interface channel 0** or **Chapter 13** of *µPD780208 Subseries User's Manual* for detailed information.

TCL37	TCL36	TCL35	TCL34	Serial interface channel 1 serial clock selection
0	1	1	0	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_X/2^9$ (9.8 kHz)
Settings other than above are prohibited				

Caution: If a value that is not the same as the previous value must be written to TCL3, stop the serial transfer before writing the value.

Remarks: fx: Main system clock frequency
Values in parentheses apply to operation with fx = 5.0 MHz.

Format of Serial Operation Mode Register 1

Symbol	<7>	6	<5>	4	3	2	1	0	Address	After Reset	R/W
CSIM1	CSIE1	DIR	ATE	0	0	0	CSIM 11	CSIM 10	FF68H	00H	R/W

CSIM 11	CSIM 10	Serial interface channel 1 clock selection
0	×	Clock externally input to $\overline{\text{SCK1}}$ pin[Note 1]
1	0	8-bit timer register 2 (TM2) output
1	1	Clock specified with bits 4 to 7 of timer clock select register 3 (TCL3)

ATE	Serial interface channel 1 operating mode selection
0	3-wire serial I/O mode
1	3-wire serial I/O mode with automatic transmit/receive function

DIR	Start Bit	SI1 Pin Function	SO1 Pin Function
0	MSB	SI1/P20 (Input)	SO1 (CMOS output)
1	LSB		

CSIE1	CSIM 11	PM20	P20	PM21	P21	PM22	P22	Shift Register 1 Operation	Serial Clock Counter Operation Control	SI1/P20 Pin Function	SO1/P21 Pin Function	$\overline{\text{SCK1}}$/P22 Pin Function
0	×	Note 2 ×	Note 2 ×	Note 2 ×	Note 2 ×	Note 2 ×	Note 2 ×	Operation stop	Clear	P20 (CMOS input/output)	P21 (CMOS input/output)	P22 (CMOS input/output)
1	0	Note 3 1	Note 3 ×	0	0	1	×	Operation enable	Count operation	SI1[Note 3] (Input)	SO1 (CMOS output)	$\overline{\text{SCK1}}$ (Input)
	1					0	1					$\overline{\text{SCK1}}$ (CMOS output)

Notes: 1. If the external clock input has been selected with CSIM11 set to 0, set bit 1 (BUSY1) and bit 2 (STRB) of the automatic data transmit/receive control register (ADTC) to 0, 0.
2. Can be used freely as a port function when not used in the 3-wire mode.
3. Can be used as P20 when only the transmitter is used. (Set bit 7 (RE) of ADTC to 0.)

Remarks: ×: Don't care
PM××: Port mode register
P××: Port output latch

Format of Automatic Data Transmit/Receive Control Register

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
ADTC	RE	ARLD	ERCE	ERR	TRF	STRB	BUSY1	BUSY0	FF69H	00H	R/W[Note 1]

R/W

BUSY1	BUSY0	Busy input control
0	×	Not using busy input
1	0	Busy input enable (active high)
1	1	Busy input enable (active low)

R/W

STRB	Strobe output control
0	Strobe output disable
1	Strobe output enable

R

TRF	Status of automatic transmit/receive function[Note 2]
0	Detection of termination of automatic transmission/ reception (This bit is set to 0 upon suspension of automatic transmission/reception or when ARLD = 0.)
1	During automatic transmission/reception (This bit is set to 1 when data is written to SIO1.)

R

ERR	Error detection of automatic transmit/receive function
0	No error (This bit is set to 0 when data is written to SIO1.)
1	Error occurred

R/W

ERCE	Error check control of automatic transmit/ receive function
0	Error check disable
1	Error check enable (only when BUSY1 = 1)

R/W

ARLD	Operating mode selection of automatic transmit/ receive function
0	Single operating mode
1	Repetitive operating mode

R/W

RE	Receive control of automatic transmit/receive function
0	Receive disable
1	Receive enable

Notes: 1. Bits 3 and 4 (TRF and ERR) are read-only bits.

2. The termination of automatic transmission/reception should be judged by using TRF, not CSIIF1 (interrupt request flag).

Caution: When an external clock input is selected with bit 1 (CSIM11) of the serial operating mode register 1 (CSIM1) set to 0, set STRB and BUSY1 of ADTC to 0, 0.

Remark: ×: Don't care

Format of Automatic Data Transmit/Receive Interval Specification Register (1/2)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADTI	ADTI7	0	0	ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	FF6BH	00H	R/W

ADTI7	Data transfer interval control
0	No control of interval by ADTI[Note 1]
1	Control of interval by ADTI (ADTI0 to ADTI4)

ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	Data transfer interval specification (f_X = 5.0-MHz operation)	
					Minimum[Note 2]	Maximum[Note 2]
0	0	0	0	0	36.8 μs + 0.5/f_{SCK}	40.0 μs + 1.5/f_{SCK}
0	0	0	0	1	62.4 μs + 0.5/f_{SCK}	65.6 μs + 1.5/f_{SCK}
0	0	0	1	0	88.0 μs + 0.5/f_{SCK}	91.2 μs + 1.5/f_{SCK}
0	0	0	1	1	113.6 μs + 0.5/f_{SCK}	116.8 μs + 1.5/f_{SCK}
0	0	1	0	0	139.2 μs + 0.5/f_{SCK}	142.4 μs + 1.5/f_{SCK}
0	0	1	0	1	164.8 μs + 0.5/f_{SCK}	168.0 μs + 1.5/f_{SCK}
0	0	1	1	0	190.4 μs + 0.5/f_{SCK}	193.6 μs + 1.5/f_{SCK}
0	0	1	1	1	216.0 μs + 0.5/f_{SCK}	219.2 μs + 1.5/f_{SCK}
0	1	0	0	0	241.6 μs + 0.5/f_{SCK}	244.8 μs + 1.5/f_{SCK}
0	1	0	0	1	267.2 μs + 0.5/f_{SCK}	270.4 μs + 1.5/f_{SCK}
0	1	0	1	0	292.8 μs + 0.5/f_{SCK}	296.0 μs + 1.5/f_{SCK}
0	1	0	1	1	318.4 μs + 0.5/f_{SCK}	321.6 μs + 1.5/f_{SCK}
0	1	1	0	0	344.0 μs + 0.5/f_{SCK}	347.2 μs + 1.5/f_{SCK}
0	1	1	0	1	369.6 μs + 0.5/f_{SCK}	372.8 μs + 1.5/f_{SCK}
0	1	1	1	0	395.2 μs + 0.5/f_{SCK}	398.4 μs + 1.5/f_{SCK}
0	1	1	1	1	420.8 μs + 0.5/f_{SCK}	424.0 μs + 1.5/f_{SCK}

Notes: 1. The interval is dependent only on CPU processing.

2. The data transfer interval includes an error. The data transfer minimum and maximum intervals are found from the following expressions (n: Value set in ADTI0 to ADTI4). However, if a minimum calculated by the following expressions is smaller than 2/f_{SCK}, the minimum interval time is 2/f_{SCK}.

$$\text{Minimum} = (n + 1) \times \frac{2^7}{f_X} + \frac{56}{f_X} + \frac{0.5}{f_{SCK}}$$

$$\text{Maximum} = (n + 1) \times \frac{2^7}{f_X} + \frac{72}{f_X} + \frac{1.5}{f_{SCK}}$$

Cautions: 1. Do not write data to ADTI during operation of the automatic data transmit/receive function.

2. Be sure to set bits 5 and 6 to 0.

3. While ADTI is used to control the interval time for data transfer by the automatic data transmit/receive function, busy control is invalid.

Remarks: f_X: Main system clock frequency

f_{SCK}: Serial clock frequency

Format of Automatic Data Transmit/Receive Interval Specification Register (2/2)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADTI	ADTI7	0	0	ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	FF6BH	00H	R/W

ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	Data transfer interval specification (f_X = 5.0-MHz operation)	
					Minimum[Note]	Maximum[Note]
1	0	0	0	0	446.4 μs + 0.5/f_{SCK}	449.6 μs + 1.5/f_{SCK}
1	0	0	0	1	472.0 μs + 0.5/f_{SCK}	475.2 μs + 1.5/f_{SCK}
1	0	0	1	0	497.6 μs + 0.5/f_{SCK}	500.8 μs + 1.5/f_{SCK}
1	0	0	1	1	523.2 μs + 0.5/f_{SCK}	526.4 μs + 1.5/f_{SCK}
1	0	1	0	0	548.8 μs + 0.5/f_{SCK}	552.0 μs + 1.5/f_{SCK}
1	0	1	0	1	574.4 μs + 0.5/f_{SCK}	577.6 μs + 1.5/f_{SCK}
1	0	1	1	0	600.0 μs + 0.5/f_{SCK}	603.2 μs + 1.5/f_{SCK}
1	0	1	1	1	625.6 μs + 0.5/f_{SCK}	628.8 μs + 1.5/f_{SCK}
1	1	0	0	0	651.2 μs + 0.5/f_{SCK}	654.4 μs + 1.5/f_{SCK}
1	1	0	0	1	676.8 μs + 0.5/f_{SCK}	680.0 μs + 1.5/f_{SCK}
1	1	0	1	0	702.4 μs + 0.5/f_{SCK}	705.6 μs + 1.5/f_{SCK}
1	1	0	1	1	728.0 μs + 0.5/f_{SCK}	731.2 μs + 1.5/f_{SCK}
1	1	1	0	0	753.6 μs + 0.5/f_{SCK}	756.8 μs + 1.5/f_{SCK}
1	1	1	0	1	779.2 μs + 0.5/f_{SCK}	782.4 μs + 1.5/f_{SCK}
1	1	1	1	0	804.8 μs + 0.5/f_{SCK}	808.0 μs + 1.5/f_{SCK}
1	1	1	1	1	830.4 μs + 0.5/f_{SCK}	833.6 μs + 1.5/f_{SCK}

Note: The data transfer interval includes an error. The data transfer minimum and maximum intervals are found from the following expressions (n: Value set in ADTI0 to ADTI4). However, if a minimum calculated by the following expressions is smaller than 2/f_{SCK}, the minimum interval time is 2/f_{SCK}.

$$\text{Minimum} = (n + 1) \times \frac{2^7}{f_X} + \frac{56}{f_X} + \frac{0.5}{f_{SCK}}$$

$$\text{Maximum} = (n + 1) \times \frac{2^7}{f_X} + \frac{72}{f_X} + \frac{1.5}{f_{SCK}}$$

Cautions:

1. **Do not write data to ADTI during operation of the automatic data transmit/receive function.**
2. **Be sure to set bits 5 and 6 to 0.**
3. **While ADTI is used to control the interval time for data transfer by the automatic data transmit/receive function, busy control is invalid.**

Remarks: f_X: Main system clock frequency

f_{SCK}: Serial clock frequency

(12) Registers controlling FIP controller

The following three registers control FIP controller:

- Display mode register 0 (DSPM0)
- Display mode register 1 (DSPM1)
- Display mode register 2 (DSPM2)

Format of Display Mode Register 0 (1/2)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
DSPM0	KSF	DSPM06	DSPM05	SEGS4	SEGS3	SEGS2	SEGS1	SEGS0	FFA0H	00H	R/W

R/W	SEGS4	SEGS3	SEGS2	SEGS1	SEGS0	Display segment (Display mode 1)	Display output total (Display mode 2)
	0	0	0	0	0	9	9
	0	0	0	0	1	10	10
	0	0	0	1	0	11	11
	0	0	0	1	1	12	12
	0	0	1	0	0	13	13
	0	0	1	0	1	14	14
	0	0	1	1	0	15	15
	0	0	1	1	1	16	16
	0	1	0	0	0	17	17
	0	1	0	0	1	18	18
	0	1	0	1	0	19	19
	0	1	0	1	1	20	20
	0	1	1	0	0	21	21
	0	1	1	0	1	22	22
	0	1	1	1	0	23	23
	0	1	1	1	1	24	24
	1	0	0	0	0	25	25
	1	0	0	0	1	26	26
	1	0	0	1	0	27	27
	1	0	0	1	1	28	28
	1	0	1	0	0	29	29
	1	0	1	0	1	30	30
	1	0	1	1	0	31	31
	1	0	1	1	1	32	32
	1	1	0	0	0	33	33
	1	1	0	0	1	34	34
	1	1	0	1	0	35	35
	1	1	0	1	1	36	36
	1	1	1	0	0	37	37
	1	1	1	0	1	38Note	38
	1	1	1	1	0	39Note	39
	1	1	1	1	1	40Note	40

Note: When the total number of digits and segments together exceeds 53, the digits will have the priority.

Format of Display Mode Register 0 (2/2)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
DSPM0	KSF	DSPM06	DSPM05	SEGS4	SEGS3	SEGS2	SEGS1	SEGS0	FFA0H	00H	R/W Note 1

R/W	DSPM05	Display mode setting
	0	Display mode 1 (Segment/character type)
	1	Display mode 2 (Type in which a segment spans two or more grids.)

R/W	DSPM06	Subsystem clock noise eliminator mode setting Note 2
	0	2.5 MHz < f_X ≤ 5.0 MHz
	1	1.25 MHz ≤ f_X ≤ 2.5 MHz Note 3

R	KSF	Timing state
	0	Display timing
	1	Key scan timing

Notes: 1. Bit 7 (KSF) is a read-only bit.
2. Set the values according to the main system clock oscillation frequency (f_X) used. The noise eliminator is effective during FIP display operations.
3. If the f_X selected is between 1.25 MHz and 2.5 MHz, set DSPM06 to 1 prior to FIP display.

Caution: When a main system clock frequency below 1.25 MHz is selected and the FIP controller/driver is used, make sure to use the main system clock for watch timer counting by setting TCL24 to 0.

Format of Display Mode Register 1

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
DSPM1	DIGS3	DIGS2	DIGS1	DIGS0	DIMS3	DIMS2	DIMS1	DIMS0	FFA1H	00H	R/W

DIMS0	Display mode cycle setting
0	1024/f_X is 1 display cycle. (1 display cycle = 204.8 μs when operated at 5.0 MHz)
1	2048/f_X is 1 display cycle. (1 display cycle = 409.6 μs when operated at 5.0 MHz)

DIMS3	DIMS2	DIMS1	FIP output signal cut width
0	0	0	1/16
0	0	1	2/16
0	1	0	4/16
0	1	1	6/16
1	0	0	8/16
1	0	1	10/16
1	1	0	12/16
1	1	1	14/16

DIGS3	DIGS2	DIGS1	DIGS0	Display digit (Display mode 1) DSPM05 = 0	Display pattern (Display mode 2) DSPM05 = 1
0	0	0	0	Display stopped (static display)Note	Display stopped (static display)Note
0	0	0	1	2 digits	2 patterns
0	0	1	0	3 digits	3 patterns
0	0	1	1	4 digits	4 patterns
0	1	0	0	5 digits	5 patterns
0	1	0	1	6 digits	6 patterns
0	1	1	0	7 digits	7 patterns
0	1	1	1	8 digits	8 patterns
1	0	0	0	9 digits	9 patterns
1	0	0	1	10 digits	10 patterns
1	0	1	0	11 digits	11 patterns
1	0	1	1	12 digits	12 patterns
1	1	0	0	13 digits	13 patterns
1	1	0	1	14 digits	14 patterns
1	1	1	0	15 digits	15 patterns
1	1	1	1	16 digits	16 patterns

Note: Static display is possible when display stop is selected, by manipulating the port output latch.

Remarks: f_X: Main system clock oscillation frequency
DSPM05: Bit 5 of the display mode register 0 (DSPM0)

Format of Display Mode Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
DSPM2	0	0	USEG5	USEG4	USEG3	USEG2	USEG1	USEG0	FFA2H	00H	R/W

USEG5	USEG4	USEG3	USEG2	USEG1	USEG0	Number of mask bits to be written
0	0	0	0	0	0	None
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
0	0	0	1	0	0	4
0	0	0	1	0	1	5
0	0	0	1	1	0	6
0	0	0	1	1	1	7
0	0	1	0	0	0	8
0	0	1	0	0	1	9
0	0	1	0	1	0	10
0	0	1	0	1	1	11
0	0	1	1	0	0	12
0	0	1	1	0	1	13
0	0	1	1	1	0	14
0	0	1	1	1	1	15
0	1	0	0	0	0	16
0	1	0	0	0	1	17
0	1	0	0	1	0	18
0	1	0	0	1	1	19
0	1	0	1	0	0	20
0	1	0	1	0	1	21
0	1	0	1	1	0	22
0	1	0	1	1	1	23
0	1	1	0	0	0	24
0	1	1	0	0	1	25
0	1	1	0	1	0	26
0	1	1	0	1	1	27
0	1	1	1	0	0	28
0	1	1	1	0	1	29
0	1	1	1	1	0	30
0	1	1	1	1	1	31
1	0	0	0	0	0	32
1	0	0	0	0	1	33
1	0	0	0	1	0	34
1	0	0	0	1	1	35
1	0	0	1	0	0	36
1	0	0	1	0	1	37
1	0	0	1	1	0	38
1	0	0	1	1	1	39
Settings other than above are prohibited.						

(13) Registers controlling interrupt function

A total of 15 interrupt sources are provided, including non-maskable, maskable, and software interrupts.

Table 6-6. Interrupt Source List

Interrupt Type	Default Priority Note	Interrupt Source		Internal/ External	Vector Table Address
		Name	Trigger		
Non-maskable	—	RESET	Low voltage level	External	0000H
		INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)		
	1	INTP0	Pin input edge detection	External	0006H
	2	INTP1			0008H
	3	INTP2			000AH
	4	INTP3			000CH
	5	INTCSI0	End of serial interface channel 0 transfer	Internal	000EH
	6	INTCSI1	End of serial interface channel 1 transfer		0010H
	7	INTTM3	Reference time interval signal from watch timer		0012H
	8	INTTM0	Generation of 16-bit timer/event counter match signal		0014H
	9	INTTM1	Generation of 8-bit timer/event counter 1 match signal		0016H
	10	INTTM2	Generation of 8-bit timer/event counter 2 match signal		0018H
	11	INTAD	End of A/D converter conversion		001AH
	12	INTKS	Key scan timing from FIP controller/driver		001CH
Software	—	BRK	BRK instruction execution	—	003EH

Note: Default priorities are intended for two or more simultaneously generated maskable interrupt requests. 0 is the highest priority and 12 is the lowest priority.

The following table gives a listing of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 6-7. Interrupt Sources and Flags

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
		Register		Register		Register
INTWDT	TMIF4	IF0L	TMMK4	MK0L	TMPR4	PR0L
INTP0	PIF0		PMK0		PPR0	
INTP1	PIF1		PMK1		PPR1	
INTP2	PIF2		PMK2		PPR2	
INTP3	PIF3		PMK3		PPR3	
INTCSI0	CSIIF0		CSIMK0		CSIPR0	
INTCSI1	CSIIF1		CSIMK1		CSIPR1	
INTTM3	TMIF3		TMMK3		TMPR3	
INTTM0	TMIF0	IF0H	TMMK0	MK0H	TMPR0	PR0H
INTTM1	TMIF1		TMMK1		TMPR1	
INTTM2	TMIF2		TMMK2		TMPR2	
INTAD	ADIF		ADMK		ADPR	
INTKS	KSIF		KSMK		KSPR	

The following six types of registers control the interrupt functions:

- Interrupt request flag registers (IF0L, IF0H)
- Interrupt mask flag registers (MK0L, MK0H)
- Priority specification flag registers (PR0L, PR0H)
- External interrupt mode register (INTM0)
- Sampling clock select register (SCS)
- Program status word (PSW)

Format of Interrupt Request Flag Registers

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
IF0L	TMIF3	CSIIF1	CSIIF0	PIF3	PIF2	PIF1	PIF0	TMIF4	FFE0H	00H	R/W
IF0H	0	0	WTIF[Note]	KSIF	ADIF	TMIF2	TMIF1	TMIF0	FFE1H	00H	R/W

xxIF	Interrupt request flag
0	No interrupt request signal
1	Interrupt request signal is generated; interrupt request state

Note: WTIF is a test input flag. A vectored interrupt request is not generated.

Cautions: 1. The TMIF4 flag is R/W enabled only when a watchdog timer is used as an interval timer. If a watchdog timer is used in watchdog timer mode 1, set the TMIF4 flag to 0.

2. Always set bits 6 and 7 of IF0H to 0.

Format of Interrupt Mask Flag Registers

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
MK0L	TMMK3	CSIMK1	CSIMK0	PMK3	PMK2	PMK1	PMK0	TMMK4	FFE4H	FFH	R/W
MK0H	1	1	WTMK[Note]	KSMK	ADMK	TMMK2	TMMK1	TMMK0	FFE5H	FFH	R/W

xxMK	Interrupt serving and Standby mode control
0	Interrupt serving enabled, Standby mode release enabled
1	Interrupt serving disabled, Standby mode release disabled

Note: WTMK controls the Standby mode release enable/disable. This bit does not control the interrupt function.

Cautions: 1. If the TMMK4 flag is read when a watchdog timer is used in watchdog timer mode 1, the MK0 value becomes undefined.

2. Because port 0 has an alternate function as the external interrupt request input, when the output level is changed by specifying the output mode of the port function, an interrupt request flag is set. Therefore, 1 should be set in the interrupt mask flag before using the output mode.

3. Always set bits 6 and 7 of MK0H to 1.

Format of Priority Specification Flag Registers

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
PR0L	TMPR3	CSIPR1	CSIPR0	PPR3	PPR2	PPR1	PPR0	TMPR4	FFE8H	FFH	R/W

	7	6	5	<4>	<3>	<2>	<1>	<0>			
PR0H	1	1	1	KSPR	ADPR	TMPR2	TMPR1	TMPR0	FFE9H	FFH	R/W

xxPR	Priority level selection
0	High priority level
1	Low priority level

Cautions: 1. When a watchdog timer is used in watchdog timer mode 1, set 1 in the TMPR4 flag.

2. Always set bits 5 through 7 of PR0H to 1.

Format of External Interrupt Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
INTM0	ES31	ES30	ES21	ES20	ES11	ES10	0	0	FFECH	00H	R/W

ES11	ES10	INTP0 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES21	ES20	INTP1 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES31	ES30	INTP2 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

Caution: Before setting the valid edges of the INTP0/TI0/P00 pins, stop the timer operation by clearing bits 1 to 3 (TMC01 to TMC03) of the 16-bit timer mode control register (TMC0) to 0, 0, 0.

Remarks: The INTP0 pin also functions as TI0/P00.

The valid edge of INTP3 is fixed at the falling edge.

Format of Sampling Clock Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
SCS	0	0	0	0	0	0	SCS1	SCS0	FF47H	00H	R/W

SCS1	SCS0	INTP0 sampling clock selection
0	0	$f_X/2^{N+1}$
0	1	Setting prohibited
1	0	$f_X/2^6$ (78.1 kHz)
1	1	$f_X/2^7$ (39.1 kHz)

Caution: $f_X/2^{N+1}$ is a clock to be supplied to the CPU, and $f_X/2^6$ and $f_X/2^7$ are clocks to be supplied to the peripheral hardware. $f_X/2^{N+1}$ stops in the HALT mode.

Remarks: N : Value (N = 0 to 4) at bits 0 to 2 (PCC0 to PCC2) of processor clock control register (PCC)
f_X : Main system clock oscillation frequency
Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of Program Status Word

Symbol	7	6	5	4	3	2	1	0	After Reset
PSW	IE	Z	RBS1	AC	RBS0	0	ISP	CY	02H

Used when normal instruction is executed

ISP	Priority of interrupt currently serviced
0	Interrupt with higher priority is serviced (interrupt with lower priority is disabled)
1	Interrupt is not accepted, or interrupt with lower priority is serviced (all maskable interrupts are enabled)

IE	Enables/disables accepting interrupt request
0	Disables
1	Enables

(14) Registers controlling test function

The names of the test input flag and test mask flag corresponding to the test input signal name are as follows.

Test Input Sources

Test Input Signal Name	Test Input Flag	Test Mask Flag
INTWT	WTIF	WTMK

The following two registers control the test function:

- Interrupt request flag register 0H (IF0H)
- Interrupt mask flag register 0H (MK0H)

Format of Interrupt Request Flag Register 0H

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
IF0H	0	0	WTIF	KSIF	ADIF	TMIF2	TMIF1	TMIF0	FFE1H	00H	R/W

WTIF	Watch timer overflow detection flag
0	Non-detection
1	Detection

Format of Interrupt Mask Flag Register 0H

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
MK0H	1	1	WTMK	KSMK	ADMK	TMMK2	TMMK1	TMMK0	FFE5H	FFH	R/W

WTMK	Standby mode control by watch timer
0	Standby mode release enable
1	Standby mode release disable

(15) Register controlling standby function

The standby function is intended to decrease the power consumption of the system. The following two modes are available: HALT and STOP.

When MCU is released from the STOP mode, a wait time is required for the crystal to resume oscillations. The wait time is controlled by the following register:

- Oscillation stabilization time select register (OSTS)

Format of Oscillation Stabilization Time Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0	FFFAH	04H	R/W

OSTS2	OSTS1	OSTS0	Selection of oscillation stabilization time after STOP mode is released
0	0	0	$2^{12}/f_X$ (819 μs)
0	0	1	$2^{14}/f_X$ (3.28 ms)
0	1	0	$2^{15}/f_X$ (6.55 ms)
0	1	1	$2^{16}/f_X$ (13.1 ms)
1	0	0	$2^{17}/f_X$ (26.2 ms)
Settings other than above are prohibited			

Remarks: f_X: Main system clock frequency

Values in parentheses apply to operation with f_X = 5.0 MHz.

The operation status in HALT mode is described below.

HALT Mode Operating Status

HALT Mode Setting / Item		When HALT Instruction Is Executed During Main System Clock Oscillation		When HALT Instruction Is Executed During Subsystem Clock Oscillation	
		Without Subsystem Clock Note 1	With Subsystem Clock Note 2	When Main System Clock Oscillation Continues	When Main System Clock Oscillation Stops
Clock generator		Both the main system clock and subsystem clock can be oscillated. Clock supply to the CPU stops.			
CPU		Operation stops			
Port (output latch)		Status before the HALT instruction execution is held			
16-bit timer/event counter		Operation enabled			Operation stops
8-bit timer/event counter					Operation is enabled when TI1 and TI2 are selected for the count clock.
Watchdog timer					
A/D converter					Operation stops
					Operation stops
Watch timer		Operation is enabled when $fx/2^8$ is selected for the count clock.	Operation enabled		Operation is enabled when f_{XT} is selected for the count clock.
FIP controller/driver		Operation disabled			
Serial Interface	Other than automatic transmit/ receive function	Operation enabled			Operation is enabled when external SCK is selected.
	Automatic transmit/ receive function	Operation stops			
External interrupt	INTP0	Operation is enabled when the clocks ($fx/2^6$ and $fx/2^7$) for the peripheral hardware are selected as sampling clocks.			Operation stops
	INTP1 to INTP3	Operation enabled			

Notes: 1. Including the case where an external clock is not supplied as the subsystem clock

2. Including the case where an external clock is supplied as the subsystem clock

The operation status in the STOP mode is shown below.

STOP Mode Operating Status

Item \ STOP Mode Setting		With Subsystem Clock	Without Subsystem Clock
Clock generator		Only the main system clock stops oscillation.	
CPU		Operation stops	
Output port (output latch)		Status before the STOP mode setting is held	
16-bit timer/event counter		Operation stops	
8-bit timer/event counter		Operation is enabled only when TI1 and TI2 are selected for the count clock.	
Watchdog timer		Operation stops	
A/D converter			
Watch timer		Operation is enabled only when f_{XT} is selected for the count clock.	Operation stops
FIP controller/driver		Operation disabled	
Serial interface	Other than automatic transmit/receive function	Operation is enabled only when an external input clock is selected as the serial clock.	
	Automatic transmit/ receive function	Operation stops	
External interrupt	INTP0	Operation disabled	
	INTP1 to INTP3	Operation enabled	

Cautions: 1. When the STOP mode is set, the X2 pin is internally connected to V_{DD} via a pull-up resistor to minimize the leakage current at the crystal oscillator. Thus, do not use the STOP mode in a system where an external clock is used for the main system clock.

2. Because the interrupt request signal is used to release the Standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the Standby mode is immediately released if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction. After the wait set using the oscillation stabilization time select register (OSTS), the operating mode is set.

(16) Reset function

The following two operations can be used to generate a reset signal.

- External reset input via the $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer in Watchdog Timer mode

Table 6-8. Hardware Status After Reset (1/2)

Hardware		Status After Reset
Program counter (PC)[Note 1]		The contents of reset vector tables (0000H and 0001H) are set
Stack pointer (SP)		Undefined
Program status word (PSW)		02H
RAM	Data memory	Undefined[Note 2]
	General register	Undefined[Note 2]
Port (Output latch)	Ports 0 to 3, ports 7 to 12 (P0 toP3, P7 to P12)	00H
Port mode registers	(PM0, PM7)	1FH
	(PM1, PM2, PM3, PM10, PM11, PM12)	FFH
Pull-up resistor option register (PUO)		00H
Processor clock control register (PCC)		04H
Internal memory size switching register (IMS)		**Note 3**
Internal expansion RAM size switching register (IXS)		**Note 3**
Oscillation stabilization time select register (OSTS)		04H
16-bit timer/event counter	Timer register (TM0)	00H
	Compare register (CR00)	Undefined
	Capture register (CR01)	Undefined
	Clock select register (TCL0)	00H
	Mode control register (TMC0)	00H
	Output control register (TOC0)	00H
8-bit timer/event counter	Timer registers (TM1, TM2)	00H
	Compare registers (CR10, CR20)	Undefined
	Clock select register (TCL1)	00H
	Mode control registers (TMC1, TMC2)	00H
	Output control register (TOC1)	00H
Watch timer	Clock select register (TCL2)	00H
Watchdog timer		
	Mode register (WDTM)	00H

Table 6-8. Hardware Status After Reset (2/2)

Hardware		Status After Reset
Serial interface	Clock select register (TCL3)	88H
	Shift registers (SIO0, SIO1)	Undefined
	Mode registers (CSIM0, CSIM1)	00H
	Serial bus interface control register (SBIC)	00H
	Slave address register (SVA)	Undefined
	Automatic data transmit/receive control register (ADTC)	00H
	Automatic data transmit/receive address pointer (ADTP)	00H
	Automatic data transmit/receive interval specification register (ADTI)	00H
	Interrupt timing specification register (SINT)	00H
A/D converter	Mode register (ADM)	01H
	Conversion result register (ADCR)	Undefined
	Input select register (ADIS)	00H
FIP controller/driver	Display mode register 0 (DSPM0)	00H
	Display mode register 1 (DSPM1)	00H
	Display mode register 2 (DSPM2)	00H
Interrupt	Request flag registers (IF0L, IF0H)	00H
	Mask flag registers (MK0L, MK0H)	FFH
	Priority specification flag registers (PR0L, PR0H)	FFH
	External interrupt mode register (INTM0)	00H
	Sampling clock select register (SCS)	00H

Notes: 1. During reset input or an oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after a reset.

2. If the reset is applied in the Standby mode, the status before reset will be held after reset.

3. The after-reset values of the internal memory size switching register (IMS) and internal expansion RAM size switching register (IXS) depend on each subseries member as shown below.

	μPD780204	μPD780205	μPD780206	μPD780208	μPD78P0208
IMS	C8H	CAH	CCH	CFH	CFH
IXS	None		0AH		

(17) Register controlling internal memory capacity

The μPD78P0208 (PROM version) allows users to select the internal memory capacity.
The following register is used to control the internal memory capacity:

- Internal memory size switching register (IMS)

Format of Internal Memory Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

ROM3	ROM2	ROM1	ROM0	Internal ROM capacity selection
1	0	0	0	32K
1	0	1	0	40K
1	1	0	0	48K
1	1	1	1	60K
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Internal high-speed RAM capacity selection
1	1	0	1024 bytes
Other than above			Setting prohibited

To map the memory of the μPD78P0208 identically to that of a mask ROM version, the value at the time the mask ROM version is reset must be set. The following table shows the set value of IMS.

Set Value of Internal Memory Size Switching Register

Target Mask ROM Version	Set Value of IMS
μPD780204	C8H
μPD780205	CAH
μPD780206	CCH
μPD780208	CFH

Caution: When using a mask ROM version, do not set a value other than those shown in the table above to IMS.

(18) Register controlling internal expansion RAM capacity

The μPD78P0208 (PROM version) allows users to select the internal expansion RAM capacity.
The following register is used to control the internal expansion RAM capacity:

- Internal expansion RAM size switching register (IXS)

Format of Internal Expansion RAM Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IXS	0	0	0	0	IX RAM3	IX RAM2	IX RAM1	IX RAM0	FFF4H	0AH	W

IX RAM3	IX RAM2	IX RAM1	IX RAM0	Internal expansion RAM capacity selection
1	0	1	0	1024 bytes
1	1	0	0	No internal expansion RAM (0 bytes)
Other than above				Setting prohibited

The following table shows the set value of IXS by which to map the internal expansion RAM of the μPD78P0208 identically to that of a mask ROM version.

Set Value of Internal Expansion RAM Size Switching Register

Target Mask ROM Version	Set Value of IXS
μPD780204 μPD780205	0CH
μPD780206 μPD780208	0AH

IXS is not incorporated in the μPD780204 and μPD780205.
However, if a write instruction to IXS is executed in the μPD780204 or the μPD780205, the operations are not affected.

Cautions: 1. The internal expansion RAM size switching register (IXS) is incorporated only in the μPD780206, μPD780208, and μPD78P0208.

2. When using a mask ROM version, do not set a value other than those shown above to IXS.

6.3 μPD780024 and 780034 Subseries

6.3.1 Documentation Reference Information

Device Series Number	User's Manual Number	Date Published
μPD780024, 780034	U12022EJ4V0UM00	January 1998

Caution: The user should check the current User's Manual with the information in this section to be sure of having the most up-to-date information.

6.3.2 Device Series Differences

Device Series Number	ROM and RAM Differences		Number of Serial Channels
	ROM Size	RAM Size	
μPD780024, 780024Y	8K/16K/24K/32K	512/1K	3 Note
μPD780034, 780034Y			

Note: Even though each product has three serial channels, there is a difference in the serial interface type between non-Y subseries products (μPD780024/34) and Y subseries products (μPD780024Y/34Y). See "**Differences Between μPD780024/34 and μPD780024Y/34Y subseries**" in **(9) Registers controlling serial interface (UART0)**.

General Programmer's Note

The NEC C-compiler and the NEC Assembler are capable of recognizing certain symbolic SFR bit names. These special bit names are identified in the user manual in one of the four ways shown below:

1. <7>
2. (7)
3. ⑦
4. 7

Example:

	<7>	<6>	<5>	<4>	3	2	1	0
PCC	MCC	FRC	CLS	CSS	0	PCC2	PCC1	PCC0

If a bit number has one of the four symbols around it, the NEC software will recognize the associated symbolic bit name. For example to set bit 7, the user can write the code in two ways:

```
1.    SET1    MCC
2.    SET1    PCC.7
```

Alternatively since bit 2 does not have any of the four symbols around it, the user can only set this bit as follows:

```
1.    SET1    PCC.2
```

Note: The attempt to employ a symbolic name of bit-2 (PCC2) will return an error. Thus the use of instruction

```
SET1    PCC2
```

is improper since neither the NEC C-compiler nor the NEC Assembler recognizes this symbolic name and will generate an error.

6.3.3 Memory Address Space

Each model in the μPD780024/24Y and 780034/34Y Subseries can access a memory space of 64K. Figures 6-12 through 6-15 show memory maps of the respective models.

Figure 6-12. Memory Map (μPD780021/21Y, 780031/31Y)

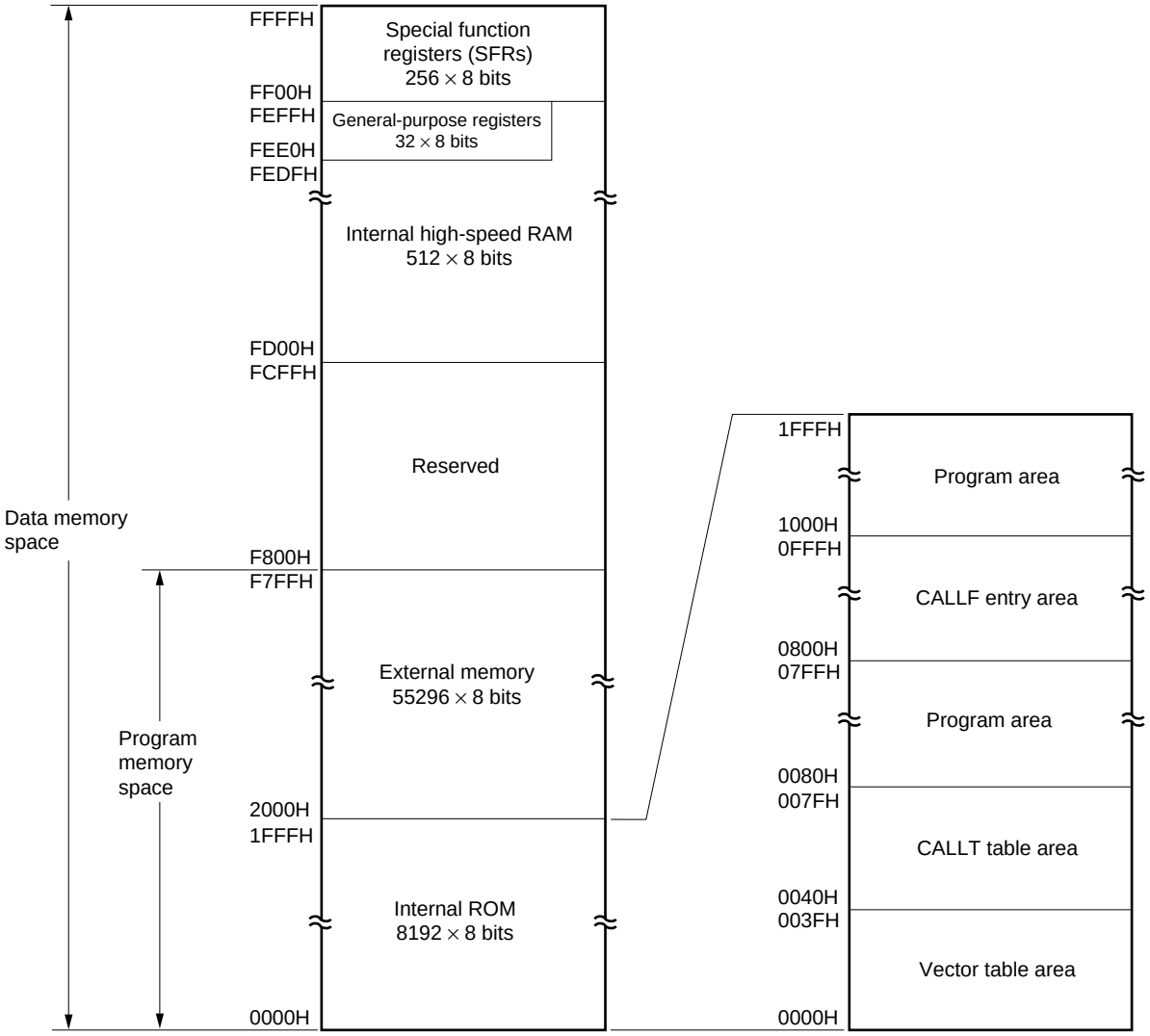


Figure 6-13. Memory Map (μPD780022/22Y, 780032/32Y)

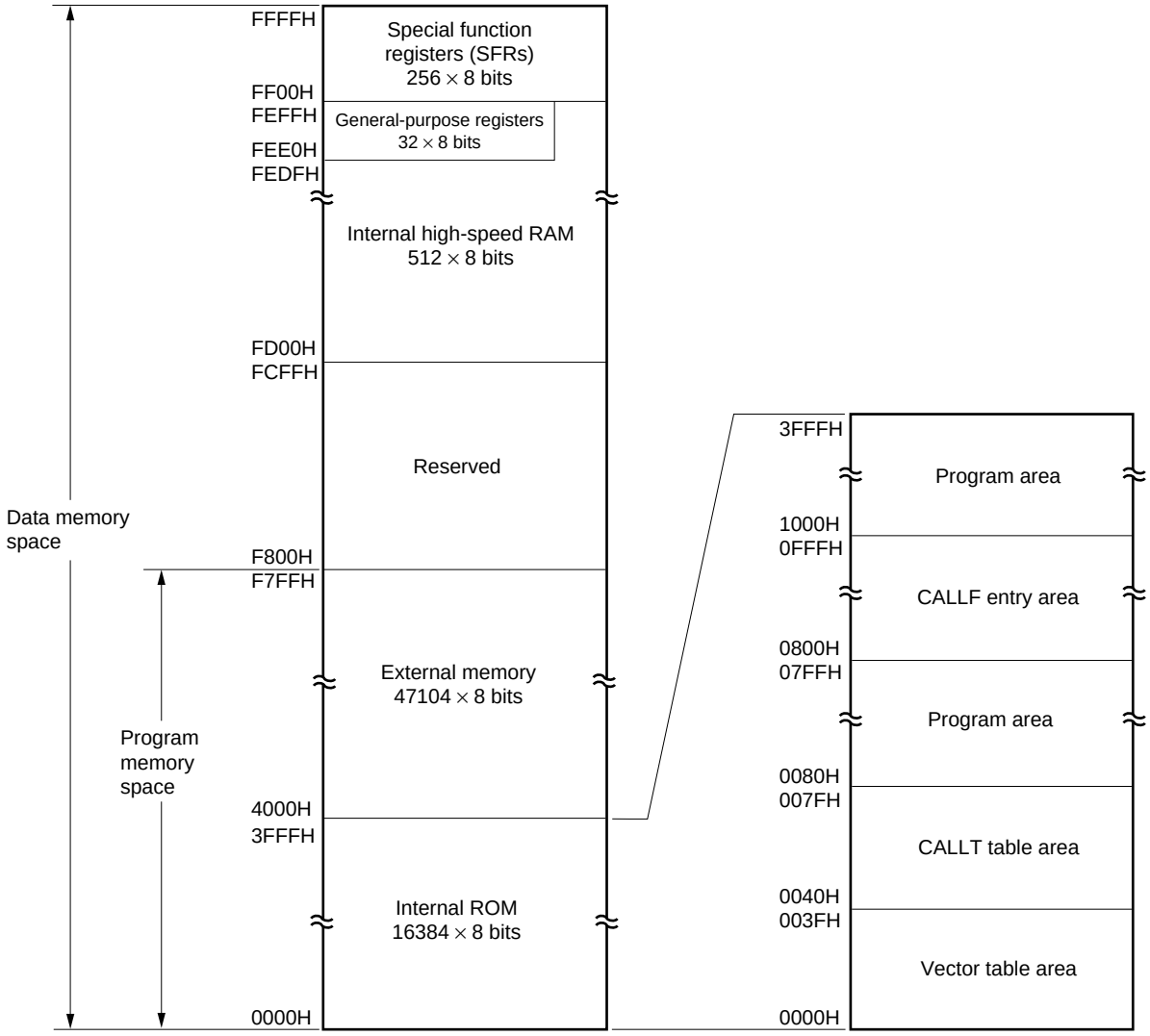


Figure 6-14. Memory Map (μPD780023/23Y, 780033/33Y)

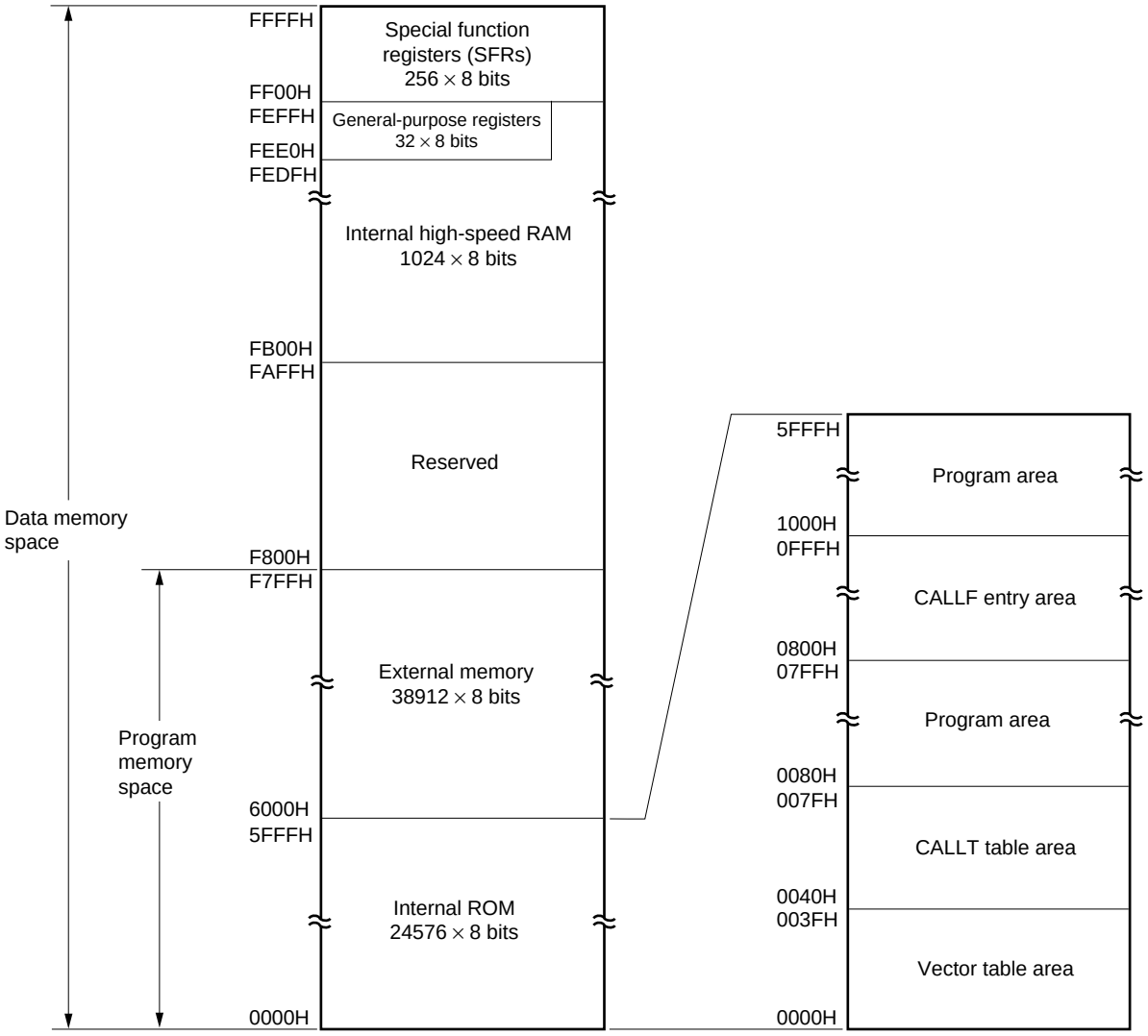
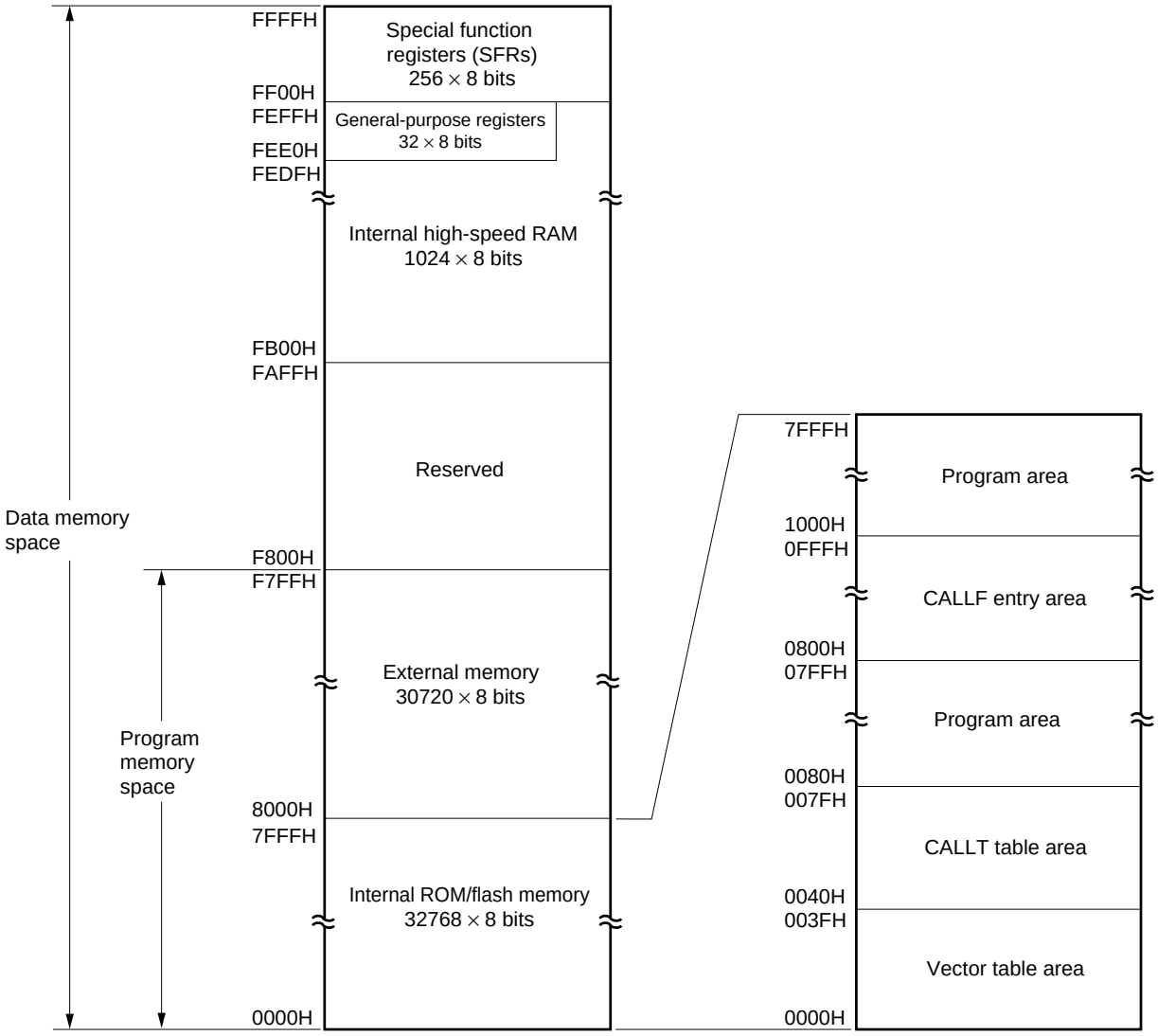


Figure 6-15. Memory Map (μPD780024/24Y, 780034/34Y, 78F0034/34Y)



6.3.4 Special Function Registers (SFRs)

Table 6-9. Special Function Register List (μPD780024/24Y and 780034/34Y Subseries) (1/3)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulatable Bit Unit			After Reset
					1 Bit	8 Bits	16 Bits	
FF00H	Port 0	P0		R/W	√	√	–	00H
FF01H	Port 1	P1		R	√	√	–	
FF02H	Port 2	P2		R/W	√	√	–	
FF03H	Port 3	P3			√	√	–	
FF04H	Port 4	P4			√	√	–	
FF05H	Port 5	P5			√	√	–	
FF06H	Port 6	P6			√	√	–	
FF07H	Port 7	P7			√	√	–	
FF0AH FF0BH	Capture/compare register 00	CR00			–	–	√	Undefined
FF0CH FF0DH	Capture/compare register 01	CR01			–	–	√	
FF0EH FF0FH	16-bit timer register	TM0		R	–	–	√	0000H
FF10H	8-bit compare register 50	CR50		R/W	–	√	–	Undefined
FF11H	8-bit compare register 51	CR51			–	√	–	
FF12H	8-bit counter 50	TM5	TM50	R	–	√	√	00H
FF13H	8-bit counter 51		TM51		–	√		
FF16H FF17H	A/D conversion result register 0	ADCR0			–	√ **Note 1**	√ **Note 2**	
FF18H	Transmit shift register	TXS0		W	–	√	–	FFH
	Receive buffer register	RXB0		R	–	√	–	
FF1AH	Serial I/O shift register 30	SIO30		R/W	–	√	–	Undefined
FF1BH	Serial I/O shift register 31 Note 3	SIO31			–	√	–	
FF1FH	IIC shift register Note 4	IIC0			–	√	–	00H

Notes: 1. μPD780024, 780024Y Subseries only
2. μPD780034, 780034Y Subseries only, 16-bit access possible
3. μPD780024, 780034 Subseries only
4. μPD780024Y, 780034Y Subseries only

Table 6-9. Special Function Register List (μPD780024/24Y and 780034/34Y Subseries) (2/3)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulatable Bit Unit			After Reset
				1 Bit	8 Bits	16 Bits	
FF20H	Port mode register 0	PM0	R/W	√	√	–	FFH
FF22H	Port mode register 2	PM2		√	√	–	
FF23H	Port mode register 3	PM3		√	√	–	
FF24H	Port mode register 4	PM4		√	√	–	
FF25H	Port mode register 5	PM5		√	√	–	
FF26H	Port mode register 6	PM6		√	√	–	
FF27H	Port mode register 7	PM7		√	√	–	
FF30H	Pull-up resistor option register 0	PU0		√	√	–	00H
FF32H	Pull-up resistor option register 2	PU2		√	√	–	
FF33H	Pull-up resistor option register 3	PU3		√	√	–	
FF34H	Pull-up resistor option register 4	PU4		√	√	–	
FF35H	Pull-up resistor option register 5	PU5		√	√	–	
FF36H	Pull-up resistor option register 6	PU6		√	√	–	
FF37H	Pull-up resistor option register 7	PU7		√	√	–	
FF40H	Clock output selection register	CKS		√	√	–	
FF41H	Watch timer mode control register	WTM		√	√	–	
FF42H	Watchdog timer clock selection register	WDCS		–	√	–	
FF47H	Memory expansion mode register	MEM		√	√	–	
FF48H	External interrupt rising edge enable register	EGP		√	√	–	
FF49H	External interrupt falling edge enable register	EGN		√	√	–	
FF60H	16-bit timer mode control register	TMC0		√	√	–	
FF61H	Prescaler mode register	PRM0		–	√	–	
FF62H	Capture/compare control register 0	CRC0		√	√	–	
FF63H	16-bit timer output control register 0	TOC0		√	√	–	
FF70H	8-bit timer mode control register 50	TMC50		√	√	–	04H
FF71H	Timer clock selection register 50	TCL50		–	√	–	00H
FF78H	8-bit timer mode control register 51	TMC51		√	√	–	04H
FF79H	Timer clock selection register 51	TCL51		–	√	–	00H
FF80H	A/D converter mode register	ADM0		√	√	–	
FF81H	Analog input channel specification register	ADS0		–	√	–	
FFA0H	Asynchronous serial interface mode register	ASIM0		√	√	–	
FFA1H	Asynchronous serial interface status register	ASIS0	R	–	√	–	
FFA2H	Baud rate generator control register	BRGC0	R/W	–	√	–	

Table 6-9. Special Function Register List (μPD780024/24Y and 780034/34Y Subseries) (3/3)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulatable Bit Unit			After Reset
					1 Bit	8 Bits	16 Bits	
FFA8H	IIC control register Note 1	IICC0		R/W	√	√	–	00H
FFA9H	IIC status register Note 1	IICS0		R	√	√	–	
FFAAH	IIC clock selection register Note 1	IICCL0		R/W	√	√	–	
FFABH	Slave address register Note 1	SVA0			–	√	–	
FFB0H	Serial operation mode register 30	CSIM30			√	√	–	
FFB8H	Serial operation mode register 31 Note 2	CSIM31			√	√	–	
FFD0H to FFDFH	External access area Note 3				√	√	–	Undefined
FFE0H	Interrupt request flag register 0L	IF0	IF0L		√	√	√	00H
FFE1H	Interrupt request flag register 0H		IF0H		√	√		
FFE2H	Interrupt request flag register 1L	IF1L			√	√	–	
FFE4H	Interrupt mask flag register 0L	MK0	MK0L		√	√	√	FFH
FFE5H	Interrupt mask flag register 0H		MK0H		√	√		
FFE6H	Interrupt mask flag register 1L	MK1L			√	√	–	
FFE8H	Priority specification flag register 0L	PR0	PR0L		√	√	√	
FFE9H	Priority specification flag register 0H		PR0H		√	√		
FFEAH	Priority specification flag register 1L	PR1L			√	√	–	
FFF0H	Internal memory size switching register	IMS			–	√	–	CFH
FFF8H	Memory expansion wait setting register	MM			√	√	–	10H
FFF9H	Watchdog timer mode register	WDTM			√	√	–	00H
FFFAH	Oscillation stabilization time select register	OSTS			–	√	–	04H
FFFBH	Processor clock control register	PCC			√	√	–	

Notes: 1. μPD780024Y, 780034Y Subseries only
2. μPD780024, 780034 Subseries only
3. The external access area cannot be accessed by SFR addressing. Access it with the direct addressing method.

(1) Registers controlling port functions

The following two types of registers control the ports:

- Port mode registers (PM0, PM2 to PM7)
- Pull-up resistor option registers (PU0, PU2 to PU7)

Format of Port Mode Registers

Address: FF20H After Reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM0	1	1	1	1	PM03	PM02	PM01	PM00

Address: FF22H After Reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	1	1	PM25	PM24	PM23	PM22	PM21	PM20

Address: FF23H After Reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	PM36	PM35	PM34	PM33	PM32	PM31	PM30

Address: FF24H After Reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM4	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40

Address: FF25H After Reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM5	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50

Address: FF26H After Reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM6	PM67	PM66	PM65	PM64	1	1	1	1

Address: FF27H After Reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM7	1	1	PM75	PM74	PM73	PM72	PM71	PM70

PMmn	Pmn Pin Input/Output Mode Select (m = 0, 2 to 7: n = 0 to 7)
0	Output Mode (Output buffer on)
1	Input Mode (Output buffer off)

Cautions: 1. Pins P10 and P17 are input-only pins.

2. As port 0 has an alternate function as an external interrupt input, when the port function output mode is specified and the output level is changed, the interrupt request flag is set. When the output mode is used, therefore, the interrupt mask flag should be set to 1 beforehand.

Format of Pull-Up Resistor Option Registers

Address: FF30H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PU0	0	0	0	0	PU03	PU02	PU01	PU00

Address: FF32H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PU2	0	0	PU25	PU24	PU23	PU22	PU21	PU20

Address: FF33H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PU3	0	PU36	PU35	PU34	0	0	0	0

Address: FF34H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PU4	PU47	PU46	PU45	PU44	PU43	PU42	PU41	PU40

Address: FF35H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PU5	PU57	PU56	PU55	PU54	PU53	PU52	PU51	PU50

Address: FF36H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PU6	PU67	PU66	PU65	PU64	0	0	0	0

Address: FF37H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PU7	0	0	PU75	PU74	PU73	PU72	PU71	PU70

PUmn	Pmn Pin Internal Pull-up Resistor Select (m = 0, 2 to 7: n = 0 to 7)
0	On-chip pull-up resistor not used
1	On-chip pull-up resistor used

Cautions: 1. The P10 and P17 pins do not incorporate a pull-up resistor.

2. When ports 4 and 6 pins are used as alternate function pins, a pull-up resistor cannot be used even if 1 is set in PUmn (m = 0, 2 to 7: n = 0 to 7).

3. Pins P30 to P33 (in μPD780024Y and 780034Y Subseries, P30 and P31 pins) can be used with a pull-up resistor by the mask option only in a mask ROM version.

(2) Register controlling clock generator

The following register controls the clock generator:

- Processor clock control register (PCC)

Format of Processor Clock Control Register

Address: FFFBH After Reset: 04H R/W Note 1

Symbol	<7>	<6>	<5>	<4>	3	2	1	0
PCC	MCC	FRC	CLS	CSS	0	PCC2	PCC1	PCC0

MCC	Main system clock oscillation control Note 2
0	Oscillation possible
1	Oscillation stopped

FRC	Subsystem clock feedback resistor select
0	Internal feedback resistor used
1	Internal feedback resistor not used

CLS	CPU clock status
0	Main system clock
1	Subsystem clock

CSS	PCC2	PCC1	PCC0	CPU clock (f_{CPU}) select
0	0	0	0	f_X
	0	0	1	$f_X/2$
	0	1	0	$f_X/2^2$
	0	1	1	$f_X/2^3$
	1	0	0	$f_X/2^4$
1	0	0	0	$f_{XT}/2$
	0	0	1	
	0	1	0	
	0	1	1	
	1	0	0	
Settings other than above are prohibited				

Notes: 1. Bit 5 is a read-only bit.

2. When the CPU is operating from the subsystem clock, MCC should be used to stop the main system clock oscillation. A STOP instruction should not be used.

Cautions: 1. Bit 3 must be set to 0.

2. When the external clock is input, MCC should not be set. This is because the X2 pin is connected to V_{DD1} via a pull-up resistor.

Remarks: f_X: Main system clock oscillation frequency

f_{XT}: Subsystem clock oscillation frequency

(3) Registers controlling 16-bit timer/event counter

The following five registers control the 16-bit timer/event counter:

- 16-bit timer mode control register (TMC0)
- Capture/compare control register (CRC0)
- 16-bit timer output control register (TOC0)
- Prescaler mode register 0 (PRM0)
- Port mode register 7 (PM7)
  - Refer to section (1) for the register format.

Format of 16-Bit Timer Mode Control Register

Address: FF60H After Reset: 00H R/W

Symbol	7	6	5	4	<3>	<2>	1	<0>
TMC0	0	0	0	0	TMC03	TMC02	TMC01	OVF0

TMC03	TMC02	TMC01	Operating mode and Clear mode selection	TO0 output timing selection	Interrupt request generation
0	0	0	Operation stop (TM0 cleared to 0)	No change	Not generated
0	0	1			
0	1	0	Free-running mode	Match between TM0 and CR00 or match between TM0 and CR01	Generated on match between TM0 and CR00, or match between TM0 and CR01
0	1	1		Match between TM0 and CR00, match between TM0 and CR01 or TI00 valid edge	
1	0	0	Clear and start on TI00 valid edge	—	
1	0	1			
1	1	0	Clear and start on match between TM0 and CR00	Match between TM0 and CR00 or match between TM0 and CR01	
1	1	1		Match between TM0 and CR00, match between TM0 and CR01 or TI00 valid edge	

OVF0	16-bit Timer Register Overflow Detection
0	Overflow not detected
1	Overflow detected

Cautions: 1. The 16-bit timer register (TM0) starts operation when a value other than 0, 0 is set to TMC02 and TMC03 (Operation Stop mode). To stop the operation, set TMC02 and TMC03 to 0, 0.

2. Timer operation must be stopped before writing to bits other than the OVF0 flag.

3. Set the valid edge of the TI00/TO0/P70 pin with prescaler mode register 0 (PRM0).

4. If Clear and Start mode on a match between TM0 and CR00 is selected, when the set value of CR00 is FFFFH and the TM0 value changes from FFFFH to 0000H, the OVF0 flag is set to 1.

Remarks: TO0: 16-bit timer/event counter output pin
TI00: 16-bit timer/event counter input pin
TM0: 16-bit timer register
CR00: Compare register 00
CR01: Compare register 01

Format of Capture/Compare Control Register 0

Address: FF62H After Reset: 04H R/W

Symbol	7	6	5	4	3	2	1	0
CRC0	0	0	0	0	0	CRC02	CRC01	CRC00

CRC02	CR01 operating mode selection
0	Operates as compare register
1	Operates as capture register

CRC01	CR00 capture trigger selection
0	Captures on valid edge of TI01n
1	Captures on valid edge of TI00n by reverse phase

CRC00	CR00n operating mode selection
0	Operates as compare register
1	Operates as capture register

Cautions 1. Timer operation must be stopped before setting CRC0.
2. When Clear and Start mode on a match between TM0 and CR00 is selected with the 16-bit timer mode control register (TMC0), CR00 should not be specified as a capture register.
3. If both the rising and falling edges have been selected as the valid edges of TI00, capture is not performed.

Format of 16-Bit Timer Output Control Register

Address: FF63H After Reset: 00H R/W

Symbol	7	<6>	<5>	4	<3>	<2>	1	<0>
TOC0	0	OSPT	OSPE	TOC04	LVS0	LVR0	TOC01	TOE0

OSPT	Control of one-shot pulse output trigger by software
0	One-shot pulse trigger not used
1	One-shot pulse trigger used

OSPE	One-shot pulse output control
0	Continuous pulse output
1	One-shot pulse output **Note**

TOC04	Timer output F/F control by match of CR01 and TM0
0	Inversion operation disabled
1	Inversion operation enabled

LVS0	LVR0	16-bit timer/event counter timer output F/F status setting
0	0	No change
0	1	Timer output F/F reset (to 0)
1	0	Timer output F/F set (to 1)
1	1	Setting prohibited

TOC01	Timer output F/F control by match of CR00 and TM0
0	Inversion operation disabled
1	Inversion operation enabled

TOE0	16-bit timer/event counter output control
0	Output disabled (Output set to level 0)
1	Output enabled

Note: One-shot pulse output operates normally only in the free-running mode.

Cautions: 1. Timer operation must be stopped before setting TOC0.

2. If LVS0 and LVR0 are read after data is set, they will be 0.

3. OSPT is cleared automatically after data setting, and will therefore be 0 if read.

Format of Prescaler Mode Register 0

Address: FF61H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PRM0	ES11	ES10	ES01	ES00	0	0	PRM01	PRM00

ES11	ES10	TI01 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES01	ES00	TI00 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

PRM01	PRM00	count clock selection
0	0	f_X (8.38 MHz)
0	1	$f_X/2^2$ (2.09 MHz)
1	0	$f_X/2^6$ (131 kHz)
1	1	TI00 valid edge

Cautions: 1. If the valid edge of TI00 is to be set to the count clock, do not set the Clear/Start mode and the capture trigger at the valid edge of TI00.
Moreover, do not use the P70/TI00/TO0 pins as timer outputs (TO0).

2. Always set data to PRM0 after stopping the timer operation.

3. If the TI00 or TI01 pin is at high level immediately after system reset, the rising edge is immediately detected after the rising edge or both the rising and falling edges are set as the valid edge(s) of the TI00 pin or TI01 pin to enable the operation of the 16-bit timer (TM0). Please be careful when pulling up the TI00 pin or the TI01 pin. However, when re-enabling operation after the operation has been stopped once, the rising edge is not detected.

Remarks: f_X: Main system clock oscillation frequency
TI00, TI01: 16-bit timer/event counter input pins
Values in parentheses are for operation with f_X = 8.38 MHz.

(4) Registers controlling 8-bit timer/event counter

The following three types of registers control the 8-bit timer/event counters:

- Timer clock select registers TCL50 & TCL51
- 8-bit timer mode control register 5n (TMC5n)
- Port mode register 7 (PM7)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 50

Address: FF71H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TCL50	0	0	0	0	0	TCL502	TCL501	TCL500

TCL502	TCL501	TCL500	Count clock selection
0	0	0	TI50 Falling edge
0	0	1	TI50 Rising edge
0	1	0	f_X (8.38 MHz)
0	1	1	$f_X/2^2$ (2.09 MHz)
1	0	0	$f_X/2^4$ (523 kHz)
1	0	1	$f_X/2^6$ (131 kHz)
1	1	0	$f_X/2^8$ (32.7 kHz)
1	1	1	$f_X/2^{10}$ (8.18 kHz)

Cautions: 1. When rewriting TCL50 to other data, stop the timer operation beforehand.

2. Set bits 3 to 7 to 0.

Remarks: When cascade connection is used, the settings of TCL500 to TCL502 are valid only for the lowermost timer.

f_X: Main system clock oscillation frequency

Values in parentheses are for operation with f_X = 8.38 MHz.

Format of Timer Clock Select Register 51

Address: FF79H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TCL51	0	0	0	0	0	TCL512	TCL511	TCL510

TCL512	TCL511	TCL510	Count clock selection
0	0	0	TI51 Falling edge
0	0	1	TI51 Rising edge
0	1	0	$f_X/2$ (4.19 MHz)
0	1	1	$f_X/2^3$ (1.04 MHz)
1	0	0	$f_X/2^5$ (261 kHz)
1	0	1	$f_X/2^7$ (65.4 kHz)
1	1	0	$f_X/2^9$ (16.3 kHz)
1	1	1	$f_X/2^{11}$ (4.09 kHz)

Cautions: 1. When rewriting TCL51 to other data, stop the timer operation beforehand.

2. Set bits 3 to 7 to 0.

Remarks: When cascade connection is used, the settings of TCL510 to TCL512 are valid only for the lowermost timer.

f_X: Main system clock oscillation frequency

Values in parentheses are for operation with f_X = 8.38 MHz.

Format of 8-Bit Timer Mode Control Register 5n (n = 0, 1)

Address: FF70H (TMC50) FF78H (TMC51) After Reset: 00H R/W

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
TMC5n	TCE5n	TMC5n6	0	TMC5n4	LVS5n	LVR5n	TMC5n1	TOE5n

TCE5n	TM5n count operation control
0	After cleaning to 0, count operation disabled (prescaler disabled)
1	Count operation start

TMC5n6	TM5n operating mode selection
0	Clear and start mode by matching between TM5n and CR5n
1	PWM (Free-running) mode

TMC5n4	Single mode/Cascade Connection mode selection
0	Single mode (use the lowest timer)
1	Cascade connection mode (connect to lower timer)

LVS5n	LVR5n	Timer output F/F status setting
0	0	No change
0	1	Timer output F/F reset (to 0)
1	0	Timer output F/F set (to 1)
1	1	Setting prohibited

TMC5n1	In other modes (TMC5n6 = 0)	In PWM mode (TMC5n6 = 1)
	Timer F/F control	Active level selection
0	Inversion operation disabled	Active high
1	Inversion operation enabled	Active low

TOE5n	Timer output control
0	Output disabled (Port mode)
1	Output enabled

Remarks: In PWM mode, PWM output will be inactive because TCE5n = 0.

If LVS5n and LVR5n are read after data is set, 0 is read.

(5) Register controlling watch timer

The following register controls the watch timer:

- Watch timer mode control register (WTM)

Format of Watch Timer Mode Control Register

Address: FF41H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	<1>	<0>
WTM	WTM7	WTM6	WTM5	WTM4	0	0	WTM1	WTM0

WTM7	Watch timer count clock selection
0	$f_X/2^7$ (65.4 kHz)
1	f_{XT} (32.768 kHz)

WTM6	WTM5	WTM4	Prescaler interval time selection
0	0	0	$2^4/f_W$
0	0	1	$2^5/f_W$
0	1	0	$2^6/f_W$
0	1	1	$2^7/f_W$
1	0	0	$2^8/f_W$
1	0	1	$2^9/f_W$
Settings other than above are prohibited			

WTM1	5-bit counter operation control
0	Clear after operation stop
1	Start

WTM0	Watch timer enables operation
0	Operation stop (clear both prescaler and timer)
1	Operation enable

Remarks: f_W: Watch timer clock frequency ($f_X/2^7$ or f_{XT})

f_X: Main system clock oscillation frequency

f_{XT}: Subsystem clock oscillation frequency

Values in parentheses apply to operation with f_X = 8.38 MHz, f_{XT} = 32.768 kHz.

(6) Registers controlling watchdog timer

The following three registers control the watchdog timer:

- Watchdog timer clock select register (WDCS)
- Watchdog timer mode register (WDTM)

Format of Watchdog Timer Clock Select Register

Address: FF42H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
WDCS	0	0	0	0	0	WDCS2	WDCS1	WDCS0

WDCS2	WDCS1	WDCS0	Overflow time of watchdog timer/interval timer
0	0	0	$2^{12}/f_X$ (489 μs)
0	0	1	$2^{13}/f_X$ (978 μs)
0	1	0	$2^{14}/f_X$ (1.96 ms)
0	1	1	$2^{15}/f_X$ (3.91 ms)
1	0	0	$2^{16}/f_X$ (7.82 ms)
1	0	1	$2^{17}/f_X$ (15.6 ms)
1	1	0	$2^{18}/f_X$ (31.3 ms)
1	1	1	$2^{20}/f_X$ (125 ms)

Remarks: f_X: Main system clock oscillation frequency
Values in parentheses are for operation with f_X = 8.38 MHz.

Format of Watchdog Timer Mode Register

Address: FFF9H After Reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
WDTM	RUN	0	0	WDTM4	WDTM3	0	0	0

RUN	Watchdog timer operation mode selection **Note 1**
0	Count stop
1	Counter is cleared and counting starts

WDTM4	WDTM3	Watchdog timer operation mode selection **Note 2**
0	×	Interval timer mode **Note 3** (Maskable interrupt request occurs upon generation of an overflow)
1	0	Watchdog timer mode 1 (Non-maskable interrupt request occurs upon generation of an overflow)
1	1	Watchdog timer mode 2 (Reset operation is activated upon generation of an overflow)

Notes: 1. Once set to 1, RUN cannot be cleared to 0 by software.
Thus, once counting starts, it can only be stopped by $\overline{\text{RESET}}$ input.
2. Once set to 1, WDTM3 and WDTM4 cannot be cleared to 0 by software.
3. The watchdog timer starts operations as the interval timer when 1 is set to RUN.

Caution: When 1 is set to RUN so that the watchdog timer is cleared, the actual overflow time is up to 0.5% shorter than the time set by the Watchdog Timer Clock Select register (WDCS).

Remark: ×: Don't care

(7) Registers controlling clock output function

The following two registers control the clock output/buzzer output control circuits:

- Clock output selection register (CKS)
- Port mode register 7 (PM7).
  - Refer to section (1) for the register format.

Format of Clock Output Selection Register

Address: FF40H After Reset: 00H R/W

Symbol	<7>	6	5	<4>	3	2	1	0
CKS	BZOE	BCS1	BCS0	CLOE	CCS3	CCS2	CCS1	CCS0

BZOE	BUZ output enable/disable specification
0	Stop clock division circuit operation. BUZ fixed to low level.
1	Enable clock division circuit operation. BUZ output enabled.

BCS1	BCS0	BUZ output clock selection
0	0	$f_X/2^{10}$ (8.18 kHz)
0	1	$f_X/2^{11}$ (4.09 kHz)
1	0	$f_X/2^{12}$ (2.04 kHz)
1	1	$f_X/2^{13}$ (1.02 kHz)

CLOE	PCL output enable/disable setting
0	Stop clock division circuit operation. PCL fixed to low level.
1	Enable clock division circuit operation. PCL output enabled.

CCS3	CCS2	CCS1	CCS0	PCL output clock selection
0	0	0	0	f_X (8.38 MHz)
0	0	0	1	$f_X/2$ (4.19 MHz)
0	0	1	0	$f_X/2^2$ (2.09 MHz)
0	0	1	1	$f_X/2^3$ (1.04 MHz)
0	1	0	0	$f_X/2^4$ (524 kHz)
0	1	0	1	$f_X/2^5$ (262 kHz)
0	1	1	0	$f_X/2^6$ (131 kHz)
0	1	1	1	$f_X/2^7$ (65.5 kHz)
1	0	0	0	f_{XT} (32.768 kHz)
Settings other than above are prohibited				

Remarks: f_X: Main system clock oscillation frequency
f_{XT}: Subsystem clock oscillation frequency
Values in parentheses are for operation with f_X = 8.38 MHz.

(8) Registers controlling A/D converter

The following four registers control the A/D converter:

- A/D converter mode register (ADM0)
- Analog input channel specification register (ADS0)
- External interrupt rising edge enable register (EGP)
  - See section (12) for the register format.
- External interrupt falling edge enable register (EGN)
  - See section (12) for the register format.

Format of A/D Converter Mode Register

Address: FF80H After Reset: 00H R/W

Symbol	<7>	<6>	5	4	3	2	1	0
ADM0	ADCS0	TRG0	FR02	FR01	FR00	EGA01	EGA00	0

ADCS0	A/D conversion operation control
0	Stop conversion operation
1	Enable conversion operation

TRG0	Software start/hardware start selection
0	Software start
1	Hardware start

FR02	FR01	FR00	Conversion time selection Note 1
0	0	0	144/f_X (17.1 μs)
0	0	1	120/f_X (14.3 μs)
0	1	0	96/f_X (Setting prohibited Note 2)
1	0	0	72/f_X (Setting prohibited Note 2)
1	0	1	60/f_X (Setting prohibited Note 2)
1	1	0	48/f_X (Setting prohibited Note 2)
Settings other than above are prohibited			

EGA01	EGA00	External trigger signal, edge specification
0	0	No edge detection
0	1	Falling edge detection
1	0	Rising edge detection
1	1	Both falling and rising edge detection

Notes: 1. Set so that the A/D conversion time is 14 μs or more.
2. Setting prohibited because A/D conversion time is less than 14 μs.

Caution: When rewriting FR00 to FR02 to other than the same data, stop A/D conversion operations once prior to performing rewrite.

Remarks: f_X: Main system clock oscillation frequency
Values in parentheses are for operation with f_X = 8.38 MHz.

Format of Analog Input Channel Specification Register

Address: FF81H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS0	0	0	0	0	0	ADS02	ADS01	ADS00

ADS02	ADS01	ADS00	Analog input channel specification
0	0	0	ANI0
0	0	1	ANI1
0	1	0	ANI2
0	1	1	ANI3
1	0	0	ANI4
1	0	1	ANI5
1	1	0	ANI6
1	1	1	ANI7

(9) Registers controlling serial interface (UART0)

The μPD780024, 780034 Subseries and the μPD780024Y, 780034Y Subseries have differences in their serial interfaces. These differences are listed in the table below.

Differences Between μPD780024/34 and μPD780024Y/34Y Subseries

Item		μPD780024, 780034	μPD780024Y, 780034Y
UART0		√	√
SIO3	SIO30	√	√
	SIO31	√	–
IIC0		–	√

The following three registers control the serial interface UART0:

- Asynchronous serial interface mode register (ASIM0)
- Asynchronous serial interface status register (ASIS0)
- Baud rate generator control register (BRGC0)

Format of Asynchronous Serial Interface Mode Register

Address: FFA0H After Reset: 00H R/W

Symbol	<7>	<6>	5	4	3	2	1	0
ASIM0	TXE0	RXE0	PS01	PS00	CL0	SL0	ISRM0	IRDAM0

TXE0	RXE0	Operation mode	RxD0/P23 pin function	TxD0/P24 pin function
0	0	Operation stop	Port function (P23)	Port function (P24)
0	1	UART mode (receive only)	Serial function (RxD0)	
1	0	UART mode (transmit only)	Port function (P23)	Serial function (TxD0)
1	1	UART mode (transmit and receive)	Serial function (RxD0)	

PS01	PS00	Parity bit specification
0	0	No parity
0	1	Zero parity always added during transmission No parity detection during reception (parity errors do not occur)
1	0	Odd parity
1	1	Even parity

CL0	Character length specification
0	7 bits
1	8 bits

SL0	Stop bit length specification for transmit data
0	1 bit
1	2 bits

ISRM0	Receive completion interrupt control when error occurs
0	Receive completion interrupt request is issued when an error occurs
1	Receive completion interrupt request is not issued when an error occurs

IRDAM0	Operation specified for infrared data transfer mode **Note 1**
0	UART (transmit/receive) mode
1	Infrared data transfer (transmit/receive) mode **Note 2**

Notes: 1. The UART/Infrared Data Transfer mode specification is controlled by TXE0 and RXE0.

2. When using Infrared Data Transfer mode, be sure to set “10H” to the baud rate generator control register (BRGC0).

Caution: Do not switch the operation mode until the current serial transmit/receive operation has stopped.

Format of Asynchronous Serial Interface Status Register

Address: FFA1H After Reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ASIS0	0	0	0	0	0	PE0	FE0	OVE0

PE0	Parity error flag
0	No parity error
1	Parity error (Incorrect parity bit detected)

FE0	Framing error flag
0	No framing error
1	Framing error **Note 1** (Stop bit not detected)

OVE0	Overrun error flag
0	No overrun error
1	Overrun error **Note 2** (Next receive operation was completed before data was read from receive buffer register)

Notes: 1. Even if a stop bit length is set to two bits by setting bit 2 (SL0) in the asynchronous serial interface mode register (ASIM0), stop bit detection during a receive operation only applies to a stop bit length of 1 bit.

2. Be sure to read the contents of the receive buffer register (RXB0) when an overrun error has occurred. Until the contents of RXB0 are read, further overrun errors will occur when receiving data.

Format of Baud Rate Generator Control Register

Address: FFA2H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BRGC0	0	TPS02	TPS01	TPS00	MDL03	MDL02	MDL01	MDL00

(f_X = 8.38 MHz)

TPS02	TPS01	TPS00	Source clock selection for 5-bit counter	n
0	0	0	P25/ASCK0	0
0	0	1	$f_X/2$	1
0	1	0	$f_X/2^2$	2
0	1	1	$f_X/2^3$	3
1	0	0	$f_X/2^4$	4
1	0	1	$f_X/2^5$	5
1	1	0	$f_X/2^6$	6
1	1	1	$f_X/2^7$	7

MDL03	MDL02	MDL01	MDL00	Input clock selection for baud rate generator	k
0	0	0	0	$f_{SCK}/16$	0
0	0	0	1	$f_{SCK}/17$	1
0	0	1	0	$f_{SCK}/18$	2
0	0	1	1	$f_{SCK}/19$	3
0	1	0	0	$f_{SCK}/20$	4
0	1	0	1	$f_{SCK}/21$	5
0	1	1	0	$f_{SCK}/22$	6
0	1	1	1	$f_{SCK}/23$	7
1	0	0	0	$f_{SCK}/24$	8
1	0	0	1	$f_{SCK}/25$	9
1	0	1	0	$f_{SCK}/26$	10
1	0	1	1	$f_{SCK}/27$	11
1	1	0	0	$f_{SCK}/28$	12
1	1	0	1	$f_{SCK}/29$	13
1	1	1	0	$f_{SCK}/30$	14
1	1	1	1	Setting prohibited	—

Cautions: 1. Writing to BRGC0 during a communication operation may cause abnormal output from the baud rate generator and disable further communication operations. Therefore, do not write to BRGC0 during a communication operation.

2. Set 10H to BRGC0 when using BRGC0 in Infrared Data Transfer mode.

Remarks: f_{SCK}: Source clock for 5-bit counter

n: Value set via TPS00 to TPS02 ($0 \leq n \leq 7$)

k: Value set via MDL00 to MDL03 ($0 \leq k \leq 14$)

(10) Register controlling serial interface (SIO3)

The following register controls serial interface SIO3:

- Serial operation mode register 30 (CSIM30)

Format of Serial Operation Mode Register 30

Address: FFB0H After Reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
CSIM30	CSIE30	0	0	0	0	MODE0	SCL301	SCL300

CSIE30	Enable/disable specification for SIO30		
	Shift register operation	Serial counter	Port
0	Operation stop	Clear	Port function **Note 1**
1	Operation enable	Count operation enable	Serial function + port function **Note 2**

MODE0	Transfer operation modes and flags		
	Operation mode	Transfer start trigger	SO30 output
0	Transmit/Transmit and Receive mode	Write to SIO30	Normal output
1	Receive-only mode	Read from SIO30	Fixed at low level

SCL301	SCL300	Clock selection
0	0	External clock input to $\overline{\text{SCK30}}$
0	1	$f_X/2^3$ (1.05 MHz)
1	0	$f_X/2^4$ (524 kHz)
1	1	$f_X/2^5$ (262 kHz)

Notes: 1. When CSIE30 = 0 (SIO30 operation stop status), the pins SI30, SO30, and $\overline{\text{SCK30}}$ can be used for port functions.

2. When CSIE30 = 1 (SIO30 operation enabled state), the SI30 pin can be used as a port pin if only the send function is used, and the SO30 pin can be used as a port pin if only the Receive-only mode is used.

Caution: In 3-wire serial I/O mode, set the port mode register (PM××) as follows. Set the output latch to 0.

- **During serial clock output (master transmission or master reception):**
  Set P22 ($\overline{\text{SCK30}}$) to output mode (PM22 = 0)
- **During serial clock input (slave transmission or slave reception):**
  Set P22 to input mode (PM22 = 1)
- **During Transmit/Transmit and Receive mode:**
  Set P21 (SO30) to output mode (PM21 = 0)
- **During Receive mode:**
  Set P20 (SI30) to Input mode (PM20 = 1)

Remarks: f_X: Main system clock oscillation frequency
Values in parentheses are for operation with f_X = 8.38 MHz.

(11) Registers controlling serial interface (I^2C)

Caution: The I^2C option is only available in 78002×Y/78003×Y devices.

The following three registers control serial interface I^2C:

- IIC control register (IICC0)
- IIC status register (IICS0)
- IIC clock select register (IICCL0)

Format of IIC Control Register (1/3)

Address: FFA8H After Reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICC0	IICE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0

IICE0	I^2C operation enable
0	Stops operation. Presets expansion register (IICS0). Stops internal operation.
1	Enables operation

Conditions for clearing (IICE0 = 0)	Condition for setting (IICE0 = 1)
• Cleared by instruction • When $\overline{\text{RESET}}$ is input	• Set by instruction

LREL0	Exit from communications
0	Normal operation
1	This exits from the current communications operation and sets Standby mode. This setting is automatically cleared after being executed. Its uses include cases in which a locally irrelevant extension code has been received. The SCL0 and SDA0 lines go into the high-impedance state. The following flags are cleared: • STD0 • ACKD0 • TRC0 • COI0 • EXC0 • MSTS0 • STT0 • SPT0

The Standby mode following exit from communications remains in effect until the following communications entry conditions are met.
- After a stop condition is detected, restart is in Master mode.
- An address match or extension code reception occurs after the start condition.

Conditions for clearing (LREL0 = 0) **Note**	Condition for setting (LREL0 = 1)
• Automatically cleared after execution • When $\overline{\text{RESET}}$ is input	• Set by instruction

WREL0	Cancel wait
0	Does not cancel wait
1	Cancels wait. This setting is automatically cleared after wait is canceled.

Conditions for clearing (WREL0 = 0) **Note**	Condition for setting (WREL0 = 1)
• Automatically cleared after execution • When $\overline{\text{RESET}}$ is input	• Set by instruction

SPIE0	Enable/disable generation of interrupt request when stop condition is detected
0	Disable
1	Enable

Conditions for clearing (SPIE0 = 0) **Note**	Condition for setting (SPIE0 = 1)
• Cleared by instruction • When $\overline{\text{RESET}}$ is input	• Set by instruction

Note: This flag's signal is invalid when IICE0 = 0.

Format of IIC Control Register (2/3)

Address: FFA8H After Reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICC0	IICE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0

WTIM0	Control of wait and interrupt request generation
0	Interrupt request is generated at the eighth clock's falling edge. Master mode: After output of eight clocks, clock output is set to low level and a wait is set. Slave mode: After input of eight clocks, the clock is set to low level and a wait is set for the master device.
1	Interrupt request is generated at the ninth clock's falling edge. Master mode: After output of nine clocks, clock output is set to low level and a wait is set. Slave mode: After input of nine clocks, the clock is set to low level and a wait is set for the master device.
This bit's setting is invalid during an address transfer and is valid after the transfer is completed. When in Master mode, a wait is inserted at the falling edge of the ninth clock during address transfers. For a slave device that has received a local address, a wait is inserted at the falling edge of the ninth clock after an ACK signal is issued. When the slave device has received an extension code, a wait is inserted at the falling edge of the eighth clock.	
Conditions for clearing (WTIM0 = 0) **Note**	Condition for setting (WTIM0 = 1)
• Cleared by instruction • When $\overline{\text{RESET}}$ is input	• Set by instruction

ACKE0	Acknowledge control
0	Disable acknowledge
1	Enable acknowledge. During the ninth clock period, the SDA0 line is set to low level. However, the ACK is invalid during address transfers and is valid when EXC0 = 1.
Conditions for clearing (ACKE0 = 0) **Note**	Condition for setting (ACKE0 = 1)
• Cleared by instruction • When $\overline{\text{RESET}}$ is input	• Set by instruction

STT0	Start condition trigger
0	Does not generate a start condition
1	When the bus is released (during STOP mode): Generates a start condition (for starting as master). The SDA0 line is changed from high level to low level and then the start condition is generated. Next, after the rated amount of time has elapsed, SCL0 is changed to low level. When the bus is not used: This trigger functions as a start condition reserve flag. When set, it releases the bus and then automatically generates a start condition. Wait status (during Master mode): Generates a restart condition after the wait is released.
Cautions concerning set timing • For master reception: Cannot be set during transfer. Can be set only at the waiting period when ACKE0 has been set to 0 and slave has been notified of final reception. • For master transmission: A start condition may not be generated normally during the ACK period. Therefore, set it during the waiting period. • Cannot be set at the same time as SPT0	
Conditions for clearing (STT0 = 0) **Note**	Condition for setting (STT0 = 1)
• Cleared by instruction • Cleared by loss in arbitration • Cleared after start condition is generated by master device • When LREL0 = 1 • When $\overline{\text{RESET}}$ is input	• Set by instruction

Note: This flag's signal is invalid when IICE0 = 0.

Format of IIC Control Register (3/3)

Address: FFA8H After Reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICC0	IICE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0

SPT0	Stop condition trigger
0	Stop condition is not generated
1	Stop condition is generated (termination of master device's transfer). After the SDA0 line goes to low level, either set the SCL0 line to high level or wait until it goes to high level. Next, after the rated amount of time has elapsed, the SDA0 line changes from low level to high level and a stop condition is generated.

Cautions concerning set timing

- For master reception: Cannot be set during transfer.
  Can be set only at the waiting period when ACKE0 has been set to 0 and slave has been notified of final reception.
- For master transmission: A stop condition cannot be generated normally during the ACK0 period. Therefore, set it during the waiting period.
- Cannot be set at the same time as STT0.
- SPT0 can be set only when in Master mode. **Note 1**
- When WTIM0 has been set to 0, if SPT0 is set during the wait period that follows output of eight clocks, note that a stop condition will be generated during the high-level period of the ninth clock.
  When a ninth clock must be output, WTIM0 should be changed from 0 to 1 during the wait period following output of eight clocks, and SPT0 should be set during the wait period that follows output of the ninth clock.

Conditions for clearing (SPT0 = 0) **Note 2**	Condition for setting (SPT0 = 1)
• Cleared by instruction • Cleared by loss in arbitration • Automatically cleared after stop condition is detected • When LREL0 = 1 • When $\overline{\text{RESET}}$ is input	• Set by instruction

Notes: 1. Set SPT0 only during Master mode. However, you must set SPT0 and generate a stop condition before the first stop condition is detected following the switch to operation enable status.

2. This flag's signal is invalid when IICE0 = 0.

Caution: When bit 3 (TRC0) of the IIC status register (IICS0) is set to "1," WREL0 is set during the ninth clock and wait is canceled, after which TRC0 is cleared and the SDA0 line is set for high impedance.

Remarks: STD0: Bit 1 of IIC status register (IICS0)
ACKD0: Bit 2 of IIC status register (IICS0)
TRC0: Bit 3 of IIC status register (IICS0)
COI0: Bit 4 of IIC status register (IICS0)
EXC0: Bit 5 of IIC status register (IICS0)
MSTS0: Bit 7 of IIC status register (IICS0)
Bits 0 and 1 (SPT0, STT0) become 0 when they are read after data setting.

Format of IIC Status Register (1/3)

Address: FFA9H After Reset: 00H R

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICS0	MSTS0	ALD0	EXC0	COI0	TRC0	ACKD0	STD0	SPD0

MSTS0	Master device status
0	Slave device status or communication standby status
1	Master device communication status

Conditions for clearing (MSTS0 = 0)	Condition for setting (MSTS0 = 1)
• When a stop condition is detected • When ALD0 = 1 • Cleared by LREL0 = 1 • When $\overline{\text{IICE0}}$ changes from 1 to 0 • When $\overline{\text{RESET}}$ is input	• When a start condition is generated

ALD0	Detection of arbitration loss
0	This status means either that there was no arbitration or that the arbitration result was a “win.”
1	This status indicates that the arbitration result was a “loss.” MSTS0 is cleared.

Conditions for clearing (ALD0 = 0)	Condition for setting (ALD0 = 1)
• Automatically cleared after IICS0 is read **Note** • When $\overline{\text{IICE0}}$ changes from 1 to 0 • When $\overline{\text{RESET}}$ is input	• When the arbitration result is a “loss”

EXC0	Detection of extension code reception
0	Extension code was not received
1	Extension code was received

Conditions for clearing (EXC0 = 0)	Condition for setting (EXC0 = 1)
• When a start condition is detected • When a stop condition is detected • Cleared by LREL0 = 1 • When $\overline{\text{IICE0}}$ changes from 1 to 0 • When $\overline{\text{RESET}}$ is input	• When the high-order four bits of the received address data is either “0000” or “1111” (set at the rising edge of the eighth clock)

Note: This register is also cleared when a bit manipulation instruction is executed for bits other than IICS0.

Format of IIC Status Register (2/3)

Address: FFA9H After Reset: 00H R

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICS0	MSTS0	ALD0	EXC0	COI0	TRC0	ACKD0	STD0	SPD0

COI0	Detection of matching addresses
0	Addresses do not match
1	Addresses match

Conditions for clearing (COI0 = 0)	Condition for setting (COI0 = 1)
• When a start condition is detected • When a stop condition is detected • Cleared by LREL0 = 1 • When IICE0 changes from 1 to 0 • When RESET is input	• When the received address matches the local address (SVA0). This bit is set at the rising edge of the eighth clock.

TRC0	Detection of transmit/receive status
0	Receive status (other than transmit status). The SDA0 line is set for high impedance.
1	Transmit status. The value in the SO0 latch is enabled for output to the SDA0 line (valid starting at the rising edge of the first byte's ninth clock).

Conditions for clearing (TRC0 = 0)	Conditions for setting (TRC0 = 1)
• When a stop condition is detected • Cleared by LREL0 = 1 • When IICE0 changes from 1 to 0 • Cleared by WREL0 = 1 • When ALD0 changes from 0 to 1 • When RESET is input Master: • When "1" is output to the first byte's LSB (transfer direction specification bit) Slave: • When a start condition is detected • When not used for communication	Master: • When a start condition is generated Slave: • When "1" is input by the first byte's LSB (transfer direction specification bit)

ACKD0	Detection of ACK
0	ACK was not detected
1	ACK was detected

Conditions for clearing (ACKD0 = 0)	Condition for setting (ACKD0 = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock • Cleared by LREL0 = 1 • When IICE0 changes from 1 to 0 • When RESET is input	• After the SDA0 line is set to low level at the rising edge of the SCL0's ninth clock

Format of IIC Status Register (3/3)

Address: FFA9H After Reset: 00H R

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICS0	MSTS0	ALD0	EXC0	COI0	TRC0	ACKD0	STD0	SPD0

STD0	Detection of start condition
0	Start condition was not detected
1	Start condition was detected. This indicates that the address transfer period is in effect.

Conditions for clearing (STD0 = 0)	Condition for setting (STD0 = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock following address transfer • Cleared by LREL0 = 1 • When IICE0 changes from 1 to 0 • When RESET is input	• When a start condition is detected

SPD0	Detection of stop condition
0	Stop condition was not detected
1	Stop condition was detected. The master device's communication is terminated and the bus is released.

Conditions for clearing (SPD0 = 0)	Condition for setting (SPD0 = 1)
• At the rising edge of the address transfer byte's first clock following setting of this bit and detection of a start condition • When IICE0 changes from 1 to 0 • When RESET is input	• When a stop condition is detected

Remarks: LREL0: Bit 6 of the IIC control register (IICC0)
IICE0: Bit 7 of the IIC control register (IICC0)

Format of IIC Clock Select Register

Address: FFAAH After Reset: 00H R/W **Note 1**

Symbol	7	6	<5>	<4>	3	2	1	0
IICCL0	0	0	CLD0	DAD0	SMC0	DFC0	0	CL00

CLD0	Detection of SCL0 line level (valid only when IICE0 = 1)
0	SCL0 line was detected at low level
1	SCL0 line was detected at high level

Conditions for clearing (CLD0 = 0)	Condition for setting (CLD0 = 1)
• When the SCL0 line is at low level • When IICE0 = 0 • When $\overline{\text{RESET}}$ is input	• When the SCL0 line is at high level

DAD0	Detection of SDA0 line level (valid only when IICE0 = 1)
0	SDA0 line was detected at low level
1	SDA0 line was detected at high level

Condition for clearing (DAD0 = 0)	Condition for setting (DAD0 = 1)
• When the SDA0 line is at low level • When IICE0 = 0 • When $\overline{\text{RESET}}$ is input	• When the SDA0 line is at high level

SMC0	Operation mode switching
0	Operation in standard mode
1	Operation in high-speed mode

Condition for clearing (SMC0 = 0)	Condition for setting (SMC0 = 1)
• Cleared by instruction • When $\overline{\text{RESET}}$ is input	• Set by instruction

DFC0	Control of digital filter operation **Note 2**
0	Digital filter ON
1	Digital filter OFF

CL00	Selection of transfer rate	
	Standard mode	High-speed mode
0	f_X/44 (191 kHz)	f_X/24 (350 kHz)
1	f_X/86 (97.5 kHz)	

Notes: 1. Bits 4 and 5 are read-only bits.

2. The digital filter can be used when in high-speed mode. Response time is slower when the digital filter is used.

Caution: Stop serial transfer once before rewriting CL00 to other than the same value.

Remarks: IICE0: Bit 7 of the IIC control register (IICC0)

f_X: Main system clock oscillation frequency

Values in parentheses are for operation with f_X = 8.38 MHz.

Format of I²C Shift Register

Address: FF1FH After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IIC0								

Format of Slave Address Register

Address: FFABH After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SVA0								0

(12) Registers controlling interrupt function

A total of 20 interrupt sources are provided, including non-maskable, maskable, and software interrupts.

Table 6-10. Interrupt Source List

Interrupt Type	Default Priority Note	Interrupt Source		Internal/ External	Vector Table Address
		Name	Trigger		
Non-maskable	—	RESET	Low voltage level	External	0000H
		INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)		
	1	INTP0	Pin input edge detection	External	0006H
	2	INTP1			0008H
	3	INTP2			000AH
	4	INTP3			000CH
	5	INTSER0	Serial interface UART0 reception error generation	Internal	000EH
	6	INTSR0	End of serial interface UART0 reception		0010H
	7	INTST0	End of serial interface UART0 transmission		0012H
	8	INTCSI30	End of serial interface SIO3 (SIO30) transfer		0014H
	9	INTCSI31	End of serial interface SIO3 (SIO31) transfer [Only for μPD780024, 780034 Subseries]		0016H
	10	INTIIC0	End of serial interface IIC0 transfer [Only for μPD780024Y, 780034Y Subseries]		0018H
	11	INTWTI	Reference time interval signal from watch timer		001AH
	12	INTTM00	Generation of 16-bit timer register and capture/ compare register 00 (CR00) match signal (with CR00 specified to compare register)		001CH
	13	INTTM01	Generation of 16-bit timer register and capture/ compare register 01 (CR01) match signal (with CR01 specified to compare register)		001EH
	14	INTTM50	Generation of 8-bit timer/event counter 50 match signal		0020H
	15	INTTM51	Generation of 8-bit timer/event counter 51 match signal		0022H
	16	INTAD0	End of A/D converter conversion		0024H
	17	INTWT	Watch timer overflow		0026H
	18	INTKR	Port 4 falling edge detection	External	0028H
Software	—	BRK	BRK instruction execution	—	003EH

Note: Default priorities are intended for two or more simultaneously generated maskable interrupt requests. 0 is the highest priority and 18 is the lowest priority.

The following table gives a listing of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 6-11. Interrupt Sources and Flags

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
		Register		Register		Register
INTWDT	WDTIF	IF0L	WDTMK	MK0L	WDTPR	PR0L
INTP0	PIF0		PMK0		PPR0	
INTP1	PIF1		PMK1		PPR1	
INTP2	PIF2		PMK2		PPR2	
INTP3	PIF3		PMK3		PPR3	
INTSER0	SERIF0		SERMK0		SERPR0	
INTSR0	SRIF0		SRMK0		SRPR0	
INTST0	STIF0		STMK0		STPR0	
INTCSI30	CSIIF30	IF0H	CSIMK30	MK0H	CSIPR30	PR0H
INTCSI31 Note 1	CSIIF31 Note 1		CSIMK31 Note 1		CSIPR31 Note 1	
INTIIC0 Note 2	IICIF0 Note 2		IICMK0 Note 2		IICPR0 Note 2	
INTWTI	WTIIF		WTIMK		WTIPR	
INTTM00	TMIF00		TMMK00		TMPR00	
INTTM01	TMIF01		TMMK01		TMPR01	
INTTM50	TMIF50		TMMK50		TMPR50	
INTTM51	TMIF51		TMMK51		TMPR51	
INTAD0	ADIF0	IF1L	ADMK0	MK1L	ADPR0	PR1L
INTWT	WTIF		WTMK		WTPR	
INTKR	KRIF		KRMK		KRPR	

Notes: 1. μPD780024, 780034 Subseries only
2. μPD780024Y, 780034Y Subseries only

The following six registers control the interrupt functions:

- Interrupt request flag registers (IF0L, IF0H, IF1L)
- Interrupt mask flag registers (MK0L, MK0H, MK1L)
- Priority specification flag registers (PR0L, PR0H, PR1L)
- External interrupt rising edge enable register (EGP)
- External interrupt falling edge enable register (EGN)
- Program status word (PSW)

Format of Interrupt Request Flag Registers

Address: FFE0H After Reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0L	STIF0	SRIF0	SERIF0	PIF3	PIF2	PIF1	PIF0	WDTIF

Address: FFE1H After Reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0H	TMIF51	TMIF50	TMIF01	TMIF00	WTIIF	IICIF0Note 1	CSIIF31Note 2	CSIIF30

Address: FFE2H After Reset: 00H R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
IF1L	0	0	0	0	0	KRIF	WTIF	ADIF0

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated; interrupt request status

Notes: 1. Incorporated only in the μPD780024 and 780034 Subseries. Be sure to set 0 for the μPD780024Y, 780034Y Subseries.

2. Incorporated only in the μPD780024Y, 780034Y Subseries. Be sure to set 0 for the μPD780024, 780034 Subseries.

Cautions: 1. The WDTIF flag is R/W enabled only when the watchdog timer is used as the interval timer. If watchdog timer mode 1 is used, set the WDTIF flag to 0.

2. Be sure to set IF1L bits 3 to 7 to 0.

3. When operating a timer, serial interface, or A/D converter after standby release, run it once after clearing an interrupt request flag. An interrupt request flag may be set by noise.

Format of Interrupt Mask Flag Registers

Address: FFE4H After Reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0L	STMK0	SRMK0	SERMK0	PMK3	PMK2	PMK1	PMK0	WDTMK

Address: FFE5H After Reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0H	TMMK51	TMMK50	TMMK01	TMMK00	WTIMK	IICMK0Note 1	CSIMK31Note 2	CSIMK30

Address: FFE6H After Reset: FFH R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
MK1L	1	1	1	1	1	KRMK	WTMK	ADMK0

XXMKX	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Notes: 1. Incorporated only in the μPD780024 and 780034 Subseries. Be sure to set 1 for the μPD780024Y, 780034Y Subseries.

2. Incorporated only in the μPD780024Y, 780034Y Subseries. Be sure to set 1 for the μPD780024, 780034 Subseries.

Cautions: 1. If the watchdog timer is used in watchdog timer mode 1, the contents of the WDTMK flag become undefined when read.

2. Because port 0 pins have an alternate function as an external interrupt request input, when the output level is changed by specifying the output mode of the port function, an interrupt request flag is set. Therefore, 1 should be set in the interrupt mask flag before using the output mode.

3. Always set MK1L bits 3 to 7 to 1.

Format of Priority Specification Flag Registers

Address: FFE8H After Reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR0L	STPR0	SRPR0	SERPR0	PPR3	PPR2	PPR1	PPR0	WDTPR

Address: FFE9H After Reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR0H	TMPR51	TMPR50	TMPR01	TMPR00	WTIPR	IICPR0Note 1	CSIPR31Note 2	CSIPR30

Address: FFEAH After Reset: FFH R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
PR1L	1	1	1	1	1	KRPR	WTPR	ADPR0

XXPRX	Priority level selection
0	High priority level
1	Low priority level

Notes: 1. Incorporated only in the μPD780024 and 780034 Subseries. Be sure to set 1 for the μPD780024Y, 780034Y Subseries.

2. Incorporated only in the μPD780024Y, 780034Y Subseries. Be sure to set 1 for the μPD780024, 780034 Subseries.

Cautions: 1. When the watchdog timer is used in the watchdog timer 1 mode, set 1 in the WDTPR flag.

2. Always set PR1L bits 3 to 7 to 1.

Format of External Interrupt Rising Edge Enable Register

Address: FF48H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	0	0	0	EGP3	EGP2	EGP1	EGP0

Format of External Interrupt Falling Edge Enable Register

Address: FF49H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN	0	0	0	0	EGN3	EGN2	EGN1	EGN0

EGPn	EGNn	INTPn pin valid edge selection (n = 0 to 3)
0	0	Interrupt disable
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

Format of Program Status Word

	7	6	5	4	3	2	1	0	After Reset
PSW	IE	Z	RBS1	AC	RBS0	0	ISP	CY	02H

These bits are used with instructions

ISP	Priority of interrupt currently being serviced
0	High-priority interrupt servicing (Low-priority interrupt disable)
1	Interrupt request not acknowledged, or low-priority interrupt servicing (All maskable interrupts enable)

IE	Interrupt request acknowledge enable/disable
0	Disable
1	Enable

(13) Registers controlling external device expansion function

The following two registers control the external device expansion function:

- Memory expansion mode register (MEM)
- Memory expansion wait setting register (MM)

Format of Memory Expansion Mode Register

Address: FF47H After Reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
MEM	0	0	0	0	0	MM2	MM1	MM0

MM2	MM1	MM0	Single-Chip/Memory Expansion mode selection		P40 to P47, P50 to P57, P64 to P67 pin state				
					P40 to P47	P50 to P53	P54, P55	P56, P57	P64 to P67
0	0	0	Single-chip mode		Port mode				
0	0	1							
0	1	1	Memory expansion mode	256-byte mode	AD0 to AD7	Port mode			P64 = $\overline{RD}$ P65 = $\overline{WR}$ P66 = $\overline{WAIT}$ P67 = ASTB
1	0	0		4K mode		A8 to A11	Port mode		
1	0	1		16K mode			A12, A13	Port mode	
1	1	1		Full-address mode **Note**				A14, A15	
Settings other than above prohibited									

Note: The full-address mode allows external expansion to the entire 64K address space except for the internal ROM, RAM, and SFR areas and the reserved areas.

Format of Memory Expansion Wait Setting Register

Address: FFF8H After Reset: 10H R/W

Symbol	7	6	5	4	3	2	1	0
MM	0	0	PW1	PW0	0	0	0	0

PW1	PW0	Wait control
0	0	No wait
0	1	Wait (one wait state inserted)
1	0	Setting prohibited
1	1	Wait control by external wait pin

(14) Register controlling standby function

The standby function is intended to decrease the power consumption of the system. The following modes are available: HALT, STOP, and SUB HALT.

When MCU is released from the STOP mode, a wait time is required for the crystal to resume oscillations. The wait time is controlled by the following register:

- Oscillation stabilization time select register (OSTS)

Format of Oscillation Stabilization Time Select Register

Address: FFFAH After Reset: 04H R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Selection of oscillation stabilization time
0	0	0	$2^{12}/f_X$ (488 μs)
0	0	1	$2^{14}/f_X$ (1.95 ms)
0	1	0	$2^{15}/f_X$ (3.91 ms)
0	1	1	$2^{16}/f_X$ (7.81 ms)
1	0	0	$2^{17}/f_X$ (15.6 ms)
Settings other than above prohibited			

Remarks: f_X: Main system clock oscillation frequency
Values in parentheses are for operation with f_X = 8.38 MHz.

The operational status of HALT mode is described below.

HALT Mode Operating Status

HALT Mode Setting / Item		During HALT Instruction Execution Using Main System Clock		During HALT Instruction Execution Using Subsystem Clock	
		Without Subsystem Clock **Note 1**	With Subsystem Clock **Note 2**	With Main System Clock Oscillation	With Main System Clock Oscillation Stopped
Clock generator		Both the main system clock and the subsystem clock can be oscillated. Clock supply to the CPU stops.			
CPU		Operation stops.			
Port (Output latch)		Status before the HALT mode setting is held.			
16-bit timer/event counter		Operable			Operable when TI00 is selected
8-bit timer/event counter		Operable			Operable when TI50, TI51 are selected as the count clock
Watch timer		Operable when $f_X/2^7$ is selected as the count clock	Operable		Operable when f_{XT} is selected as the count clock
Watchdog timer		Operable			Operation stops
A/D converter		Stop			
Serial interface		Operable			Operable during external SCK
External interrupt		Operable			
Bus line during external expansion	AD0 to AD7	High impedance			
	A8 to A15	Status before the HALT mode setting is held			
	ASTB	Low level			
	$\overline{WR}$, $\overline{RD}$	High level			
	$\overline{WAIT}$	High impedance			

Notes: 1. Including the case in which an external clock is not supplied

2. Including the case in which an external clock is supplied

The operational status of STOP Mode is described below.

STOP Mode Operating Status

Item \ STOP Mode Setting		With Subsystem Clock	Without Subsystem Clock
Clock generator		Only main system clock oscillation is stopped.	
CPU		Operation stops	
Port (Output latch)		Status before the STOP mode setting is held	
16-bit timer/event counter		Operation stops	
8-bit timer/event counter		Operable only when TI50, TI51 are selected as the count clock	
Watch timer		Operable when f_{XT} is selected as the count clock	Operation stops
Watchdog timer		Operation stops	
Clock output/buzzer output		PCL and BUZ at low level	
A/D converter		Operation stops	
Serial interface	Other than UART	Operable only when an externally supplied clock is specified as the serial clock	
	UART	Operation stops. (Transmit shift register (TXS0), receive shift register (RX0), and receive buffer register (RXB0) hold the value just before the clock stops.)	
External interrupt		Operable	
Bus line during external expansion	AD0 to AD7	High impedance	
	A8 to A15	Status before the STOP mode setting is held	
	ASTB	Low level	
	$\overline{WR}$, $\overline{RD}$	High level	
	$\overline{WAIT}$	High impedance	

Cautions: 1. When the STOP mode is set, the X2 pin is internally connected to V_{DD1} via a pull-up resistor to minimize the leakage current at the crystal oscillator. Thus, do not use the STOP mode in a system where an external clock is used for the main system clock.

2. Because the interrupt request signal is used to release the Standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the Standby mode is immediately released if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction. After the wait set using the oscillation stabilization time select register (OSTS), the operating mode is set.

(15) Reset function

The following two operations can generate a reset signal.

- External reset input via the $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer in Watchdog Timer mode

Table 6-12. Hardware Status After Reset (1/2)

Hardware		Status After Reset
Program counter (PC) Note 1		Contents of reset vector tables (0000H, 0001H) are set
Stack pointer (SP)		Undefined
Program status word (PSW)		02H
RAM	Data memory	Undefined Note 2
	General register	Undefined Note 2
Port (Output latch)		00H
Port mode registers (PM0, PM2 to PM7)		FFH
Pull-up resistor option registers (PU0, PU2 to PU7)		00H
Processor clock control register (PCC)		04H
Internal memory size switching register (IMS)		CFH Note 3
Memory expansion mode register (MEM)		00H
Memory expansion wait setting register (MM)		10H
Oscillation stabilization time select register (OSTS)		04H
16-bit timer/event counter	Timer register (TM0)	00H
	Capture/compare registers (CR00, CR01)	Undefined
	Prescaler mode register (PRM0)	00H
	Mode control register (TMC0)	00H
	Output control register (TOC0)	00H
8-bit timer/event counter	Timer counters (TM50, TM51)	00H
	Compare registers (CR50, CR51)	Undefined
	Clock select registers (TCL50, TCL51)	00H
	Mode control registers (TMC50, TMC51)	04H
Watch timer	Mode control register (WTM)	00H
Watchdog timer	Clock select register (WDCS)	00H
	Mode register (WDTM)	00H

Notes: 1. During reset input or an oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after a reset.

2. When a reset is executed in the Standby mode, the pre-reset status is held even after reset.

3. Although the initial value is CFH, use the following values to be set for each version.

   μPD780021, 780021Y, 780031, 780031Y: 42H
   μPD780022, 780022Y, 780032, 780032Y: 44H
   μPD780023, 780023Y, 780033, 780033Y: C6H
   μPD780024, 780024Y, 780034, 780034Y: C8H
   μPD78F0034, 78F0034Y: C8H

Table 6-12. Hardware Status After Reset (2/2)

Hardware		Status After Reset
Clock output/buzzer output controller	Clock output select register (CKS)	00H
A/D converter	Conversion result register (ADCR0)	00H
	Mode register (ADM0)	00H
	Analog input channel specification register (ADS0)	00H
Serial interface (UART0)	Asynchronous serial interface mode register (ASIM0)	00H
	Asynchronous serial interface status register (ASIS0)	00H
	Baud rate generator control register (BRGC0)	00H
	Transmit shift register (TXS0)	FFH
	Receive buffer register (RXB0)	
Serial interface (SIO3)	Shift registers (SIO30, SIO31 **Note 1**)	Undefined
	Operating mode registers (CSIM30, CSIM31 **Note 1**)	00H
Serial interface (IIC0) **Note 2**	Clock select register (IICCL0)	00H
	Shift register (IIC0)	00H
	Control register (IICC0)	00H
	Status register (IICS0)	00H
	Slave address register (SVA0)	00H
Interrupt	Request flag registers (IF0L, IF0H, IF1L)	00H
	Mask flag registers (MK0L, MK0H, MK1L)	FFH
	Priority specification flag registers (PR0L, PR0H, PR1L)	FFH
	External interrupt rising edge enable register (EGP)	00H
	External interrupt falling edge enable register (EGN)	00H

Notes: 1. Provided only in the μPD780024, 780034 Subseries

2. Provided only in the μPD780024Y, 780034Y Subseries

(16) Register controlling internal memory capacity

The μPD78F0034 and μPD78F0034Y (flash memory versions) allow users to select the internal memory capacity. The following register controls the internal memory capacity:

- Internal memory size switching register (IMS)

Format of Internal Memory Size Switching Register

Address: FFF0H After Reset: CFH W

Symbol	7	6	5	4	3	2	1	0
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0

RAM2	RAM1	RAM0	Selects internal high-speed RAM size
0	1	0	512 bytes
1	1	0	1024 bytes
Settings other than above are prohibited			

ROM3	ROM2	ROM1	ROM0	Selects internal ROM size
0	0	1	0	8K
0	1	0	0	16K
0	1	1	0	24K
1	0	0	0	32K
1	1	1	1	60K (setting prohibited)
Settings other than above are prohibited				

To map the memory of a flash version identical to that of a mask ROM version, the value at the time the mask ROM version is reset must be set. The following table shows the set value of IMS.

Set Value of Internal Memory Size Switching Register

Target Mask ROM Version	Set Value of IMS
μPD780021, 780031	42H
μPD780022, 780032	44H
μPD780023, 780033	C6H
μPD780024, 780034	C8H

Caution: When using a mask ROM version, do not set a value other than those shown in the above table to IMS.

6.4 μPD78044F and 78044H Subseries

6.4.1 Documentation Reference Information

Device Series Number	User's Manual Number	Date Published
μPD78044F	U10908EJ2V0UM00	July 1997
μPD78044H	U11756EJ1V0UM00	December 1996

Caution: The user should check the current User's Manual with the information in this section to be sure of having the most up-to-date information.

6.4.2 Device Series Differences

Device Series Number	ROM and RAM Differences		Number of Serial Channels
	ROM Size	RAM Size	
μPD78044F	16K/24K/32K/40K/60K	512/1K	2
μPD78044H	32K/40K/48K/60K	1K	1

General Programmer's Note

The NEC C-compiler and the NEC Assembler are capable of recognizing certain symbolic SFR bit names. These special bit names are identified in the user manual in one of the four ways shown below:

1. <7>
2. (7)
3. ⑦
4. [7]

Example:

	<7>	<6>	<5>	<4>	3	2	1	0
PCC	MCC	FRC	CLS	CSS	0	PCC2	PCC1	PCC0

If a bit number has one of the four symbols around it, the NEC software will recognize the associated symbolic bit name. For example to set bit 7, the user can write the code in two ways:

```
1.    SET1    MCC
2.    SET1    PCC.7
```

Alternatively since bit 2 does not have any of the four symbols around it, the user can only set this bit as follows:

```
1.    SET1    PCC.2
```

Note: The attempt to employ a symbolic name of bit-2 (PCC2) will return an error. Thus the use of instruction

```
SET1    PCC2
```

is improper since neither the NEC C-compiler nor the NEC Assembler recognizes this symbolic name and will generate an error.

6.4.3 Memory Address Space

Each model in the μPD78044F and 78044H Subseries can access a memory space of 64K. Figures 6-16 through 6-23 show memory maps of the respective models.

Figure 6-16. Memory Map (μPD78042F)

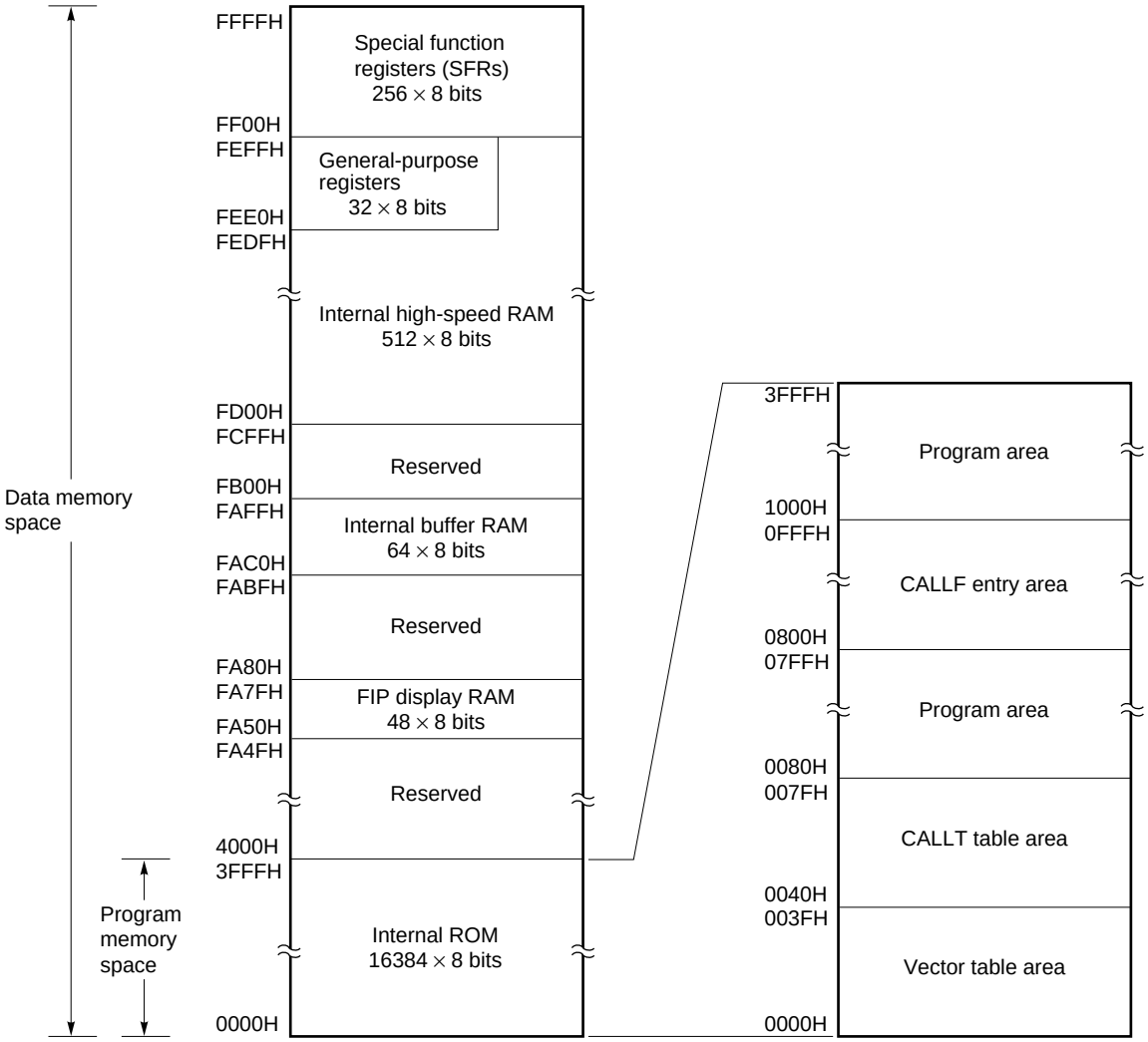


Figure 6-17. Memory Map (μPD78043F)

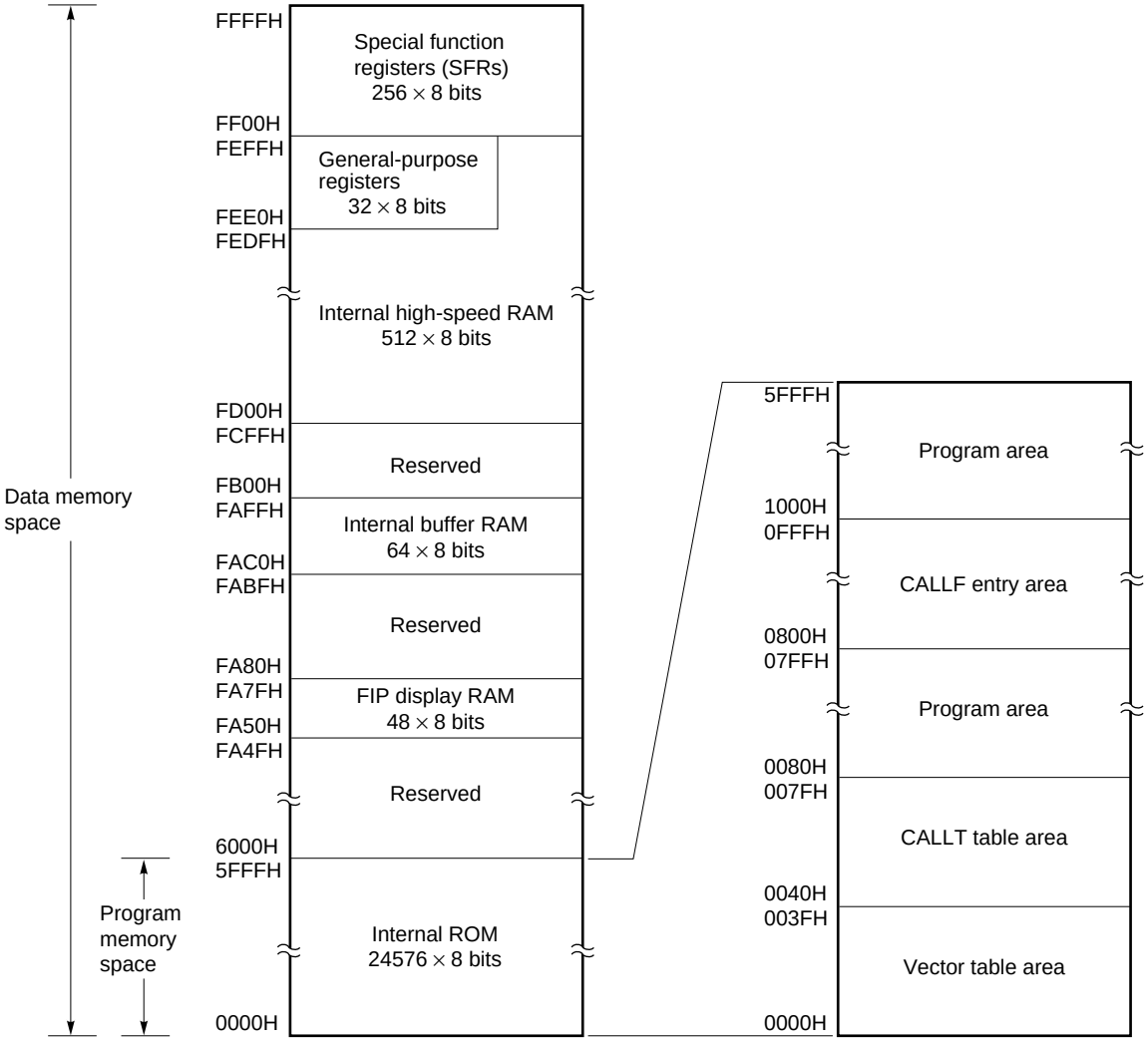


Figure 6-18. Memory Map (μPD78044F)

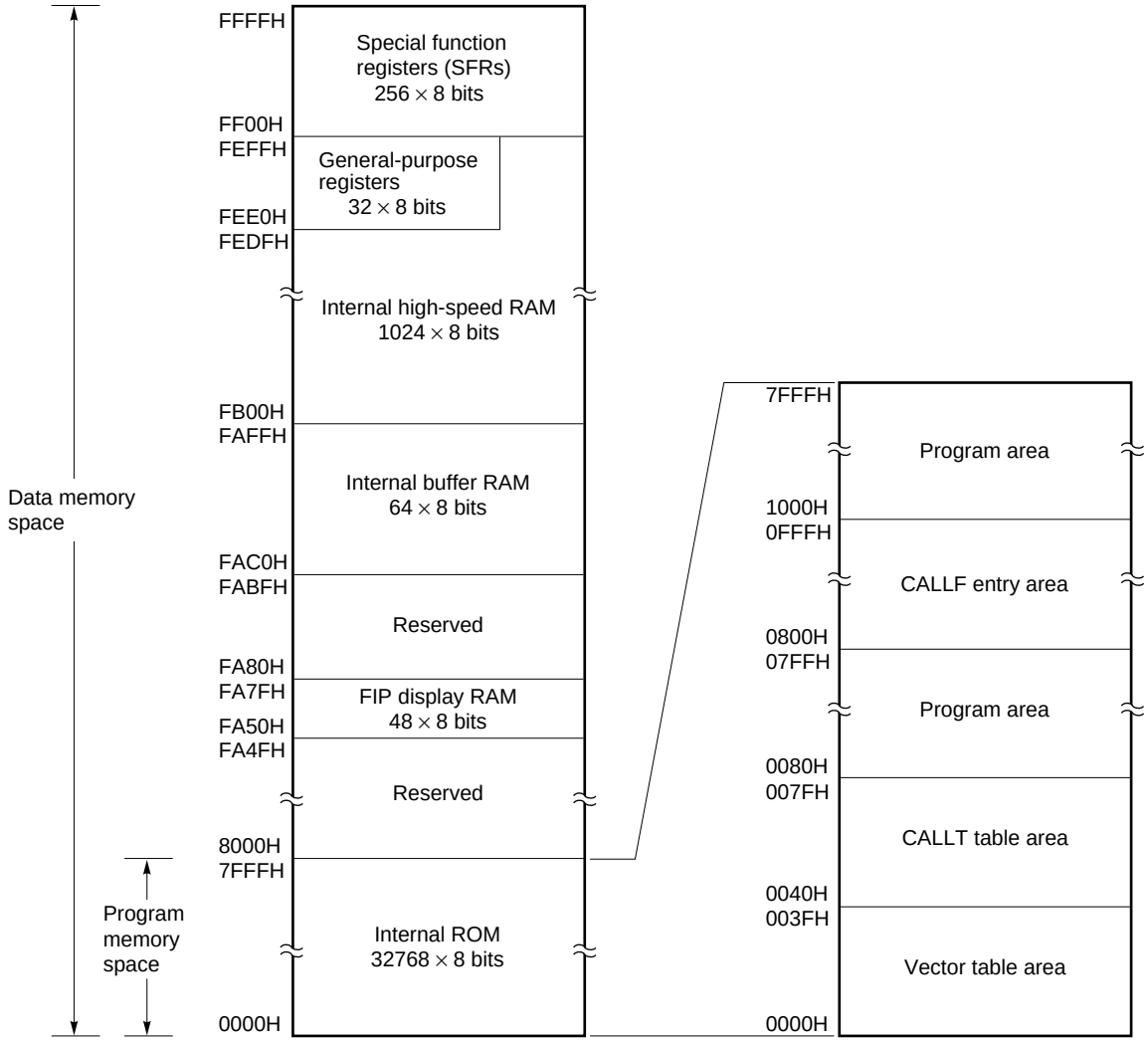


Figure 6-19. Memory Map (μPD78044H)

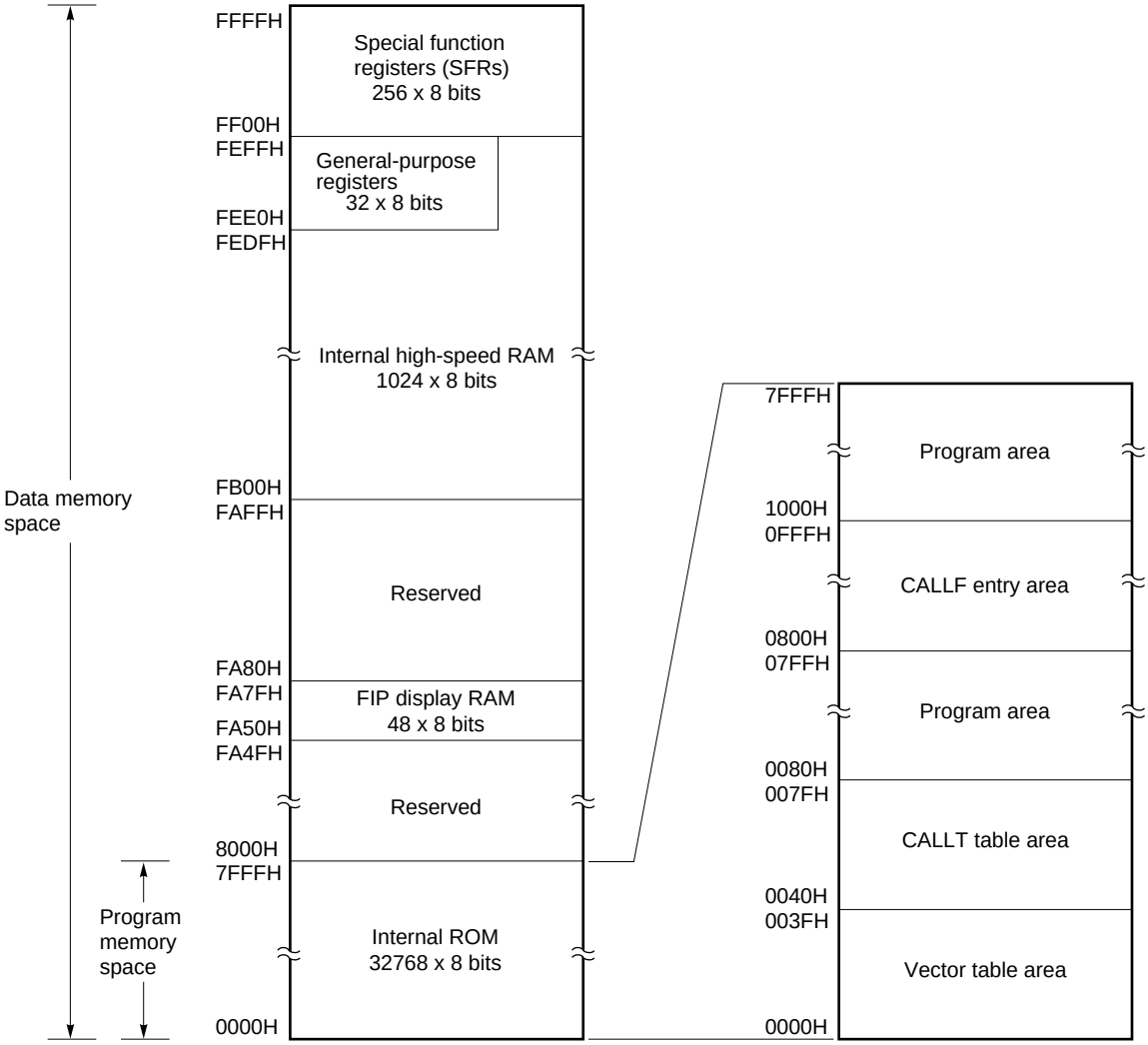


Figure 6-20. Memory Map (μPD78045F)

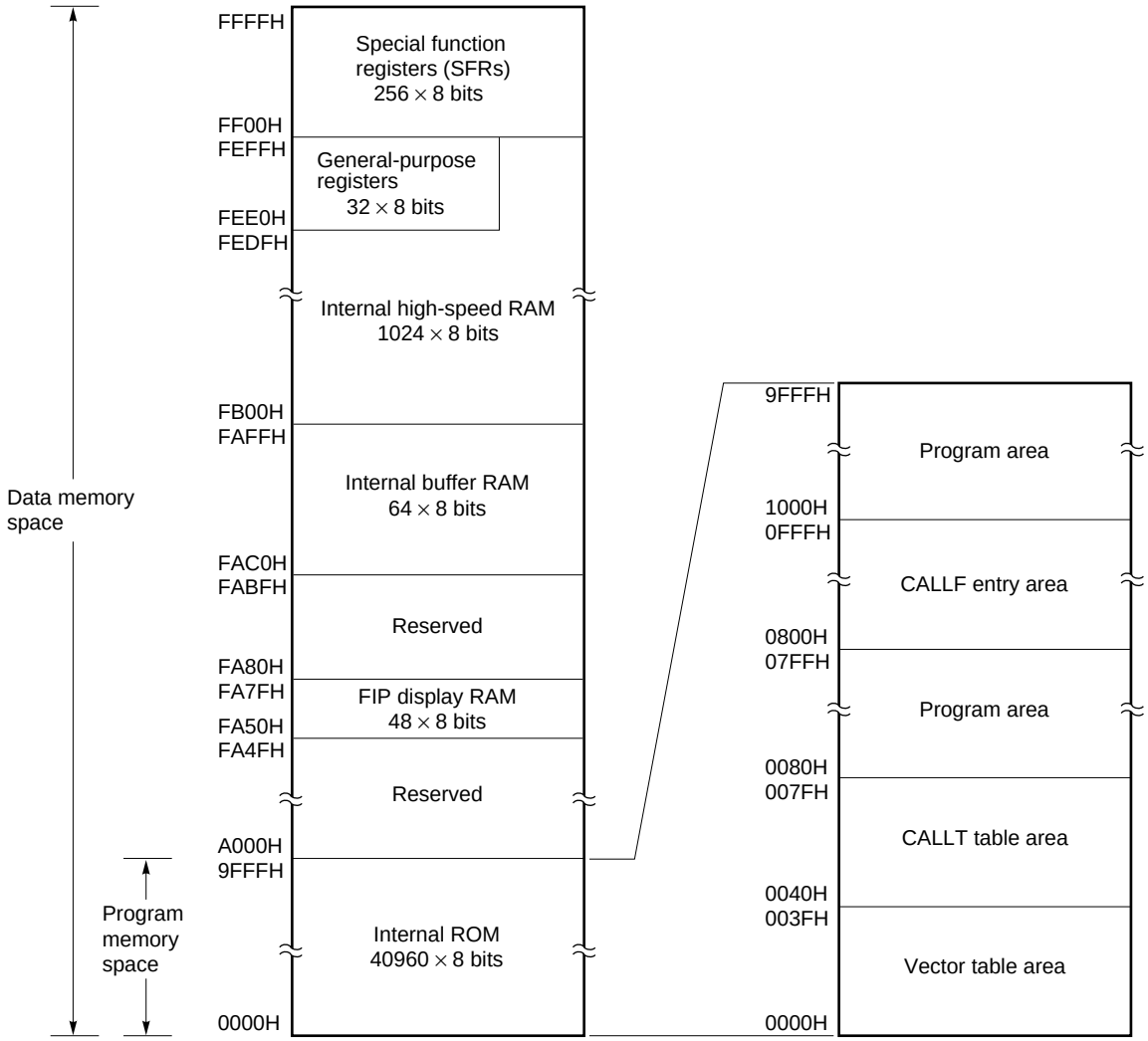


Figure 6-21. Memory Map (μPD78045H)

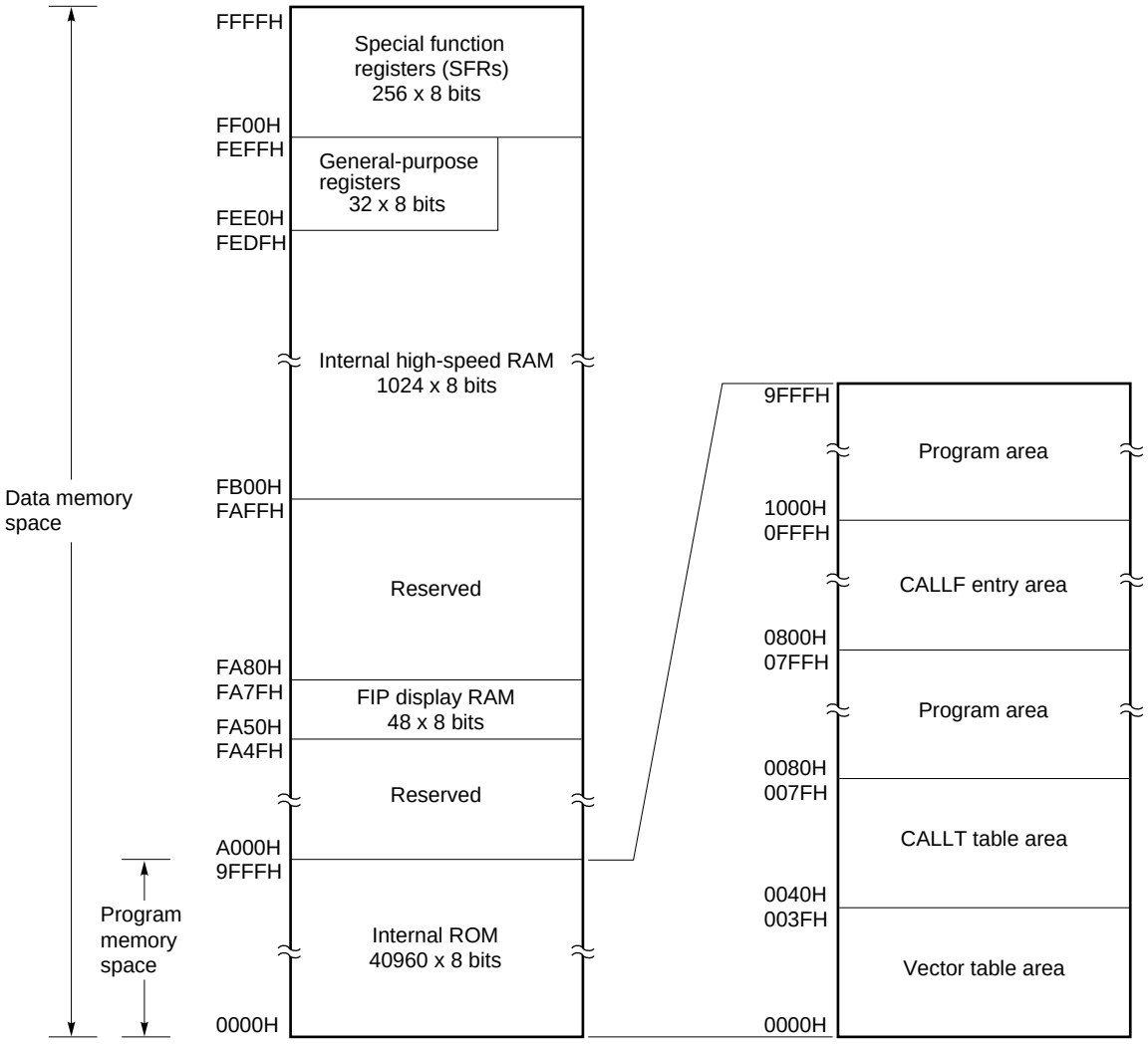


Figure 6-22. Memory Map (μPD78046H)

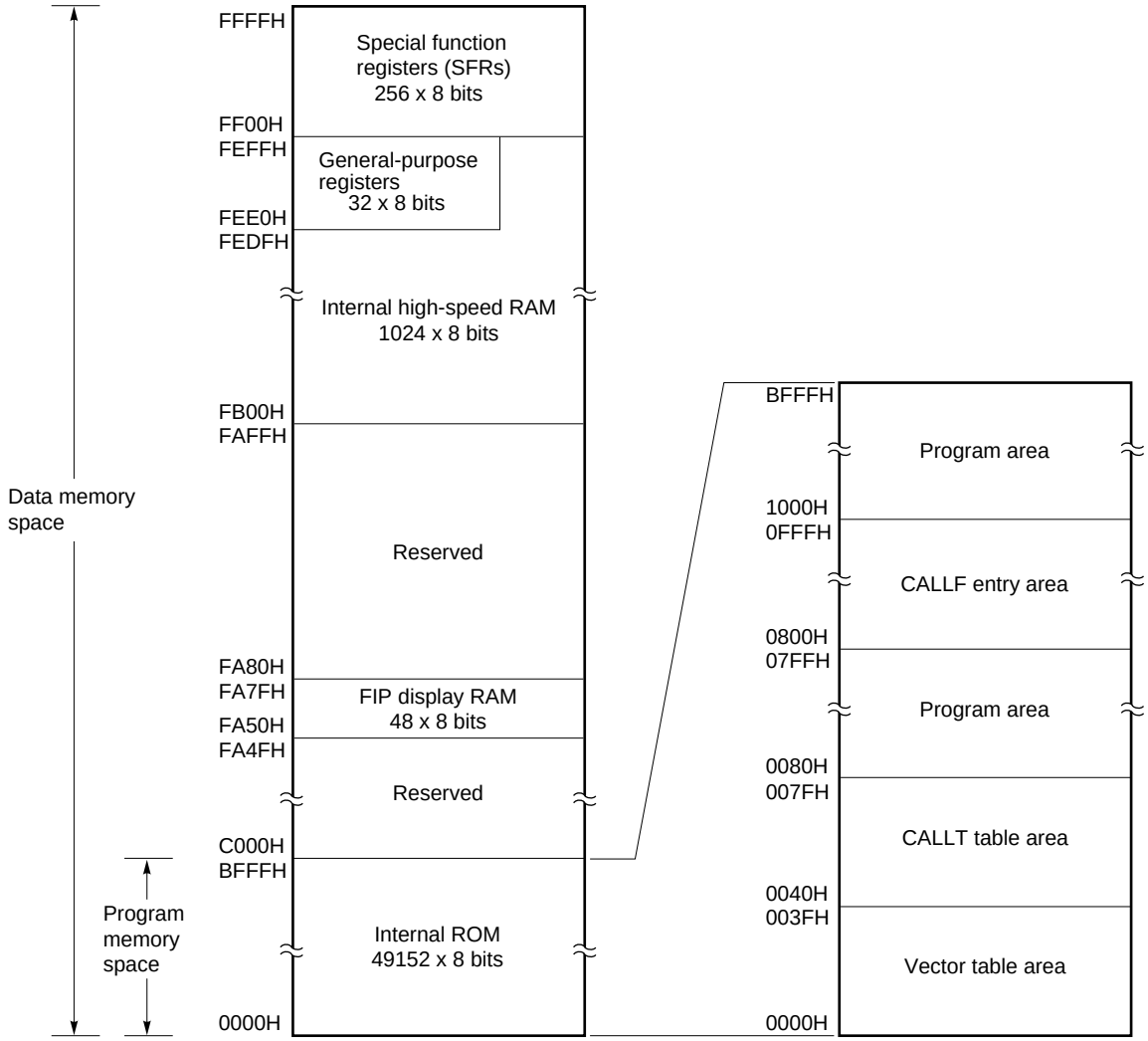
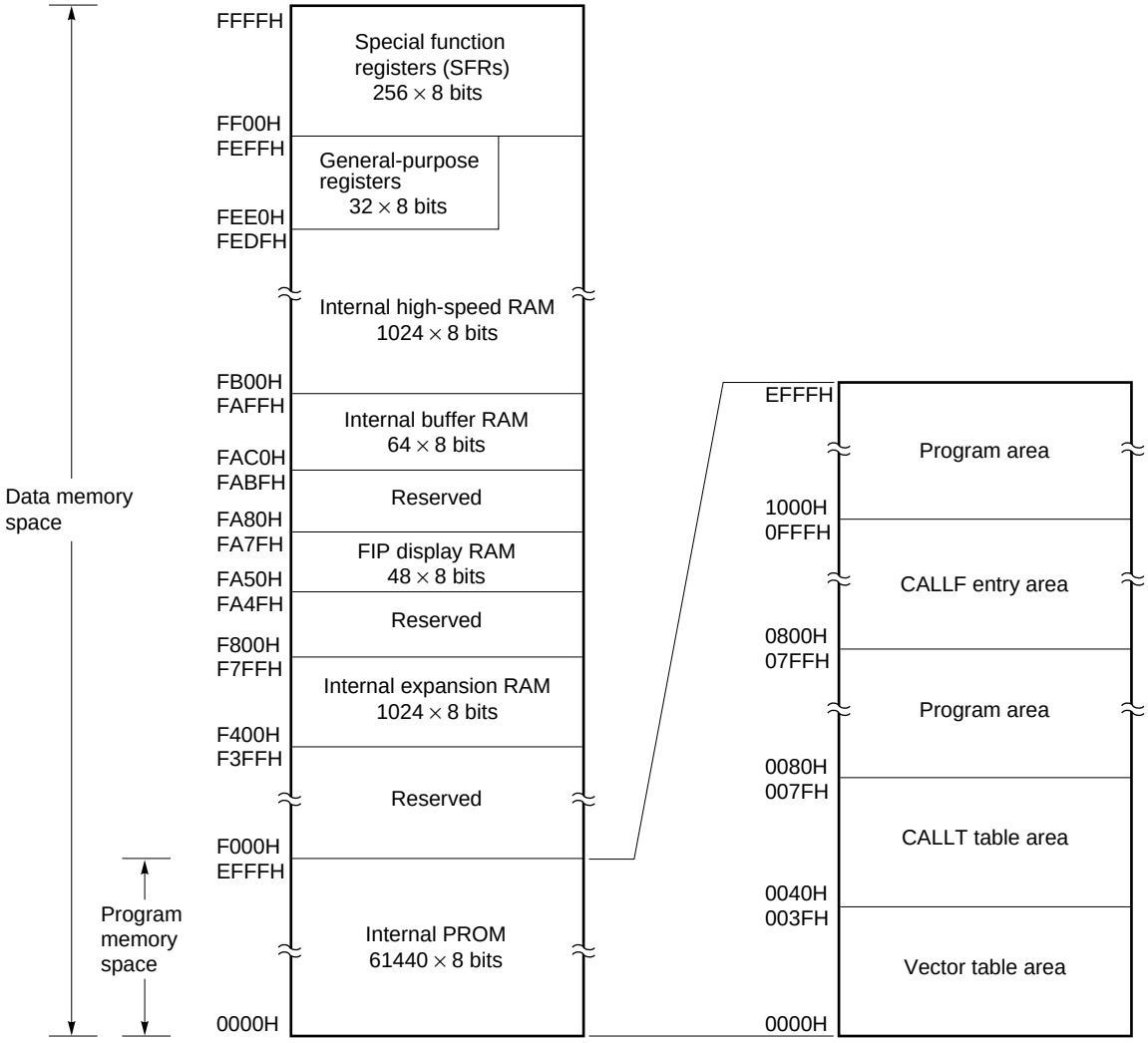


Figure 6-23. Memory Map (μPD78P048A, 78P048B)



6.4.4 Special Function Registers (SFRs)

Table 6-13. Special Function Register List (μPD78044F and 78044H Subseries) (1/3)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulatable Bit Unit			After Reset
				1 Bit	8 Bits	16 Bits	
FF00H	Port 0	P0	R/W	√	√	–	00H
FF01H	Port 1	P1		√	√	–	
FF02H	Port 2	P2		√	√	–	
FF03H	Port 3	P3		√	√	–	
FF07H	Port 7	P7		√	√	–	
FF08H	Port 8	P8	W	√	√	–	
FF09H	Port 9	P9		√	√	–	
FF0AH	Port 10	P10		√	√	–	
FF0BH	Port 11	P11	R/W	√	√	–	
FF0CH	Port 12	P12		√	√	–	
FF10H FF11H	16-bit compare register	CR00		–	–	√	Undefined
FF12H FF13H	16-bit capture register	CR01	R	–	–	√	
FF14H FF15H	16-bit timer register	TM0		–	–	√	0000H
FF16H	8-bit compare register	CR10	R/W	–	√	–	Undefined
FF17H	8-bit compare register	CR20		–	√	–	
FF18H	8-bit timer register 1	TMS TM1	R	–	√	√	00H
FF19H	8-bit timer register 2	TM2		–	√		
FF1AH	Serial I/O shift register 0 Note	SIO0	R/W	–	√	–	Undefined
FF1BH	Serial I/O shift register 1	SIO1		–	√	–	
FF1FH	A/D conversion result register	ADCR	R	–	√	–	
FF20H	Port mode register 0	PM0	R/W	√	√	–	1FH
FF21H	Port mode register 1	PM1		√	√	–	FFH
FF22H	Port mode register 2	PM2		√	√	–	
FF23H	Port mode register 3	PM3		√	√	–	
FF27H	Port mode register 7	PM7		√	√	–	1FH
FF2BH	Port mode register 11	PM11		√	√	–	FFH
FF2CH	Port mode register 12	PM12		√	√	–	

Note: This register is provided for μPD78044F Subseries products only.

Table 6-13. Special Function Register List (μPD78044F and 78044H Subseries) (2/3)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulatable Bit Unit			After Reset
					1 Bit	8 Bits	16 Bits	
FF40H	Timer clock select register 0	TCL0		R/W	√	√	–	00H
FF41H	Timer clock select register 1	TCL1			–	√	–	
FF42H	Timer clock select register 2	TCL2			–	√	–	
FF43H	Timer clock select register 3	TCL3			–	√	–	88H
FF47H	Sampling clock select register	SCS			–	√	–	00H
FF48H	16-bit timer mode control register	TMC0			√	√	–	
FF49H	8-bit timer mode control register	TMC1			√	√	–	
FF4AH	Watch timer mode control register	TMC2			√	√	–	
FF4EH	16-bit timer output control register	TOC0			√	√	–	
FF4FH	8-bit timer output control register	TOC1			√	√	–	
FF60H	Serial operation mode register 0 Note	CSIM0			√	√	–	
FF61H	Serial bus interface control register Note	SBIC			√	√	–	
FF62H	Slave address register Note	SVA			–	√	–	Undefined
FF63H	Interrupt timing specification register Note	SINT			√	√	–	00H
FF68H	Serial operation mode register 1	CSIM1			√	√	–	
FF69H	Automatic data transmit/receive control register Note	ADTC			√	√	–	
FF6AH	Automatic data transmit/receive address pointer Note	ADTP			–	√	–	
FF6BH	Automatic data transmit/receive interval specification register Note	ADTI			√	√	–	
FF80H	A/D converter mode register	ADM			√	√	–	01H
FF84H	A/D converter input select register	ADIS			–	√	–	00H
FFA0H	Display mode register 0	DSPM0			Δ Note 2	√	–	
FFA1H	Display mode register 1	DSPM1			–	√	–	
FFA8H	6-bit up/down counter mode register Note	UDM			√	√	–	
FFA9H	6-bit up/down counter Note	UDC			–	√	–	
FFAAH	6-bit up/down counter compare register Note	UDCC			–	√	–	
FFE0H	Interrupt request flag register 0L	IF0	IF0L		√	√	√	
FFE1H	Interrupt request flag register 0H		IF0H		√	√		
FFE4H	Interrupt request mask register 0L	MK0	MK0L		√	√	√	FFH
FFE5H	Interrupt request mask register 0H		MK0H		√	√		
FFE8H	Priority order specification flag register 0L	PR0	PR0L		√	√	√	
FFE9H	Priority order specification flag register 0H		PR0H		√	√		
FFECH	External interrupt mode register 0	INTM0			–	√	–	00H

Note: This register is provided for μPD78044F Subseries products only.

Table 6-13. Special Function Register List (μPD78044F and 78044H Subseries) (3/3)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulatable Bit Unit			After Reset
				1 Bit	8 Bits	16 Bits	
FFF0H	Internal memory size switching register	IMS	R/W	–	√	–	**Note 1**
FFF4H	Internal expansion RAM size switching register Note 2	IXS	W	–	√	–	0AH
FFF7H	Pull-up resistor option register	PUO	R/W	√	√	–	00H
FFF9H	Watchdog timer mode register	WDTM		√	√	–	04H
FFFAH	Oscillation stabilization time select register	OSTS		–	√	–	
FFFBH	Processor clock control register	PCC		√	√	–	

Notes: 1. The value after reset differs depending on the product, as follows:

	μPD78042F	μPD78043F	μPD78044F μPD78044H	μPD78045F μPD78045H	μPD78046H	μPD78P048A μPD78P048B
IMS	44H	46H	C8H	CAH	CCH	CFH

If using the mask ROM version, do not set any value other than that of IMS after reset.

2. This register is provided for the μPD78P048A and 78P048B only.

(1) Registers controlling port functions

The following two types of registers control the ports:

- Port mode registers (PM0 to PM3, PM7, PM11, PM12)
- Pull-up resistor option register (PUO)

Format of Port Mode Registers

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PM0	0	0	0	1	PM03	PM02	PM01	1	FF20H	1FH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W
PM3	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	FF23H	FFH	R/W
PM7	0	0	0	PM74	PM73	PM72	PM71	PM70	FF27H	1FH	R/W
PM11	PM117	PM116	PM115	PM114	PM113	PM112	PM111	PM110	FF2BH	FFH	R/W
PM12	PM127	PM126	PM125	PM124	PM123	PM122	PM121	PM120	FF2CH	FFH	R/W

PMmn	Pmn pin input/output mode selection (m = 0, 1, 2, 3, 7, 11, 12; n = 0 to 7)
0	Output mode (output buffer ON)
1	Input mode (output buffer OFF)

Format of Pull-Up Resistor Option Register (μPD78044F Subseries)

Symbol	7	6	5	4	<3>	<2>	<1>	<0>	Address	After Reset	R/W
PUO	0	0	0	0	PUO3	PUO2	PUO1	PUO0	FFF7H	00H	R/W

PUOm	Pm internal pull-up resistor selection (m = 0, 1, 2, 3)
0	Internal pull-up resistor not used
1	Internal pull-up resistor used

Format of Pull-Up Resistor Option Register (μPD78044H Subseries)

Symbol	7	6	5	4	3	<2>	<1>	<0>	Address	After Reset	R/W
PUO	0	0	0	0	PUO3	PUO2	PUO1	PUO0	FFF7H	00H	R/W

PUOm	Pm internal pull-up resistor selection (m = 0, 1, 2)
0	Internal pull-up resistor not used
1	Internal pull-up resistor used

Cautions: 1. P00 and P04 pins do not incorporate a pull-up resistor.

2. When port 1 is used as the analog input port for an A/D converter, an on-chip pull-up resistor cannot be connected even if 1 is set in PUO1.

(2) Registers controlling clock generator

The following three registers control the clock generator:

- Processor clock control register (PCC)
- Display mode register 0 (DSPM0)
- Display mode register 1 (DSPM1)

Format of Processor Clock Control Register

Symbol	<7>	<6>	<5>	<4>	3	2	1	0	Address	After Reset	R/W
PCC	MCC	FRC	CLS	CSS	0	PCC2	PCC1	PCC0	FFFBH	04H	R/W Note 1

R/W

CSS	PCC2	PCC1	PCC0	CPU clock (f_{CPU}) selection Note 2
0	0	0	0	f_X (0.4 μs)
	0	0	1	$f_X/2$ (0.8 μs)
	0	1	0	$f_X/2^2$ (1.6 μs)
	0	1	1	$f_X/2^3$ (3.2 μs)
	1	0	0	$f_X/2^4$ (6.4 μs)
1	0	0	0	$f_{XT}/2$ (122 μs)
	0	0	1	
	0	1	0	
	0	1	1	
	1	0	0	
Settings other than above are prohibited				

R

CLS	CPU clock status
0	Main system clock
1	Subsystem clock

R/W

FRC	Subsystem clock feedback resistor selection
0	Internal feedback resistor used
1	Internal feedback resistor not used

R/W

MCC	Main system clock oscillation control Note 3
0	Oscillation possible
1	Oscillation stopped

Notes: 1. Bit 5 is a read-only bit.
2. FIP can be displayed only when CSS is 0 and PCC2 to PCC0 are 000 or 001.
3. When the CPU is operating on the subsystem clock, MCC should be used to stop the main system clock oscillation. A STOP instruction should not be used.

Caution: Bit 3 must be set to 0.

Remarks: f_X: Main system clock oscillation frequency
f_{XT}: Subsystem clock oscillation frequency
Values in parentheses indicate minimum instruction execution time when operating at f_X = 5.0 MHz or f_{XT} = 32.768 kHz: $2/f_{CPU}$.

Format of Display Mode Register 0

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
DSPM0	KSF	DSPM06	0	0	SEGS3	SEGS2	SEGS1	SEGS0	FFA0H	00H	R/W Note 1

SEGS3	SEGS2	SEGS1	SEGS0	Display segment
0	0	0	0	9 segments
0	0	0	1	10 segments
0	0	1	0	11 segments
0	0	1	1	12 segments
0	1	0	0	13 segments
0	1	0	1	14 segments
0	1	1	0	15 segments
0	1	1	1	16 segments
1	0	0	0	17 segments
1	0	0	1	18 segments
1	0	1	0	19 segments
1	0	1	1	20 segments
1	1	0	0	21 segments
1	1	0	1	22 segments
1	1	1	0	23 segments
1	1	1	1	24 segments

DSPM06	Subsystem clock noise reduction circuit mode setting Note 2
0	2.5 MHz < $f_X \leq$ 5.0 MHz
1	1.25 MHz < $f_X \leq$ 2.5 MHz

KSF	Timing status
0	Display timing
1	Key scan timing

Notes: 1. Bit 7 (KSF) is a read-only bit.

2. Set the value following the main system clock frequency (f_X) to be used. The noise elimination circuit is effective when FIP is driven.

Remark: f_X: Main system clock oscillation frequency

Format of Display Mode Register 1

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
DSPM1	DIGS3	DIGS2	DIGS1	DIGS0	DIMS3	DIMS2	DIMS1	DIMS0	FFA1H	00H	R/W

DIMS0	Display cycle selection
0	1024/f_X is 1 display cycle. (1 display cycle = 204.8 s when operated at 5.0 MHz)
1	2048/f_X is 1 display cycle. (1 display cycle = 409.6 s when operated at 5.0 MHz)

DIMS3	DIMS2	DIMS1	Digit signal cut width
0	0	0	1/16
0	0	1	2/16
0	1	0	4/16
0	1	1	6/16
1	0	0	8/16
1	0	1	10/16
1	1	0	12/16
1	1	1	14/16

DIGS3	DIGS2	DIGS1	DIGS0	Display digit
0	0	0	0	Display stopped (Static display)[Note]
0	0	0	1	2 digits
0	0	1	0	3 digits
0	0	1	1	4 digits
0	1	0	0	5 digits
0	1	0	1	6 digits
0	1	1	0	7 digits
0	1	1	1	8 digits
1	0	0	0	9 digits
1	0	0	1	10 digits
1	0	1	0	11 digits
1	0	1	1	12 digits
1	1	0	0	13 digits
1	1	0	1	14 digits
1	1	1	0	15 digits
1	1	1	1	16 digits

Note: When setting to the display is stopped, a static display can be set by operating the port output latch.

Remark: f_X: Main system clock oscillation frequency

(3) Registers controlling 16-bit timer/event counter

The following six registers control the 16-bit timer/event counter:

- Timer clock select register 0 (TCL0)
- 16-bit timer mode control register (TMC0)
- 16-bit timer output control register (TOC0)
- Port mode register 3 (PM3)
  - Refer to section (1) for the register format.
- External interrupt mode register (INTM0)
  - Refer to section (14) for the register format.
- Sampling clock select register (SCS)
  - Refer to secton (14) for the register format.

Format of Timer Clock Select Register 0

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL0	CLOE	TCL06	TCL05	TCL04	TCL03	TCL02	TCL01	TCL00	FF40H	00H	R/W

This section controls clock output circuit.
Refer to **(8) Registers controlling clock output function** or **Chapter 11** of *μPD78044F Subseries User's Manual,* **Chapter 10** of *μPD78044H Subseries User's Manual* for detailed information.

TCL06	TCL05	TCL04	16-bit timer register count clock selection
0	0	0	TI0 (Valid edge specifiable)
0	0	1	f_X (5.0 MHz)
0	1	0	$f_X/2$ (2.5 MHz)
0	1	1	$f_X/2^2$ (1.25 MHz)
1	0	0	$f_X/2^3$ (625 kHz)
Settings other than above are prohibited			

Cautions:
1. **Setting of the TI0/INTP0 pin valid edge is performed by the external Interrupt mode register (INTM0), and selection of the sampling clock frequency is performed by the sampling clock selection register (SCS).**
2. **To read the count value when TI0 has been specified as the TM0 count clock, the value should be read from TM0, not from the 16-bit capture register (CR01).**
3. **To write data other than that already written to TCL0, stop the timer operation once.**

Remarks: f_X: Main system clock oscillation frequency
TI0: 16-bit timer/event counter input pin
TM0: 16-bit timer register
Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of 16-Bit Timer Mode Control Register

Symbol	7	6	5	4	3	2	1	<0>	Address	After Reset	R/W
TMC0	0	0	0	0	TMC03	TMC02	TMC01	OVF0	FF48H	00H	R/W

OVF0	16-Bit Timer Register Overflow Detection
0	Overflow not detected
1	Overflow detected

TMC03	TMC02	TMC01	Operating Mode Clear Mode Selection	TO0 Output Timing Selection	Interrupt Generation
0	0	0	Operation stop (TM0 cleared to 0)	No change	Not Generated
0	0	1	PWM mode (free running)	PWM pulse output	Generated on match between TM0 and CR00
0	1	0	Free running mode	Match between TM0 and CR00	
0	1	1		Match between TM0 and CR00 or TI0 valid edge	
1	0	0	Clear & start on TI0 valid edge	Match between TM0 and CR00	
1	0	1		Match between TM0 and CR00 or TI0 valid edge	
1	1	0	Clear & start on match between TM0 and CR00	Match between TM0 and CR00	
1	1	1		Match between TM0 and CR00 or TI0 valid edge	

Cautions:
1. **The 16-bit timer register (TM0) starts operation when a value other than 0, 0, 0 is set to TMC01 to TMC03 (Operation Stop mode). To stop the operation, set TMC01 to TMC03 to 0, 0, 0.**
2. **Switch the Clear mode and the TO0 output timing after stopping the timer operation (by setting TMC01 to TMC03 to 0, 0, 0).**
3. **Set the valid edge of the TI0/INTP0 pin with an external interrupt mode register (INTM0) and select the sampling clock frequency with the sampling clock select register (SCS).**
4. **When using the PWM mode, set the PWM and then set data to CR00.**

Remarks: TO0: 16-bit timer/event counter output pin
TI0: 16-bit timer/event counter input pin
TM0: 16-bit timer register
CR00: Compare register 00

Format of 16-Bit Timer Output Control Register

Symbol	7	6	5	4	<3>	<2>	1	<0>	Address	After Reset	R/W
TOC0	0	0	0	0	LVS0	LVR0	TOC01	TOE0	FF4EH	00H	R/W

TOE0	16-bit timer/event counter output control
0	Output disabled (Port mode)
1	Output enabled

TOC01	In PWM mode	In other modes
	Active level selection	Timer output F/F control
0	Active high	Inversion operation disabled
1	Active low	Inversion operation enabled

LVS0	LVR0	16-bit timer/event counter timer output F/F status setting
0	0	No change
0	1	Timer output F/F reset (to 0)
1	0	Timer output F/F set (to 1)
1	1	Setting prohibited

Cautions: 1. Timer operation must be stopped before setting TOC0.

2. If LVS0 and LVR0 are read after data is set, they will be 0.

(4) Registers controlling 8-bit timer/event counter

The following four registers control the 8-bit timer/event counters:

- Timer clock select register 1 (TCL1)
- 8-bit timer mode control register (TMC1)
- 8-bit timer output control register (TOC1)
- Port mode register 3 (PM3)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 1

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL1	TCL17	TCL16	TCL15	TCL14	TCL13	TCL12	TCL11	TCL10	FF41H	00H	R/W

TCL13	TCL12	TCL11	TCL10	8-bit timer register 1 count clock selection
0	0	0	0	TI1 falling edge Note
0	0	0	1	TI1 rising edge Note
0	1	0	1	$f_X/2$ (2.5 MHz)
0	1	1	0	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_X/2^9$ (9.8 kHz)
1	1	1	0	$f_X/2^{10}$ (4.9 kHz)
1	1	1	1	$f_X/2^{12}$ (1.2 kHz)
Settings other than above are prohibited				

TCL17	TCL16	TCL15	TCL14	8-bit timer register 2 count clock selection
0	0	0	0	TI2 falling edge Note
0	0	0	1	TI2 rising edge Note
0	1	0	1	$f_X/2$ (2.5 MHz)
0	1	1	0	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_X/2^9$ (9.8 kHz)
1	1	1	0	$f_X/2^{10}$ (4.9 kHz)
1	1	1	1	$f_X/2^{12}$ (1.2 kHz)
Settings other than above are prohibited				

Note: Setting prohibited for the μPD78044H Subseries.

Caution: To write data other than that already written to TCL1, stop the timer operation once.

Remarks: f_X: Main system clock frequency
TI1: 8-bit timer register 1 input pin
TI2: 8-bit timer register 2 input pin
Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of 8-Bit Timer Mode Control Register

Symbol	7	6	5	4	3	2	<1>	<0>	Address	After Reset	R/W
TMC1	0	0	0	0	0	TMC12	TCE2	TCE1	FF49H	00H	R/W

TCE1	8-bit timer register 1 operation control
0	Operation stop (TM1 clear to 0)
1	Operation enable

TCE2	8-bit timer register 2 operation control
0	Operation stop (TM2 clear to 0)
1	Operation enable

TMC12	Operating mode selection
0	8-bit timer register × 2-channel mode (TM1, TM2)
1	16-bit timer register × 1-channel mode (TMS)

Cautions: 1. Switch the operation mode after stopping timer operation.

2. When used as 16-bit timer register (TMS), TCE1 should be used for operation enable/stop.

Format of 8-Bit Timer Output Control Register

Symbol	<7>	<6>	5	<4>	<3>	<2>	1	<0>	Address	After Reset	R/W
TOC1	LVS2	LVR2	TOC15	TOE2	LVS1	LVR1	TOC11	TOE1	FF4FH	00H	R/W

TOE1	8-bit timer/event counter 1 output control
0	Output disable (Port mode)
1	Output enable

TOC11	8-bit timer/event counter 1 timer output F/F control
0	Inverted operation disable
1	Inverted operation enable

LVS1	LVR1	8-bit timer/event counter 1 timer output F/F status set
0	0	Unchanged
0	1	Timer output F/F reset (to 0)
1	0	Timer output F/F set (to 1)
1	1	Setting prohibited

TOE2	8-bit timer/event counter 2 output control
0	Output disable (Port mode)
1	Output enable

TOC15	8-bit timer/event counter 2 timer output F/F control
0	Inverted operation disable
1	Inverted operation enable

LVS2	LVR2	8-bit timer/event counter 2 timer output F/F status set
0	0	Unchanged
0	1	Timer output F/F reset (to 0)
1	0	Timer output F/F set (to 1)
1	1	Setting prohibited

Cautions: 1. Be sure to set TOC1 after stopping timer operation.

2. After data setting, 0 can be read from LVS1, LVS2, LVR1, and LVR2.

(5) Registers controlling watch timer

The following two registers control the watch timer:

- Timer clock select register 2 (TCL2)
- Watch timer mode control register (TMC2)

Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL2	TCL27	TCL26	TCL25	TCL24	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

This section controls the watchdog timer.
Refer to **(6) Registers controlling watchdog timer** or **Chapter 9** of *µPD78044F Subseries User's Manual*, **Chapter 9** of *µPD78044H Subseries User's Manual* for detailed information.

TCL24	Watch timer count clock selection [Note]
0	$f_X/2^8$ (19.5 kHz)
1	f_{XT} (32.768 kHz)

This section controls buzzer output.
Refer to **(9) Registers controlling buzzer output function** or **Chapter 12** of *µPD78044F Subseries User's Manual*, **Chapter 11** of *µPD78044H Subseries User's Manual* for detailed information.

Note: When using a main system clock of 1.25 MHz or less and an FIP controller/driver, select $f_X/2^8$ as the counter clock for the watch timer.

Caution: If TCL2 is to be rewritten in data other than identical data, the timer operation must be stopped first.

Remarks: f_X: Main system clock frequency
f_{XT}: Subsystem clock oscillation frequency
Values in parentheses apply to operation with f_X = 5.0 MHz or f_{XT} = 32.768 kHz.
This register is also used to control the watchdog timer and the buzzer.

Format of Watch Timer Mode Control Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TMC2	0	TMC26	TMC25	TMC24	TMC23	TMC22	TMC21	TMC20	FF4AH	00H	R/W

TMC23	TMC20	Watch flag set time selection
0	0	$2^{14}/f_W$ (0.5 s)
1		$2^{13}/f_W$ (0.25 s)
0	1	$2^5/f_W$ (977 μs)
1		$2^4/f_W$ (488 μs)

TMC21	Prescaler operation control [Note]
0	Clear after operation stops
1	Operation enable

TMC22	5-bit counter operation control
0	Clear after operation stops
1	Operation enable

TMC26	TMC25	TMC24	Prescaler interval time selection
0	0	0	$2^4/f_W$ (488 μs)
0	0	1	$2^5/f_W$ (977 μs)
0	1	0	$2^6/f_W$ (1.95 ms)
0	1	1	$2^7/f_W$ (3.91 ms)
1	0	0	$2^8/f_W$ (7.81 ms)
1	0	1	$2^9/f_W$ (15.6 ms)
Settings other than above are prohibited			

Note: Do not frequently clear the prescaler when using the watch timer.

Remarks: f_W: Watch timer clock frequency ($f_X/2^8$ or f_{XT})
Values in parentheses apply to operation with f_W = 32.768 kHz.

A 0.5 second interval can be generated either with a 4.19304 MHz main system clock or a 32.768 kHz subsystem clock.

(6) Registers controlling watchdog timer

The following two registers control the watchdog timer:

- Timer clock select register 2 (TCL2)
- Watchdog timer mode register (WDTM)

Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL2	TCL27	TCL26	TCL25	TCL24	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

TCL22	TCL21	TCL20	Count clock selection	
			Watchdog Timer mode	Interval Timer mode
0	0	0	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
0	0	1	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
0	1	0	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
0	1	1	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	0	0	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	0	1	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
1	1	0	$f_X/2^9$ (9.8k Hz)	$f_X/2^{10}$ (4.9 kHz)
1	1	1	$f_X/2^{11}$ (2.4 kHz)	$f_X/2^{12}$ (1.2 kHz)

This section controls the watch timer.
Refer to **(5) Registers controlling watch timer** or **Chapter 9** of *μPD78044F Subseries User's Manual*, **Chapter 9** of *μPD78044H Subseries User's Manual* for detailed information.

This section controls buzzer output.
Refer to **(9) Registers controlling buzzer output function** or **Chapter 12** of *μPD78044F Subseries User's Manual*, **Chapter 11** of *μPD78044H Subseries User's Manual* for detailed information.

Caution: If TCL2 is to be rewritten in data other than identical data, the timer operation must be stopped first.

Remarks: f_X: Main system clock frequency
Values in parentheses apply to operation with f_X = 5.0 MHz.
This register is also used to control the watch timer and the buzzer.

Format of Watchdog Timer Mode Register

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
WDTM	RUN	0	0	WDTM4	WDTM3	0	0	0	FFF9H	00H	R/W

WDTM4	WDTM3	Watchdog timer operating mode selection[Note 1]
0	x	Interval timer mode[Note 2] (Maskable interrupt request occurs upon generation of an overflow.)
1	0	Watchdog timer mode 1 (Non-maskable interrupt request occurs upon generation of an overflow.)
1	1	Watchdog timer mode 2 (Reset operation is activated upon generation of an overflow.)

RUN	Watchdog timer operation selection[Note 3]
0	Count stops
1	Counter is cleared and counting starts

Notes: 1. Once set to 1, WDTM3 and WDTM4 cannot be cleared to 0 by software.
2. The watchdog timer starts operation as an interval timer as soon as RUN has been set to 1.
3. Once set to 1, RUN cannot be cleared to 0 by software. Thus, once counting starts, it can only be stopped by $\overline{\text{RESET}}$ input.

Cautions: 1. When 1 is set in RUN so that the watchdog timer is cleared, the actual overflow time is up to 0.5% shorter than the time set by timer clock select register 2 (TCL2).
2. When using the Watchdog Timer mode 1 or 2, set WDTM4 to 1 after confirming that the interrupt request flag (TMIF4) is 0. If WDTM4 is set to 1 while TMIF4 is 1, the non-maskable interrupt request is generated regardless of the contents of WDTM3.

Remark: ×: Don't care

(7) Register controlling 6-bit up/down counter

The following register controls the 6-bit up/down counter: (only available for 7804xF and 78P048A)

- 6-bit up/down counter mode register (UDM)

Format of 6-Bit Up/Down Counter Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
UDM	0	0	0	UDM4	UDM3	UDM2	UDM1	UDM0	FFA8H	00H	R/W

UDM0	Valid edge selection
0	CI0 falling edge
1	CI0 rising edge

UDM1	Operation mode selection
0	Down counter operation
1	Up counter operation

UDM2	Count operation control
0	The count operation is stopped (the count value is retained)
1	The count operation is enabled

UDM3	Counter clear
0	Count operation
1	The counter is cleared

UDM4	INTP3 flag set signal selection
0	Set using the INTP3 interrupt signal
1	Set using the INTUD interrupt signal

Cautions: 1. Do not set the UDM0, UDM1, and UDM3 using the same timings as the effective edges input to the CI0/P03/INTP3 pin.

2. The UDC is cleared to 0 by writing 1 in the UDM3.
When the UDC is cleared, the UDM3 is automatically cleared to 0.

3. The UDC cannot be read/written until the $\overline{\text{RESET}}$ signal is input and data is set to the UDM.

4. Be sure to stop count operation before setting the 6-bit up/down counter (UDC) or the 6-bit up/down counter compare register (UDCC).

(8) Registers controlling clock output function

The following two registers control the clock output function:

- Timer clock select register 0 (TCL0)
- Port mode register 3 (PM3)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 0

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL0	CLOE	TCL06	TCL05	TCL04	TCL03	TCL02	TCL01	TCL00	FF40H	00H	R/W

TCL03	TCL02	TCL01	TCL00	PCL output clock selection
0	0	0	0	f_{XT} (32.768 kHz)
0	1	1	1	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_X/2^8$ (19.5 kHz)
Settings other than above are prohibited				

This section controls the 16-bit timer.
Refer to **(3) Registers controlling 16-bit timer/event counter** or **Chapter 6** of *μPD78044F Subseries User's Manual*, **Chapter 6** of *μPD78044H Subseries User's Manual* for detailed information.

CLOE	PCL output control
0	Output disable
1	Output enable

Cautions: 1. When enabling PCL output, set TCL00 to TCL03, then set 1 in CLOE with a 1-bit memory manipulation instruction.

2. To write data other than that already written to TCL0, stop the timer operation once.

Remarks: f_X: Main system clock frequency

f_{XT}: Subsystem clock oscillation frequency

Values in parentheses apply to operation with f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

This register is also used to set the count clock of the 16-bit timer, in addition to setting the clock for PCL output.

(9) Registers controlling buzzer output function

The following two registers control the buzzer output function:

- Timer clock select register 2 (TCL2)
- Port mode register 3 (PM3)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL2	TCL27	TCL26	TCL25	TCL24	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

This section controls the watchdog timer.
Refer to **(6) Registers controlling watchdog timer** or **Chapter 9** of *μPD78044F Subseries User's Manual*, **Chapter 9** of *μPD78044H Subseries User's Manual* for detailed information.

This section controls the watch timer.
Refer to **(5) Registers controlling watch timer** or **Chapter 8** of *μPD78044F Subseries User's Manual*, **Chapter 8** of *μPD78044H Subseries User's Manual* for detailed information.

TCL27	TCL26	TCL25	Buzzer output frequency selection
0	×	×	Buzzer output disable
1	0	0	$f_X/2^{10}$ (4.9 kHz)
1	0	1	$f_X/2^{11}$ (2.4 kHz)
1	1	0	$f_X/2^{12}$ (1.2 kHz)
1	1	1	Setting prohibited

Caution: If TCL2 is to be rewritten in data other than identical data, the timer operation must be stopped first.

Remarks: f_X: Main system clock frequency
×: Don't care
Values in parentheses apply to operation with f_X = 5.0 MHz.
This register is also used to control the watch timer and the watchdog timer.

(10) Registers controlling A/D converter

The following two registers control the A/D converter:

- A/D converter mode register (ADM)
- A/D converter input select register (ADIS)

Format of A/D Converter Mode Register

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After Reset	R/W
ADM	CS	TRG	FR1	FR0	ADM3	ADM2	ADM1	1	FF80H	01H	R/W

ADM3	ADM2	ADM1	Analog input channel selection
0	0	0	ANI0
0	0	1	ANI1
0	1	0	ANI2
0	1	1	ANI3
1	0	0	ANI4
1	0	1	ANI5
1	1	0	ANI6
1	1	1	ANI7

FR1	FR0	A/D conversion time selection Note 1	
		When operated at f_X = 5.0 MHz	When operated at f_X = 4.19 MHz
0	0	160/f_X (32.0 μs)	160/f_X (38.1 μs)
0	1	80/f_X (setting prohibited Note 2)	80/f_X (19.1 μs)
1	0	200/f_X (40.0 μs)	200/f_X (47.7 μs)
1	1	Setting prohibited	

TRG	External trigger selection
0	No external trigger (software starts mode)
1	Conversion started by external trigger (hardware starts mode)

CS	A/D conversion operation control
0	Operation stop
1	Operation start

Notes: 1. Set so that the A/D conversion time is 19.1 μs or more.
2. Setting prohibited because the A/D conversion time is less than 19.1 μs.

Cautions: 1. "1" should be set for bit 0.
2. In consideration of power consumption reduction at the A/D converter when the standby function is working, clear bit 7 (CS) of this register to 0 to stop the A/D conversion operation before executing a HALT or STOP instruction.
3. When restarting the stopped A/D conversion operation, start the A/D conversion operation after clearing the interrupt request flag (ADIF) to 0.

Remark: f_X: Main system clock frequency

Format of A/D Converter Input Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADIS	0	0	0	0	ADIS3	ADIS2	ADIS1	ADIS0	FF84H	00H	R/W

ADIS3	ADIS2	ADIS1	ADIS0	Number of analog input channel selection
0	0	0	0	No analog input channel (P10 to P17)
0	0	0	1	1 channel (ANI0, P11 to P17)
0	0	1	0	2 channels (ANI0, ANI1, P12 to P17)
0	0	1	1	3 channels (ANI0 to ANI2, P13 to P17)
0	1	0	0	4 channels (ANI0 to ANI3, P14 to P17)
0	1	0	1	5 channels (ANI0 to ANI4, P15 to P17)
0	1	1	0	6 channels (ANI0 to ANI5, P16, P17)
0	1	1	1	7 channels (ANI0 to ANI6, P17)
1	0	0	0	8 channels (ANI0 to ANI7)
Settings other than above are prohibited				

Cautions: 1. Set the analog input channel in the following order:

a. Set the number of analog input channels with ADIS.

b. Using the A/D converter mode register (ADM), select one channel to undergo A/D conversion among the channels that are set for analog input with ADIS.

2. No internal pull-up resistor can be connected to the channels set for analog input with ADIS, irrespective of the value of bit 1 (PUO1) of the pull-up resistor option register (PUO).

(11) Registers controlling serial interface channel 0 (μPD78044F Subseries only)

The following four registers control serial interface channel 0:

- Timer clock select register 3 (TCL3)
- Serial operation mode register 0 (CSIM0)
- Serial bus interface control register (SBIC)
- Interrupt timing specification register (SINT)

Caution: The registers above are provided only in the μPD78044F Subseries.

Format of Timer Clock Select Register 3

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL3	TCL37	TCL36	TCL35	TCL34	TCL33	TCL32	TCL31	TCL30	FF43H	88H	R/W

TCL33	TCL32	TCL31	TCL30	Serial interface channel 0 serial clock selection
0	1	1	0	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_X/2^9$ (9.8 kHz)
Settings other than above are prohibited				

This section controls serial interface channel 1.
Refer to **(12) Registers controlling serial interface channel 1** or **Chapter 15** of *μPD78044F Subseries User's Manual* for detailed information.

Cautions: 1. If a value that is not the same as the previous value must be written to TCL3, stop the serial transfer before writing the value.

2. μPD78044H Subseries products also have TCL3, but its format is different from that of μPD78044F Subseries products. For details, see "Format of Timer Clock Select Register 3 (For μPD78044H Subseries)" in (12) Registers controlling serial interface channel 1 or Chapter 13 Serial Interface Channel 1 in *μPD78044H Subseries User's Manual*.

Remarks: fx: Main system clock frequency
Values in parentheses apply to operation with fx = 5.0 MHz.
This register is also used to set the serial clock of serial interface channel 1.

Format of Serial Operation Mode Register 0

Symbol	<7>	<6>	<5>	4	3	2	1	0	Address	After Reset	R/W
CSIM0	CSIE0	COI	WUP	CSIM04	CSIM03	CSIM02	CSIM01	CSIM00	FF60H	00H	R/W Note 1

R/W	CSIE0	Serial interface channel 0 operation control
	0	Operation stopped
	1	Operation enable

R	COI	Slave address comparison result flag Note 2
	0	Slave address register (SVA) not equal to serial I/O shift register 0 (SIO0) data
	1	Slave address register (SVA) equal to serial I/O shift register 0 (SIO0) data

R/W	WUP	Wake-up function control Note 3
	0	Interrupt request signal generation with each serial transfer in any mode
	1	Interrupt request signal generation when the address received after bus release (when CMDD = RELD = 1) matches the slave address register (SVA) data in SBI mode

R/W

CSIM 04	CSIM 03	CSIM 02	PM25	P25	PM26	P26	PM27	P27	Operation mode	Start bit	SI0/P25 pin function	SO0/P26 pin function	$\overline{SCK0}$/P27 pin function
0	×	0	1	×	0	0	0	1	3-wire serial I/O mode	MSB	SI0 Note 4 (Input)	SO0 (CMOS output)	$\overline{SCK0}$ (CMOS input/output)
		1								LSB			
1	0	0	Note 5 ×	Note 5 ×	0	0	0	1	SBI mode	MSB	P25 (CMOS input/output)	SB1 (N-ch open-drain input/output)	$\overline{SCK0}$ (CMOS input/output)
		1	0	0	Note 5 ×	Note 5 ×	0	1			SB0 (N-ch open-drain input/output)	P26 (CMOS input/output)	
1	1	0	Note 5 ×	Note 5 ×	0	0	0	1	2-wire serial I/O mode	MSB	P25 (CMOS input/output)	SB1 (N-ch open-drain input/output)	$\overline{SCK0}$ (N-ch open-drain input/output)
		1	0	0	Note 5 ×	Note 5 ×	0	1			SB0 (N-ch open-drain input/output)	P26 (CMOS input/output)	

R/W	CSIM01	CSIM00	Serial interface channel 0 clock selection
	0	×	Input clock to $\overline{SCK0}$ pin from off-chip
	1	0	8-bit timer register 2 (TM2) output
	1	1	Clock specified with bits 0 to 3 of timer clock select register 3 (TCL3)

Notes:
1. Bit 6 (COI) is a read-only bit.
2. COI becomes 0 when CSIE0 = 0.
3. To use the wake-up function (WUP = 1), clear bit 5 (SIC) of the interrupt timing specification register (SINT) to 0.
4. Can be used as P25 (CMOS input) when serial channel is used only for transmission.
5. Can be used freely as port function when not used in SBI or 2-wire mode.

Caution: Do not change the operation mode (3-wire serial I/O, 2-wire serial I/O, or SBI) while the operation of serial interface channel 0 is enabled. Stop the serial operation before changing the operation mode.

Remarks: ×: Don't care
PM××: Port mode register
P××: Port output latch

Format of Serial Bus Interface Control Register (1/2)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
SBIC	BSYE	ACKD	ACKE	ACKT	CMDD	RELD	CMDT	RELT	FF61H	00H	R/W Note 1

R/W

Note 2 BSYE	Synchronizing Busy Signal Output Control
0	Disables busy signal which is output in synchronization with the falling edge of $\overline{SCK0}$ clock just after execution of the instruction to be cleared to 0.
1	Outputs busy signal at the falling edge of $\overline{SCK0}$ clock following the acknowledge signal.

R

ACKD	Acknowledge Detection	
Clear Conditions (ACKD = 0)		Set Conditions (ACKD = 1)
• Falling edge of the $\overline{SCK0}$ immediately after the busy mode is released while executing the transfer start instruction • When CSIE0 = 0 • When $\overline{RESET}$ input is applied		• When acknowledge signal ($\overline{ACK}$) is detected at the rising edge of $\overline{SCK0}$ clock after completion of transfer

R/W

ACKE	Acknowledge Signal Automatic Output Control	
0	Acknowledge signal automatic output disable (output with ACKT enable)	
1	Before completion of transfer	Acknowledge signal is output in synchronization with the falling edge of the 9th $\overline{SCK0}$ clock (automatically output when ACKE = 1).
	After completion of transfer	Acknowledge signal is output in synchronization with the falling edge of $\overline{SCK0}$ just after execution of the instruction to be set to 1 (automatically output when ACKE = 1). However, not automatically cleared to 0 after acknowledge signal output.

R/W

ACKT	Acknowledge signal is output in synchronization with the falling edge clock of $\overline{SCK0}$ just after execution of the instruction to be set to 1, and after acknowledge signal output, automatically cleared to 0. Used as ACKE = 0. Also cleared to 0 upon start of serial interface transfer or when CSIE0 = 0.

R

CMDD	Command Detection
Clear Conditions (CMDD = 0)	Set Conditions (CMDD = 1)
• When transfer start instruction is executed • When bus release signal (REL) is detected • When CSIE0 = 0 • When $\overline{RESET}$ input is applied	• When command signal (CMD) is detected

Notes: 1. Bits 2, 3, and 6 (RELD, CMDD, and ACKD) are read-only bits.
2. Busy mode can be cleared by starting a serial interface transfer. However, the BSYE flag is not cleared to 0.

Remarks: Bit 4 (ACKT) is 0 when read after data setting.
CSIE0: Bit 7 of serial operating mode register 0 (CSIM0)

Format of Serial Bus Interface Control Register (2/2)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
SBIC	BSYE	ACKD	ACKE	ACKT	CMDD	RELD	CMDT	RELT	FF61H	00H	R/W Note 1

R

RELD	Bus Release Detection	
	Clear Conditions (RELD = 0)	Set Conditions (RELD = 1)
	• When transfer start instruction is executed • If SIO0 and SVA values do not match in address reception • When CSIE0 = 0 • When $\overline{\text{RESET}}$ input is applied	• When bus release signal (REL) is detected

R/W

CMDT	Used for command signal output. When CMDT = 1, SO0 latch is cleared to 0. After SO0 latch clearance, automatically cleared to 0. Also cleared to 0 when CSIE0 = 0.

R/W

RELT	Used for bus release signal output. When RELT = 1, SO0 latch is set to 1. After SO0 latch setting, automatically cleared to 0. Also cleared to 0 when CSIE0 = 0.

Remarks: 1. Bits 0 and 1 (RELT and CMDT) are 0 when read after data setting.

2. CSIE0: Bit 7 of serial operating mode register 0 (CSIM0)

Format of Interrupt Timing Specification Register

Symbol	7	<6>	<5>	<4>	3	2	1	0	Address	After Reset	R/W
SINT	0	CLD	SIC	SVAM	0	0	0	0	FF63H	00H	R/W Note 1

R/W

SVAM	SVA bit to be used as slave address
0	Bits 0 to 7
1	Bits 1 to 7

R/W

SIC	INTCSI0 interrupt factor selection Note 2
0	CSIIF0 is set upon termination of serial interface channel 0 transfer
1	CSIIF0 is set upon bus release detection or termination of serial interface channel 0 transfer

R

CLD	$\overline{\text{SCK0}}$ pin level Note 3
0	Low level
1	High level

Notes: 1. Bit 6 (CLD) is a read-only bit.
2. When using the wake-up function, set SIC to 0.
3. When CSIE = 0, CLD becomes 0.

Caution: Be sure to set bits 0 through 3 to 0.

Remark: SVA: Slave address register
CSIIF0: Interrupt request flag for INTCSI0
CSIE0: Bit 7 of serial operation mode register 0 (CSIM0)

(12) Registers controlling serial interface channel 1

The following four registers control serial interface channel 1:

- Timer clock select register 3 (TCL3)
- Serial operation mode register 1 (CSIM1)
- Automatic data transmit/receive control register (ADTC) Note
- Automatic data transmit/receive interval specification register (ADTI) Note

Note: This register is provided only in the μPD78044F Subseries.

Format of Timer Clock Select Register 3 (For μPD78044F Subseries)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W	
TCL3	TCL37	TCL36	TCL35	TCL34	TCL33	TCL32	TCL31	TCL30	FF43H	88H	R/W	(7804xF and 78P048A)
									FF43H	8xH	R/W	(7804xH and 78P048B)

This section controls serial interface channel 0.
Refer to **(11) Registers controlling serial interface channel 0** or **Chapter 14** of *μPD78044F Subseries User's Manual* for detailed information.

TCL37	TCL36	TCL35	TCL34	Serial interface channel 1 serial clock selection
0	1	1	0	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_X/2^9$ (9.8 kHz)
Settings other than above are prohibited				

Caution: If a value that is not the same as the previous value must be written to TCL3, stop the serial transfer before writing the value.

Remarks: fx: Main system clock frequency
Values in parentheses apply to operation with fx = 5.0 MHz.
This register is also used to set the serial clock of serial interface channel 0.

Format of Timer Clock Select Register 3 (For μPD78044H Subseries)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL3	TCL37	TCL36	TCL35	TCL34	0	0	0	0	FF43H	88H	R/W Note

TCL37	TCL36	TCL35	TCL34	Serial interface channel 1 serial clock selection
0	1	1	0	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_X/2^9$ (9.8 kHz)
Settings other than above are prohibited				

Note: Bits 0 to 3 are read-only bits. The values of these bits are undefined when they are read.

Caution: If a value that is not the same as the previous value must be written to TCL3, stop the serial transfer before writing the value.

Remarks: fx: Main system clock frequency
Values in parentheses apply to operation with fx = 5.0 MHz.

Format of Serial Operation Mode Register 1 (For μPD78044F Subseries)

Symbol	<7>	6	<5>	4	3	2	1	0	Address	After Reset	R/W
CSIM1	CSIE1	DIR	ATE	0	0	0	CSIM11	CSIM10	FF68H	00H	R/W

CSIM11	CSIM10	Serial Interface Channel 1 Clock Selection
0	×	Clock externally input to $\overline{SCK1}$ pin Note 1
1	0	8-bit timer register 2 (TM2) output
1	1	Clock specified with bits 4 to 7 of timer clock select register 3 (TCL3)

ATE	Serial Interface Channel 1 Operating Mode Selection
0	3-wire serial I/O mode
1	3-wire serial I/O mode with automatic transmit/receive function

DIR	Start Bit	SI1 Pin Function	SO1 Pin Function
0	MSB	SI1/P20 (Input)	SO1 (CMOS output)
1	LSB		

CSIE1	CSIM11	PM20	P20	PM21	P21	PM22	P22	Shift Register 1 Operation	Serial Clock Counter Operation Control	SI1/P20 Pin Function	SO1/P21 Pin Function	$\overline{SCK1}$/P22 Pin Function
0	×	Note 2 ×	Note 2 ×	Note 2 ×	Note 2 ×	Note 2 ×	Note 2 ×	Operation stop	Clear	P20 (CMOS input/output)	P21 (CMOS input/output)	P22 (CMOS input/output)
1	0	Note 3 1	Note 3 ×	0	0	1	×	Operation enable	Count operation	SI1 Note 3 (input)	SO1 (CMOS output)	$\overline{SCK1}$ (Input)
	1					0	1					$\overline{SCK1}$ (CMOS output)

Notes: 1. If the external clock input has been selected with CSIM11 set to 0, set bit 1 (BUSY1) and bit 2 (STRB) of the automatic data transmit/receive control register (ADTC) to 0, 0.
2. Can be used freely as port function when not used in SBI or 2-wire mode.
3. Can be used as P20 when serial channel is used only for transmission. (Set bit 7 (RE) of ADTC to 0.)

Remarks: ×: Don't care
PM××: Port mode register
P××: Port output latch

Format of Serial Operation Mode Register 1 (For μPD78044H Subseries)

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
CSIM1	CSIE1	DIR	0 Note 1	0	0	0	CSIM11	CSIM10	FF68H	00H	R/W

CSIM11	CSIM10	Serial Interface Channel 1 Clock Selection
0	×	Clock externally input to $\overline{SCK1}$ pin
1	0	8-bit timer register 2 (TM2) output
1	1	Clock specified with bits 4 to 7 of timer clock select register 3 (TCL3)

DIR	Start Bit	SI1 Pin Function	SO1 Pin Function
0	MSB	SI1/P20 (Input)	SO1 (CMOS output)
1	LSB		

CSIE1	CSIM11	PM20	P20	PM21	P21	PM22	P22	Shift Register 1 Operation	Serial Clock Counter Operation Control	SI1/P20 Pin Function	SO1/P21 Pin Function	$\overline{SCK1}$/P22 Pin Function
0	×	Note 2 ×	Note 2 ×	Note 2 ×	Note 2 ×	Note 2 ×	Note 2 ×	Operation stop	Clear	P20 (CMOS input/output)	P21 (CMOS input/output)	P22 (CMOS input/output)
1	0	Note 3 1	Note 3 ×	0	0	1	×	Operation enable	Count operation	SI1 Note 3 (input)	SO1 (CMOS output)	$\overline{SCK1}$ (Input)
	1					0	1					$\overline{SCK1}$ (CMOS output)

Notes: 1. Bit 5 must be set to zero.
2. Can be used freely as port function.
3. Can be used as P20 when only transmitter is used. (Set bit 7 (RE) of ADTC to 0.)

Remarks: ×: Don't care
PM××: Port mode register
P××: Port output latch

Format of Automatic Data Transmit/Receive Control Register (μPD78044F Subseries Only)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
ADTC	RE	ARLD	ERCE	ERR	TRF	STRB	BUSY1	BUSY0	FF69H	00H	R/W Note 1

R/W

BUSY1	BUSY0	Busy input control
0	×	Not using busy input
1	0	Busy input enable (active high)
1	1	Busy input enable (active low)

R/W

STRB	Strobe output control
0	Strobe output disable
1	Strobe output enable

R

TRF	Status of automatic transmit/receive function Note 2
0	Detection of termination of automatic transmission/reception (This bit is set to 0 upon suspension of automatic transmission/reception or when ARLD = 0.)
1	During automatic transmission/reception (This bit is set to 1 when data is written to SIO1.)

R

ERR	Error detection of automatic transmit/receive function
0	No error (This bit is set to 0 when data is written to SIO1)
1	Error occurred

R/W

ERCE	Error check control of automatic transmit/receive function
0	Error check disable
1	Error check enable (only when BUSY1 = 1)

R/W

ARLD	Operating mode selection of automatic transmit/receive function
0	Single operating mode
1	Repetitive operating mode

R/W

RE	Receive control of automatic transmit/receive function
0	Receive disable
1	Receive enable

Notes: 1. Bits 3 and 4 (TRF and ERR) are read-only bits.

2. The termination of automatic transmission/reception should be judged by using TRF, not CSIIF1 (interrupt request flag).

Caution: When an external clock input is selected with bit 1 (CSIM11) of serial operating mode register 1 (CSIM1) set to 0, set STRB and BUSY1 of ADTC to 0, 0.

Remark: ×: Don't care

Format of Automatic Data Transmit/Receive Interval Specification Register (μPD78044F Subseries Only) (1/2)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADTI	ADTI7	0	0	ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	FF6BH	00H	R/W

ADTI7	Data Transfer Interval Control
0	No control of interval by ADTI Note 1
1	Control of interval by ADTI (ADTI0 to ADTI4)

ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	Data Transfer Interval Specification (f_{XX} = 2.5 MHz Operation)	
					Minimum Note 2	Maximum Note 2
0	0	0	0	0	36.8 μs + 0.5/f_{SCK}	40.0 μs + 1.5/f_{SCK}
0	0	0	0	1	62.4 μs + 0.5/f_{SCK}	65.6 μs + 1.5/f_{SCK}
0	0	0	1	0	88.0 μs + 0.5/f_{SCK}	91.2 μs + 1.5/f_{SCK}
0	0	0	1	1	113.6 μs + 0.5/f_{SCK}	116.8 μs + 1.5/f_{SCK}
0	0	1	0	0	139.2 μs + 0.5/f_{SCK}	142.4 μs + 1.5/f_{SCK}
0	0	1	0	1	164.8 μs + 0.5/f_{SCK}	168.0 μs + 1.5/f_{SCK}
0	0	1	1	0	190.4 μs + 0.5/f_{SCK}	193.6 μs + 1.5/f_{SCK}
0	0	1	1	1	216.0 μs + 0.5/f_{SCK}	219.2 μs + 1.5/f_{SCK}
0	1	0	0	0	241.6 μs + 0.5/f_{SCK}	244.8 μs + 1.5/f_{SCK}
0	1	0	0	1	267.2 μs + 0.5/f_{SCK}	270.4 μs + 1.5/f_{SCK}
0	1	0	1	0	292.8 μs + 0.5/f_{SCK}	296.0 μs + 1.5/f_{SCK}
0	1	0	1	1	318.4 μs + 0.5/f_{SCK}	321.6 μs + 1.5/f_{SCK}
0	1	1	0	0	344.0 μs + 0.5/f_{SCK}	347.2 μs + 1.5/f_{SCK}
0	1	1	0	1	369.6 μs + 0.5/f_{SCK}	372.8 μs + 1.5/f_{SCK}
0	1	1	1	0	395.2 μs + 0.5/f_{SCK}	398.4 μs + 1.5/f_{SCK}
0	1	1	1	1	420.8 μs + 0.5/f_{SCK}	424.0 μs + 1.5/f_{SCK}

Notes: 1. The interval is dependent only on CPU processing.

2. The data transfer interval includes an error. The data transfer minimum and maximum intervals are found from the following expressions (n: Value set in ADTI0 to ADTI4). However, if a minimum calculated by the following expressions is smaller than 2/f_{SCK}, the minimum interval time is 2/f_{SCK}.

$$\text{Minimum} = (n + 1) \times \frac{2^7}{f_X} + \frac{56}{f_X} + \frac{0.5}{f_{SCK}}$$

$$\text{Maximum} = (n + 1) \times \frac{2^7}{f_X} + \frac{72}{f_X} + \frac{1.5}{f_{SCK}}$$

Cautions: 1. Do not write data to ADTI during operation of the automatic data transmit/receive function.

2. Be sure to set bits 5 and 6 to 0.

3. While ADTI is used to control the interval time for data transfer by the automatic data transmit/receive function, busy control is invalid.

Remarks: f_X: Main system clock frequency

f_{SCK}: Serial clock frequency

Format of Automatic Data Transmit/Receive Interval Specification Register (μPD78044F Subseries Only) (2/2)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADTI	ADTI7	0	0	ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	FF6BH	00H	R/W

ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	Data Transfer Interval Specification (f_{XX} = 2.5 MHz Operation)	
					Minimum Note	Maximum Note
1	0	0	0	0	446.4 μs + 0.5/f_{SCK}	449.6 μs + 1.5/f_{SCK}
1	0	0	0	1	472.0 μs + 0.5/f_{SCK}	475.2 μs + 1.5/f_{SCK}
1	0	0	1	0	497.6 μs + 0.5/f_{SCK}	500.8 μs + 1.5/f_{SCK}
1	0	0	1	1	523.2 μs + 0.5/f_{SCK}	526.4 μs + 1.5/f_{SCK}
1	0	1	0	0	548.8 μs + 0.5/f_{SCK}	552.0 μs + 1.5/f_{SCK}
1	0	1	0	1	574.4 μs + 0.5/f_{SCK}	577.6 μs + 1.5/f_{SCK}
1	0	1	1	0	600.0 μs + 0.5/f_{SCK}	603.2 μs + 1.5/f_{SCK}
1	0	1	1	1	625.6 μs + 0.5/f_{SCK}	628.8 μs + 1.5/f_{SCK}
1	1	0	0	0	651.2 μs + 0.5/f_{SCK}	654.4 μs + 1.5/f_{SCK}
1	1	0	0	1	676.8 μs + 0.5/f_{SCK}	680.0 μs + 1.5/f_{SCK}
1	1	0	1	0	702.4 μs + 0.5/f_{SCK}	705.6 μs + 1.5/f_{SCK}
1	1	0	1	1	728.0 μs + 0.5/f_{SCK}	731.2 μs + 1.5/f_{SCK}
1	1	1	0	0	753.6 μs + 0.5/f_{SCK}	756.8 μs + 1.5/f_{SCK}
1	1	1	0	1	779.2 μs + 0.5/f_{SCK}	782.4 μs + 1.5/f_{SCK}
1	1	1	1	0	804.8 μs + 0.5/f_{SCK}	808.0 μs + 1.5/f_{SCK}
1	1	1	1	1	830.4 μs + 0.5/f_{SCK}	833.6 μs + 1.5/f_{SCK}

Notes: The data transfer interval includes an error. The data transfer minimum and maximum intervals are found from the following expressions (n: Value set in ADTI0 to ADTI4). However, if a minimum calculated by the following expressions is smaller than 2/f_{SCK}, the minimum interval time is 2/f_{SCK}.

$$\text{Minimum} = (n + 1) \times \frac{2^7}{f_X} + \frac{56}{f_X} + \frac{0.5}{f_{SCK}}$$

$$\text{Maximum} = (n + 1) \times \frac{2^7}{f_X} + \frac{72}{f_X} + \frac{1.5}{f_{SCK}}$$

Cautions: 1. Do not write data to ADTI during operation of the automatic data transmit/receive function.

2. Be sure to set bits 5 and 6 to 0.

3. While ADTI is used to control the interval time for data transfer by the automatic data transmit/receive function, busy control is invalid.

Remarks: 1. f_X: Main system clock frequency

2. f_{SCK}: Serial clock frequency

(13) Registers controlling FIP controller

The following two registers control the FIP controller:

- Display mode register 0 (DSPM0)
- Display mode register 1 (DSPM1)

Format of Display Mode Register 0

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
DSPM0	KSF	DSPM06	0	0	SEGS3	SEGS2	SEGS1	SEGS0	FFA0H	00H	R/W Note 1

SEGS3	SEGS2	SEGS1	SEGS0	Display segment
0	0	0	0	9 segments
0	0	0	1	10 segments
0	0	1	0	11 segments
0	0	1	1	12 segments
0	1	0	0	13 segments
0	1	0	1	14 segments
0	1	1	0	15 segments
0	1	1	1	16 segments
1	0	0	0	17 segments
1	0	0	1	18 segments
1	0	1	0	19 segments
1	0	1	1	20 segments
1	1	0	0	21 segments
1	1	0	1	22 segments
1	1	1	0	23 segments
1	1	1	1	24 segments

DSPM06	Subsystem clock noise reduction circuit mode setting Note 2
0	2.5 MHz < $f_X \leq$ 5.0 MHz
1	1.25 MHz < $f_X \leq$ 2.5 MHz

KSF	Timing status
0	Display timing
1	Key scan timing

Notes: 1. Bit 7 (KSF) is a read-only bit.

2. Set the values according to the main system clock oscillation frequency (fx) used. The noise eliminator is effective during FIP display operations.

Caution: When using a main system clock frequency below 1.25 MHz together with the FIP controller/driver, be sure to use the main system clock for watch timer counting by setting TCL24 to 0.

Remark: f_X: Main system clock oscillation frequency

Format of Display Mode Register 1

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
DSPM1	DIGS3	DIGS2	DIGS1	DIGS0	DIMS3	DIMS2	DIMS1	DIMS0	FFA1H	00H	R/W

DIMS0	Display cycle selection
0	1024/f_X is 1 display cycle. (1 display cycle = 204.8 s when operated at 5.0 MHz)
1	2048/f_X is 1 display cycle. (1 display cycle = 409.6 s when operated at 5.0 MHz)

DIMS3	DIMS2	DIMS1	Digit signal cut width
0	0	0	1/16
0	0	1	2/16
0	1	0	4/16
0	1	1	6/16
1	0	0	8/16
1	0	1	10/16
1	1	0	12/16
1	1	1	14/16

DIGS3	DIGS2	DIGS1	DIGS0	Display digit
0	0	0	0	Display stopped (Static display) Note
0	0	0	1	2 digits
0	0	1	0	3 digits
0	0	1	1	4 digits
0	1	0	0	5 digits
0	1	0	1	6 digits
0	1	1	0	7 digits
0	1	1	1	8 digits
1	0	0	0	9 digits
1	0	0	1	10 digits
1	0	1	0	11 digits
1	0	1	1	12 digits
1	1	0	0	13 digits
1	1	0	1	14 digits
1	1	1	0	15 digits
1	1	1	1	16 digits

Note: Static display is possible, when display stop is selected, by manipulating the port output latch.

Remark: f_X: Main system clock oscillation frequency

(14) Registers controlling interrupt function

A total of 15 interrupt sources are provided for the μPD78044F Subseries and 14 interrupt sources are provided for the μPD78044H Subseries, including non-maskable, maskable, and software interrupts. The following table represents all interrupt generation sources with priority.

Table 6-14. Interrupt Source List (for μPD78044F Subseries)

Interrupt Type	Default Priority Note	Interrupt Source		Internal/ External	Vector Table Address
		Name	Trigger		
Non-maskable	—	RESET	Low voltage level	External	0000H
		INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)		
	1	INTP0	Pin input edge detection	External	0006H
	2	INTP1			0008H
	3	INTP2			000AH
	4	INTP3			000CH
		INTUD	Generation of 6-bit up/down counter match signal	Internal	
	5	INTCSI0	End of serial interface channel 0 transfer		000EH
	6	INTCSI1	End of serial interface channel 1 transfer		0010H
	7	INTTM3	Reference time interval signal from watch timer		0012H
	8	INTTM0	Generation of 16-bit timer/event counter match signal		0014H
	9	INTTM1	Generation of 8-bit timer/event counter 1 match signal		0016H
	10	INTTM2	Generation of 8-bit timer/event counter 2 match signal		0018H
	11	INTAD	End of A/D converter conversion		001AH
	12	INTKS	Key scan timing from FIP controller/driver		001CH
Software	—	BRK	BRK instruction execution	—	003EH

Note: Default priorities are intended for two or more simultaneously generated maskable interrupt requests. 0 is the highest priority and 12 is the lowest priority.

Table 6-15. Interrupt Source List (for μPD78044F Subseries)

Interrupt Type	Default Priority Note	Interrupt Source		Internal/ External	Vector Table Address
		Name	Trigger		
Non-maskable	—	RESET	Low voltage level	External	0000H
		INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)		
	1	INTP0	Pin input edge detection	External	0006H
	2	INTP1			0008H
	3	INTP2			000AH
	4	INTP3			000CH
	5	INTCSI1	End of serial interface channel 1 transfer	Internal	0010H
	6	INTTM3	Reference time interval signal from watch timer		0012H
	7	INTTM0	Generation of 16-bit timer/event counter match signal		0014H
	8	INTTM1	Generation of 8-bit timer/event counter 1 match signal		0016H
	9	INTTM2	Generation of 8-bit timer/event counter 2 match signal		0018H
	10	INTAD	End of A/D converter conversion		001AH
	11	INTKS	Key scan timing from FIP controller/driver		001CH
Software	—	BRK	BRK instruction execution	—	003EH

Note: Default priorities are intended for two or more simultaneously generated maskable interrupt requests. 0 is the highest priority and 11 is the lowest priority.

The following table lists interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 6-16. Interrupt Sources and Flags

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
		Register		Register		Register
INTWDT	TMIF4	IF0L	TMMK4	MK0L	TMPR4	PR0L
INTP0	PIF0		PMK0		PPR0	
INTP1	PIF1		PMK1		PPR1	
INTP2	PIF2		PMK2		PPR2	
INTP3/INTUD Note	PIF3		PMK3		PPR3	
INTCSI0 Note	CSIIF0		CSIMK0		CSIPR0	
INTCSI1	CSIIF1		CSIMK1		CSIPR1	
INTTM3	TMIF3		TMMK3		TMPR3	
INTTM0	TMIF0	IF0H	TMMK0	MK0H	TMPR0	PR0H
INTTM1	TMIF1		TMMK1		TMPR1	
INTTM2	TMIF2		TMMK2		TMPR2	
INTAD	ADIF		ADMK		ADPR	
INTKS	KSIF		KSMK		KSPR	

Note: The following interrupt sources are not provided for the μPD78044H Subseries:

INTUD, INTCSI0

The following six types of registers control the interrupt functions:

- Interrupt request flag registers (IF0L, IF0H)
- Interrupt mask flag registers (MK0L, MK0H)
- Priority specification flag registers (PR0L, PR0H)
- External interrupt mode register (INTM0)
- Sampling clock select register (SCS)
- Program status word (PSW)

Format of Interrupt Request Flag Registers (For μPD78044F Subseries)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
IF0L	TMIF3	CSIIF1	CSIIF0	PIF3	PIF2	PIF1	PIF0	TMIF4	FFE0H	00H	R/W

	7	6	<5>	<4>	<3>	<2>	<1>	<0>			
IF0H	0	0	WTIF Note	KSIF	ADIF	TMIF2	TMIF1	TMIF0	FFE1H	00H	R/W

xxIF	Interrupt request flag
0	No interrupt request signal
1	Interrupt request signal is generated: Interrupt request state

Note: WTIF is a test input flag. A vectored interrupt request is not generated.

Cautions: 1. The TMIF4 flag is R/W enabled only when a watchdog timer is used as an interval timer. If a watchdog timer is used in Watchdog Timer mode 1, set the TMIF4 flag to 0.

2. Always set bits 6 and 7 of IF0L to 0.

Format of Interrupt Request Flag Registers (For μPD78044H Subseries)

Symbol	<7>	<6>	5	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
IF0L	TMIF3	CSIIF1	0	PIF3	PIF2	PIF1	PIF0	TMIF4	FFE0H	00H	R/W

	7	6	<5>	<4>	<3>	<2>	<1>	<0>			
IF0H	0	0	WTIF Note	KSIF	ADIF	TMIF2	TMIF1	TMIF0	FFE1H	00H	R/W

xxIF	Interrupt request flag
0	No interrupt request signal
1	Interrupt request signal is generated: Interrupt request state

Note: WTIF is a test input flag. A vectored interrupt request is not generated.

Cautions: 1. The TMIF4 flag is R/W enabled only when a watchdog timer is used as an interval timer. If a watchdog timer is used in Watchdog Timer mode 1, set the TMIF4 flag to 0.

2. Always set bit 5 of IF0L and bits 6 and 7 of IF0H to 0.

Format of Interrupt Mask Flag Registers (For μPD78044F Subseries)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
MK0L	TMMK3	CSIMK1	CSIMK0	PMK3	PMK2	PMK1	PMK0	TMMK4	FFE4H	FFH	R/W

	7	6	<5>	<4>	<3>	<2>	<1>	<0>			
MK0H	1	1	WTMK Note	KSMK	ADMK	TMMK2	TMMK1	TMMK0	FFE5H	FFH	R/W

xxMK	Interrupt servicing and Standby mode control
0	Interrupt servicing enabled, Standby mode release enabled
1	Interrupt servicing disabled, Standby mode release disabled

Note: WTMK controls standby mode release enable/disable. This bit does not control the interrupt function.

Cautions: 1. If TMMK4 flag is read when a watchdog timer is used in watchdog timer mode 1, MK0 value becomes undefined.

2. Because port 0 has an alternate function as the external interrupt request input, when the output level is changed by specifying the output mode of the port function, an interrupt request flag is set. Therefore, 1 should be set in the interrupt mask flag before using the output mode.

3. Always set bits 6 and 7 of MK0H to 1.

Format of Interrupt Mask Flag Registers (For μPD78044H Subseries)

Symbol	<7>	<6>	5	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
MK0L	TMMK3	CSIMK1	0	PMK3	PMK2	PMK1	PMK0	TMMK4	FFE4H	FFH	R/W

	7	6	<5>	<4>	<3>	<2>	<1>	<0>			
MK0H	1	1	WTMK Note	KSMK	ADMK	TMMK2	TMMK1	TMMK0	FFE5H	FFH	R/W

xxMK	Interrupt servicing and Standby mode control
0	Interrupt servicing enabled, Standby mode release enabled
1	Interrupt servicing disabled, Standby mode release disabled

Note: WTMK controls the Standby mode release enable/disable. This bit does not control the interrupt function.

Cautions: 1. If the TMMK4 flag is read when a watchdog timer is used in Watchdog Timer mode 1, the MK0 value becomes undefined.

2. Because port 0 has an alternate function as the external interrupt request input, when the output level is changed by specifying the output mode of the port function, an interrupt request flag is set. Therefore, 1 should be set in the interrupt mask flag before using the output mode.

3. Always set bit 5 of MK0L to 0 and set bits 6 and 7 of MK0H to 1.

Format of Priority Specification Flag Registers (For μPD78044F Subseries)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
PR0L	TMPR3	CSIPR1	CSIPR0	PPR3	PPR2	PPR1	PPR0	TMPR4	FFE8H	FFH	R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
PR0H	1	1	1	KSPR	ADPR	TMPR2	TMPR1	TMPR0	FFE9H	FFH	R/W

xxPR	Priority level selection
0	High priority level
1	Low priority level

Cautions: 1. When a watchdog timer is used in Watchdog Timer mode 1, set 1 to TMPR4 flag.

2. Always set bits 5 to 7 of PR0H to 1.

Format of Priority Specification Flag Registers (For μPD78044H Subseries)

Symbol	<7>	<6>	5	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
PR0L	TMPR3	CSIPR1	0	PPR3	PPR2	PPR1	PPR0	TMPR4	FFE8H	FFH	R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
PR0H	1	1	1	KSPR	ADPR	TMPR2	TMPR1	TMPR0	FFE9H	FFH	R/W

xxPR	Priority level selection
0	High priority level
1	Low priority level

Cautions: 1. When a watchdog timer is used in Watchdog Timer mode 1, set 1 in the TMPR4 flag.

2. Always set bit 5 of PR0L to 0 and set bits 5 to 7 of PR0H to 1.

Format of External Interrupt Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
INTM0	ES31	ES30	ES21	ES20	ES11	ES10	0	0	FFECH	00H	R/W

ES11	ES10	INTP0 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES21	ES20	INTP1 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES31	ES30	INTP2 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

Caution: Before setting the valid edges of the INTP0/TI0/P00 pins, stop the timer operation by clearing bits 1 to 3 (TMC01 to TMC03) of the 16-bit timer mode control register (TMC0) to 0, 0, 0.

Remarks: INTP0 pin also functions as TI0/P00.

The valid edge of INTP3 is fixed at the falling edge.

Format of Sampling Clock Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
SCS	0	0	0	0	0	0	SCS1	SCS0	FF47H	00H	R/W

SCS1	SCS0	INTP0 sampling clock selection
0	0	$f_X/2^{N+1}$
0	1	Setting prohibited
1	0	$f_X/2^6$ (78.1 kHz)
1	1	$f_X/2^7$ (39.1 kHz)

Caution: $f_X/2^{N+1}$ is a clock to be supplied to the CPU; $f_X/2^6$ and $f_X/2^7$ are clocks to be supplied to the peripheral hardware. $f_X/2^{N+1}$ stops in the HALT mode.

Remarks: N: Value (N = 0 to 4) at bits 0 to 2 (PCC0 to PCC2) of processor clock control register (PCC)
f_X: Main system clock oscillation frequency
Figures in parentheses apply to operation with f_X = 5.0 MHz.

Format of Program Status Word

Symbol	7	6	5	4	3	2	1	0	After Reset
PSW	IE	Z	RBS1	AC	RBS0	0	ISP	CY	02H

→ Used when a normal instruction is executed

ISP	Priority of interrupt currently being received
0	High-priority interrupt servicing (low-priority interrupt disable)
1	Interrupt request not acknowledged or low-priority interrupt servicing (all maskable interrupts enable)

IE	Interrupt request acknowledge enable/disable
0	Disable
1	Enable

(15) Registers controlling test function

The following two registers control the test function:

- Interrupt request flag register 0H (IF0H)
- Interrupt mask flag register 0H (MK0H)

Format of Interrupt Request Flag Register 0H

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
IF0H	0	0	WTIF	KSIF	ADIF	TMIF2	TMIF1	TMIF0	FFE1H	00H	R/W

WTIF	Watch timer overflow detection flag
0	Non-detection
1	Detection

Format of Interrupt Mask Flag Register 0H

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
MK0H	1	1	WTMK	KSMK	ADMK	TMMK2	TMMK1	TMMK0	FFE5H	FFH	R/W

WTMK	Standby mode control by watch timer
0	Standby mode release enable
1	Standby mode release disable

(16) Register controlling standby function

- Oscillation stabilization time select register (OSTS)

Format of Oscillation Stabilization Time Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0	FFFAH	04H	R/W

OSTS2	OSTS1	OSTS0	Selection of oscillation stabilization time when STOP mode is released
0	0	0	$2^{12}/f_X$ (819 μs)
0	0	1	$2^{14}/f_X$ (3.28 ms)
0	1	0	$2^{15}/f_X$ (6.55 ms)
0	1	1	$2^{16}/f_X$ (13.1 ms)
1	0	0	$2^{17}/f_X$ (26.2 ms)
Settings other than above are prohibited			

Remarks: f_X: Main system clock frequency

Values in parentheses apply to operation with f_X = 5.0 MHz.

The operation status in the HALT mode is described below.

HALT Mode Operating Status (For μPD78044F Subseries)

Setting of HALT Mode / Item		On Execution of HALT Instruction during Main System Clock Operation		On Execution of HALT Instruction during Subsystem Clock Operation	
		Without Subsystem Clock Note 1	With Subsystem Clock Note 2	When Main System Clock Continues Oscillation	When Main System Clock Clock Stops Oscillation
Clock generator		Both main system and subsystem clocks can be oscillated. Clock supply to the CPU stops.			
CPU		Operation stops			
Port (output latch)		Status before HALT mode setting is held			
16-bit timer/event counter		Operable			Operation stops
8-bit timer/event counter					Operable when TI1 or TI2 is selected for the count clock
Watchdog timer					Operation stops
A/D converter					
Watch timer		Operable when $f_X/2^8$ is selected for the count clock	Operable		Operable when f_{XT} is selected for the count clock
6-bit up/down counter		Operable			
FIP controller/driver		Not operable			
Serial interface	Other than automatic transmit/receive function	Operable			Operable when external SCK is selected
	Automatic transmit/receive function	Operation stops			
External interrupt request	INTP0	INTP0 is operable when the clocks ($f_{XX}/2^6$ and $f_{XX}/2^7$) for peripheral hardware are selected as the sampling clock.			Operation stops
	INTP1 to INTP3	Operable			

Notes: 1. Including when an external clock is not supplied as the subsystem clock.

2. Including when an external clock is supplied as the subsystem clock.

HALT Mode Operating Status (For μPD78044H Subseries)

Setting of HALT Mode / Item		On Execution of HALT Instruction during Main System Clock Operation		On Execution of HALT Instruction during Subsystem Clock Operation	
		Without Subsystem Clock Note 1	With Subsystem Clock Note 2	When Main System Clock Continues Oscillation	When Main System Clock Clock Stops Oscillation
Clock generator		Both main system and subsystem clocks can be oscillated. Clock supply to the CPU stops.			
CPU		Operation stops			
Port (output latch)		Status before HALT mode setting is held			
16-bit timer/event counter		Operable			Operation stops
8-bit timer/event counter					
Watchdog timer					
A/D converter					
Watch timer		Operable when $f_X/2^8$ is selected for the count clock	Operable		Operable when f_{XT} is selected for the count clock
FIP controller/driver		Not operable			
Serial interface		Operable			Operable when external SCK is selected
External interrupt request	INTP0	INTP0 is operable when the clocks ($f_{XX}/2^6$ and $f_{XX}/2^7$) for peripheral hardware are selected as the sampling clock.			Operation stops
	INTP1 to INTP3	Operable			

Notes: 1. Including when an external clock is not supplied as the subsystem clock.

2. Including when an external clock is supplied as the subsystem clock.

The operation status in the STOP mode is shown below.

STOP Mode Operating Status (μPD78044F Subseries)

Item \ Setting of STOP Mode		With Subsystem Clock	Without Subsystem Clock
Clock generator		Only main system clock stops oscillation	
CPU		Operation stops	
Port (output latch)		Status before STOP mode setting is held	
16-bit timer/event counter		Operation stops	
8-bit timer/event counter		Operable when TI1 or TI2 is selected for the count clock	
Watchdog timer		Operation stops	
A/D converter			
Watch timer		Operable when f_{XT} is selected for the count clock	Operation stops
6-bit up/down counter		Operable	
FIP controller/driver		Not operable	
Serial interface	Other than automatic transmit/receive function	Operable when externally supplied clock is specified as the serial clock	
	Automatic transmit/receive function	Operation stops	
External interrupt request	INTP0	Not operable	
	INTP1 to INTP3	Operable	

Cautions: 1. When the STOP mode is set, the X2 pin is internally connected to V_{DD} via a pull-up resistor to minimize the leakage current at the crystal oscillator. Thus, do not use the STOP mode in a system where an external clock is used for the main system clock.

2. Because the interrupt request signal is used to release the Standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the Standby mode is immediately released if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction. After the wait set using the oscillation stabilization time select register (OSTS), the operating mode is set.

STOP Mode Operating Status (μPD78044H Subseries)

Item \ Setting of STOP Mode		With Subsystem Clock	Without Subsystem Clock
Clock generator		Only main system clock stops oscillation	
CPU		Operation stops	
Port (output latch)		Status before STOP mode setting is held	
16-bit timer/event counter		Operation stops	
8-bit timer/event counter			
Watchdog timer			
A/D converter			
Watch timer		Operable when f_{XT} is selected for the count clock	Operation stops
FIP controller/driver		Not operable	
Serial interface		Operable when externally supplied clock is specified as the serial clock	
External interrupt request	INTP0	Not operable	
	INTP1 to INTP3	Operable	

Cautions: 1. When the STOP mode is set, the X2 pin is internally connected to V_{DD} via a pull-up resistor to minimize the leakage current at the crystal oscillator. Thus, do not use the STOP mode in a system where an external clock is used for the main system clock.

2. Because the interrupt request signal is used to release the Standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the Standby mode is immediately released if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction. After the wait set using the oscillation stabilization time select register (OSTS), the operating mode is set.

(17) Reset function

The following operations generate a reset signal:

- External reset input via the $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer in Watchdog Timer mode

Table 6-17. Hardware Status After Reset (1/2)

Hardware		Status After Reset
Program counter (PC) Note 1		Contents of reset vector tables (0000H, 0001H) are set
Stack pointer (SP)		Undefined
Program status word (PSW)		02H
RAM	Data memory	Undefined Note 2
	General-purpose register	Undefined Note 2
Port (output latch)	Ports 0 to 3, Ports 7 to 12 (P0 to P3, P7 to P12)	00H
Port mode registers	(PM0, PM7)	1FH
	(PM1 to PM3, PM11, PM12)	FFH
Pull-up resistor option register (PUO)		00H
Processor clock control register (PCC)		04H
Internal memory size switching register (IMS)		**Note 3**
Internal expansion RAM size switching register (IXS) Note 4		0AH
Oscillation stabilization time select register (OSTS)		04H
16-bit timer/event counter	Timer register (TM0)	00H
	Compare register (CR00)	Undefined
	Capture register (CR01)	Undefined
	Clock select register (TCL0)	00H
	Mode control register (TMC0)	00H
	Output control register (TOC0)	00H
8-bit timer/event counter	Timer registers (TM1, TM2)	00H
	Compare registers (CR10, CR20)	Undefined
	Clock select register (TCL1)	00H
	Mode control registers (TMC1, TMC2)	00H
	Output control register (TOC1)	00H
Watch timer	Clock select register (TCL2)	00H
Watchdog timer		
	Mode register (WDTM)	00H
6-bit up/down counter (**Note 5**)	Counter (UDC)	00H
	Compare register (UDC)	00H
	Mode register (UDM)	00H
Serial interface	Clock select register (TCL3)	88H
	Shift registers (SIO0 Note 5, SIO1)	Undefined
	Mode registers (CSIM0 Note 5, CSIM1)	00H
	Serial bus interface control register (SBIC) Note 5	00H
	Slave address register (SVA) Note 5	Undefined

Table 6-17. Hardware Status After Reset (2/2)

Hardware		Status After Reset
Serial interface (**Note 5**)	Automatic data transmit/receive control register (ADTC)	00H
	Automatic data transmit/receive address pointer (ADTP)	00H
	Automatic data transmit/receive interval specification register (ADTI)	00H
	Interrupt timing specification register (SINT)	00H
A/D converter	Mode register (ADM)	01H
	Conversion result register (ADCR)	Undefined
	Input select register (ADIS)	00H
FIP controller/ driver	Display mode register 0 (DSPM0)	00H
	Display mode register 1 (DSPM1)	00H
Interrupt	Request flag registers (IF0L, IF0H)	00H
	Mask flag registers (MK0L, MK0H)	FFH
	Priority specification flag registers (PR0L, PR0H)	FFH
	External interrupt mode register (INTM0)	00H
	Sampling clock select register (SCS)	00H

Notes: 1. During reset input or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. If the reset signal is input in the Standby mode, the status before reset is retained even after reset.

3. The value after reset differs depending on the product, as follows:

	μPD78042F	μPD78043F	μPD78044F μPD78044H	μPD78045F μPD78045H	μPD78046H	μPD78P048A μPD78P048B
IMS	44H	46H	C8H	CAH	CCH	CFH

4. This register is provided to the μPD78P048A and 78P048B (PROM version) only.

5. The following registers are provided by μPD78044F Subseries products only:
UDC, UDCC, UDM, SIO0, CSIM0, SBIC, SVA, ADTC, ADTP, ADTI, SINT.

(18) Register controlling internal memory capacity

The μPD78P048A and 78P048B allow users to select the internal memory capacity.
The following register is used to control the internal memory capacity:

- Internal memory size switching register (IMS)

To map the memory of the μPD78P048A or 78P048B identically to that of a mask ROM version, the value at the time the mask ROM version is reset must be set.

For the mask ROM version, IMS need not be set.

Format of Internal Memory Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

ROM3	ROM2	ROM1	ROM0	Selects internal ROM capacity
0	1	0	0	16K Note 1
0	1	1	0	24K Note 1
1	0	0	0	32K
1	0	1	0	40K
1	1	0	0	48K Note 2
1	1	1	1	60K
Settings other than above are prohibited				

RAM2	RAM1	RAM0	Selects internal high-speed RAM capacity
0	1	0	512 bytes Note 1
1	1	0	1024 bytes
Settings other than above are prohibited			

Notes: 1. Setting prohibited for μPD78P048B.
2. Setting prohibited for μPD78P048A.

The following table shows the set value of IMS by which to map the memory of the μPD78P048A or 78P048B identically to that of a mask ROM version.

Set Value of Internal Memory Size Switching Register

Target Mask ROM Version	Set Value of IMS
μPD78042F	44H
μPD78043F	46H
μPD78044F, 78044H	C8H
μPD78045F, 78045H	CAH
μPD78046H	CCH

Caution: When using a mask ROM version, do not set a value to IMS other than those shown in the table above.

(19) Register controlling internal expansion RAM capacity

The μPD78P048A and 78P048B allow users to select the internal expansion RAM capacity.
The following register is used to control the internal expansion RAM capacity:

- Internal expansion RAM size switching register (IXS)

Format of Internal Expansion RAM Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IXS	0	0	0	0	IX RAM3	IX RAM2	IX RAM1	IX RAM0	FFF4H	0AH	W

IX RAM3	IX RAM2	IX RAM1	IX RAM0	Selects internal expansion RAM capacity
1	0	1	0	1024 bytes
1	1	0	0	No internal expansion RAM
Settings other than above are prohibited				

The following table shows the set value of IXS by which to map the internal expansion RAM of the μPD78P048A/48B identically to the memory of a mask ROM version.

Set Value of Internal Expansion RAM Size Switching Register

Target Mask ROM Version	Set Value of IXS
μPD78042F	0CH
μPD78043F	
μPD78044F, 78044H	
μPD78045F, 78045H	
μPD78046H	

Remark: IXS is only incorporated in the μPD78P048A and 78P048B. However, if a write instruction to this register is executed in the mask ROM version, the operation is not affected.

[MEMO]

6.5 μPD78054, 78058F, and 780058 Subseries

6.5.1 Documentation Reference Information

Device Series Number	User's Manual Number	Date Published
μPD78054, 54Y	U11747EJ5V0UM00	April 1998
μPD78058F, 58FY	U12068EJ2V0UM00	April 1998
μPD780058, 58Y	U12013EJ2V0UM00	February 1998

Caution: The user should check the current User's Manual with the information in this section to be sure of having the most up-to-date information.

6.5.2 Device Series Differences

Device Series Number	ROM and RAM Differences		Number of Serial Channels
	ROM Size	RAM Size	
μPD78054, 78054Y	16K/24K/32K/40K/48K/60K	512/1K	3
μPD78058F, 78058FY	48K/60K	1K	
μPD780058, 780058Y	24K/32K/40K/48K/60K		

General Programmer's Note

The NEC C-compiler and the NEC Assembler are capable of recognizing certain symbolic SFR bit names. These special bit names are identified in the user manual in one of the four ways shown below:

1. <7>
2. (7)
3. ⑦
4. [7]

Example:

	<7>	<6>	<5>	<4>	3	2	1	0
PCC	MCC	FRC	CLS	CSS	0	PCC2	PCC1	PCC0

If a bit number has one of the four symbols around it, the NEC software will recognize the associated symbolic bit name. For example to set bit 7, the user can write the code in two ways:

```
1.    SET1    MCC
2.    SET1    PCC.7
```

Alternatively since bit 2 does not have any of the four symbols around it, the user can only set this bit as follows:

```
1.    SET1    PCC.2
```

Note: The attempt to employ a symbolic name of bit-2 (PCC2) will return an error. Thus the use of instruction

```
SET1    PCC2
```

is improper since neither the NEC C-compiler nor the NEC Assembler recognizes this symbolic name and will generate an error.

6.5.3 Memory Address Space

Each model in the μPD78054/54Y, 78058F/58FY, and 780058/58Y Subseries can access a memory space of 64K. Figures 6-24 through 6-29 show memory maps of the respective models.

Figure 6-24. Memory Map (μPD78052/52Y)

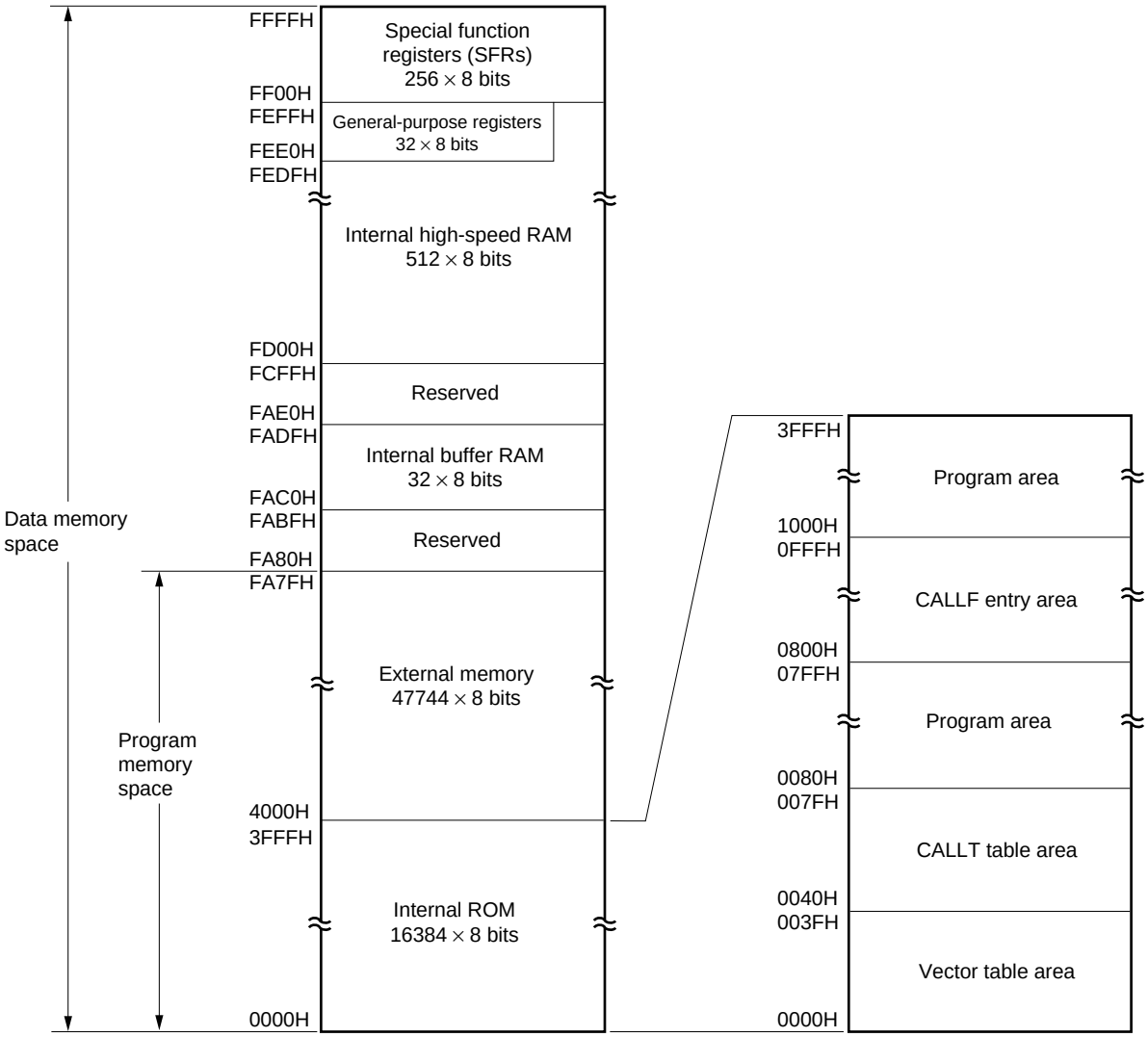


Figure 6-25. Memory Map (μPD78053/53Y, 780053/53Y)

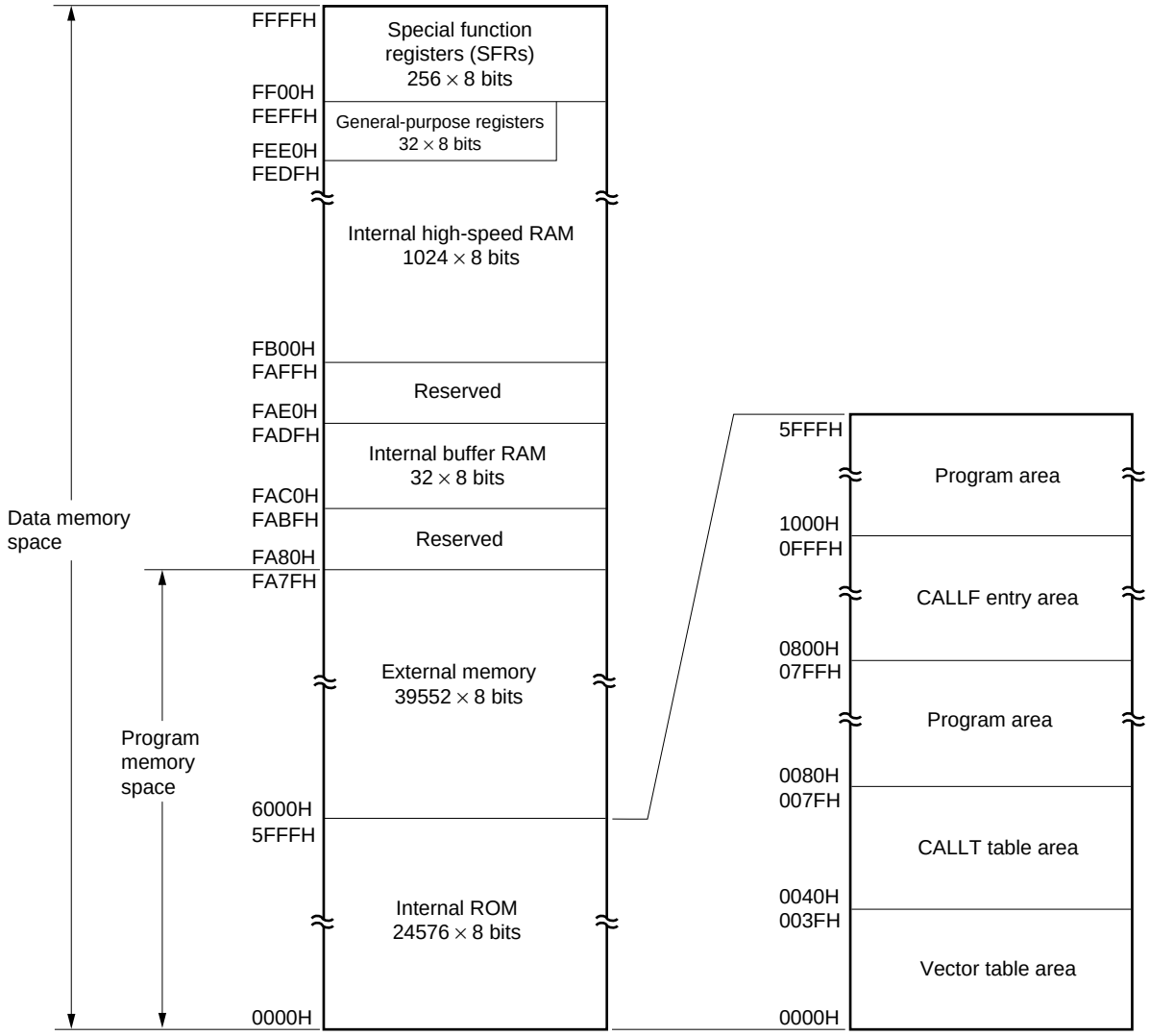


Figure 6-26. Memory Map (μPD78054/54Y, 78P054, 780054/54Y)

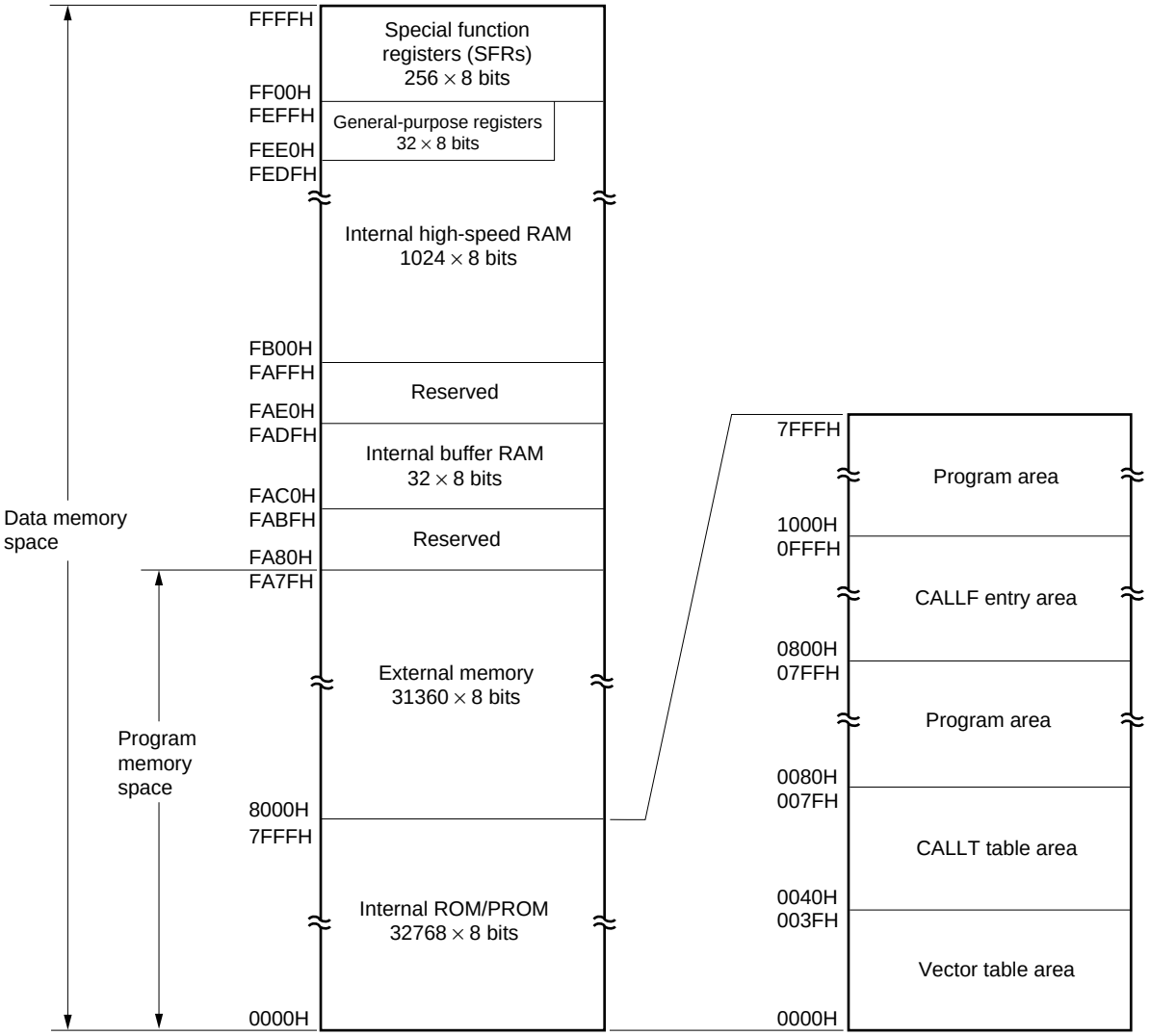


Figure 6-27. Memory Map (μPD78055/55Y, 780055/55Y)

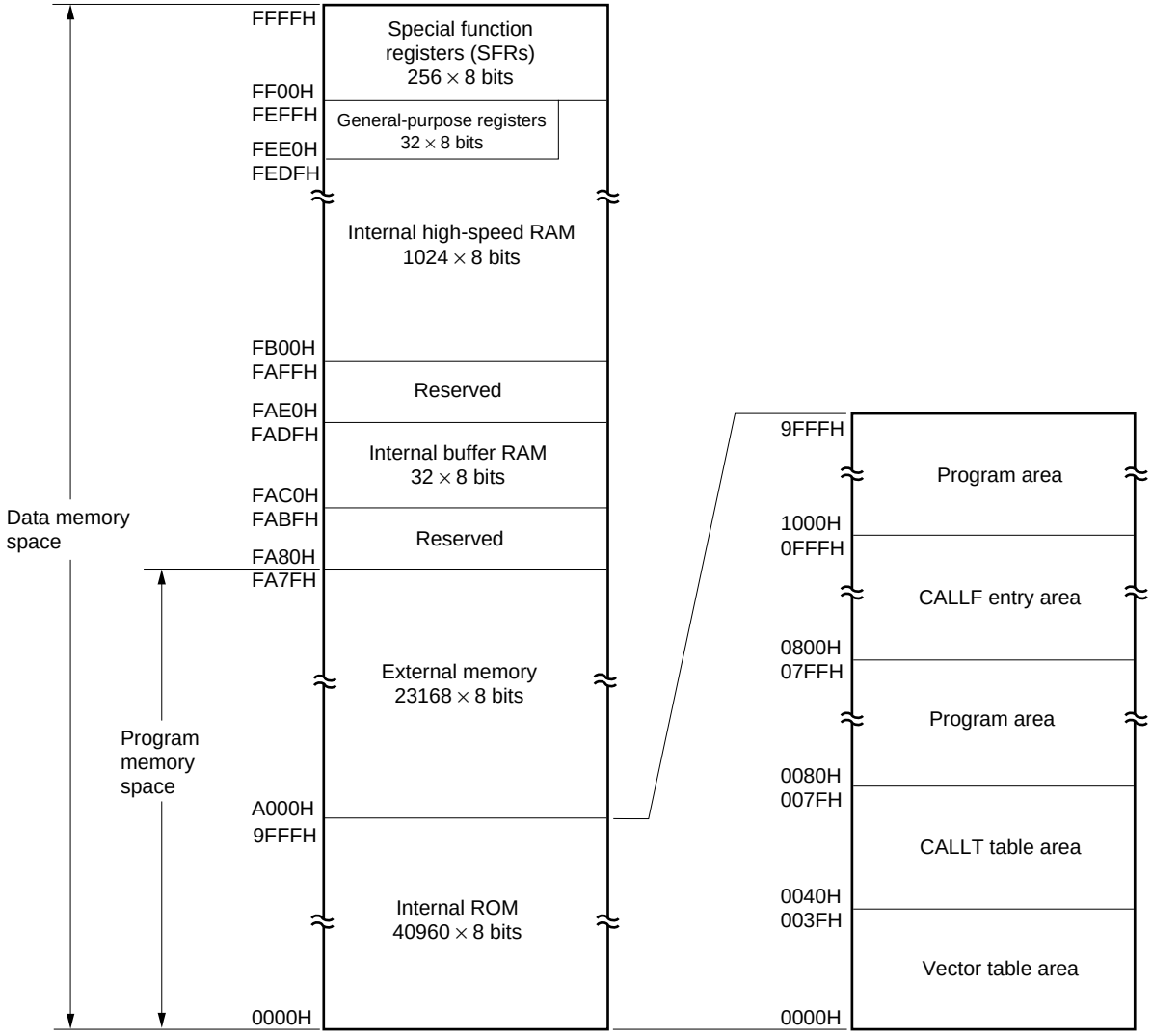


Figure 6-28. Memory Map (μPD78056/56Y, 78056F/56FY, 780056/56Y)

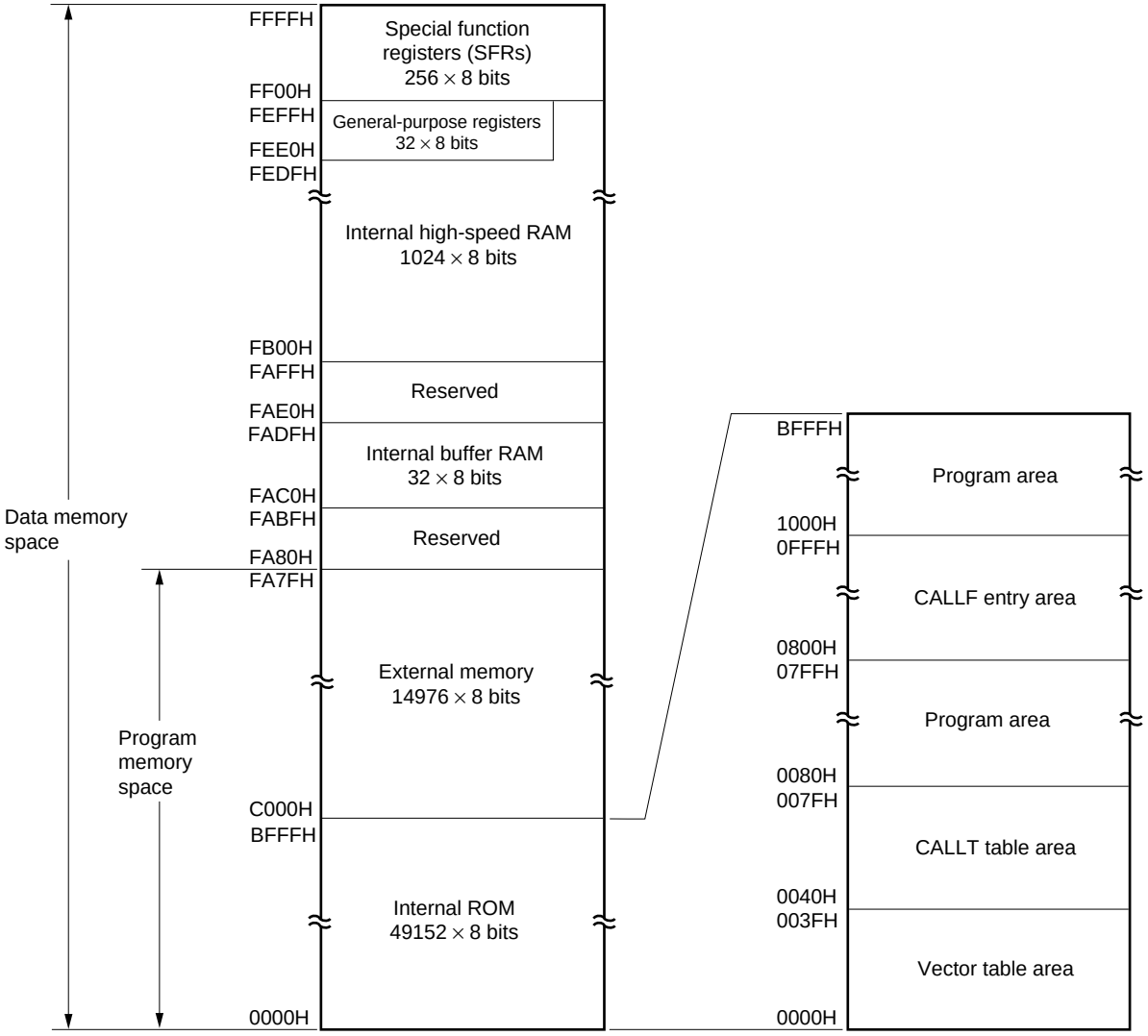
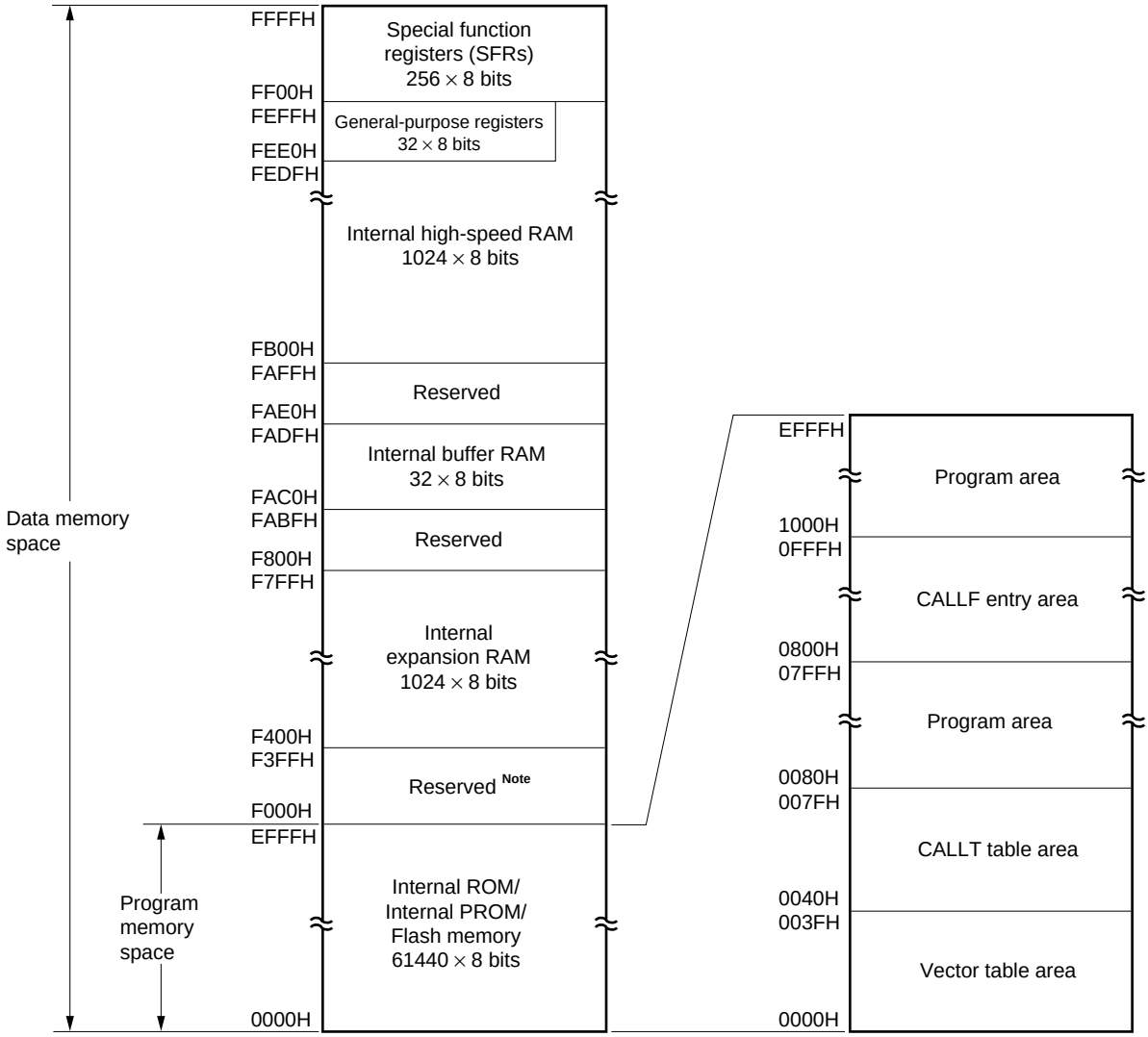


Figure 6-29. Memory Map (μPD78058/58Y, 78P058/58Y, 78058F/58FY, 78P058F/58FY, 780058/58Y, 78F0058/58Y)



Note: When internal ROM, internal PROM, or Flash memory size is 60K, the area F000H to F3FFH cannot be used. F000H to F3FFH can be used as external memory by setting the internal ROM/PROM/Flash memory size to less than 56K via the internal memory size switching register (IMS).

6.5.4 Special Function Registers (SFRs)

Table 6-18. Special Function Register List (μPD78054/54Y, 78058F/58FY, and 780058/58Y Subseries) (1/3)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulatable Bit Unit			After Reset
					1 Bit	8 Bits	16 Bits	
FF00H	Port 0	P0		R/W	√	√	–	00H
FF01H	Port 1	P1			√	√	–	
FF02H	Port 2	P2			√	√	–	
FF03H	Port 3	P3			√	√	–	
FF04H	Port 4	P4			√	√	–	Undefined
FF05H	Port 5	P5			√	√	–	
FF06H	Port 6	P6			√	√	–	
FF07H	Port 7	P7			√	√	–	00H
FF0CH	Port 12	P12			√	√	–	
FF0DH	Port 13	P13			√	√	–	
FF10H FF11H	Capture/compare register 00	CR00			–	–	√	Undefined
FF12H FF13H	Capture/compare register 01	CR01			–	–	√	
FF14H FF15H	16-bit timer register	TM0		R	–	–	√	0000H
FF16H	Compare register 10	CR10		R/W	–	√	–	Undefined
FF17H	Compare register 20	CR20			–	√	–	
FF18H	8-bit timer register 1	TMS	TM1	R	–	√	√	00H
FF19H	8-bit timer register 2		TM2		–	√		
FF1AH	Serial I/O shift register 0	SIO0		R/W	–	√	–	Undefined
FF1BH	Serial I/O shift register 1	SIO1			–	√	–	
FF1FH	A/D conversion result register	ADCR		R	–	√	–	
FF20H	Port mode register 0	PM0		R/W	√	√	–	FFH
FF21H	Port mode register 1	PM1			√	√	–	
FF22H	Port mode register 2	PM2			√	√	–	
FF23H	Port mode register 3	PM3			√	√	–	
FF25H	Port mode register 5	PM5			√	√	–	
FF26H	Port mode register 6	PM6			√	√	–	
FF27H	Port mode register 7	PM7			√	√	–	
FF2CH	Port mode register 12	PM12			√	√	–	
FF2DH	Port mode register 13	PM13			√	√	–	
FF30H	Real-time output buffer register L	RTBL			–	√	–	00H
FF31H	Real-time output buffer register H	RTBH			–	√	–	
FF34H	Real-time output port mode register	RTPM			√	√	–	
FF36H	Real-time output port control register	RTPC			√	√	–	

Table 6-18. Special Function Register List (μPD78054/54Y, 78058F/58FY, and 780058/58Y Subseries) (2/3)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulatable Bit Unit			After Reset
				1 Bit	8 Bits	16 Bits	
FF38H FF39H	Correction address register 0 Note 1	CORAD0	R/W	–	–	√	0000H
FF3AH FF3BH	Correction address register 1 Note 1	CORAD1		–	–	√	
FF40H	Timer clock select register 0	TCL0		√	√	–	00H
FF41H	Timer clock select register 1	TCL1		–	√	–	
FF42H	Timer clock select register 2	TCL2		–	√	–	
FF43H	Timer clock select register 3	TCL3		–	√	–	88H
FF47H	Sampling clock select register	SCS		–	√	–	00H
FF48H	16-bit timer mode control register	TMC0		√	√	–	
FF49H	8-bit timer mode control register 1	TMC1		√	√	–	
FF4AH	Watch timer mode control register	TMC2		√	√	–	
FF4CH	Capture/compare control register 0	CRC0		√	√	–	04H
FF4EH	16-bit timer output control register	TOC0		√	√	–	00H
FF4FH	8-bit timer output control register	TOC1		√	√	–	
FF60H	Serial operation mode register 0	CSIM0		√	√	–	
FF61H	Serial bus interface control register	SBIC		√	√	–	
FF62H	Slave address register	SVA		–	√	–	Undefined
FF63H	Interrupt timing specification register	SINT		√	√	–	00H
FF68H	Serial operation mode register 1	CSIM1		√	√	–	
FF69H	Automatic data transmit/receive control register	ADTC		√	√	–	
FF6AH	Automatic data transmit/receive address pointer	ADTP		–	√	–	
FF6BH	Automatic data transmit/receive interval specification register	ADTI		√	√	–	
FF70H	Asynchronous serial interface mode register	ASIM		√	√	–	
FF71H	Asynchronous serial interface status register	ASIS	R	–	√	–	
FF72H	Serial operation mode register 2	CSIM2	R/W	√	√	–	
FF73H	Baud rate generator control register	BRGC		–	√	–	
FF74H	Transmit shift register	TXS, SIO2	W	–	√	–	FFH
	Receive buffer register	RXB	R				
FF75H	Serial interface pin select register Note 2	SIPS	R/W	√	√	–	00H
FF80H	A/D converter mode register	ADM		√	√	–	01H
FF84H	A/D converter input select register	ADIS		–	√	–	00H
FF8AH	Correction control register Note 1	CORCN		√	√	–	
FF90H	D/A conversion value set register 0	DACS0		–	√	–	
FF91H	D/A conversion value set register 1	DACS1		–	√	–	
FF98H	D/A converter mode register	DAM		√	√	–	

Notes: 1. This register is provided for the μPD78058/58F, 78P058/58F, 78058Y/58FY, 78P058Y/58FY, 780058/58Y, and 78F0058/58Y only.

2. This register is provided for μPD780058/58Y Subseries products only.

Table 6-18. Special Function Register List (μPD78054/54Y, 78058F/58FY, and 780058/58Y Subseries) (3/3)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulatable Bit Unit			After Reset
					1 Bit	8 Bits	16 Bits	
FFD0H to FFDFH	External access area Note 1			R/W	√	√	–	Undefined
FFE0H	Interrupt request flag register 0L	IF0	IF0L		√	√	√	00H
FFE1H	Interrupt request flag register 0H		IF0H		√	√		
FFE2H	Interrupt request flag register 1L	IF1L			√	√	–	
FFE4H	Interrupt request mask register 0L	MK0	MK0L		√	√	√	FFH
FFE5H	Interrupt request mask register 0H		MK0H		√	√		
FFE6H	Interrupt request mask register 1L	MK1L			√	√	–	
FFE8H	Priority order specification flag register 0L	PR0	PR0L		√	√	√	
FFE9H	Priority order specification flag register 0H		PR0H		√	√		
FFEAH	Priority order specification flag register 1L	PR1L			√	√	–	
FFECH	External interrupt mode register 0	INTM0			–	√	–	00H
FFEDH	External interrupt mode register 1	INTM1			–	√	–	
FFF0H	Internal memory size switching register	IMS			–	√	–	**Note 2**
FFF2H	Oscillation mode select register	OSMS		W	–	√	–	00H
FFF3H	Pull-up resistor option register H	PUOH		R/W	√	√	–	
FFF4H	Internal expansion RAM size switching register Note 3	IXS		W	–	√	–	0AH
FFF6H	Key return mode register	KRM		R/W	√	√	–	02H
FFF7H	Pull-up resistor option register L	PUOL			√	√	–	00H
FFF8H	Memory expansion mode register	MM			√	√	–	10H
FFF9H	Watchdog timer mode register	WDTM			√	√	–	00H
FFFAH	Oscillation stabilization time select register	OSTS			–	√	–	04H
FFFBH	Processor clock control register	PCC			√	√	–	

Notes: 1. The external access area cannot be accessed in SFR addressing. Access the area with direct addressing.

2. The value after reset differs depending on the product, as follows:

	μPD78052 μPD78052Y	μPD78053 μPD78053Y μPD780053 μPD780053Y	μPD78054 μPD78054Y μPD78P054 μPD780054 μPD780054Y	μPD78055 μPD78055Y μPD780055 μPD780055Y	μPD78056 μPD78056Y μPD78056F μPD78056FY μPD780056 μPD780056Y	μPD78058 μPD78058Y μPD78058F μPD78058FY μPD780058 μPD780058Y	μPD78P058 μPD78P058Y μPD78P058F μPD78P058FY μPD78F0058 μPD78F0058Y
IMS	44H	C6H	C8H	CAH	CCH	CFH	

3. This register is provided for the μPD78058/58Y, 78058F/58FY, 78P058/58Y, 78P058F/58FY, 780058/58Y, and 78F0058/58Y only.

(1) Registers controlling port functions

The following four types of registers control the ports:

- Port mode registers (PM0 to PM7, PM12, PM13)
- Pull-up resistor option registers (PUOH, PUOL)
- Memory expansion mode register (MM)
  - Refer to section (18) for the register format.
- Key return mode register (KRM)
  - Refer to section (17) for the register format.

Format of Port Mode Registers (μPD78054/54Y and 78058F/58FY Subseries)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	1	FF20H	FFH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W
PM3	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	FF23H	FFH	R/W
PM4	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	FF24H	FFH	R/W
PM5	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	FF25H	FFH	R/W
PM6	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	FF26H	FFH	R/W
PM7	1	1	1	1	1	PM72	PM71	PM70	FF27H	FFH	R/W
PM12	PM127	PM126	PM125	PM124	PM123	PM122	PM121	PM120	FF2CH	FFH	R/W
PM13	1	1	1	1	1	1	PM131	PM130	FF2DH	FFH	R/W

PMmn	Pmn pin input/output mode selection (m = 0 to 3, 5 to 7, 12, 13 : n = 0 to 7)
0	Output mode (output buffer ON)
1	Input mode (output buffer OFF)

Format of Port Mode Registers (μPD780058/58Y Subseries)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PM0	1	1	PM05	PM04	PM03	PM02	PM01	1	FF20H	FFH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W
PM3	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	FF23H	FFH	R/W
PM4	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	FF24H	FFH	R/W
PM5	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	FF25H	FFH	R/W
PM6	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	FF26H	FFH	R/W
PM7	1	1	1	1	1	PM72	PM71	PM70	FF27H	FFH	R/W
PM12	PM127	PM126	PM125	PM124	PM123	PM122	PM121	PM120	FF2CH	FFH	R/W
PM13	1	1	1	1	1	1	PM131	PM130	FF2DH	FFH	R/W

PMmn	Pmn pin input/output mode selection (m = 0 to 3, 5 to 7, 12, 13 : n = 0 to 7)
0	Output mode (output buffer ON)
1	Input mode (output buffer OFF)

Format of Pull-up Resistor Option Registers

Symbol	7	6	<5>	<4>	3	2	1	0	Address	After Reset	R/W
PUOH	0	0	PUO13	PUO12	0	0	0	0	FFF3H	00H	R/W

	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>			
PUOL	PUO7	PUO6	PUO5	PUO4	PUO3	PUO2	PUO1	PUO0	FFF7H	00H	R/W

PUOm	Pm internal pull-up resistor selection (m = 0 to 7, 12, 13)
0	Internal pull-up resistor not used
1	Internal pull-up resistor used

Cautions: 1. P00 and P07 pins do not incorporate a pull-up resistor.

2. When ports 1, 4, 5, and P64 to P67 pins are used as alternate function pins, an on-chip pull-up resistor cannot be used even if 1 is set in the PUOm bit of PUOH, PUOL (m = 1, 4 to 6).

3. Pins P60 to P63 can be connected with a pull-up resistor by the mask option only for the mask ROM version.

4. Bits 0 to 3, 6, and 7 of PUOH should be set to 0.

(2) Registers controlling clock generator

The following two registers control the clock generator:

- Processor clock control register (PCC)
- Oscillation mode select register (OSMS)

Format of Processor Clock Control Register

Symbol	<7>	<6>	<5>	<4>	3	2	1	0	Address	After Reset	R/W
PCC	MCC	FRC	CLS	CSS	0	PCC2	PCC1	PCC0	FFFBH	04H	R/W Note 1

R/W	CSS	PCC2	PCC1	PCC0	CPU clock (f_{CPU}) selection		
						MCS = 1	MCS = 0
	0	0	0	0	f_{XX}	f_X (0.4 μs)	$f_X/2$ (0.8 μs)
		0	0	1	$f_{XX}/2$	$f_X/2$ (0.8 μs)	$f_X/2^2$ (1.6 μs)
		0	1	0	$f_{XX}/2^2$	$f_X/2^2$ (1.6 μs)	$f_X/2^3$ (3.2 μs)
		0	1	1	$f_{XX}/2^3$	$f_X/2^3$ (3.2 μs)	$f_X/2^4$ (6.4 μs)
		1	0	0	$f_{XX}/2^4$	$f_X/2^4$ (6.4 μs)	$f_X/2^5$ (12.8 μs)
	1	0	0	0	$f_{XT}/2$ (122 μs)		
		0	0	1			
		0	1	0			
		0	1	1			
		1	0	0			
	Settings other than above are prohibited						

R	CLS	CPU clock status
	0	Main system clock
	1	Subsystem clock

R/W	FRC	Subsystem clock feedback resistor selection
	0	Internal feedback resistor used
	1	Internal feedback resistor not used

R/W	MCC	Main system clock oscillation control Note 2
	0	Oscillation possible
	1	Oscillation stopped

Notes: 1. Bit 5 is a read-only bit.

2. When the CPU is operating on the subsystem clock, MCC should be used to stop the main system clock oscillation. A STOP instruction should not be used.

Caution: Bit 3 must be set to 0.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)

f_X: Main system clock oscillator frequency

f_{XT}: Subsystem clock oscillator frequency

MCS: Bit 0 of oscillation mode select register (OSMS)

Values in parentheses indicate minimum instruction execution time: $2/f_{CPU}$ when operating at f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

Format of Oscillation Mode Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
OSMS	0	0	0	0	0	0	0	MCS	FFF2H	00H	W

MCS	Main system clock scaler control
0	Scaler used
1	Scaler not used

Caution: The main system clock cycle is longer by up to 2/fx only when writing data to OSMS (including when writing the same data that was written previously). This causes a temporary error in the count clock cycle of timers in the peripheral hardware that operates with the main system clock. In addition, when the oscillation mode is changed, the clocks provided for the peripheral hardware as well as those for the CPU are switched. Therefore, it is recommended that only one-time writing to OSMS be performed between the reset release and the peripheral hardware operation.

(3) Registers controlling 16-bit timer/event counter

The following seven registers control the 16-bit timer/event counter:

- Timer clock select register 0 (TCL0)
- 16-bit timer mode control register (TMC0)
- Capture/compare control register 0 (CRC0)
- 16-bit timer output control register (TOC0)
- Port mode register 3 (PM3)
  - Refer to section (1) for the register format.
- External interrupt mode register 0 (INTM0)
  - Refer to section (16) for the register format.
- Sampling clock select register (SCS)
  - Refer to section (16) for the register format.

Format of Timer Clock Select Register 0

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL0	CLOE	TCL06	TCL05	TCL04	TCL03	TCL02	TCL01	TCL00	FF40H	00H	R/W

This section controls the clock output circuit.
Refer to **(7) Registers controlling clock output function** or **Chapter 12** of *µPD78054, 78054Y Subseries User's Manual*, **Chapter 12** of *µPD78058F, 78058FY Subseries User's Manual*, or **Chapter 12** of *µPD780058, 780058Y Subseries User's Manual* for detailed information.

TCL06	TCL05	TCL04	16-bit timer register count clock selection		
				MCS = 1	MCS = 0
0	0	0	TI00 (Valid edge specifiable)		
0	0	1	$2f_{XX}$	Setting prohibited	f_X (5.0 MHz)
0	1	0	f_{XX}	f_X (5.0 MHz)	$f_X/2$ (2.5 MHz)
0	1	1	$f_{XX}/2$	$f_X/2$ (2.5 MHz)	$f_X/2^2$ (1.25 MHz)
1	0	0	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	1	1	Watch timer output (INTTM3)		
Settings other than above are prohibited					

Cautions: 1. Setting of the TI00/INTP0 pin valid edge is performed by external interrupt mode register 0, and selection of the sampling clock frequency is performed by the sampling clock select register.

2. To read the count value when TI00 has been specified as the TM0 count clock, the value should be read from TM0, not from capture/compare register 01 (CR01).

3. To write data other than that already written to TCL0, stop the timer operation once.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)

f_X: Main system clock oscillation frequency

TI00: 16-bit timer/event counter input pin

TM0: 16-bit timer register

MCS: Bit 0 of oscillation mode select register (OSMS)

Values in parentheses apply to operation with f_X = 5.0 MHz.

This register is also used to set the clock for PCL output, in addition to setting the count clock of the 16-bit timer register.

Format of 16-Bit Timer Mode Control Register

Symbol	7	6	5	4	3	2	1	<0>	Address	After Reset	R/W
TMC0	0	0	0	0	TMC03	TMC02	TMC01	OVF0	FF48H	00H	R/W

OVF0	16-bit timer register overflow detection
0	Overflow not detected
1	Overflow detected

TMC03	TMC02	TMC01	Operating mode Clear mode selection	TO0 output timing selection	Interrupt generation
0	0	0	Operation stop (TM0 cleared to 0)	No change	Not generated
0	0	1	PWM mode (free running)	PWM pulse output	Generated on match between TM0 and CR00 or match between TM0 and CR01
0	1	0	Free-running mode	Match between TM0 and CR00 or match between TM0 and CR01	
0	1	1		Match between TM0 and CR00, match between TM0 and CR01, or TI00 valid edge	
1	0	0	Clear and start on TI00 valid edge	Match between TM0 and CR00 or match between TM0 and CR01	
1	0	1		Match between TM0 and CR00, match between TM0 and CR01, or TI00 valid edge	
1	1	0	Clear and start on match between TM0 and CR00	Match between TM0 and CR00 or match between TM0 and CR01	
1	1	1		Match between TM0 and CR00, match between TM0 and CR01, or TI00 valid edge	

Cautions: 1. The 16-bit timer register starts operation when a value other than 0, 0, 0 is set to TMC01 to TMC03 (Operation Stop mode). To stop the operation, set TMC01 to TMC03 to 0, 0, 0.

2. Switch the Clear mode and the T00 output timing after stopping the timer operation (by setting TMC01 to TMC03 to 0, 0, 0).

3. Set the valid edge of the TI00/INTP0 pin with an external interrupt mode register 0 and select the sampling clock frequency with a sampling clock select register.

4. When using the PWM mode, set the PWM mode and then set data to CR00.

5. If Clear and Start mode on a match between TM0 and CR00 is selected, when the set value of CR00 is FFFFH and the TM0 value changes from FFFFH to 0000H, the OVF0 flag is set to 1.

Remarks: TO0: 16-bit timer/event counter output pin
TI00: 16-bit timer/event counter input pin
TM0: 16-bit timer register
CR00: Compare register 00
CR01: Compare register 01

Format of Capture/Compare Control Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
CRC0	0	0	0	0	0	CRC02	CRC01	CRC00	FF4CH	04H	R/W

CRC00	CR00 operating mode selection
0	Operates as compare register
1	Operates as capture register

CRC01	CR00 capture trigger selection
0	Captures on valid edge of TI01
1	Captures on valid edge of TI00

CRC02	CR01 operating mode selection
0	Operates as compare register
1	Operates as capture register

Cautions: 1. Timer operation must be stopped before setting CRC0.

2. When Clear and Start mode on a match between TM0 and CR00 is selected with the 16-bit timer mode control register, CR00 should not be specified as a capture register.

Format of 16-Bit Timer Output Control Register

Symbol	7	<6>	<5>	4	<3>	<2>	1	<0>	Address	After Reset	R/W
TOC0	0	OSPT	OSPE	TOC04	LVS0	LVR0	TOC01	TOE0	FF4EH	00H	R/W

TOE0	16-bit timer/event counter output control
0	Output disabled (Port mode)
1	Output enabled

TOC01	In PWM mode	In other modes
	Active level selection	Timer output F/F control by match of CR00 and TM0
0	Active high	Inversion operation disabled
1	Active low	Inversion operation enabled

LVS0	LVR0	16-bit timer/event counter timer output F/F status setting
0	0	No change
0	1	Timer output F/F reset (to 0)
1	0	Timer output F/F set (to 1)
1	1	Setting prohibited

TOC04	Timer output F/F control by match of CR01 and TM0
0	Inversion operation disabled
1	Inversion operation enabled

OSPE	One-shot pulse output control
0	Continuous pulse output
1	One-shot pulse output

OSPT	Control of one-shot pulse output trigger by software
0	One-shot pulse trigger not used
1	One -shot pulse trigger used

Cautions: 1. Timer operation must be stopped before setting TOC0 (except, however, OSPT).

2. If LVS0 and LVR0 are read after data is set, they will be 0.

3. OSPT is cleared automatically after data setting, and will therefore be 0 if read.

(4) Registers controlling 8-bit timer/event counter

The following four registers control the 8-bit timer/event counters:

- Timer clock select register 1 (TCL1)
- 8-bit timer mode control register 1 (TMC1)
- 8-bit timer output control register (TOC1)
- Port mode register 3 (PM3)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 1

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL1	TCL17	TCL16	TCL15	TCL14	TCL13	TCL12	TCL11	TCL10	FF41H	00H	R/W

TCL13	TCL12	TCL11	TCL10	8-bit timer register 1 count clock selection		
					MCS = 1	MCS = 0
0	0	0	0	TI1 falling edge		
0	0	0	1	TI1 rising edge		
0	1	1	0	$f_{XX}/2$	$f_X/2$ (2.5 MHz)	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
1	1	1	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)
1	1	1	1	$f_{XX}/2^{11}$	$f_X/2^{11}$ (2.4 kHz)	$f_X/2^{12}$ (1.2 kHz)
Settings other than above are prohibited						

TCL17	TCL16	TCL15	TCL14	8-bit timer register 2 count clock selection		
					MCS = 1	MCS = 0
0	0	0	0	TI2 falling edge		
0	0	0	1	TI2 rising edge		
0	1	1	0	$f_{XX}/2$	$f_X/2$ (2.5 MHz)	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
1	1	1	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)
1	1	1	1	$f_{XX}/2^{11}$	$f_X/2^{11}$ (2.4 kHz)	$f_X/2^{12}$ (1.2 kHz)
Settings other than above are prohibited						

Caution: To write data other than that already written in TCL1, stop the timer operation once.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
TI1: 8-bit timer register 1 input pin
TI2: 8-bit timer register 2 input pin
MCS: Oscillation mode select register (OSMS) bit 0
Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of 8-Bit Timer Mode Control Register 1

Symbol	7	6	5	4	3	2	<1>	<0>	Address	After Reset	R/W
TMC1	0	0	0	0	0	TMC12	TCE2	TCE1	FF49H	00H	R/W

TCE1	8-bit timer register 1 operation control
0	Operation stop (TM1 clear to 0)
1	Operation enable

TCE2	8-bit timer register 2 operation control
0	Operation stop (TM2 clear to 0)
1	Operation enable

TMC12	Operating mode selection
0	8-bit timer register × 2 channel mode (TM1, TM2)
1	16-bit timer register × 1 channel mode (TMS)

Cautions: 1. Stop the timer operation before switching the operation mode.

2. When used as a 16-bit timer register, TCE1 should be used to control enable/stop operations.

Format of 8-Bit Timer Output Control Register

Symbol	<7>	<6>	5	<4>	<3>	<2>	1	<0>	Address	After Reset	R/W
TOC1	LVS2	LVR2	TOC15	TOE2	LVS1	LVR1	TOC11	TOE1	FF4FH	00H	R/W

TOE1	8-bit timer/event counter 1 outptut control
0	Output disable (Port mode)
1	Output enable

TOC11	8-bit timer/event counter 1 timer output F/F control
0	Inverted operation disable
1	Inverted operation enable

LVS1	LVR1	8-bit timer/event counter 1 timer output F/F status set
0	0	Unchanged
0	1	Timer output F/F reset (to 0)
1	0	Timer output F/F set (to 1)
1	1	Setting prohibited

TOE2	8-bit timer/event counter 2 output control
0	Output disable (Port mode)
1	Output enable

TOC15	8-bit timer/event counter 2 timer output F/F control
0	Inverted operation disable
1	Inverted operation enable

LVS2	LVR2	8-bit timer/event counter 2 timer output F/F status set
0	0	Unchanged
0	1	Timer output F/F reset (to 0)
1	0	Timer output F/F set (to 1)
1	1	Setting prohibited

Cautions: 1. Be sure to set TOC1 after stopping the timer operation.

2. After data setting, 0 can be read from LVS1, LVS2, LVR1, and LVR2.

(5) Registers controlling watch timer

The following two registers control the watch timer:

- Timer clock select register 2 (TCL2)
- Watch timer mode control register (TMC2)

Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL2	TCL27	TCL26	TCL25	TCL24	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

This section controls the watchdog timer.
Refer to **(6) Registers controlling watchdog timer** or
Chapter 11 of *μPD78054, 78054Y Subseries User's Manual*,
Chapter 11 of *μPD78058F, 78058FY Subseries User's Manual*, or
Chapter 11 of *μPD780058, 780058Y Subseries User's Manual*
for detailed information.

This section controls the buzzer output function.
Refer to **(8) Registers controlling buzzer output function** or
Chapter 13 of *μPD78054, 78054Y Subseries User's Manual*,
Chapter 13 of *μPD78058F, 78058FY Subseries User's Manual*, or
Chapter 13 of *μPD780058, 780058Y Subseries User's Manual*
for detailed information.

TCL24	Watch timer count clock selection		
		MCS = 1	MCS = 0
0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	f_{XT} (32.768 kHz)		

Caution: When rewriting TCL2 to other data, stop the timer operation beforehand.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
f_{XT}: Subsystem clock oscillation frequency
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

Format of Watch Timer Mode Control Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TMC2	0	TMC26	TMC25	TMC24	TMC23	TMC22	TMC21	TMC20	FF4AH	00H	R/W

TMC20	Watch operating mode selection
0	Normal operating mode (flag set at $f_W/2^{14}$)
1	Fast feed operating mode (flag set at $f_W/2^5$)

TMC21	Prescaler operation control
0	Clear after operation stop
1	Operation enable

TMC22	5-bit counter operation control
0	Clear after operation stop
1	Operation enable

TMC23	Watch flag set time selection		
	f_{XX} = 5.0 MHz operation	f_{XX} = 4.19 MHz operation	f_{XT} = 32.768 kHz operation
0	$2^{14}/f_W$ (0.4 sec)	$2^{14}/f_W$ (0.5 sec)	$2^{14}/f_W$ (0.5 sec)
1	$2^{13}/f_W$ (0.2 sec)	$2^{13}/f_W$ (0.25 sec)	$2^{13}/f_W$ (0.25 sec)

TMC26	TMC25	TMC24	Prescaler interval time selection		
			f_{XX} = 5.0 MHz operation	f_{XX} = 4.19 MHz operation	f_{XT} = 32.768 kHz operation
0	0	0	$2^4/f_W$ (410 μs)	$2^4/f_W$ (488 μs)	$2^4/f_W$ (488 μs)
0	0	1	$2^5/f_W$ (819 μs)	$2^5/f_W$ (977 μs)	$2^5/f_W$ (977 μs)
0	1	0	$2^6/f_W$ (1.64 ms)	$2^6/f_W$ (1.95 ms)	$2^6/f_W$ (1.95 ms)
0	1	1	$2^7/f_W$ (3.28 ms)	$2^7/f_W$ (3.91 ms)	$2^7/f_W$ (3.91 ms)
1	0	0	$2^8/f_W$ (6.55 ms)	$2^8/f_W$ (7.81 ms)	$2^8/f_W$ (7.81 ms)
1	0	1	$2^9/f_W$ (13.1 ms)	$2^9/f_W$ (15.6 ms)	$2^9/f_W$ (15.6 ms)
Settings other than above are prohibited					

Caution: When the watch timer is used, the prescaler should not be cleared frequently.

Remarks: f_W: Watch timer clock frequency ($f_{XX}/2^7$ or f_{XT})

f_{XX}: Main system clock frequency (f_X or $f_X/2$)

f_X: Main system clock oscillation frequency

f_{XT}: Subsystem clock oscillation frequency

A 0.5 second interval can be generated either with a 4.19304 MHz main system clock or a 32.768 kHz sub system clock

(6) Registers controlling watchdog timer

The following two registers control the watchdog timer:

- Timer clock select register 2 (TCL2)
- Watchdog timer mode register (WDTM)

Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL2	TCL27	TCL26	TCL25	TCL24	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

This section controls the watch timer.
Refer to **(5) registers controlling watch timer** or
Chapter 10 of *μPD78054, 78054Y Subseries User's Manual*,
Chapter 10 of *μPD78058F, 78058FY Subseries User's Manual*, or
Chapter 10 of *μPD780058, 780058Y Subseries User's Manual*
for detailed information.

This section controls the buzzer output function.
Refer to **(8) Registers controlling buzzer output function** or
Chapter 13 of *μPD78054, 78054Y Subseries User's Manual*,
Chapter 13 of *μPD78058F, 78058FY Subseries User's Manual*, or
Chapter 13 of *μPD780058, 780058Y Subseries User's Manual*
for detailed information.

TCL22	TCL21	TCL20	Watchdog timer count clock selection		
				MCS = 1	MCS = 0
0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
1	1	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)
1	1	1	$f_{XX}/2^{11}$	$f_X/2^{11}$ (2.4 kHz)	$f_X/2^{12}$ (1.2 kHz)

Caution: When rewriting TCL2 to other data, first stop the timer operation.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of Watchdog Timer Mode Register

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
WDTM	RUN	0	0	WDTM4	WDTM3	0	0	0	FFF9H	00H	R/W

WDTM4	WDTM3	Watchdog timer operation mode selection Note 1
0	×	Interval Timer mode Note 2 (Maskable interrupt request occurs upon generation of an overflow.)
1	0	Watchdog Timer mode 1 (Non-maskable interrupt request occurs upon generation of an overflow.)
1	1	Watchdog Timer mode 2 (Reset operation is activated upon generation of an overflow.)

RUN	Watchdog timer operation mode selection Note 3
0	Count stops.
1	Counter is cleared and counting starts.

Notes: 1. Once set to 1, WDTM3 and WDTM4 cannot be cleared to 0 by software.

2. The watchdog timer starts operating as an interval timer as soon as RUN has been set to 1.

3. Once set to 1, RUN cannot be cleared to 0 by software.
   Thus, once counting starts, counting can only be stopped by $\overline{\text{RESET}}$ input.

Cautions: 1. When 1 is set in RUN so that the watchdog timer is cleared, the actual overflow time is up to 0.5% shorter than the time set by timer clock select register 2 (TCL2).

2. To use Watchdog Timer modes 1 and 2, make sure that the interrupt request flag (TMIF4) is 0, and then set WDTM4 to 1.
If WDTM4 is set to 1 when TMIF4 is 1, the non-maskable interrupt request occurs, regardless of the contents of WDTM3.

Remark: ×: Don't care

(7) Registers controlling clock output function

The following two registers control the clock output function:

- Timer clock select register 0 (TCL0)
- Port mode register 3 (PM3)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 0

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL0	CLOE	TCL06	TCL05	TCL04	TCL03	TCL02	TCL01	TCL00	FF40H	00H	R/W

This section controls the 16-bit timer.
Refer to **(3) Registers controlling 16-bit timer/event counter** or **Chapter 8** of *μPD78054, 78054Y Subseries User's Manual*, **Chapter 8** of *μPD78058F, 78058FY Subseries User's Manual*, or **Chapter 8** of *μPD780058, 780058Y Subseries User's Manual* for detailed information.

TCL03	TCL02	TCL01	TCL00	PCL output clock selection		
					MCS = 1	MCS = 0
0	0	0	0	f_{XT} (32.768 kHz)		
0	1	0	1	f_{XX}	f_X (5.0 MHz)	$f_X/2$ (2.5 MHz)
0	1	1	0	$f_{XX}/2$	$f_X/2$ (2.5 MHz)	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
Settings other than above are prohibited						

CLOE	PCL output control
0	Output disable
1	Output enable

Cautions: 1. When enabling PCL output, set TCL00 to TCL03, then set 1 in CLOE with a 1-bit memory manipulation instruction.

2. To write data other than that already written to TCL0, first stop the clock operation.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)

f_X: Main system clock oscillation frequency

f_{XT}: Subsystem clock oscillation frequency

MCS: Bit 0 of oscillation mode select register (OSMS)

Values in parentheses apply to operation with f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

This register is also used to set the count clock of the 16-bit timer and to set the clock for PCL output.

(8) Registers controlling buzzer output function

The following two registers control the buzzer output function:

- Timer clock select register 2 (TCL2)
- Port mode register 3 (PM3)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL2	TCL27	TCL26	TCL25	TCL24	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

This section controls the watchdog timer.
Refer to **(6) Registers controlling watchdog timer** or
Chapter 11 of *μPD78054, 78054Y Subseries User's Manual*,
Chapter 11 of *μPD78058F, 78058FY Subseries User's Manual*, or
Chapter 11 of *μPD780058, 780058Y Subseries User's Manual*
for detailed information.

This section controls the watch timer.
Refer to **(5) Registers controlling watch timer** or
Chapter 10 of *μPD78054, 78054Y Subseries User's Manual*,
Chapter 10 of *μPD78058F, 78058FY Subseries User's Manual*, or
Chapter 10 of *μPD780058, 780058Y Subseries User's Manual*
for detailed information.

TCL27	TCL26	TCL25	Buzzer output frequency selection		
				MCS = 1	MCS = 0
0	×	×	Buzzer output disable		
1	0	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)
1	0	1	$f_{XX}/2^{10}$	$f_X/2^{10}$ (4.9 kHz)	$f_X/2^{11}$ (2.4 kHz)
1	1	0	$f_{XX}/2^{11}$	$f_X/2^{11}$ (2.4 kHz)	$f_X/2^{12}$ (1.2 kHz)
1	1	1	Setting prohibited		

Caution: When rewriting TCL2 to other data, stop the timer operation beforehand.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
×: Don't care
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz.

(9) Registers controlling A/D converter

The following three registers control the A/D converter:

- A/D converter mode register (ADM)
- A/D converter input select register (ADIS)
- External interrupt mode register 1 (INTM1)
  - Refer to section (16) for the register format.

Format of A/D Converter Mode Register

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After Reset	R/W
ADM	CS	TRG	FR1	FR0	ADM3	ADM2	ADM1	HSC	FF80H	01H	R/W

ADM3	ADM2	ADM1	Analog input channel selection
0	0	0	ANI0
0	0	1	ANI1
0	1	0	ANI2
0	1	1	ANI3
1	0	0	ANI4
1	0	1	ANI5
1	1	0	ANI6
1	1	1	ANI7

FR1	FR0	HSC	A/D conversion time selection Note 1			
			f_X = 5.0 MHz operation		f_X = 4.19 MHz operation	
			MCS = 1	MCS = 0	MCS = 1	MCS = 0
0	0	1	80/f_X (Setting prohibited Note 2)	160/f_X (32.0 μs)	80/f_X (19.1 μs)	160/f_X (38.1 μs)
0	1	1	40/f_X (Setting prohibited Note 2)	80/f_X (Setting prohibited Note 2)	40/f_X (Setting prohibited Note 2)	80/f_X (19.1 μs)
1	0	0	50/f_X (Setting prohibited Note 2)	100/f_X (20.0 μs)	50/f_X (Setting prohibited Note 2)	100/f_X (23.8 μs)
1	0	1	100/f_X (20.0 μs)	200/f_X (40.0 μs)	100/f_X (23.8 μs)	200/f_X (47.7 μs)
Settings other than above are prohibited						

TRG	External trigger selection
0	No external trigger (software starts)
1	Conversion started by external trigger (hardware starts)

CS	A/D conversion operation control
0	Operation stop
1	Operation start

Notes: 1. Set so that the A/D conversion time is 19.1 μs or more.
2. Setting prohibited because A/D conversion time is less than 19.1 μs.

Cautions: 1. The following sequence is recommended for power consumption reduction of the A/D converter when the standby function is used: Clear bit 7 (CS) to 0 first to stop the A/D conversion operation, and then execute the HALT or STOP instruction.

2. When restarting the stopped A/D conversion operation, start the A/D conversion operation after clearing the interrupt request flag (ADIF) to 0.

Remarks: f_X: Main system clock oscillation frequency
MCS: Bit 0 of oscillation mode select register (OSMS)

Format of A/D Converter Input Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADIS	0	0	0	0	ADIS3	ADIS2	ADIS1	ADIS0	FF84H	00H	R/W

ADIS3	ADIS2	ADIS1	ADIS0	Number of analog input channel selection
0	0	0	0	No analog input channel (P10 to P17)
0	0	0	1	1 channel (ANI0, P11 to P17)
0	0	1	0	2 channels (ANI0, ANI1, P12 to P17)
0	0	1	1	3 channels (ANI0 to ANI2, P13 to P17)
0	1	0	0	4 channels (ANI0 to ANI3, P14 to P17)
0	1	0	1	5 channels (ANI0 to ANI4, P15 to P17)
0	1	1	0	6 channels (ANI0 to ANI5, P16, P17)
0	1	1	1	7 channels (ANI0 to ANI6, P17)
1	0	0	0	8 channels (ANI0 to ANI7)
Settings other than above are prohibited				

Cautions: 1. Set the analog input channel in the following order.

a. Set the number of analog input channels with ADIS.

b. Using A/D converter mode register (ADM), select one channel to undergo A/D conversion from among the channels set for analog input with ADIS.

2. No internal pull-up resistor can be used to the channels set for analog input with ADIS, irrespective of the value of bit 1 (PUO1) of the pull-up resistor option register L (PUOL).

(10) Register controlling D/A converter

The following register controls the D/A converter:

- D/A converter mode register (DAM)

Format of D/A Converter Mode Register

Symbol	7	6	5	4	3	2	<1>	<0>	Address	After Reset	R/W
DAM	0	0	DAM5	DAM4	0	0	DACE1	DACE0	FF98H	00H	R/W

DACE0	D/A converter channel 0 control
0	D/A conversion stop
1	D/A conversion enable

DACE1	D/A converter channel 1 control
0	D/A conversion stop
1	D/A conversion enable

DAM4	D/A converter channel 0 operating mode
0	Normal mode
1	Real-time output mode

DAM5	D/A converter channel 1 operating mode
0	Normal mode
1	Real-time output mode

Cautions: 1. When using the D/A converter, an alternate-function port pin should be set to the input mode, and a pull-up resistor should be disconnected.

2. Always set bits 2, 3, 6, and 7 to 0.

3. When D/A conversion is stopped, the output state is high impedance.

4. The output triggers are INTTM1 and INTTM2 for channel 0 and channel 1, respectively, in the real-time output mode.

(11) Registers controlling serial interface channel 0 (Non-Y Subseries)

The μPD78054, 78058F, and 780058 Subseries are provided with three channels of serial interfaces. The differences among channels 0, 1, and 2 are indicated in the table below.

Differences Among Channels 0, 1, and 2

Serial Transfer Mode		Channel 0	Channel 1	Channel 2
3-wire serial I/O	Clock selection	$f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, $f_{XX}/2^8$, external clock, TO2 output	$f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, $f_{XX}/2^8$, external clock, TO2 output	External clock [Note], baud rate generator output
	Transfer method	MSB/LSB first switchable	MSB/LSB first switchable Automatic transmit/receive function	MSB/LSB first switchable
	Transfer end flag	Serial transfer end interrupt request flag (CSIIF0)	Serial transfer end interrupt request flag (CSIIF1)	Serial transfer end interrupt request flag (SRIF)
SBI (serial bus interface)		Use possible	None	None
2-wire serial I/O				
UART (Asynchronous serial interface)		None		Use possible Time-division transfer function [Note]

Note: Provided for the μPD780058 Subseries only.

The following four registers control serial interface channel 0:

- Timer clock select register 3 (TCL3)
- Serial operation mode register 0 (CSIM0)
- Serial bus interface control register (SBIC)
- Interrupt timing specification register (SINT)
- Port Mode Register 2 (PM2)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 3

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL3	TCL37	TCL36	TCL35	TCL34	TCL33	TCL32	TCL31	TCL30	FF43H	88H	R/W

This section controls serial interface channel 1.
Refer to **(13) Registers controlling serial interface channel 1** or **Chapter 18** of *µPD78054, 78054Y Subseries User's Manual*, **Chapter 18** of *µPD78058F, 78058FY Subseries User's Manual*, or **Chapter 18** of *µPD780058, 780058Y Subseries User's Manual* for detailed information.

TCL33	TCL32	TCL31	TCL30	Serial interface channel 0 serial clock selection		
					MCS = 1	MCS = 0
0	1	1	0	$f_{XX}/2$	Setting prohibited	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
Settings other than above are prohibited						

Caution: To write data other than that already written to TCL3, stop the serial transfer operation once.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz.
This register is also used to set the serial clock of serial interface channel 1.

Format of Serial Operation Mode Register 0 (1/2)

Symbol	<7>	<6>	<5>	4	3	2	1	0	Address	After Reset	R/W
CSIM0	CSIE0	COI	WUP	CSIM04	CSIM03	CSIM02	CSIM01	CSIM00	FF60H	00H	R/W Note 1

R/W

CSIM01	CSIM00	Serial interface channel 0 clock selection
0	×	Input clock to $\overline{\text{SCK0}}$ pin from off chip
1	0	8-bit timer register 2 (TM2) output
1	1	Clock specified with bits 0 to 3 of timer clock select register 3 (TCL3)

R/W

CSIM 04	CSIM 03	CSIM 02	PM25	P25	PM26	P26	PM27	P27	Operation mode	Start bit	SI0/SB0/P25 pin function	SO0/SB1/P26 pin function	$\overline{\text{SCK0}}$/P27 pin function
0	×	0	Note 2 1	Note 2 ×	0	0	0	1	3-wire serial I/O mode	MSB	SI0 Note 2 (Input)	SO0 (CMOS output)	$\overline{\text{SCK0}}$ (CMOS input/output)
		1								LSB			
1	0	0	Note 3 ×	Note 3 ×	0	0	0	1	SBI mode	MSB	P25 (CMOS input/output)	SB1 (N-ch open-drain input/output)	$\overline{\text{SCK0}}$ (CMOS input/output)
		1	0	0	Note 3 ×	Note 3 ×	0	1			SB0 (N-ch open-drain input/output)	P26 (CMOS input/output)	
1	1	0	Note 3 ×	Note 3 ×	0	0	0	1	2-wire serial I/O mode	MSB	P25 (CMOS input/output)	SB1 (N-ch open-drain input/output)	$\overline{\text{SCK0}}$ (N-ch open-drain input/output)
		1	0	0	Note 3 ×	Note 3 ×	0	1			SB0 (N-ch open-drain input/output)	P26 (CMOS input/output)	

Notes: 1. Bit 6 (COI) is a read-only bit.
2. Can be used as P25 (CMOS input/output) when serial channel is used only for transmission.
3. Can be used freely as a port function when not used in SBI or 2-wire mode.

Caution: Do not change the operation mode (3-wire serial I/O, 2-wire serial I/O, or SBI) while serial interface channel 0 is enabled to operate. To change the operation mode, stop the serial operation once.

Remarks: ×: Don't care
PM××: Port mode register
P××: Port output latch

Format of Serial Operation Mode Register 0 (2/2)

Symbol	<7>	<6>	<5>	4	3	2	1	0	Address	After Reset	R/W
CSIM0	CSIE0	COI	WUP	CSIM04	CSIM03	CSIM02	CSIM01	CSIM00	FF60H	00H	R/W Note 1

R/W	WUP	Wake-up function control Note 1
	0	Interrupt request signal generation with each serial transfer in any mode
	1	Interrupt request signal generation when the address received after bus release (when CMDD = RELD = 1) matches the slave address register (SVA) data in SBI mode

R	COI	Slave address comparison result flag Note 2
	0	Slave address register (SVA) not equal to serial I/O shift register 0 (SIO0) data
	1	Slave address register (SVA) equal to serial I/O shift register 0 (SIO0) data

R/W	CSIE0	Serial interface channel 0 operation control Note 3
	0	Operation stopped
	1	Operation enable

Notes: 1. When using the wake-up function (WUP = 1), clear bit 5 (SIC) of the interrupt timing specification register (SINT) to 0.

2. When CSIE = 0, COI becomes 0.

3. In the SBI mode, the operation of serial interface channel 0 should be stopped (by clearing CSIE to 0) after clearing WUP to 0. Otherwise, P25 is fixed to the high level and may not be able to be used as a normal port.

Format of Serial Bus Interface Control Register (1/2)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
SBIC	BSYE	ACKD	ACKE	ACKT	CMDD	RELD	CMDT	RELT	FF61H	00H	R/W Note

R/W

RELT	Used for bus release signal output. When RELT = 1, SO0 latch is set to 1. After SO0 latch setting, automatically cleared to 0. Also cleared to 0 when CSIE0 = 0.

R/W

CMDT	Used for command signal output. When CMDT = 1, SO0 latch is cleared to 0. After SO0 latch clearance, automatically cleared to 0. Also cleared to 0 when CSIE0 = 0.

R

RELD	Bus release detection	
Clear Conditions (RELD = 0)		Set Condition (RELD = 1)
• When transfer start instruction is executed • If SIO0 and SVA values do not match in address reception • When $\overline{\text{CSIE0}}$ = 0 • When $\overline{\text{RESET}}$ input is applied		• When bus release signal (REL) is detected

R

CMDD	Command detection	
Clear Conditions (CMDD = 0)		Set Condition (CMDD = 1)
• When transfer start instruction is executed • When bus release signal (REL) is detected • When $\overline{\text{CSIE0}}$ = 0 • When $\overline{\text{RESET}}$ input is applied		• When command signal (CMD) is detected

R/W

ACKT	Acknowledge signal is output in synchronization with the falling edge clock of $\overline{\text{SCK0}}$ just after execution of the instruction to be set to 1, and after acknowledge signal output, automatically cleared to 0. Used as ACKE = 0. Also cleared to 0 upon start of a serial interface transfer or when CSIE0 = 0.

Note: Bits 2, 3, and 6 (RELD CMDD, and ACKD) are read-only bits.

Remarks: Bits 0, 1, and 4 (RELT, CMDT, and ACKT) are 0 when read after data setting.
CSIE0: Bit 7 of serial operation mode register 0 (CSIM0)

Format of Serial Bus Interface Control Register (2/2)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
SBIC	BSYE	ACKD	ACKE	ACKT	CMDD	RELD	CMDT	RELT	FF61H	00H	R/W Note

R/W

ACKE	Acknowledge signal automatic output control	
0	Acknowledge signal automatic output disable (output with ACKT enable)	
1	Before completion of transfer	Acknowledge signal is output in synchronization with the falling edge of the 9th $\overline{SCK0}$ clock (automatically output when ACKE = 1).
	After completion of transfer	Acknowledge signal is output in synchronization with the falling edge of $\overline{SCK0}$ just after execution of the instruction to be set to 1 (automatically output when ACKE = 1). However, not automatically cleared to 0 after acknowledge signal output.

R

ACKD	Acknowledge detection	
Clear Conditions (ACKD = 0)		Set Condition (ACKD = 1)
• Falling edge of the $\overline{SCK0}$ immediately after the busy mode is released while executing the transfer start instruction • When CSIE0 = 0 • When $\overline{RESET}$ input is applied		• When acknowledge signal ($\overline{ACK}$) is detected at the rising edge of the $\overline{SCK0}$ clock after completion of a transfer

R/W

BSYE Note	Synchronizing busy signal output control
0	Disables the busy signal, which is output in synchronization with the falling edge of the $\overline{SCK0}$ clock just after execution of the instruction to be cleared to 0.
1	Outputs a busy signal at the falling edge of the $\overline{SCK0}$ clock following the acknowledge signal.

Note: The busy mode can be canceled by starting serial interface transfer. However, the BSYE flag is not cleared to 0.

Remark: CSIE0: Bit 7 of serial operation mode register 0 (CSIM0)

Format of Interrupt Timing Specification Register

Symbol	7	<6>	<5>	<4>	3	2	1	0	Address	After Reset	R/W
SINT	0	CLD	SIC	SVAM	0	0	0	0	FF63H	00H	R/W Note 1

R/W

SVAM	SVA bit to be used as slave address
0	Bits 0 to 7
1	Bits 1 to 7

R/W

SIC	INTCSI0 interrupt cause selection Note 2
0	CSIIF0 is set upon termination of serial interface channel 0 transfer
1	CSIIF0 is set upon bus release detection or termination of serial interface channel 0 transfer

R

CLD	$\overline{SCK0}$/P27 pin level Note 3
0	Low level
1	High level

Notes: 1. Bit 6 (CLD) is a read-only bit.
2. When using the wake-up function in the SBI mode, set SIC to 0.
3. When CSIE0 = 0, CLD becomes 0.

Caution: Be sure to set bits 0 to 3 to 0.

Remarks: SVA: Slave address register
CSIIF0: Interrupt request flag for INTCSI0
CSIE0: Bit 7 of serial operation mode register 0 (CSIM0)

(12) Registers controlling serial interface channel 0 (Y Subseries)

The μPD78054Y, 78058FY, and 780058Y Subseries are provided with three channels of serial interfaces. The differences among channels 0, 1, and 2 are indicated in the table below.

Differences Among Channels 0, 1, and 2

Serial Transfer Mode		Channel 0	Channel 1	Channel 2
3-wire serial I/O	Clock selection	$f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, $f_{XX}/2^8$, external clock, TO2 output	$f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, $f_{XX}/2^8$, external clock, TO2 output	External clock [Note], baud rate generator output
	Transfer method	MSB/LSB first switchable	MSB/LSB first switchable Automatic transmit/receive function	MSB/LSB first switchable
	Transfer end flag	Serial transfer end interrupt request flag (CSIIF0)	Serial transfer end interrupt request flag (CSIIF1)	Serial transfer end interrupt request flag (SRIF)
I^2C bus (inter-IC bus)		Use possible	None	None
2-wire serial I/O				
UART (Asynchronous serial interface)		None		Use possible Time-division transfer function [Note]

Note: Provided for the μPD780058Y Subseries only.

The following four registers control serial interface channel 0:

- Timer clock select register 3 (TCL3)
- Serial operation mode register 0 (CSIM0)
- Serial bus interface control register (SBIC)
- Interrupt timing specification register (SINT)
- Port Mode Register 2 (PM2)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 3

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL3	TCL37	TCL36	TCL35	TCL34	TCL33	TCL32	TCL31	TCL30	FF43H	88H	R/W

This section controls serial interface channel 1.
Refer to **(13) Registers controlling serial interface channel 1** or **Chapter 18** of *μPD78054, 78054Y Subseries User's Manual*, **Chapter 18** of *μPD78058F, 78058FY Subseries User's Manual*, or **Chapter 18** of *μPD780058, 780058Y Subseries User's Manual* for detailed information.

TCL33	TCL32	TCL31	TCL30	Serial interface channel 0 serial clock selection					
				Serial clock in I^2C bus mode			Serial clock in 2-wire or 3-wire serial I/O mode		
					MCS = 1	MCS = 0		MCS = 1	MCS = 0
0	1	1	0	$f_{XX}/2^5$	Setting prohibited	$f_X/2^6$ (78.1 kHz)	$f_{XX}/2$	Setting prohibited	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.77 kHz)	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_{XX}/2^9$	$f_X/2^9$ (9.77 kHz)	$f_X/2^{10}$ (4.88 kHz)	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_{XX}/2^{10}$	$f_X/2^{10}$ (4.88 kHz)	$f_X/2^{11}$ (2.44 kHz)	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_{XX}/2^{11}$	$f_X/2^{11}$ (2.44 kHz)	$f_X/2^{12}$ (1.22 kHz)	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_{XX}/2^{12}$	$f_X/2^{12}$ (1.22 kHz)	$f_X/2^{13}$ (0.61 kHz)	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
Settings other than above are prohibited									

Caution: To write data other than that already written to TCL3, stop the serial transfer operation once.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz.
This register is also used to set serial interface channel 1.

Format of Serial Operation Mode Register 0

Symbol	<7>	<6>	<5>	4	3	2	1	0	Address	After Reset	R/W
CSIM0	CSIE0	COI	WUP	CSIM04	CSIM03	CSIM02	CSIM01	CSIM00	FF60H	00H	R/W Note 1

R/W

CSIM01	CSIM00	Serial interface channel 0 clock selection
0	×	Input clock to $\overline{SCK0}$/SCL pin from off chip
1	0	8-bit timer register 2 (TM2) output Note 2
1	1	Clock specified with bits 0 to 3 of timer clock select register 3 (TCL3)

R/W

CSIM 04	CSIM 03	CSIM 02	PM25	P25	PM26	P26	PM27	P27	Operation mode	Start bit	SI0/SB0/SDA0/ P25 pin function	SO0/SB1/SDA1/ P26 pin function	$\overline{SCK0}$/SCL/P27 pin function
0	×	0	Note 3 1	Note 3 ×	0	0	0	1	3-wire serial I/O mode	MSB	SI0 Note 3 (Input)	SO0 (CMOS output)	$\overline{SCK0}$ (CMOS input/output)
		1								LSB			
1	1	0	Note 4 ×	Note 4 ×	0	0	0	1	2-wire serial I/O mode or I^2C bus mode	MSB	P25 (CMOS input/output)	SB1/SDA1 (N-ch open-drain input/output)	$\overline{SCK0}$/SCL (N-ch open-drain input/ output)
		1	0	0	Note 4 ×	Note 4 ×	0	1			SB0/SDA0 (N-ch open-drain input/output)	P26 (CMOS input/output)	

R/W

WUP	Wake-up function control Note 5
0	Interrupt request signal generation with each serial transfer in any mode
1	Interrupt request signal generation when the address received after detecting the start condition (when CMDD = 1) matches the slave address register (SVA) data in I^2C bus mode

R

COI	Slave address comparison result flag Note 6
0	Slave address register (SVA) not equal to serial I/O shift register 0 (SIO0) data
1	Slave address register (SVA) equal to serial I/O shift register 0 (SIO0) data

R/W

CSIE0	Serial interface channel 0 operation control
0	Operation stopped
1	Operation enabled

Notes: 1. Bit 6 (COI) is a read-only bit.
2. I^2C bus mode, the clock frequency becomes 1/16 of that output from TO2.
3. Can be used as P25 (CMOS input/output) when serial channel is used only for transmission.
4. Can be used freely as port function when not used in 2-wire or I^2C mode.
5. When using the wake-up function (WUP = 1), set the bit 5 (SIC) of the interrupt timing specification register (SINT) to 1. Do not execute an instruction that writes the serial I/O shift register 0 (SIO0) while WUP = 1.
6. When CSIE0 = 0, COI becomes 0.

Caution: Do not change the operation mode (3-wire serial I/O, 2-wire serial I/O, or I^2C) while serial interface channel 0 is enabled to operate. To change the operation mode, stop the serial operation once.

Remarks: ×: Don't care
PM××: Port mode register
P××: Port output latch

Format of Serial Bus Interface Control Register (1/2)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
SBIC	BSYE	ACKD	ACKE	ACKT	CMDD	RELD	CMDT	RELT	FF61H	00H	R/W Note

R/W

RELT	Used for stop condition signal output. When RELT = 1, SO0 latch is set to 1. After SO0 latch setting, automatically cleared to 0. Also cleared to 0 when CSIE0 = 0.

R/W

CMDT	Used for start condition signal output. When CMDT = 1, SO0 latch is cleared to 0. After SO0 latch clearance, automatically cleared to 0. Also cleared to 0 when CSIE0 = 0.

R

RELD	Stop condition detection	
Clear Conditions (RELD = 0)		Set Condition (RELD =1)
• When transfer start instruction is executed • If SIO0 and SVA values do not match in address reception • When $\overline{\text{CSIE0}}$ = 0 • When $\overline{\text{RESET}}$ input is applied		• When stop condition signal is detected

R

CMDD	Start condition detection	
Clear Conditions (CMDD = 0)		Set Condition (CMDD = 1)
• When transfer start instruction is executed • When stop condition signal is detected • When $\overline{\text{CSIE0}}$ = 0 • When $\overline{\text{RESET}}$ input is applied		• When start condition signal is detected

R/W

ACKT	Used to generate the $\overline{\text{ACK}}$ signal by software when an 8-clock wait mode is selected. Keeps SDA0 (SDA1) low from set instruction (ACKT = 1) execution to the next falling edge of SCL. Also cleared to 0 upon start of a serial interface transfer or when CSIE0 = 0.

Note: Bits 2, 3, and 6 (RELD, CMDD, and ACKD) are read-only bits.

Remark: CSIE0: Bit 7 of serial operation mode register 0 (CSIM0)

Format of Serial Bus Interface Control Register (2/2)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
SBIC	BSYE	ACKD	ACKE	ACKT	CMDD	RELD	CMDT	RELT	FF61H	00H	R/W Note

R/W

ACKE	Acknowledge signal output control Note 1
0	Disables acknowledge signal automatic output (however, output with ACKT is enabled). Used for reception when an 8-clock wait mode is selected or for transmission. Note 2
1	Enables acknowledge signal automatic output. Outputs the acknowledge signal in synchronization with the falling edge of the 9th SCL clock cycle (automatically output when ACKE = 1). However, it is not automatically cleared to 0 after acknowledge signal output. Used in reception with a 9-clock wait mode selected.

R

ACKD	Acknowledge detection	
Clear Conditions (ACKD = 0)		Set Condition (ACKD = 1)
• While executing the transfer start instruction • When CSIE0 = 0 • When $\overline{\text{RESET}}$ input is applied		• When acknowledge signal ($\overline{\text{ACK}}$) is detected at the rising edge of SCL clock after completion of a transfer

R/W

BSYE Note 3	Control of N-ch open-drain output for transmission in I ^{2}C bus mode Note 4
0	Output enabled (transmission)
1	Output disabled (reception)

Notes: 1. Setting should be performed before transfer.
2. If an 8-clock wait mode is selected, the acknowledge signal at reception time must be output using ACKT.
3. The busy mode can be canceled by start of a serial interface transfer or reception of an address signal. However, the BSYE flag is not cleared to 0.
4. When using the wake-up function, be sure to set the BSYE to 1.

Remark: CSIE0: Bit 7 of serial operation mode register 0 (CSIM0)

Format of Interrupt Timing Specification Register (1/2)

Symbol	7	<6>	<5>	<4>	<3>	<2>	1	0	Address	After Reset	R/W
SINT	0	CLD	SIC	SVAM	CLC	WREL	WAT1	WAT0	FF63H	00H	R/W Note 1

R/W	WAT1	WAT0	Wait and interrupt control
	0	0	Generates an interrupt service request at the rising edge of the 8th $\overline{SCK0}$ clock cycle (keeping clock output in high impedance).
	0	1	Setting prohibited
	1	0	Used in I^2C bus mode (8-clock wait) Generates an interrupt service request at the rising edge of the 8th $\overline{SCK0}$ clock cycle. (In the case of a master device, makes SCL output low to enter the wait state after 8 clock pulses are output. In the case of a slave device, makes SCL output low to request the wait state after 8 clock pulses are input.)
	1	1	Used in I^2C bus mode. (9-clock wait) Generates an interrupt service request at the rising edge of the 9th $\overline{SCK0}$ clock cycle. (In the case of a master device, makes SCL output low to enter the wait state after 9 clock pulses are output. In the case of a slave device, makes SCL output low to request the wait state after 9 clock pulses are input.)

R/W	WREL	Wait state cancellation control
	0	Wait state has been canceled.
	1	Cancels wait state. Automatically cleared to 0 when the state is canceled. (Used to cancel the wait state by means of WAT0 and WAT1.)

R/W	CLC	Clock level control Note 2
	0	Used in I^2C bus mode Make output level of SCL pin low unless a serial transfer is being performed.
	1	Used in I^2C bus mode Make the SCL pin enter a high-impedance state unless a serial transfer is being performed (except for the clock line, which is kept high). Used to enable a master device to generate start condition and stop condition signals.

Notes: 1. Bit 6 (CLD) is a read-only bit.

2. When not using the I^2C mode, set CLC to 0.

Format of Interrupt Timing Specification Register (2/2)

Symbol	7	<6>	<5>	<4>	<3>	<2>	1	0	Address	After Reset	R/W
SINT	0	CLD	SIC	SVAM	CLC	WREL	WAT1	WAT0	FF63H	00H	R/W Note 1

R/W

SVAM	SVA bit to be used as slave address
0	Bits 0 to 7
1	Bits 1 to 7

R/W

SIC	INTCSI0 interrupt cause selection Note1
0	CSIIF0 is set to 1 upon termination of serial interface channel 0 transfer
1	CSIIF0 is set to 1 upon stop condition detection or termination of serial interface channel 0 transfer

R

CLD	$\overline{SCK0}$/SCL pin level Note 2
0	Low level
1	High level

Notes: 1. When using the wake-up function in the I^2C mode, set SIC to 0.
2. When CSIE = 0, CLD becomes 0.

Remarks: SVA: Slave address register
CSIIF0: Interrupt request flag for INTCSI0
CSIE0: Bit 7 of serial operation mode register 0 (CSIM0)

(13) Registers controlling serial interface channel 1

The following four registers control serial interface channel 1:

- Timer clock select register 3 (TCL3)
- Serial operation mode register 1 (CSIM1)
- Automatic data transmit/receive control register (ADTC)
- Automatic data transmit/receive time interval specification register (ADTI)

Format of Timer Clock Select Register 3

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL3	TCL37	TCL36	TCL35	TCL34	TCL33	TCL32	TCL31	TCL30	FF43H	88H	R/W

This section controls the serial interface channel 0.
Refer to **(11) Registers controlling serial interface channel 0 (Non-Y Subseries)** or **(12) Registers controlling serial interface channel 0 (Y Subseries),** or
Chapters 16, 17 of *μPD78054, 78054Y Subseries User's Manual*,
Chapters 16, 17 of *μPD78058F, 78058FY Subseries User's Manual*, or
Chapters 16, 17 of *μPD780058, 780058Y Subseries User's Manual*
for detailed information.

TCL37	TCL36	TCL35	TCL34	Serial interface channel 1 serial clock selection		
					MCS = 1	MCS = 0
0	1	1	0	$f_{XX}/2$	Setting prohibited	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
Settings other than above are prohibited						

Caution: To write data other than that already written to TCL3, stop the serial transfer operation once.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz.
This register is also used to set the serial clock of serial interface channel 0.

Format of Serial Operation Mode Register 1

Symbol	<7>	6	<5>	4	3	2	1	0	Address	After Reset	R/W
CSIM1	CSIE1	DIR	ATE	0	0	0	CSIM11	CSIM10	FF68H	00H	R/W

CSIM11	CSIM10	Serial interface channel 1 clock selection
0	×	Clock externally input to $\overline{\text{SCK1}}$ pin Note 1
1	0	8-bit timer register 2 (TM2) output
1	1	Clock specified with bits 4 to 7 of timer clock select register 3 (TCL3)

ATE	Serial interface channel 1 operating mode selection
0	3-wire serial I/O mode
1	3-wire serial I/O mode with automatic transmit/receive function

DIR	Start bit	SI1 pin function	SO1 pin function
0	MSB	SI1/P20 (Input)	SO1 (CMOS output)
1	LSB		

CSIE1	CSIM11	PM20	P20	PM21	P21	PM22	P22	Shift register 1 operation	Serial clock counter operation control	SI1/P20 pin function	SO1/P21 pin function	$\overline{\text{SCK1}}$/P22 pin function
0	×	Note 2 ×	Note 2 ×	Note 2 ×	Note 2 ×	Note 2 ×	Note 2 ×	Operation stop	Clear	P20 (CMOS input/output)	P21 (CMOS input/output)	P22 (CMOS input/output)
1	0	Note 3 1	Note 3 ×	0	0	1	×	Operation enable	Count operation	SI1 Note 3 (Input)	SO1 (CMOS output)	$\overline{\text{SCK1}}$ (Input)
	1					0	1					$\overline{\text{SCK1}}$ (CMOS output)

Notes: 1. If the external clock input has been selected with CSIM11 set to 0, set bit 1 (BUSY1) and bit 2 (STRB) of the automatic data transmit/receive control register (ADTC) to 0, 0.

2. Can be used freely as a port function when not used in 3-wire mode.
3. Can be used as P20 (CMOS input/output) when serial channel is only transmission performed (clear bit 7 (RE) of ADTC to 0).

Remarks: ×: Don't care
PM××: Port mode register
P××: Port output latch

Format of Automatic Data Transmit/Receive Control Register

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
ADTC	RE	ARLD	ERCE	ERR	TRF	STRB	BUSY1	BUSY0	FF69H	00H	R/W Note 1

R/W

BUSY1	BUSY0	Busy input control
0	×	Not using busy input
1	0	Busy input enable (active high)
1	1	Busy input enable (active low)

R/W

STRB	Strobe output control
0	Strobe output disable
1	Strobe output enable

R

TRF	Status of automatic transmit/receive function Note 2
0	Detection of termination of automatic transmission/ reception (This bit is set to 0 upon suspension of automatic transmission/reception or when ARLD = 0.)
1	During automatic transmission/reception (This bit is set to 1 when data is written to SIO1.)

R

ERR	Error detection of automatic transmit/receive function
0	No error (This bit is set to 0 when data is written to SIO1)
1	Error occurred

R/W

ERCE	Error check control of automatic transmit/ receive function
0	Error check disable
1	Error check enable (only when BUSY1 = 1)

R/W

ARLD	Operating mode selection of automatic transmit/ receive function
0	Single operating mode
1	Repetitive operating mode

R/W

RE	Receive control of automatic transmit/receive function
0	Receive disable
1	Receive enable

Notes: 1. Bits 3 and 4 (TRF and ERR) are read-only bits.
2. The termination of automatic transmission/reception should be judged by using TRF, not CSIIF1 (interrupt request flag).

Cautions: **1. When an external clock input is selected by setting bit 1 (CSIM11) of serial operating mode register 1 (CSIM1) to 0, set STRB and BUSY1 of ADTC to 0, 0.**
2. When using the P23/STB/TxD1 and P24/BUSY/RxD1 pins in the asynchronous serial interface (UART) mode of serial interface channel 2, the busy control option and busy and strobe control option are invalid.

Remark: ×: Don't care

Format of Automatic Data Transmit/Receive Interval Time Specification Register (1/4)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADTI	ADTI7	0	0	ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	FF6BH	00H	R/W

ADTI7	Data transfer interval control
0	No control of interval by ADTI Note 1
1	Control of interval by ADTI (ADTI0 to ADTI4)

ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	Data transfer interval specification (f_{XX} = 5.0 MHz Operation)	
					Minimum Note 2	Maximum Note 2
0	0	0	0	0	18.4 μs + 0.5/f_{SCK}	20.0 μs + 1.5/f_{SCK}
0	0	0	0	1	31.2 μs + 0.5/f_{SCK}	32.8 μs + 1.5/f_{SCK}
0	0	0	1	0	44.0 μs + 0.5/f_{SCK}	45.6 μs + 1.5/f_{SCK}
0	0	0	1	1	56.8 μs + 0.5/f_{SCK}	58.4 μs + 1.5/f_{SCK}
0	0	1	0	0	69.6 μs + 0.5/f_{SCK}	71.2 μs + 1.5/f_{SCK}
0	0	1	0	1	82.4 μs + 0.5/f_{SCK}	84.0 μs + 1.5/f_{SCK}
0	0	1	1	0	95.2 μs + 0.5/f_{SCK}	96.8 μs + 1.5/f_{SCK}
0	0	1	1	1	108.0 μs + 0.5/f_{SCK}	109.6 μs + 1.5/f_{SCK}
0	1	0	0	0	120.8 μs + 0.5/f_{SCK}	122.4 μs + 1.5/f_{SCK}
0	1	0	0	1	133.6 μs + 0.5/f_{SCK}	135.2 μs + 1.5/f_{SCK}
0	1	0	1	0	146.4 μs + 0.5/f_{SCK}	148.0 μs + 1.5/f_{SCK}
0	1	0	1	1	159.2 μs + 0.5/f_{SCK}	160.8 μs + 1.5/f_{SCK}
0	1	1	0	0	172.0 μs + 0.5/f_{SCK}	173.6 μs + 1.5/f_{SCK}
0	1	1	0	1	184.8 μs + 0.5/f_{SCK}	186.4 μs + 1.5/f_{SCK}
0	1	1	1	0	197.6 μs + 0.5/f_{SCK}	199.2 μs + 1.5/f_{SCK}
0	1	1	1	1	210.4 μs + 0.5/f_{SCK}	212.0 μs + 1.5/f_{SCK}

Notes: 1. The interval is dependent only on CPU processing.

2. The data transfer interval includes an error. The data transfer minimum and maximum intervals are found from the following expressions (n: Value set in ADTI0 to ADTI4). However, if a minimum calculated by the following expressions is smaller than 2/f_{SCK}, the minimum interval time is 2/f_{SCK}.

$$\text{Minimum} = (n+1) \times \frac{2^6}{f_{XX}} + \frac{28}{f_{XX}} + \frac{0.5}{f_{SCK}}, \quad \text{Maximum} = (n+1) \times + \frac{2^6}{f_{XX}} + \frac{36}{f_{XX}} \quad \frac{1.5}{f_{SCK}}$$

Cautions: 1. Do not write data to ADTI during operation of the automatic data transmit/receive function.

2. Be sure to set bits 5 and 6 to 0.

3. While ADTI is used to control the interval time for data transfer by the automatic data transmit/receive function, busy control is invalid.

Remarks: f_{XX}: Main system clock frequency (f_X or f_X/2)

f_X: Main system clock oscillation frequency

f_{SCK}: Serial clock frequency

Format of Automatic Data Transmit/Receive Interval Time Specification Register (2/4)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADTI	ADTI7	0	0	ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	FF6BH	00H	R/W

ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	Data transfer interval specification (f_{XX} = 5.0 MHz operation)	
					Minimum Note	Maximum Note
1	0	0	0	0	223.2 μs + 0.5/f_{SCK}	224.8 μs + 1.5/f_{SCK}
1	0	0	0	1	236.0 μs + 0.5/f_{SCK}	237.6 μs + 1.5/f_{SCK}
1	0	0	1	0	248.8 μs + 0.5/f_{SCK}	250.4 μs + 1.5/f_{SCK}
1	0	0	1	1	261.6 μs + 0.5/f_{SCK}	263.2 μs + 1.5/f_{SCK}
1	0	1	0	0	274.4 μs + 0.5/f_{SCK}	276.0 μs + 1.5/f_{SCK}
1	0	1	0	1	287.2 μs + 0.5/f_{SCK}	288.8 μs + 1.5/f_{SCK}
1	0	1	1	0	300.0 μs + 0.5/f_{SCK}	301.6 μs + 1.5/f_{SCK}
1	0	1	1	1	312.8 μs + 0.5/f_{SCK}	314.4 μs + 1.5/f_{SCK}
1	1	0	0	0	325.6 μs + 0.5/f_{SCK}	327.2 μs + 1.5/f_{SCK}
1	1	0	0	1	338.4 μs + 0.5/f_{SCK}	340.0 μs + 1.5/f_{SCK}
1	1	0	1	0	351.2 μs + 0.5/f_{SCK}	352.8 μs + 1.5/f_{SCK}
1	1	0	1	1	364.0 μs + 0.5/f_{SCK}	365.6 μs + 1.5/f_{SCK}
1	1	1	0	0	376.8 μs + 0.5/f_{SCK}	378.4 μs + 1.5/f_{SCK}
1	1	1	0	1	389.6 μs + 0.5/f_{SCK}	391.2 μs + 1.5/f_{SCK}
1	1	1	1	0	402.4 μs + 0.5/f_{SCK}	404.0 μs + 1.5/f_{SCK}
1	1	1	1	1	415.2 μs + 0.5/f_{SCK}	416.8 μs + 1.5/f_{SCK}

Note: The data transfer interval includes an error. The data transfer minimum and maximum intervals are found from the following expressions (n: Value set in ADTI0 to ADTI4). However, if a minimum calculated by the following expressions is smaller than 2/f_{SCK}, the minimum interval time is 2/f_{SCK}.

$$\text{Minimum} = (n+1) \times \frac{2^6}{f_{XX}} + \frac{28}{f_{XX}} + \frac{0.5}{f_{SCK}}$$

$$\text{Maximum} = (n+1) \times \frac{2^6}{f_{XX}} + \frac{36}{f_{XX}} + \frac{1.5}{f_{SCK}}$$

Cautions: 1. Do not write data to ADTI during operation of the automatic data transmit/receive function.

2. Be sure to set bits 5 and 6 to 0.

3. While ADTI is used to control the interval time for data transfer by the automatic data transmit/receive function, busy control is invalid.

Remarks: f_{XX}: Main system clock frequency (f_X or f_X/2)

f_X: Main system clock oscillation frequency

f_{SCK}: Serial clock frequency

Format of Automatic Data Transmit/Receive Interval Time Specification Register (3/4)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADTI	ADTI7	0	0	ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	FF6BH	00H	R/W

ADTI7	Data transfer interval control
0	No control of interval by ADTI Note 1
1	Control of interval by ADTI (ADTI0 to ADTI4)

ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	Data transfer interval specification (f_{XX} = 2.5 MHz operation)	
					Minimum Note 2	Maximum Note 2
0	0	0	0	0	36.8 μs + 0.5/f_{SCK}	40.0 μs + 1.5/f_{SCK}
0	0	0	0	1	62.4 μs + 0.5/f_{SCK}	65.6 μs + 1.5/f_{SCK}
0	0	0	1	0	88.0 μs + 0.5/f_{SCK}	91.2 μs + 1.5/f_{SCK}
0	0	0	1	1	113.6 μs + 0.5/f_{SCK}	116.8 μs + 1.5/f_{SCK}
0	0	1	0	0	139.2 μs + 0.5/f_{SCK}	142.4 μs + 1.5/f_{SCK}
0	0	1	0	1	164.8 μs + 0.5/f_{SCK}	168.0 μs + 1.5/f_{SCK}
0	0	1	1	0	190.4 μs + 0.5/f_{SCK}	193.6 μs + 1.5/f_{SCK}
0	0	1	1	1	216.0 μs + 0.5/f_{SCK}	219.2 μs + 1.5/f_{SCK}
0	1	0	0	0	241.6 μs + 0.5/f_{SCK}	244.8 μs + 1.5/f_{SCK}
0	1	0	0	1	267.2 μs + 0.5/f_{SCK}	270.4 μs + 1.5/f_{SCK}
0	1	0	1	0	292.8 μs + 0.5/f_{SCK}	296.0 μs + 1.5/f_{SCK}
0	1	0	1	1	318.4 μs + 0.5/f_{SCK}	321.6 μs + 1.5/f_{SCK}
0	1	1	0	0	344.0 μs + 0.5/f_{SCK}	347.2 μs + 1.5/f_{SCK}
0	1	1	0	1	369.6 μs + 0.5/f_{SCK}	372.8 μs + 1.5/f_{SCK}
0	1	1	1	0	395.2 μs + 0.5/f_{SCK}	398.4 μs + 1.5/f_{SCK}
0	1	1	1	1	420.8 μs + 0.5/f_{SCK}	424.0 μs + 1.5/f_{SCK}

Notes: 1. The interval is dependent only on CPU processing.

2. The data transfer interval includes an error. The data transfer minimum and maximum intervals are found from the following expressions (n: Value set in ADTI0 to ADTI4). However, if a minimum calculated by the following expressions is smaller than $2/f_{SCK}$, the minimum interval time is $2/f_{SCK}$.

$$\text{Minimum} = (n+1) \times \frac{2^6}{f_{XX}} + \frac{28}{f_{XX}} + \frac{0.5}{f_{SCK}}, \quad \text{Maximum} = (n+1) \times + \frac{2^6}{f_{XX}} + \frac{36}{f_{XX}} \quad \frac{1.5}{f_{SCK}}$$

Cautions: 1. Do not write data to ADTI during operation of the automatic data transmit/receive function.

2. Be sure to set bits 5 and 6 to 0.

3. While ADTI is used to control the interval time for data transfer by the automatic data transmit/receive function, busy control is invalid.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)

f_X: Main system clock oscillation frequency

f_{SCK}: Serial clock frequency

Format of Automatic Data Transmit/Receive Interval Time Specification Register (4/4)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADTI	ADTI7	0	0	ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	FF6BH	00H	R/W

ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	Data transfer interval specification (f_{XX} = 2.5 MHz operation)	
					Minimum Note	Maximum Note
1	0	0	0	0	446.4 μs + 0.5/f_{SCK}	449.6 μs + 1.5/f_{SCK}
1	0	0	0	1	472.0 μs + 0.5/f_{SCK}	475.2 μs + 1.5/f_{SCK}
1	0	0	1	0	497.6 μs + 0.5/f_{SCK}	500.8 μs + 1.5/f_{SCK}
1	0	0	1	1	523.2 μs + 0.5/f_{SCK}	526.4 μs + 1.5/f_{SCK}
1	0	1	0	0	548.8 μs + 0.5/f_{SCK}	552.0 μs + 1.5/f_{SCK}
1	0	1	0	1	574.4 μs + 0.5/f_{SCK}	577.6 μs + 1.5/f_{SCK}
1	0	1	1	0	600.0 μs + 0.5/f_{SCK}	603.2 μs + 1.5/f_{SCK}
1	0	1	1	1	625.6 μs + 0.5/f_{SCK}	628.8 μs + 1.5/f_{SCK}
1	1	0	0	0	651.2 μs + 0.5/f_{SCK}	654.4 μs + 1.5/f_{SCK}
1	1	0	0	1	676.8 μs + 0.5/f_{SCK}	680.0 μs + 1.5/f_{SCK}
1	1	0	1	0	702.4 μs + 0.5/f_{SCK}	705.6 μs + 1.5/f_{SCK}
1	1	0	1	1	728.0 μs + 0.5/f_{SCK}	731.2 μs + 1.5/f_{SCK}
1	1	1	0	0	753.6 μs + 0.5/f_{SCK}	756.8 μs + 1.5/f_{SCK}
1	1	1	0	1	779.2 μs + 0.5/f_{SCK}	782.4 μs + 1.5/f_{SCK}
1	1	1	1	0	804.8 μs + 0.5/f_{SCK}	808.0 μs + 1.5/f_{SCK}
1	1	1	1	1	830.4 μs + 0.5/f_{SCK}	833.6 μs + 1.5/f_{SCK}

Note: The data transfer interval includes an error. The data transfer minimum and maximum intervals are found from the following expressions (n: Value set in ADTI0 to ADTI4). However, if a minimum calculated by the following expressions is smaller than 2/f_{SCK}, the minimum interval time is 2/f_{SCK}.

$$\text{Minimum} = (n + 1) \times \frac{2^6}{f_{XX}} + \frac{28}{f_{XX}} + \frac{0.5}{f_{SCK}}$$

$$\text{Maximum} = (n + 1) \times \frac{2^6}{f_{XX}} + \frac{36}{f_{XX}} + \frac{1.5}{f_{SCK}}$$

Cautions: 1. Do not write data to ADTI during operation of the automatic data transmit/receive function.

2. Be sure to set bits 5 and 6 to 0.

3. While ADTI is used to control the interval time for data transfer by the automatic data transmit/receive function, busy control is invalid.

Remarks: f_{XX}: Main system clock frequency (f_X or f_X/2)

f_X: Main system clock oscillation frequency

f_{SCK}: Serial clock frequency

(14) Registers controlling serial interface channel 2

The following five registers control serial interface channel 2:

- Serial operation mode register 2 (CSIM2)
- Asynchronous serial interface mode register (ASIM)
- Asynchronous serial interface status register (ASIS)
- Baud rate generator control register (BRGC)
- Serial interface pin select register (SIPS) Note

Note: This register is provided only for μPD780058/58Y Subseries products.

Format of Serial Operation Mode Register 2 (For μPD78054/54Y and μPD78058F/58FY Subseries)

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
CSIM2	CSIE2	0	0	0	0	CSIM 22	CSCK	0	FF72H	00H	R/W

CSCK	Selection of serial operating mode
0	UART mode
1	3-wire serial I/O mode

CSIM22	First bit specification
0	MSB
1	LSB

CSIE2	Operation control in 3-wire serial I/O mode
0	Operation stopped
1	Operation enabled

Cautions: 1. Ensure that bits 0 and 3 to 6 are set to 0.

2. When UART mode is selected, CSIM2 should be set to 00H.

Format of Serial Operation Mode Register 2 (For 780058/58Y Subseries)

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
CSIM2	CSIE2	0	0	0	0	CSIM 22	CSCK	0	FF72H	00H	R/W

CSCK	Clock selection in 3-wire serial I/O mode
0	Input clock from off chip to $\overline{\text{SCK2}}$ pin
1	Dedicated baud rate generator output

CSIM22	First bit specification
0	MSB
1	LSB

CSIE2	Operation control in 3-wire serial I/O mode
0	Operation stopped
1	Operation enabled

Cautions: 1. Ensure that bits 0 and 3 to 6 are set to 0.

2. When UART mode is selected, CSIM2 should be set to 00H.

Format of Asynchronous Serial Interface Mode Register

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After Reset	R/W
ASIM	TXE	RXE	PS1	PS0	CL	SL	ISRM	SCK	FF70H	00H	R/W

SCK	Clock selection in asynchronous serial interface mode
0	Input clock from off chip to ASCK pin
1	Dedicated baud rate generator output Note

ISRM	Control of reception completion interrupt request in case of error generation
0	Reception completion interrupt request generated in case of error generation
1	Reception completion interrupt request not generated in case of error generation

SL	Transmit data stop bit length specification
0	1 bit
1	2 bits

CL	Character length specification
0	7 bits
1	8 bits

PS1	PS0	Parity bit specification
0	0	No parity
0	1	0 parity always added in transmission No parity test in reception (parity error not generated)
1	0	Odd parity
1	1	Even parity

RXE	Receive operation control
0	Receive operation stopped
1	Receive operation enabled

TXE	Transmit operation control
0	Transmit operation stopped
1	Transmit operation enabled

Note: When SCK is set to 1 and the baud rate generator output is selected, the ASCK pin can be used as an input/output port.

Cautions: 1. When the 3-wire serial I/O mode is selected, 00H should be set in ASIM.

2. The serial transmit/receive operation must be stopped before changing the operating mode.

Format of Asynchronous Serial Interface Status Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ASIS	0	0	0	0	0	PE	FE	OVE	FF71H	00H	R

OVE	Overrun error flag
0	Overrun error not generated
1	Overrun error generated Note 1 (when next receive operation is completed before data is read from receive buffer register)

FE	Framing error flag
0	Framing error not generated
1	Framing error generated Note 2 (when stop bit is not detected)

PE	Parity error flag
0	Parity error not generated
1	Parity error generated (when transmit data parity does not match)

Notes: 1. The receive buffer register (RXB) must be read when an overrun error is generated. Overrun errors will continue to be generated until RXB is read.

2. Even if the stop bit length has been set as 2 bits by bit 2 (SL) of the asynchronous serial interface mode register (ASIM), only single stop bit detection is performed during reception.

Format of Baud Rate Generator Control Register (1/2)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
BRGC	TPS3	TPS2	TPS1	TPS0	MDL3	MDL2	MDL1	MDL0	FF73H	00H	R/W

MDL3	MDL2	MDL1	MDL0	Baud rate generator input clock selection	k
0	0	0	0	$f_{SCK}/16$	0
0	0	0	1	$f_{SCK}/17$	1
0	0	1	0	$f_{SCK}/18$	2
0	0	1	1	$f_{SCK}/19$	3
0	1	0	0	$f_{SCK}/20$	4
0	1	0	1	$f_{SCK}/21$	5
0	1	1	0	$f_{SCK}/22$	6
0	1	1	1	$f_{SCK}/23$	7
1	0	0	0	$f_{SCK}/24$	8
1	0	0	1	$f_{SCK}/25$	9
1	0	1	0	$f_{SCK}/26$	10
1	0	1	1	$f_{SCK}/27$	11
1	1	0	0	$f_{SCK}/28$	12
1	1	0	1	$f_{SCK}/29$	13
1	1	1	0	$f_{SCK}/30$	14
1	1	1	1	f_{SCK} **Note**	

Note: Can only be used in 3-wire serial I/O mode.

Remarks: f_{SCK}: 5-bit counter source clock
k: Value set in MDL0 to MDL3 ($0 \leq k \leq 14$)

Format of Baud Rate Generator Control Register (2/2)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
BRGC	TPS3	TPS2	TPS1	TPS0	MDL3	MDL2	MDL1	MDL0	FF73H	00H	R/W

TPS3	TPS2	TPS1	TPS0	5-bit counter source clock selection			n
					MCS = 1	MCS = 0	
0	0	0	0	$f_{XX}/2^{10}$	$f_{XX}/2^{10}$ (4.9 kHz)	$f_X/2^{11}$ (2.4 kHz)	11
0	1	0	1	f_{XX}	f_X (5.0 MHz)	$f_X/2$ (2.5 MHz)	1
0	1	1	0	$f_{XX}/2$	$f_X/2$ (2.5 MHz)	$f_X/2^2$ (1.25 MHz)	2
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)	3
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)	4
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)	5
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)	6
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)	7
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)	8
1	1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)	9
1	1	1	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)	10
Settings other than above are prohibited							

Caution: When a write is performed to BRGC during a communication operation, baud rate generator output is disrupted and communication cannot be performed normally. Therefore, BRGC must not be written to during a communication operation.

Remarks: f_X: Main system clock oscillation frequency

f_{XX}: Main system clock frequency (f_X or $f_X/2$)

MCS: Bit 0 of oscillation mode selection register (OSMS)

n: Value set in TPS0 to TPS3 ($1 \leq n \leq 11$)

Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of Serial Interface Pin Select Register (μPD780058/58Y Subseries Only)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
SIPS	0	0	SIPS21	SIPS20	0	0	0	0	FF75H	00H	R/W

SIPS21	SIPS20	Selects input/output pin of asynchronous serial interface
0	0	Input pin: RxD0/SI2/P70 Output pin: TxD0/SO2/P71
0	1	Input pin: RxD1/BUSY/P24 Output pin: TxD0/SO2/P71
1	0	Input pin: RxD0/SI2/P70 Output pin: TxD1/STB/P23
1	1	Input pin: RxD1/BUSY/P24 Output pin: TxD1/STB/P23

Cautions: 1. Select input/output pins after stopping serial transmission/reception.

2. When using the busy control option or busy and strobe control option in the three-wire serial I/O mode with the automatic transmit/receive function of the serial interface channel 1, the RxD1/BUSY/P24 and TxD1/STB/P23 pins cannot be used as data I/O pins.

3. This register is provided only for μPD780058/58Y Subseries products.

(15) Registers controlling real-time output port

The following three registers control the real-time output port:

- Port mode register 12 (PM12)
  - Refer to section (1) for the register format.
- Real-time output port mode register (RTPM)
- Real-time output port control register (RTPC)

Format of Real-Time Output Port Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
RTPM	RTPM7	RTPM6	RTPM5	RTPM4	RTPM3	RTPM2	RTPM1	RTPM0	FF34H	00H	R/W

RTPMn	Real-time output port selection (n = 0 to 7)
0	Port mode
1	Real-time output Port mode

Cautions: 1. When using these bits as a real-time output port, set the ports to which real-time output is performed to the output mode (clear the corresponding bit of Port mode register 12 (PM12) to 0).

2. In the port specified as a real-time output port, data cannot be set to the output latch. Therefore, when setting an initial value, data should be set to the output latch before setting the real-time output mode.

Format of Real-Time Output Port Control Register

Symbol	7	6	5	4	3	2	<1>	<0>	Address	After Reset	R/W
RTPC	0	0	0	0	0	0	BYTE	EXTR	FF36H	00H	R/W

EXTR	Real-time output control by INTP2
0	INTP2 not specified as real-time output trigger
1	INTP2 specified as real-time output trigger

BYTE	Real-time output port operating mode
0	4 bits × 2 channels
1	8 bits × 1 channel

(16) Registers controlling interrupt function

A total of 22 interrupt sources are provided for the μPD78054/54Y and 78058F/58FY Subseries and 21 interrupt sources are provided for the μPD780058/58Y Subseries, including non-maskable, maskable, and software interrupts.

Table 6-19. Interrupt Source List (μPD78054/54Y and 78058F/58FY Subseries)

Interrupt Type	Default Priority Note	Interrupt Source		Internal/ External	Vector Table Address
		Name	Trigger		
Non-maskable	—	RESET	Low voltage level	External	0000H
		INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)		
	1	INTP0	Pin input edge detection	External	0006H
	2	INTP1			0008H
	3	INTP2			000AH
	4	INTP3			000CH
	5	INTP4			000EH
	6	INTP5			0010H
	7	INTP6			0012H
	8	INTCSI0	End of serial interface channel 0 transfer	Internal	0014H
	9	INTCSI1	End of serial interface channel 1 transfer		0016H
	10	INTSER	Serial interface channel 2 UART reception error generation		0018H
	11	INTSR	End of serial interface channel 2 UART reception		001AH
		INTCSI2	End of serial interface channel 2 3-wire transfer		
	12	INTST	End of serial interface channel 2 UART transmission		001CH
	13	INTTM3	Reference time interval signal from watch timer		001EH
	14	INTTM00	Generation of 16-bit timer register and capture/ compare register 00 (CR00) match signal		0020H
	15	INTTM01	Generation of 16-bit timer register and capture/ compare register 01 (CR01) match signal		0022H
	16	INTTM1	Generation of 8-bit timer/event counter 1 match signal		0024H
	17	INTTM2	Generation of 8-bit timer/event counter 2 match signal		0026H
	18	INTAD	End of A/D converter conversion		0028H
Software	—	BRK	BRK instruction execution	—	003EH

Note: Default priorities are intended for two or more simultaneously generated maskable interrupt requests. 0 is the highest priority and 18 is the lowest priority.

Table 6-20. Interrupt Source List (μPD780058/58Y Subseries)

Interrupt Type	Default Priority Note	Interrupt Source		Internal/ External	Vector Table Address
		Name	Trigger		
Non-maskable	—	RESET	Low voltage level	External	0000H
		INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)		
	1	INTP0	Pin input edge detection	External	0006H
	2	INTP1			0008H
	3	INTP2			000AH
	4	INTP3			000CH
	5	INTP4			000EH
	6	INTP5			0010H
	7	INTCSI0	End of serial interface channel 0 transfer	Internal	0014H
	8	INTCSI1	End of serial interface channel 1 transfer		0016H
	9	INTSER	Serial interface channel 2 UART reception error generation		0018H
	10	INTSR	End of serial interface channel 2 UART reception		001AH
		INTCSI2	End of serial interface channel 2 3-wire transfer		
	11	INTST	End of serial interface channel 2 UART transmission		001CH
	12	INTTM3	Reference time interval signal from watch timer		001EH
	13	INTTM00	Generation of 16-bit timer register and capture/ compare register 00 (CR00) match signal		0020H
	14	INTTM01	Generation of 16-bit timer register and capture/ compare register 01 (CR01) match signal		0022H
	15	INTTM1	Generation of 8-bit timer/event counter 1 match signal		0024H
	16	INTTM2	Generation of 8-bit timer/event counter 2 match signal		0026H
	17	INTAD	End of A/D converter conversion		0028H
Software	—	BRK	BRK instruction execution	—	003EH

Note: Default priorities are intended for two or more simultaneously generated maskable interrupt requests. 0 is the highest priority and 17 is the lowest priority.

The following table gives a listing of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 6-21. Interrupt Sources and Flags

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
		Register		Register		Register
INTWDT	TMIF4	IF0L	TMMK4	MK0L	TMPR4	PR0L
INTP0	PIF0		PMK0		PPR0	
INTP1	PIF1		PMK1		PPR1	
INTP2	PIF2		PMK2		PPR2	
INTP3	PIF3		PMK3		PPR3	
INTP4	PIF4		PMK4		PPR4	
INTP5	PIF5		PMK5		PPR5	
INTP6 Note	PIF6 Note		PMK6 Note		PPR6 Note	
INTCSI0	CSIIF0	IF0H	CSIMK0	MK0H	CSIPR0	PR0H
INTCSI1	CSIIF1		CSIMK1		CSIPR1	
INTSER	SERIF		SERMK		SERPR	
INTSR/INTCSI2	SRIF		SRMK		SRPR	
INTST	STIF		STMK		STPR	
INTTM3	TMIF3		TMMK3		TMPR3	
INTTM00	TMIF00		TMMK00		TMPR00	
INTTM01	TMIF01		TMMK01		TMPR01	
INTTM1	TMIF1	IF1L	TMMK1	MK1L	TMPR1	PR1L
INTTM2	TMIF2		TMMK2		TMPR2	
INTAD	ADIF		ADMK		ADPR0	

Note: Not provided for the μPD780058/58Y Subseries.

The following six types of registers control the interrupt functions:

- Interrupt request flag registers (IF0L, IF0H, IF1L)
- Interrupt mask flag registers (MK0L, MK0H, MK1L)
- Priority specification flag registers (PR0L, PR0H, PR1L)
- External interrupt mode registers (INTM0, INTM1)
- Sampling clock select register (SCS)
- Program status word (PSW)

Format of Interrupt Request Flag Registers (For μPD78054/54Y and 78058F/58FY Subseries)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
IF0L	PIF6	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	TMIF4	FFE0H	00H	R/W
IF0H	TMIF01	TMIF00	TMIF3	STIF	SRIF	SERIF	CSIIF1	CSIIF0	FFE1H	00H	R/W
IF1L	WTIF Note	0	0	0	0	ADIF	TMIF2	TMIF1	FFE2H	00H	R/W

××IF×	Interrupt request flag
0	No interrupt request signal
1	Interrupt request signal is generated Interrupt request state

Note: WTIF is a test input flag. A vectored interrupt request is not generated.

Cautions: 1. The TMIF4 flag is R/W enabled only when a watchdog timer is used as an interval timer. If a watchdog timer is used in watchdog timer mode 1, set the TMIF4 flag to 0.

2. Always set IF1L bits 3 to 6 to 0.

Format of Interrupt Request Flag Registers (For μPD780058/58Y Subseries)

Symbol	7	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
IF0L	0	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	TMIF4	FFE0H	00H	R/W
IF0H	TMIF01	TMIF00	TMIF3	STIF	SRIF	SERIF	CSIIF1	CSIIF0	FFE1H	00H	R/W
IF1L	WTIF Note	0	0	0	0	ADIF	TMIF2	TMIF1	FFE2H	00H	R/W

××IF×	Interrupt request flag
0	No interrupt request signal
1	Interrupt request signal is generated Interrupt request state

Note: WTIF is a test input flag. A vectored interrupt request is not generated.

Cautions: 1. The TMIF4 flag is R/W enabled only when a watchdog timer is used as an interval timer. If a watchdog timer is used in watchdog timer mode 1, set the TMIF4 flag to 0.

2. Always set IF0L bit 7 and IF1L bits 3 to 6 to 0.

Format of Interrupt Mask Flag Registers (For μPD78054/54Y and 78058F/58FY Subseries)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
MK0L	PMK6	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	TMMK4	FFE4H	FFH	R/W
MK0H	TMMK01	TMMK00	TMMK3	STMK	SRMK	SERMK	CSIMK1	CSIMK0	FFE5H	FFH	R/W
MK1L	WTMK Note	1	1	1	1	ADMK	TMMK2	TMMK1	FFE6H	FFH	R/W

××MK×	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Note: WTMK controls Standby mode release enable/disable. It does not control the interrupt function.

Cautions: 1. If the TMIF4 flag is read when a watchdog timer is used in watchdog timer mode 1, the MK0 value becomes undefined.

2. Because port 0 has an alternate function as the external interrupt input, when the output level is changed by specifying the output mode of the port function, an interrupt request flag is set. Therefore, 1 should be set in the interrupt mask flag before using the output mode.

3. Always set MK1L bits 3 to 6 to 1.

Format of Interrupt Mask Flag Registers (For μPD780058/58Y Subseries)

Symbol	7	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
MK0L	1	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	TMMK4	FFE4H	FFH	R/W
MK0H	TMMK01	TMMK00	TMMK3	STMK	SRMK	SERMK	CSIMK1	CSIMK0	FFE5H	FFH	R/W
MK1L	WTMK Note	1	1	1	1	ADMK	TMMK2	TMMK1	FFE6H	FFH	R/W

××MK×	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Note: WTMK controls Standby mode release enable/disable. It does not control the interrupt function.

Cautions: 1. If the TMIF4 flag is read when a watchdog timer is used in watchdog timer mode 1, the MK0 value becomes undefined.

2. Because port 0 has an alternate function as the external interrupt input, when the output level is changed by specifying the output mode of the port function, an interrupt request flag is set. Therefore, 1 should be set in the interrupt mask flag before using the output mode.

3. Always set MK0L bit 7 and MK1L bits 3 to 6 to 1.

Format of Priority Specification Flag Registers (For μPD78054/54Y and 78058F/58FY Subseries)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
PR0L	PPR6	PPR5	PPR4	PPR3	PPR2	PPR1	PPR0	TMPR4	FFE8H	FFH	R/W
	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>			
PR0H	TMPR01	TMPR00	TMPR3	STPR	SRPR	SERPR	CSIPR1	CSIPR0	FFE9H	FFH	R/W
	7	6	5	4	3	<2>	<1>	<0>			
PR1L	1	1	1	1	1	ADPR	TMPR2	TMPR1	FFEAH	FFH	R/W

××PR×	Priority level selection
0	High priority level
1	Low priority level

Cautions: 1. If a watchdog timer is used in Watchdog Timer mode 1, set the TMPR4 flag to 1.

2. Always set PR1L bits 3 to 7 to 1.

Format of Priority Specification Flag Registers (For μPD780058/58Y Subseries)

Symbol	7	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
PR0L	1	PPR5	PPR4	PPR3	PPR2	PPR1	PPR0	TMPR4	FFE8H	FFH	R/W
	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>			
PR0H	TMPR01	TMPR00	TMPR3	STPR	SRPR	SERPR	CSIPR1	CSIPR0	FFE9H	FFH	R/W
	7	6	5	4	3	<2>	<1>	<0>			
PR1L	1	1	1	1	1	ADPR	TMPR2	TMPR1	FFEAH	FFH	R/W

××PR×	Priority level selection
0	High priority level
1	Low priority level

Cautions: 1. If a watchdog timer is used in Watchdog Timer mode 1, set the TMPR4 flag to 1.

2. Always set PR0L bit 7 and PR1L bits 3 to 7 to 1.

Format of External Interrupt Mode Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
INTM0	ES31	ES30	ES21	ES20	ES11	ES10	0	0	FFECH	00H	R/W

ES11	ES10	INTP0 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES21	ES20	INTP1 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES31	ES30	INTP2 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

Caution: Before setting the valid edge of the INTP0/TIO0/P00 pin, stop the timer operation by clearing bits 1 to 3 (TMC01 to TMC03) of the 16-bit timer mode control register to 0, 0, 0.

Format of External Interrupt Mode Register 1 (For μPD78054/54Y and 78058F/58FY Subseries)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
INTM1	ES71	ES70	ES61	ES60	ES51	ES50	ES41	ES40	FFEDH	00H	R/W

ES41	ES40	INTP3 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES51	ES50	INTP4 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES61	ES60	INTP5 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES71	ES70	INTP6 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

Format of External Interrupt Mode Register 1 (For μPD780058/58Y Subseries)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
INTM1	0	0	ES61	ES60	ES51	ES50	ES41	ES40	FFEDH	00H	R/W

ES41	ES40	INTP3 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES51	ES50	INTP4 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES61	ES60	INTP5 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

Format of Sampling Clock Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
SCS	0	0	0	0	0	0	SCS1	SCS0	FF47H	00H	R/W

SCS1	SCS0	INTP0 sampling clock selection		
			MCS = 1	MCS = 0
0	0	$f_{XX}/2^N$		
0	1	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	0	$f_{XX}/2^5$	$f_X/2^5$ (156.3 kHz)	$f_X/2^6$ (78.1 kHz)
1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)

Caution: $f_{XX}/2^N$ is a clock to be supplied to the CPU and $f_{XX}/2^5$, $f_{XX}/2^6$, and $f_{XX}/2^7$ are clocks to be supplied to the peripheral hardware. $f_{XX}/2^N$ stops in the HALT mode.

Remarks: N: Value (N = 0 to 4) at bits 0 to 2 (PCC0 to PCC2) of the processor clock control register
f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
MCS: Bit 0 of oscillation mode selection register
Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of Program Status Word

	7	6	5	4	3	2	1	0	After Reset
PSW	IE	Z	RBS1	AC	RBS0	0	ISP	CY	02H

Used when a normal instruction is executed

ISP	Priority of interrupt currently being received
0	High-priority interrupt servicing (low-priority interrupt disable)
1	Interrupt request not acknowledged or low-priority interrupt servicing (all maskable interrupts enable)

IE	Interrupt request acknowledge enable/disable
0	Disable
1	Enable

(17) Registers controlling test function

- Interrupt request flag register 1L (IF1L)
- Interrupt mask flag register 1L (MK1L)
- Key return mode register (KRM)

Format of Interrupt Request Flag Register 1L

Symbol	<7>	6	5	4	3	<2>	<1>	<0>	Address	After Reset	R/W
IF1L	WTIF	0	0	0	0	ADIF	TMIF2	TMIF1	FFE2H	00H	R/W

WTIF	Watch timer overflow detection flag
0	Not detected
1	Detected

Caution: Be sure to set bits 3 through 6 to 0.

Format of Interrupt Mask Flag Register 1L

Symbol	<7>	6	5	4	3	<2>	<1>	<0>	Address	After Reset	R/W
MK1L	WTMK	1	1	1	1	ADMK	TMMK2	TMMK1	FFE6H	FFH	R/W

WTMK	Standby mode control by watch timer
0	Enables releasing the Standby mode
1	Disables releasing the Standby mode

Caution: Be sure to set bits 3 through 6 to 1.

Format of Key Return Mode Register

Symbol	7	6	5	4	3	2	<1>	<0>	Address	After Reset	R/W
KRM	0	0	0	0	0	0	KRMK	KRIF	FFF6H	02H	R/W

KRIF	Key return signal
0	Not detected
1	Detected (port 4 falling edge detection)

KRMK	Standby mode control by key return signal
0	Standby mode release enabled
1	Standby mode release disabled

Caution: When port 4 falling edge detection is used, be sure to clear KRIF to 0 (it is not cleared to 0 automatically).

(18) Registers controlling external device expansion function

The following two registers control the external device expansion function:

- Memory expansion mode register (MM)
- Internal memory size switching register (IMS)

Format of Memory Expansion Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
MM	0	0	PW1	PW0	0	MM2	MM1	MM0	FFF8H	10H	R/W

MM2	MM1	MM0	Single-chip/memory expansion mode selection		P40 to P47, P50 to P57, P64 to P67 pin state				
					P40 to P47	P50 to P53	P54, P55	P56, P57	P64 to P67
0	0	0	Single-chip mode		Port mode: Input	Port mode			
0	0	1			Port mode: Output				
0	1	1	Memory expansion mode	256-byte mode	AD0 to AD7	Port mode			P64 = $\overline{RD}$, P65 = $\overline{WR}$, P66 = $\overline{WAIT}$, P67 = ASTB
1	0	0		4K mode		A8 to A11	Port mode		
1	0	1		16K mode			A12, A13	Port mode	
1	1	1		Full address mode Note				A14, A15	
Settings other than above are prohibited									

PW1	PW0	Wait control
0	0	No wait
0	1	Wait (one wait state insertion)
1	0	Setting prohibited
1	1	Wait control by external wait pin

Note: The full address mode allows external expansion to the entire 64K address space except for the internal ROM (or PROM, flash memory), RAM, and SFR areas and the reserved areas.

Remark: P60 to P63 are used as port pins without regard to the mode (single-chip mode or memory expansion mode).

Format of Internal Memory Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	**Note 1**	R/W

ROM3	ROM2	ROM1	ROM0	Internal ROM size selection
0	1	0	0	16K Notes 2, 3
0	1	1	0	24K Note 2
1	0	0	0	32K Note 2
1	0	1	0	40K Note 2
1	1	0	0	48K
1	1	1	0	56K Note 4
1	1	1	1	60K
Settings other than above are prohibited				

RAM2	RAM1	RAM0	Internal high-speed RAM size selection
0	1	0	512 bytes Notes 2, 3
1	1	0	1024 bytes
Settings other than above are prohibited			

Notes: 1. The value of this register after reset differs depending on the model (refer to the table below).
2. Setting prohibited for the μPD78058F/58FY Subseries.
3. Setting prohibited for the μPD780058/58Y Subseries.
4. When the external device expansion function of the μPD78058/58Y, 78P058/58Y, 78058F/58FY, 78P058F/58FY, 780058/58Y, or 78F0058/58Y is used, set the internal ROM capacity to 56K or less.

Value of Internal Memory Size Switching Register After Reset (μPD78054/54Y and 78058F/58FY Subseries)

Part Number	Value After Reset
μPD78052/52Y	44H
μPD78053/53Y	C6H
μPD78054/54Y, 78P054	C8H
μPD78055/55Y	CAH
μPD78056/56Y/56F/56FY	CCH
μPD78058/58Y/58F/58FY, 78P058/58Y/58F/58FY	CFH

Value of Internal Memory Size Switching Register After Reset (μPD780058/58Y Subseries)

Part Number	Value After Reset
μPD780053/53Y	C6H
μPD780054/54Y	C8H
μPD780055/55Y	CAH
μPD780056/56Y	CCH
μPD780058/58Y, 78F0058/58Y	CFH

(19) Register controlling standby function

The standby function is intended to decrease the power consumption of the system. The following two modes are available: HALT and STOP.

When MCU is released from the STOP mode, a wait time is required for the crystal to resume oscillations. The wait time is controlled by the following register:

- Oscillation stabilization time select register (OSTS)

Format of Oscillation Stabilization Time Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0	FFFAH	04H	R/W

OSTS2	OSTS1	OSTS0	Selection of oscillation stabilization time when STOP mode is released		
				MCS = 1	MCS = 0
0	0	0	$2^{12}/f_{XX}$	$2^{12}/f_X$ (819 μs)	$2^{13}/f_X$ (1.64 ms)
0	0	1	$2^{14}/f_{XX}$	$2^{14}/f_X$ (3.28 ms)	$2^{15}/f_X$ (6.55 ms)
0	1	0	$2^{15}/f_{XX}$	$2^{15}/f_X$ (6.55 ms)	$2^{16}/f_X$ (13.1 ms)
0	1	1	$2^{16}/f_{XX}$	$2^{16}/f_X$ (13.1 ms)	$2^{17}/f_X$ (26.2 ms)
1	0	0	$2^{17}/f_{XX}$	$2^{17}/f_X$ (26.2 ms)	$2^{18}/f_X$ (52.4 ms)
Settings other than above are prohibited					

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)

f_X: Main system clock oscillation frequency

MCS: Bit 0 of oscillation mode select register (OSMS)

Values in parentheses apply to operation with f_X = 5.0 MHz.

The operation status in the HALT mode is described below.

HALT Mode Operating Status

Setting of HALT Mode / Item		On Execution of HALT Instruction during Main System Clock Operation		On Execution of HALT Instruction during Subsystem Clock Operation	
		Without Subsystem Clock Note 1	With Subsystem Clock Note 2	When Main System Clock Continues Oscillation	When Main System Clock Clock Stops Oscillation
Clock generator		Both main system and subsystem clocks can be oscillated. Clock supply to the CPU stops.			
CPU		Operation stops			
Port (output latch)		Status before HALT mode setting is held			
16-bit timer/event counter		Operable			Operable when watch timer output is selected as count clock (f_{XT} is selected as count clock of watch timer) or when TI00 is selected
8-bit timer/event counter		Operable			Operable when TI1 or TI2 is selected as count clock
Watch timer		Operable when $f_{XX}/2^7$ is selected as count clock	Operable		Operable when f_{XT} is selected as count clock
Watchdog timer		Operable		Operation stops	
A/D converter		Operable			Operation stops
D/A converter		Operable			
Real-time output port		Operable			
Serial interface	Other than automatic transmit/receive function	Operable			Operable when external SCK is used
	Automatic transmit/receive function	Operation stops			
External interrupt request	INTP0	INTP0 is operable when the clock supplied for peripheral hardware is selected as the sampling clock ($f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$)			Operation stops
	INTP1 to INTP5 (**Note 3**)	Operable			
Bus line for external expansion	AD0 to AD7	High impedance			
	A0 to A15	Status before HALT mode setting is held			
	ASTB	Low level			
	$\overline{WR}$, $\overline{RD}$	High level			
	$\overline{WAIT}$	High impedance			

Notes: 1. Including when an external clock is not supplied.
2. Including when an external clock is supplied.
3. In the μPD78054/54Y and 78058/58FY Subseries: INTP1 to INTP6.

The operation in the STOP mode is described below.

STOP Mode Operating Status

Item \ Setting of STOP Mode		With Subsystem Clock	Without Subsystem Clock
Clock generator		Only main system clock stops oscillation	
CPU		Operation stops	
Port (output latch)		Status before STOP mode setting is held	
16-bit timer/event counter		Operable when watch timer output is selected as count clock (f_{XT} is selected as count clock of watch timer)	Operation stops
8-bit timer/event counter		Operable when TI1 and TI2 are selected for the count clock	
Watch timer		Operable when f_{XT} is selected for the count clock	Operation stops
Watchdog timer		Operation stops	
A/D converter			
D/A converter		Operable	
Real-time output port		Operable when external trigger is used or TI1 and TI2 are selected for the 8-bit timer/event counter count clock	
Serial interface	Other than automatic transmit/receive function and UART	Operable when an externally supplied clock is specified as the serial clock	
	Automatic transmit/receive function and UART	Operation stops	
External interrupt request	INTP0	Not operable	
	INTP1 to INTP5 (**Note**)	Operable	
Bus line for external expansion	AD0 to AD7	High impedance	
	A0 to A15	Status before STOP mode setting is held	
	ASTB	Low level	
	$\overline{WR}$, $\overline{RD}$	High level	
	$\overline{WAIT}$	High impedance	

Note: In μPD78054/54Y and 78058F/58FY Subseries: INTP1 to INTP6.

Cautions: 1. When the STOP mode is set, the X2 pin is internally connected to V_{DD1} via a pull-up resistor to minimize the leakage current at the crystal oscillator. Thus, do not use the STOP mode in a system where an external clock is used for the main system clock.

2. Because the interrupt request signal is used to release the Standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the Standby mode is immediately released if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction. After the wait set using the oscillation stabilization time select register (OSTS), the operating mode is set.

(20) Reset function

The following two operations can generate a reset signal:

- External reset input via the $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer in Watchdog Timer mode

Table 6-22. Hardware Status After Reset (1/2)

Hardware		Status After Reset
Program counter (PC) Note 1		Contents of reset vector tables (0000H, 0001H) are set
Stack pointer (SP)		Undefined
Program status word (PSW)		02H
RAM	Data memory	Undefined Note 2
	General-purpose register	Undefined Note 2
Port (output latch)	Ports 0 to 3, Ports 7, 12, 13 (P0 to P3, P7, P12, P13)	00H
	Ports 4 to 6 (P4 to P6)	Undefined
Port mode registers (PM0 to PM7, PM12, PM13)		FFH
Pull-up resistor option registers (PUOH, PUOL)		00H
Processor clock control register (PCC)		04H
Oscillation mode select register (OSMS)		00H
Internal memory size switching register (IMS)		**Note 3**
Internal expansion RAM size switching register (IXS) Note 4		0AH
Memory expansion mode register (MM)		10H
Oscillation stabilization time select register (OSTS)		04H
16-bit timer/event counter	Timer register (TM0)	00H
	Capture/Compare registers (CR00, CR01)	Undefined
	Clock select register (TCL0)	00H
	Mode control register (TMC0)	00H
	Capture/Compare control register 0 (CRC0)	04H
	Output control register (TOC0)	00H
8-bit timer/event counters 1 and 2	Timer registers (TM1, TM2)	00H
	Compare registers (CR10, CR20)	Undefined
	Clock select register (TCL1)	00H
	Mode control register (TMC1)	00H
	Output control register (TOC1)	00H
Watch timer	Mode control register (TMC2)	00H
	Clock select register (TCL2)	00H
Watchdog timer	Mode register (WDTM)	00H
Serial interface	Clock select register (TCL3)	88H
	Shift registers (SIO0, SIO1)	Undefined
	Mode registers (CSIM0, CSIM1, CSIM2)	00H
	Serial bus interface control register (SBIC)	00H
	Slave address register (SVA)	Undefined

Table 6-22. Hardware Status After Reset (2/2)

Hardware		Status After Reset
Serial interface	Automatic data transmit/receive control register (ADTC)	00H
	Automatic data transmit/receive address pointer (ADTP)	00H
	Automatic data transmit/receive interval specification register (ADTI)	00H
	Asynchronous serial interface mode register (ASIM)	00H
	Asynchronous serial interface status register (ASIS)	00H
	Baud rate generator control register (BRGC)	00H
	Transmit shift register (TXS)	FFH
	Receive buffer register (RXB)	
	Serial interface pin select register (SIPS) Note 5	00H
	Interrupt timing specification register (SINT)	00H
A/D converter	Mode register (ADM)	01H
	Conversion result register (ADCR)	Undefined
	Input select register (ADIS)	00H
D/A converter	Mode register (DAM)	00H
	Conversion value setting registers (DACS0, DACS1)	00H
Real-time output port	Mode register (RTPM)	00H
	Control register (RTPC)	00H
	Buffer registers (RTBL, RTBH)	00H
ROM correction **Note 4**	Correction address registers (CORAD0, CORAD1)	0000H
	Correction control register (CORCN)	00H
Interrupt	Request flag registers (IF0L, IF0H, IF1L)	00H
	Mask flag registers (MK0L, MK0H, MK1L)	FFH
	Priority specification flag registers (PR0L, PR0H, PR1L)	FFH
	External interrupt mode registers (INTM0, INTM1)	00H
	Key return mode register (KRM)	02H
Sampling clock select register (SCS)		00H

Notes: 1. During reset input or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. If the reset signal is input in the Standby mode, the status before reset is retained even after reset.

3. The values after reset depend on the product, as follows:

	μPD78052/52Y	μPD78053/53Y μPD780053/53Y	μPD78054/54Y μPD78P054/54Y μPD780054/54Y	μPD78055/55Y μPD780055/55Y	μPD78056/56Y μPD78056F/56FY μPD780056/56Y	μPD78058/58Y μPD78P058/58Y μPD78058F/58FY μPD78P058F/58FY	μPD780058/58Y μPD78F0058/58Y
IMS	44H	C6H	C8H	CAH	CCH	CFH	

4. Provided to μPD78058/58Y, 78P058/58Y, 78058F/58FY, 78P058F/58FY, 780058/58Y, and 78F0058/58Y only.

5. Provided in μPD780058/58Y subseries only.

(21) Registers controlling ROM correction (μPD78058/58Y, 78058F/58FY, and 780058/58Y only)

The following two types of registers control the ROM correction:

- Correction address registers 0 and 1 (CORAD0 and CORAD1)
- Correction control register (CORCN)

Format of Correction Address Registers 0 and 1

Symbol	15	0	Address	After Reset	R/W
CORAD0			FF38H/FF39H	0000H	R/W
CORAD1			FF3AH/FF3BH	0000H	R/W

Cautions: 1. Set CORAD0 and CORAD1 when bits 1 (COREN0) and 3 (COREN1) of the correction control register (CORCN; refer to the figure below) are 0.

2. Only addresses at which operation codes are stored can be set in CORAD0 and CORAD1.

3. Do not set the following addresses to CORAD0 and CORAD1:

a. Address value in table area of table reference instruction (CALLT instruction): 0040H to 007FH

b. Address value in vector table area: 0000H to 003FH

Format of Correction Control Register

Symbol	7	6	5	4	<3>	<2>	<1>	<0>	Address	After Reset	R/W
CORCN	0	0	0	0	COREN1	CORST1	COREN0	CORST0	FF8AH	00H	R/W Note

CORST0	Correction address register 0 and fetch address match detection
0	Not detected
1	Detected

COREN0	Correction address register 0 and fetch address match detection control
0	Disabled
1	Enabled

CORST1	Correction address register 1 and fetch address match detection
0	Not detected
1	Detected

COREN1	Correction address register 1 and fetch address match detection control
0	Disabled
1	Enabled

Note: Bits 0 and 2 are read-only bits.

(22) Register controlling internal memory capacity

The μPD78P054, 78P058/58Y/58F/58FY, and 78F0058/58Y allow users to select the internal memory capacity. The following register is used to control the internal memory capacity:

- Internal memory size switching register (IMS)

Remarks: The μPD78P054 is a PROM version corresponding to the μPD78052/53/54.
The μPD78P058 is a PROM version corresponding to the μPD78055/56/58.

(a) μPD78P054 (for μPD78052/52Y, 78053/53Y, 78054/54Y Subseries)

To map the memory of the μPD78P054 identically to that of a mask ROM version, the value at the time the mask ROM version is reset must be set.

For the mask ROM version, IMS does not need to be set.

Format of Internal Memory Size Switching Register (μPD78P054)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	C8H	W

ROM3	ROM2	ROM1	ROM0	Selects internal ROM capacity
0	1	0	0	16K
0	1	1	0	24K
1	0	0	0	32K
Settings other than above are prohibited				

RAM2	RAM1	RAM0	Selects internal high-speed RAM capacity
0	1	0	512 bytes
1	1	0	1024 bytes
Settings other than above are prohibited			

The following table shows the set value of IMS to map the memory of the μPD78P054 identically to that of a mask ROM version.

Set Value of Internal Memory Size Switching Register (μPD78P054)

Target Mask ROM Version	Set Value of IMS
μPD78052/52Y	44H
μPD78053/53Y	C6H
μPD78054/54Y	C8H

Caution: When using a mask ROM version, do not set a value to IMS other than those shown in the table above.

(b) μPD78P058, 78P058Y (for μPD78054/54Y Subseries)

To map the memory of the μPD78P058 or 78P058Y identically to that of a mask ROM version, the value at the time the mask ROM version is reset must be set.

For the mask ROM version, IMS does not need to be set.

Format of Internal Memory Size Switching Register (μPD78P058/58Y)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	W

ROM3	ROM2	ROM1	ROM0	Selects internal ROM capacity
0	1	0	0	16K
0	1	1	0	24K
1	0	0	0	32K
1	0	1	0	40K
1	1	0	0	48K
1	1	1	0	56K Note
1	1	1	1	60K
Settings other than above are prohibited				

RAM2	RAM1	RAM0	Selects internal high-speed RAM capacity
0	1	0	512 bytes
1	1	0	1024 bytes
Settings other than above are prohibited			

Note: When the external device expansion function of the μPD78P058/58Y is used, set the internal PROM capacity to 56K or less.

The following table shows the set value of IMS to map the memory of the μPD78P058/58Y identically to that of a mask ROM version.

Set Value of Internal Memory Size Switching Register (μPD78P058/58Y)

Target Mask ROM Version	Set Value of IMS
μPD78052/52Y	44H
μPD78053/53Y	C6H
μPD78054/54Y	C8H
μPD78055/55Y	CAH
μPD78056/56Y	CCH
μPD78058/58Y	CFH

Caution: When using a mask ROM version, do not set a value to IMS other than those shown in the table above, except when the external device expansion function of the μPD78058/58Y is used.

(c) μPD78P058F, 78P058FY (for μPD78058F/58FY Subseries)

To map the memory of the μPD78P058F or 78P058FY identically to that of a mask ROM version, the value at the time the mask ROM version is reset must be set.

For the mask ROM version, IMS does not need to be set.

Format of Internal Memory Size Switching Register (μPD78P058F/58FY)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	W

ROM3	ROM2	ROM1	ROM0	Selects internal ROM capacity
1	1	0	0	48K
1	1	1	0	56K Note
1	1	1	1	60K
Settings other than above are prohibited				

RAM2	RAM1	RAM0	Selects internal high-speed RAM capacity
1	1	0	1024 bytes
Settings other than above are prohibited			

Note: When the external device expansion function of the μPD78P058F/58FY is used, set the internal PROM capacity to 56K or less.

The following table shows the set value of IMS to map the memory of the μPD78P058F/58FY identically to that of a mask ROM version.

Set Value of Internal Memory Size Switching Register (μPD78P058F/58FY)

Target Mask ROM Version	Set Value of IMS
μPD78056F/56FY	CCH
μPD78058F/58FY	CFH

Caution: When using a mask ROM version, do not set a value to IMS other than those shown in the table above, except when the external device expansion function of the μPD78058F/58FY is used.

(d) μPD78F0058, 78F0058Y (for μPD780058/58Y Subseries)

To map the memory of the μPD78F0058 or 78F0058Y identical to that of a mask ROM version, the value at the time the mask ROM version is reset must be set.

For the mask ROM version, IMS does not need to be set.

Format of Internal Memory Size Switching Register (μPD78F0058/58Y)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	W

ROM3	ROM2	ROM1	ROM0	Selects internal ROM capacity
0	1	1	0	24K
1	0	0	0	32K
1	0	1	0	40K
1	1	0	0	48K
1	1	1	0	56K Note
1	1	1	1	60K
Settings other than above are prohibited				

RAM2	RAM1	RAM0	Selects internal high-speed RAM capacity
1	1	0	1024 bytes
Settings other than above are prohibited			

Note: When the external device expansion function of the μPD78F0058/58Y is used, set the internal flash memory capacity to 56K or less.

The following table shows the set value of IMS to map the memory of the μPD78F0058/58Y identically to that of a mask ROM version.

Set Value of Internal Memory Size Switching Register (μPD78F0058/58Y)

Target Mask ROM Version	Set Value of IMS
μPD780053/53Y	C6H
μPD780054/54Y	C8H
μPD780055/55Y	CAH
μPD780056/56Y	CCH
μPD780058/58Y	CFH

Caution: When using a mask ROM version, do not set a value to IMS other than those shown in the table above, except when the external device expansion function of the μPD780058/58Y is used.

(23) Register controlling internal expansion RAM capacity

The μPD78P058/58Y/58F/58FY and 78F0058/58Y allow users to select the internal expansion RAM capacity. The following register is used to control the internal expansion RAM capacity:

- Internal expansion RAM size switching register (IXS)

Remark: This register is provided only for the μPD78058/58Y, 78P058/58Y, 78058F/58FY, 78P058F/58FY, 780058/58Y, and 78F0058/58Y.

Format of Internal Expansion RAM Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IXS	0	0	0	0	IX RAM3	IX RAM2	IX RAM1	IX RAM0	FFF4H	0AH	W

IX RAM3	IX RAM2	IX RAM1	IX RAM0	Selects internal expansion RAM capacity
1	1	0	0	0 bytes
1	0	1	0	1024 bytes
Settings other than above are prohibited				

The following table shows the set value of IXS to map the internal expansion RAM of the μPD78P058/58Y, 78P058F/58FY, or 78F0058/58Y identically to that of a mask ROM version.

Set Value of Internal Expansion RAM Size Switching Register

Target Mask ROM Version	Set Value of IXS
μPD78052/52Y	0CH
μPD78053/53Y, 780053/53Y	
μPD78054/54Y, 780054/54Y	
μPD78055/55Y, 780055/55Y	
μPD78056/56Y/56F/56FY, 780056/56Y	
μPD78058/58Y/58F/58FY, 780058/58Y	0AH

Cautions: 1. For the mask ROM version, IXS does not need to be set.

2. When using a mask ROM version, do not set a value to IXS other than those shown in the table above.

6.6 μPD78064, 78064B, and 780308 Subseries

6.6.1 Documentation Reference Information

Device Series Number	User's Manual Number	Date Published
μPD78064, 64Y	U10105EJ4V0UM01	September 1995
μPD78064B	U10785EJ2V0UM00	August 1997
μPD780308, 780308Y	U11377EJ2V0UM00	August 1997

Caution: The user should check the current User's Manual with the information in this section to be sure of having the most up-to-date information.

6.6.2 Device Series Differences

Device Series Number	ROM and RAM Differences		Number of Serial Channels
	ROM Size	RAM Size	
μPD78064, 78064Y	16K/24K/32K	512/1K	2
μPD78064B	32K	1K	
μPD780308, 780308Y	48K/60K	2K	3

General Programmer's Note

The NEC C-compiler and the NEC Assembler are capable of recognizing certain symbolic SFR bit names. These special bit names are identified in the user manual in one of the four ways shown below:

1. <7>
2. (7)
3. ⑦
4. [7]

Example:

	<7>	<6>	<5>	<4>	3	2	1	0
PCC	MCC	FRC	CLS	CSS	0	PCC2	PCC1	PCC0

If a bit number has one of the four symbols around it, the NEC software will recognize the associated symbolic bit name. For example to set bit 7, the user can write the code in two ways:

```
1.    SET1    MCC
2.    SET1    PCC.7
```

Alternatively since bit 2 does not have any of the four symbols around it, the user can only set this bit as follows:

```
1.    SET1    PCC.2
```

Note: The attempt to employ a symbolic name of bit-2 (PCC2) will return an error. Thus the use of instruction

```
SET1    PCC2
```

is improper since neither the NEC C-compiler nor the NEC Assembler recognizes this symbolic name and will generate an error.

6.6.3 Memory Address Space

Each model in the μPD78064/64Y, 78064B, and 780308/308Y Subseries can access a memory space of 64K. Figures 6-30 through 6-34 show memory maps of the respective models.

Figure 6-30. Memory Map (μPD78062/62Y)

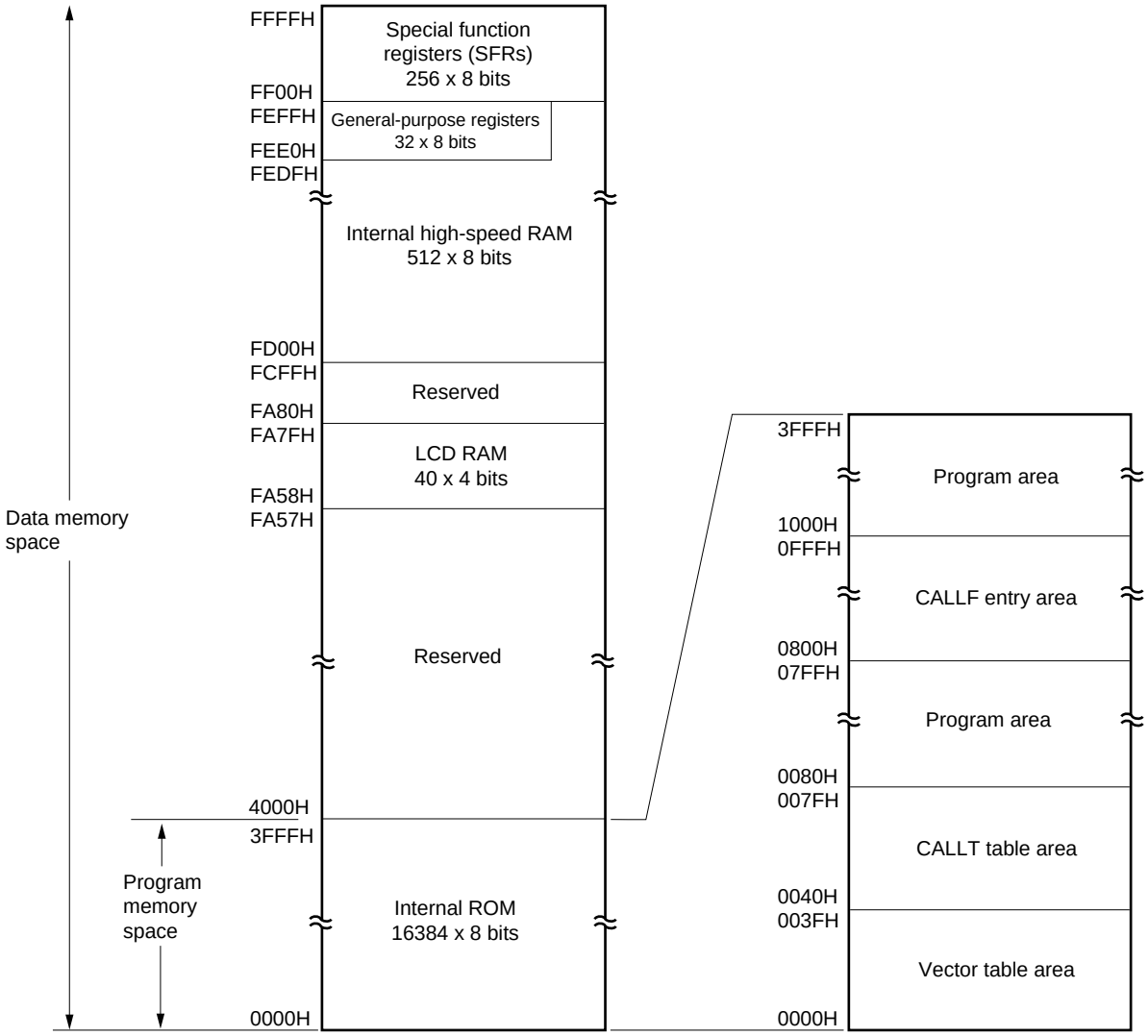


Figure 6-31. Memory Map (μPD78063/63Y)

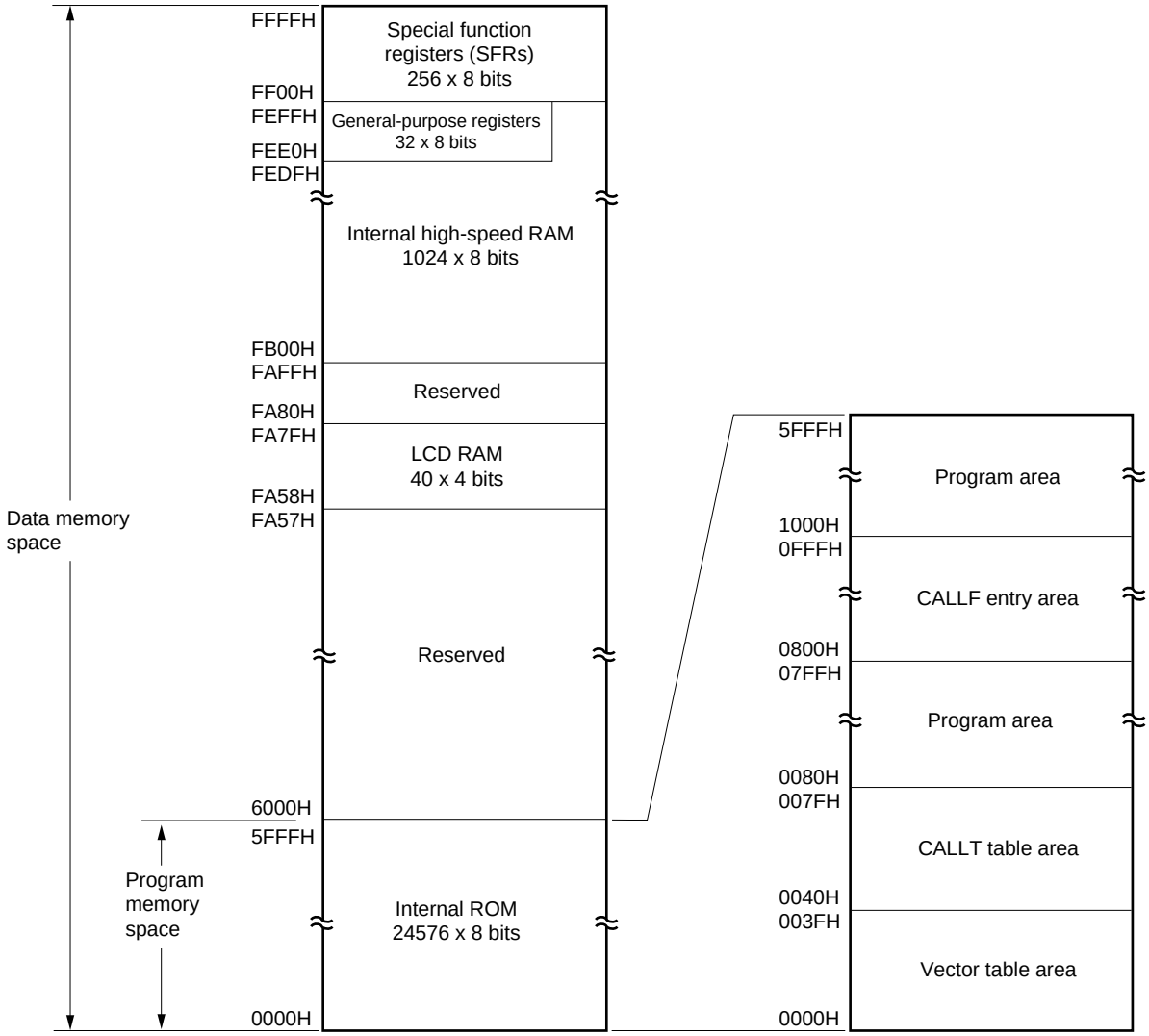


Figure 6-32. Memory Map (μPD78064/64Y/64B, 78P064/64Y/64B)

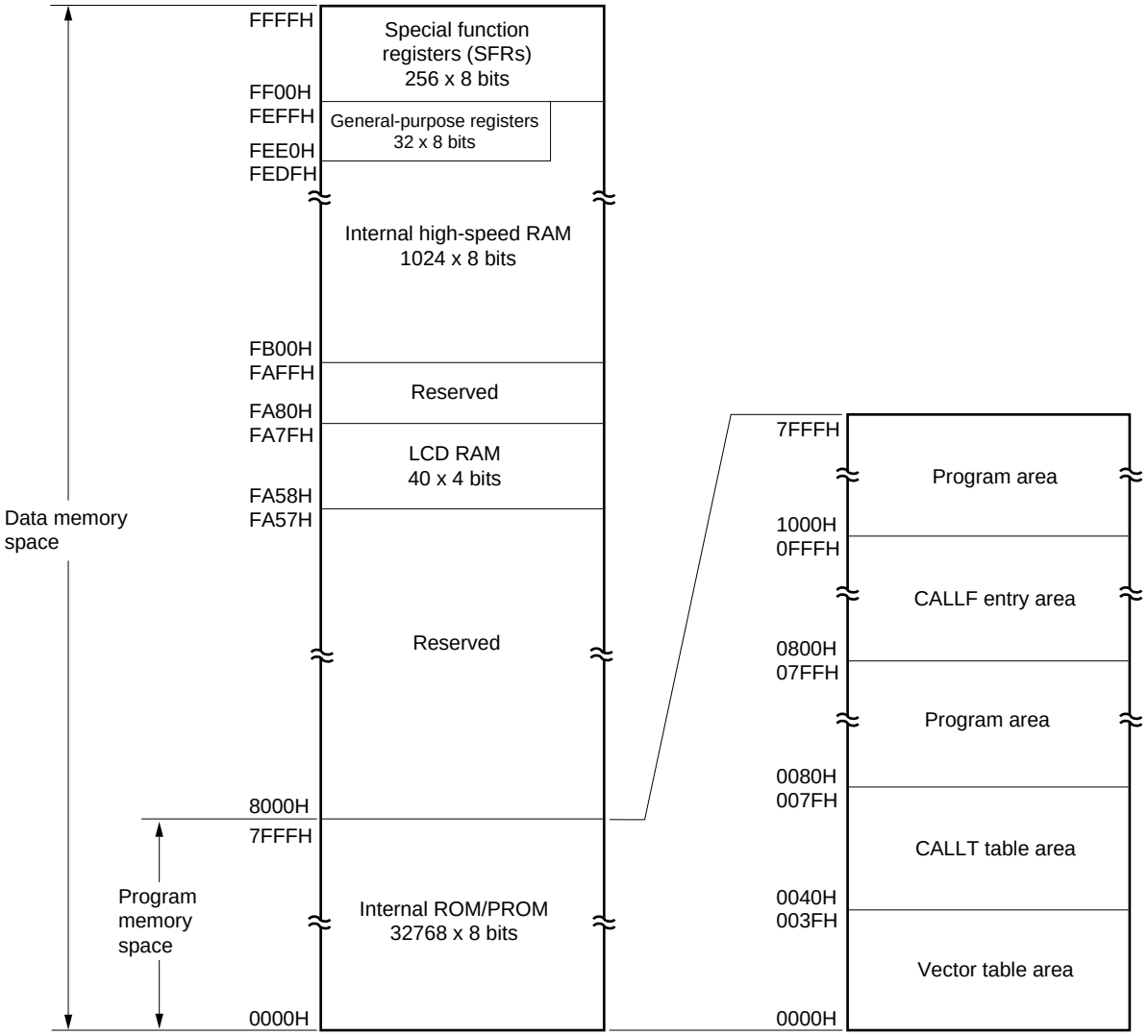


Figure 6-33. Memory Map (μPD780306/P306Y)

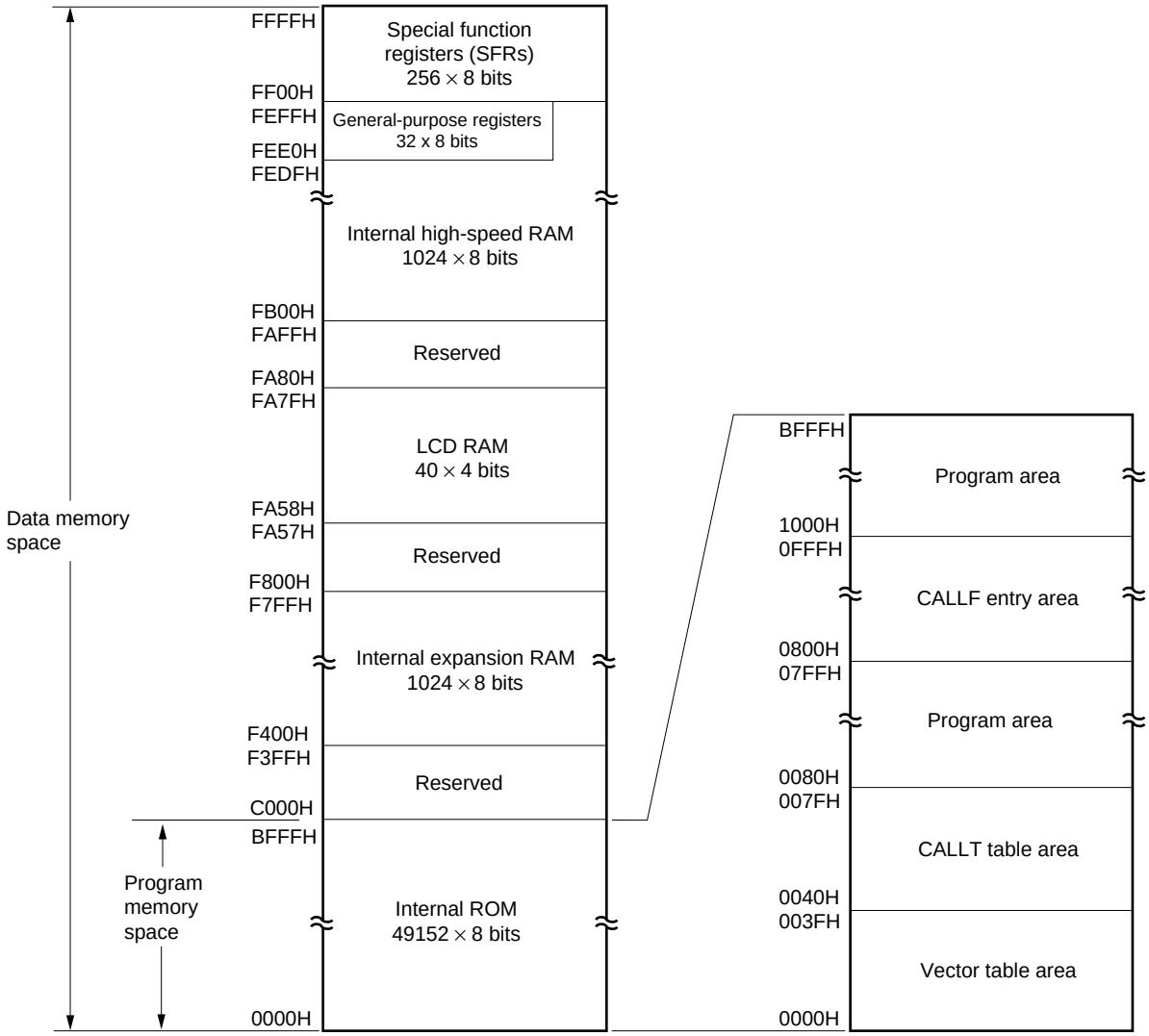
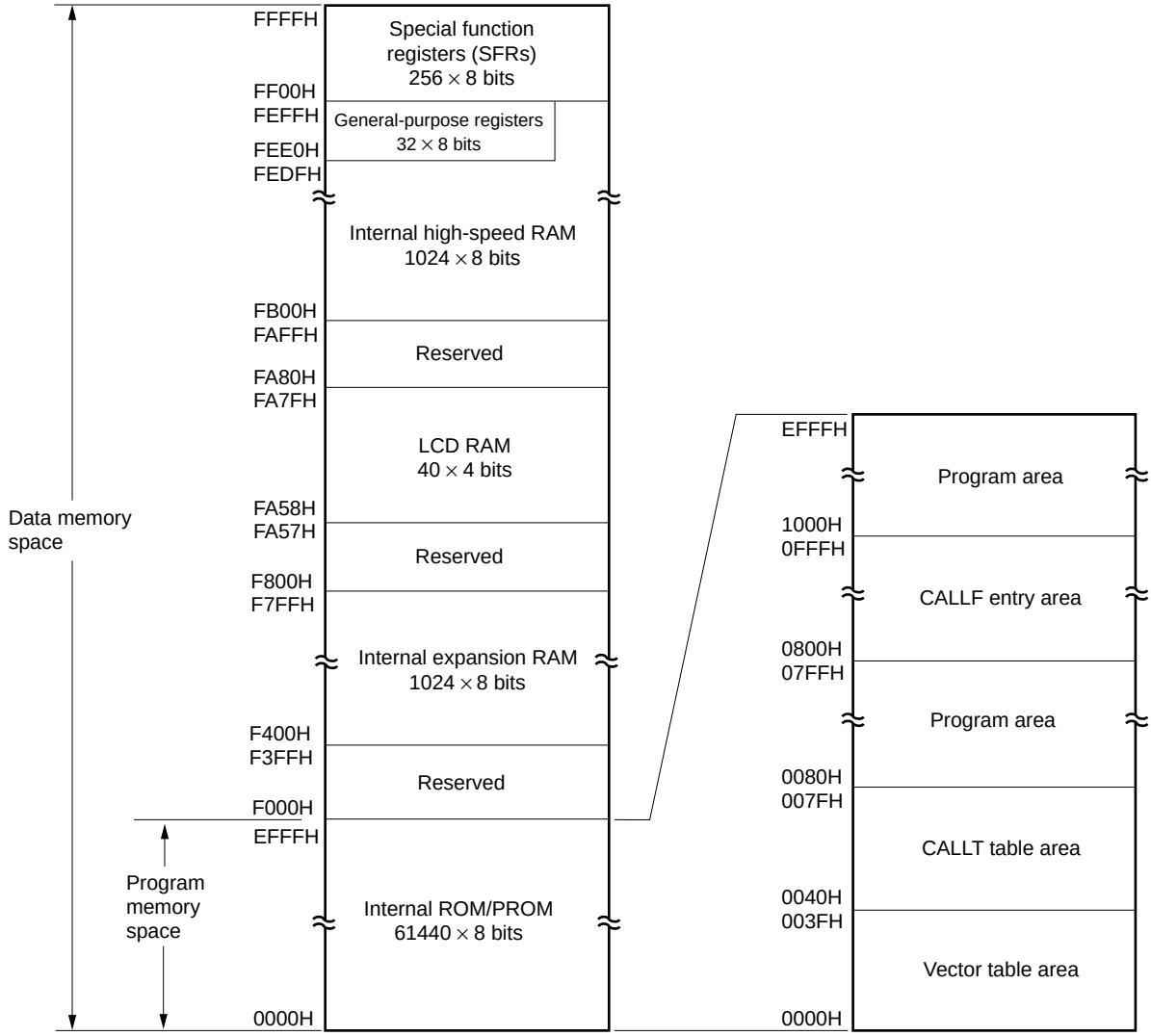


Figure 6-34. Memory Map (μPD780308/308Y, 78P0308/P308Y)



6.6.4 Special Function Registers (SFRs)

Table 6-23. Special Function Register List (μPD78064/64Y, 78064B, and 780308/308Y Subseries) (1/3)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulatable Bit Unit			After Reset
					1 Bit	8 Bits	16 Bits	
FF00H	Port 0	P0		R/W	√	√	–	00H
FF01H	Port 1	P1			√	√	–	
FF02H	Port 2	P2			√	√	–	
FF03H	Port 3	P3			√	√	–	
FF07H	Port 7	P7			√	√	–	
FF08H	Port 8	P8			√	√	–	
FF09H	Port 9	P9			√	√	–	
FF0AH	Port 10	P10			√	√	–	
FF0BH	Port 11	P11			√	√	–	
FF10H FF11H	Capture/compare register 00	CR00			–	–	√	Undefined
FF12H FF13H	Capture/compare register 01	CR01			–	–	√	
FF14H FF15H	16-bit timer register	TM0		R	–	–	√	00H
FF16H	Compare register 10	CR10		R/W	–	√	–	Undefined
FF17H	Compare register 20	CR20			–	√	–	
FF18H	8-bit timer register 1	TMS	TM1	R	–	√	√	00H
FF19H	8-bit timer register 2		TM2		–	√		
FF1AH	Serial I/O shift register 0	SIO0		R/W	–	√	–	Undefined
FF1FH	A/D conversion result register	ADCR		R	–	√	–	
FF20H	Port mode register 0	PM0		R/W	√	√	–	FFH
FF21H	Port mode register 1	PM1			√	√	–	
FF22H	Port mode register 2	PM2			√	√	–	
FF23H	Port mode register 3	PM3			√	√	–	
FF27H	Port mode register 7	PM7			√	√	–	
FF28H	Port mode register 8	PM8			√	√	–	
FF29H	Port mode register 9	PM9			√	√	–	
FF2AH	Port mode register 10	PM10			√	√	–	
FF2BH	Port mode register 11	PM11			√	√	–	
FF40H	Timer clock select register 0	TCL0			√	√	–	00H
FF41H	Timer clock select register 1	TCL1			–	√	–	
FF42H	Timer clock select register 2	TCL2			–	√	–	
FF43H	Timer clock select register 3	TCL3			–	√	–	88H
FF44H	Timer clock select register 4 Note	TCL4			–	√	–	

Note: This register is provided for μPD780308/308Y Subseries products only.

Table 6-23. Special Function Register List (μPD78064/64Y, 78064B, and 780308/308Y Subseries) (2/3)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulatable Bit Unit			After Reset
					1 Bit	8 Bits	16 Bits	
FF47H	Sampling clock select register	SCS		R/W	–	√	–	00H
FF48H	16-bit timer mode control register	TMC0			√	√	–	
FF49H	8-bit timer mode control register	TMC1			√	√	–	
FF4AH	Watch timer mode control register	TMC2			√	√	–	
FF4CH	Capture/compare control register 0	CRC0			√	√	–	04H
FF4EH	16-bit timer output control register	TOC0			√	√	–	00H
FF4FH	8-bit timer output control register	TOC1			√	√	–	
FF60H	Serial operation mode register 0	CSIM0			√	√	–	
FF61H	Serial bus interface control register	SBIC			√	√	–	
FF62H	Slave address register	SVA			–	√	–	Undefined
FF63H	Interrupt timing specification register	SINT			√	√	–	00H
FF6CH	Serial operation mode register 3 Note	CSIM3			√	√	–	
FF6DH	Serial I/O shift register 3 Note	SIO3			–	√	–	Undefined
FF70H	Asynchronous serial interface mode register	ASIM			√	√	–	00H
FF71H	Asynchronous serial interface status register	ASIS		R	–	√	–	
FF72H	Serial operation mode register 2	CSIM2		R/W	√	√	–	
FF73H	Baud rate generator control register	BRGC			–	√	–	
FF74H	Transmit shift register	TXS	SIO2	W	–	√	–	FFH
	Receive buffer register	RXB		R				
FF75H	Serial interface pin select register Note	SIPS		R/W	√	√	–	00H
FF80H	A/D converter mode register	ADM			√	√	–	01H
FF84H	A/D converter input select register	ADIS			–	√	–	00H
FFB0H	LCD display mode register	LCDM			√	√	–	
FFB2H	LCD display control register	LCDC			√	√	–	
FFB8H	Key return mode register	KRM			√	√	–	02H
FFE0H	Interrupt request flag register 0L	IF0	IF0L		√	√	√	00H
FFE1H	Interrupt request flag register 0H		IF0H		√	√		
FFE2H	Interrupt request flag register 1L	IF1L			√	√	–	
FFE4H	Interrupt request mask register 0L	MK0	MK0L		√	√	√	FFH
FFE5H	Interrupt request mask register 0H		MK0H		√	√		
FFE6H	Interrupt request mask register 1L	MK1L			√	√	–	
FFE8H	Priority order specification flag register 0L	PR0	PR0L		√	√	√	
FFE9H	Priority order specification flag register 0H		PR0H		√	√		
FFEAH	Priority order specification flag register 1L	PR1L			√	√	–	
FFECH	External interrupt mode register 0	INTM0			–	√	–	00H
FFEDH	External interrupt mode register 1	INTM1			–	√	–	

Note: This register is provided for μPD780308/308Y Subseries products only.

Table 6-23. Special Function Register List (μPD78064/64Y, 78064B, and 780308/308Y Subseries) (3/3)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulatable Bit Unit			After Reset
				1 Bit	8 Bits	16 Bits	
FFF0H	Internal memory size switching register	IMS	R/W	–	√	–	C8H
FFF2H	Oscillation mode select register	OSMS	W	–	√	–	00H
FFF3H	Pull-up resistor option register H	PUOH	R/W	√	√	–	
FFF4H	Internal expansion RAM size switching register Note 2	IXS	W	–	√	–	0AH
FFF7H	Pull-up resistor option register L	PUOL	R/W	√	√	–	00H
FFF9H	Watchdog timer mode register	WDTM		√	√	–	
FFFAH	Oscillation stabilization time select register	OSTS		–	√	–	04H
FFFBH	Processor clock control register	PCC		√	√	–	

(1) Registers controlling port functions

The following three types of registers control the ports:

- Port mode registers (PM0 to PM3, PM7 to PM11)
- Pull-up resistor option registers (PUOH, PUOL)
- Key return mode register (KRM).
  - Refer to section (15) for the register format.

Format of Port Mode Registers

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PM0	1	1	PM05	PM04	PM03	PM02	PM01	1	FF20H	FFH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FF21H	FFH	R/W
PM2	PM27	PM26	PM25	1	1	1	1	1	FF22H	FFH	R/W
PM3	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	FF23H	FFH	R/W
PM7	1	1	1	1	1	PM72	PM71	PM70	FF27H	FFH	R/W
PM8	PM87	PM86	PM85	PM84	PM83	PM82	PM81	PM80	FF28H	FFH	R/W
PM9	PM97	PM96	PM95	PM94	PM93	PM92	PM91	PM90	FF29H	FFH	R/W
PM10	1	1	1	1	PM103	PM102	PM101	PM100	FF2AH	FFH	R/W
PM11	PM117	PM116	PM115	PM114	PM113	PM112	PM111	PM110	FF2BH	FFH	R/W

PMmn	Pmn pin input/output mode selection (m = 0 to 3, 7 to 11 : n = 0 to 7)
0	Output mode (output buffer ON)
1	Input mode (output buffer OFF)

Format of Pull-Up Resistor Option Registers

Symbol	7	6	5	4	<3>	<2>	<1>	<0>	Address	After Reset	R/W
PUOH	0	0	0	0	PUO11	PUO10	PUO9	PUO8	FFF3H	00H	R/W
	<7>	6	5	4	<3>	<2>	<1>	<0>			
PUOL	PUO7	0	0	0	PUO3	PUO2	PUO1	PUO0	FFF7H	00H	R/W

PUOm	Pm internal pull-up resistor selection (m = 0 to 3, 7 to 11)
0	Internal pull-up resistor not used
1	Internal pull-up resistor used

Cautions: 1. Zeros must be set to bits 4 through 7 of PUOH and bits 4 through 6 of PUOL.

2. P00 and P07 pins do not incorporate a pull-up resistor.

3. When ports 1, 8, and 9 are used as alternate function pins, a pull-up resistor cannot be used even if 1 is set in PUOm (m = 1, 8, 9).

(2) Registers controlling clock generator

The following two registers control the clock generator:

- Processor clock control register (PCC)
- Oscillation mode select register (OSMS)

Format of Processor Clock Control Register

Symbol	<7>	<6>	<5>	<4>	3	2	1	0	Address	After Reset	R/W
PCC	MCC	FRC	CLS	CSS	0	PCC2	PCC1	PCC0	FFFBH	04H	R/W Note 1

R/W	MCC	Main system clock oscillation control Note 2
	0	Oscillation possible
	1	Oscillation stopped

R/W	FRC	Subsystem clock feedback resistor selection
	0	Internal feedback resistor used
	1	Internal feedback resistor not used

R	CLS	CPU clock status
	0	Main system clock
	1	Subsystem clock

R/W	CSS	PCC2	PCC1	PCC0	CPU clock selection (f_{CPU})		
						MCS = 1	MCS = 0
	0	0	0	0	f_{XX}	f_X (0.4 μs)	f_X/2 (0.8 μs)
		0	0	1	$f_{XX}/2$	$f_X/2$ (0.8 μs)	$f_X/2^2$ (1.6 μs)
		0	1	0	$f_{XX}/2^2$	$f_X/2^2$ (1.6 μs)	$f_X/2^3$ (3.2 μs)
		0	1	1	$f_{XX}/2^3$	$f_X/2^3$ (3.2 μs)	$f_X/2^4$ (6.4 μs)
		1	0	0	$f_{XX}/2^4$	$f_X/2^4$ (6.4 μs)	$f_X/2^5$ (12.8 μs)
	1	0	0	0	$f_{XT}/2$ (122 μs)		
		0	0	1			
		0	1	0			
		0	1	1			
		1	0	0			
	Settings other than above are prohibited						

Notes: 1. Bit 5 is a read-only bit.

2. When the CPU is operating on the subsystem clock, MCC should be used to stop the main system clock oscillation. A STOP instruction should not be used.

Caution: Bit 3 must be set to 0.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)

f_X: Main system clock oscillator frequency

f_{XT}: Subsystem clock oscillator frequency

MCS: Bit 0 of oscillation mode select register (OSMS)

Values in parentheses indicate minimum instruction execution time: $2/f_{CPU}$ when operating at f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

Format of Oscillation Mode Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
OSMS	0	0	0	0	0	0	0	MCS	FFF2H	00H	W

MCS	Main system clock scaler control
0	Scaler used
1	Scaler not used

Cautions: 1. Writing to OSMS should be performed only immediately after reset signal release and before peripheral hardware operation starts. Writing data (including the same data as previously) to OSMS causes a delay of the main system clock cycle of up to 2/f_x during the write operation. Therefore, if this register is written during the operation, in peripheral hardware that operates with the main system clock, a temporary error occurs in the count clock cycle of the timer, etc. In addition, because the oscillation mode is changed by this register, the clocks for peripheral hardware as well as that for the CPU are switched.

2. When writing "1" to MCS, V_{DD} must be 2.7 V or higher before the write execution.

(3) Registers controlling 16-bit timer/event counter

The following seven registers control the 16-bit timer/event counter:

- Timer clock select register 0 (TCL0)
- 16-bit timer mode control register (TMC0)
- Capture/compare control register 0 (CRC0)
- 16-bit timer output control register (TOC0)
- Port mode register 3 (PM3)
  - Refer to section (1) for the register format.
- External interrupt mode register 0 (INTM0)
  - Refer to section (15) for the register format.
- Sampling clock select register (SCS)
  - Refer to section (15) for the register format.

Format of Timer Clock Select Register 0

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL0	CLOE	TCL06	TCL05	TCL04	TCL03	TCL02	TCL01	TCL00	FF40H	00H	R/W

This section controls the clock output circuit.
Refer to **(7) Registers controlling clock output function** or **Chapter 12** of *μPD78064, 78064Y Subseries User's Manual*, **Chapter 10** of *μPD78064B Subseries User's Manual*, or **Chapter 12** of *μPD780308, 780308Y Subseries User's Manual* for detailed information.

TCL06	TCL05	TCL04	16-bit timer register count clock selection		
				MCS = 1	MCS = 0
0	0	0	TI00 (Valid edge specifiable)		
0	0	1	$2f_{XX}$	Setting prohibited	f_X (5.0 MHz)
0	1	0	f_{XX}	f_X (5.0 MHz)	$f_X/2$ (2.5 MHz)
0	1	1	$f_{XX}/2$	$f_X/2$ (2.5 MHz)	$f_X/2^2$ (1.25 MHz)
1	0	0	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	1	1	Watch timer output (INTTM3)		
Settings other than above are prohibited					

Cautions: 1. Setting of the TI00/INTP0 pin valid edge is performed by external interrupt mode register 0, and selection of the sampling clock frequency is performed by the sampling clock select register.

2. To read the count value when TI00 has been specified as the TM0 count clock, the value should be read from TM0, not from capture/compare register 01 (CR01).

3. To write data other than that already written to TCL0, stop the timer operation once.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
TI00: 16-bit timer/event counter input pin
TM0: 16-bit timer register
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of 16-Bit Timer Mode Control Register

Symbol	7	6	5	4	3	2	1	<0>	Address	After Reset	R/W
TMC0	0	0	0	0	TMC03	TMC02	TMC01	OVF0	FF48H	00H	R/W

TMC03	TMC02	TMC01	Operating mode clear mode selection	TO0 output timing selection	Interrupt generation
0	0	0	Operation stop (TM0 cleared to 0)	No change	Not generated
0	0	1	PWM mode (free-running)	PWM pulse output	Generated on match between TM0 and CR00 and match between TM0 and CR01
0	1	0	Free-running mode	Match between TM0 and CR00 or match between TM0 and CR01	
0	1	1		Match between TM0 and CR00, match between TM0 and CR01, or TI00 valid edge	
1	0	0	Clear and start on TI00 valid edge	Match between TM0 and CR00 or match between TM0 and CR01	
1	0	1		Match between TM0 and CR00, match between TM0 and CR01, or TI00 valid edge	
1	1	0	Clear and start on match between TM0 and CR00	Match between TM0 and CR00 or match between TM0 and CR01	
1	1	1		Match between TM0 and CR00, match between TM0 and CR01, or TI00 valid edge	

OVF0	16-bit timer register overflow detection
0	Overflow not detected
1	Overflow detected

Cautions:

1. **The 16-bit timer register (TM0) starts operation when a value other than 0, 0, 0 is set to TMC01 to TMC03 (Operation Stop mode). To stop the operation, set TMC01 to TMC03 to 0, 0, 0.**
2. **Switch the Clear mode and the T00 output timing after stopping the timer operation (by setting TMC01 to TMC03 to 0, 0, 0).**
3. **Set the valid edge of the TI00/INTP0 pin with external interrupt mode register 0 and select the sampling clock frequency with the sampling clock select register.**
4. **When using the PWM mode, set the PWM mode and then set data to CR00.**
5. **If Clear and Start mode on a match between TM0 and CR00 is selected, when the set value of CR00 is FFFFH and the TM0 value changes from FFFFH to 0000H, the OVF0 flag is set to 1.**

Remarks:

TO0:	16-bit timer/event counter output pin
TI00:	16-bit timer/event counter input pin
TM0:	16-bit timer register
CR00:	Compare register 00
CR01:	Compare register 01

Format of Capture/Compare Control Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
CRC0	0	0	0	0	0	CRC02	CRC01	CRC00	FF4CH	04H	R/W

CRC00	CR00 operating mode selection
0	Operates as compare register
1	Operates as capture register

CRC01	CR00 capture trigger selection
0	Captures on valid edge of TI01
1	Captures on valid edge of TI00

CRC02	CR01 operating mode selection
0	Operates as compare register
1	Operates as capture register

Cautions: 1. Timer operation must be stopped before setting CRC0.

2. When Clear and Start mode on a match between TM0 and CR00 is selected with the 16-bit timer mode control register, CR00 should not be specified as a capture register.

Format of 16-Bit Timer Output Control Register

Symbol	7	<6>	<5>	4	<3>	<2>	1	<0>	Address	After Reset	R/W
TOC0	0	OSPT	OSPE	TOC04	LVS0	LVR0	TOC01	TOE0	FF4EH	00H	R/W

TOE0	16-bit timer/event counter output control
0	Output disabled (Port mode)
1	Output enabled

TOC01	In PWM mode	In other modes
	Active level selection	Timer output F/F control by match of CR00 and TM0
0	Active high	Inversion operation disabled
1	Active low	Inversion operation enabled

LVS0	LVR0	16-bit timer/event counter timer output F/F status setting
0	0	No change
0	1	Timer output F/F reset (to 0)
1	0	Timer output F/F set (to 1)
1	1	Setting prohibited

TOC04	Timer output F/F control by match of CR01 and TM0
0	Inversion operation disabled
1	Inversion operation enabled

OSPE	One-shot pulse output control
0	Continuous pulse output
1	One-shot pulse output

OSPT	Control of one-shot pulse output trigger by software
0	One-shot pulse trigger not used
1	One-shot pulse trigger used

Cautions: 1. Timer operation must be stopped before setting TOC0.

2. If LVS0 and LVR0 are read after data is set, they will be 0.

3. OSPT is cleared automatically after data setting, and will therefore be 0 if read.

(4) Registers controlling 8-bit timer/event counters 1 and 2

The following four registers control the 8-bit timer/event counters:

- Timer clock select register 1 (TCL1)
- 8-bit timer mode control register 1 (TMC1)
- 8-bit timer output control register (TOC1)
- Port mode register 3 (PM3).
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 1

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL1	TCL17	TCL16	TCL15	TCL14	TCL13	TCL12	TCL11	TCL10	FF41H	00H	R/W

TCL17	TCL16	TCL15	TCL14	8-bit timer register 2 count clock selection		
					MCS = 1	MCS = 0
0	0	0	0	TI2 falling edge		
0	0	0	1	TI2 rising edge		
0	1	1	0	$f_{XX}/2$	$f_X/2$ (2.5 MHz)	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
1	1	1	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)
1	1	1	1	$f_{XX}/2^{11}$	$f_X/2^{11}$ (2.4 kHz)	$f_X/2^{12}$ (1.2 kHz)
Settings other than above are prohibited						

TCL13	TCL12	TCL11	TCL10	8-bit timer register 1 count clock selection		
					MCS = 1	MCS = 0
0	0	0	0	TI1 falling edge		
0	0	0	1	TI1 rising edge		
0	1	1	0	$f_{XX}/2$	$f_X/2$ (2.5 MHz)	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
1	1	1	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)
1	1	1	1	$f_{XX}/2^{11}$	$f_X/2^{11}$ (2.4 kHz)	$f_X/2^{12}$ (1.2 kHz)
Settings other than above are prohibited						

Caution: When rewriting TCL1 to other data, stop the timer operation beforehand.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
TI1: 8-bit timer register 1 input pin
TI2: 8-bit timer register 2 input pin
MCS: Oscillation mode select register (OSMS) bit 0
Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of 8-Bit Timer Mode Control Register 1

Symbol	7	6	5	4	3	2	<1>	<0>	Address	After Reset	R/W
TMC1	0	0	0	0	0	TMC12	TCE2	TCE1	FF49H	00H	R/W

TCE1	8-bit timer register 1 operation control
0	Operation stop (TM1 clear to 0)
1	Operation enable

TCE2	8-bit timer register 2 operation control
0	Operation stop (TM2 clear to 0)
1	Operation enable

TMC12	Operating mode selection
0	8-bit timer register × 2 channel mode (TM1, TM2)
1	16-bit timer register × 1 channel mode (TMS)

Cautions: 1. Switch the operating mode after stopping timer operation.

2. When used as a 16-bit timer register, TCE1 should be used to control enable/stop.

Format of 8-Bit Timer Output Control Register

Symbol	<7>	<6>	5	<4>	<3>	<2>	1	<0>	Address	After Reset	R/W
TOC1	LVS2	LVR2	TOC15	TOE2	LVS1	LVR1	TOC11	TOE1	FF4FH	00H	R/W

TOE1	8-bit timer/event counter 1 output control
0	Output disable (Port mode)
1	Output enable

TOC11	8-bit timer/event counter 1 timer output F/F control
0	Inverted operation disable
1	Inverted operation enable

LVS1	LVR1	8-bit timer/event counter 1 timer output F/F status set
0	0	Unchanged
0	1	Timer output F/F reset (to 0)
1	0	Timer output F/F set (to 1)
1	1	Setting prohibited

TOE2	8-bit timer/event counter 2 output control
0	Output disable (Port mode)
1	Output enable

TOC15	8-bit timer/event counter 2 timer output F/F control
0	Inverted operation disable
1	Inverted operation enable

LVS2	LVR2	8-bit timer/event counter 2 timer output F/F status set
0	0	Unchanged
0	1	Timer output F/F reset (to 0)
1	0	Timer output F/F set (to 1)
1	1	Setting prohibited

Cautions: 1. Be sure to set TOC1 after stopping timer operation.

2. After data setting, 0 can be read from LVS1, LVS2, LVR1, and LVR2.

(5) Registers controlling watch timer

The following two registers control the watch timer:

- Timer clock select register 2 (TCL2)
- Watch timer mode control register (TMC2)

Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL2	TCL27	TCL26	TCL25	TCL24	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

This section controls the watchdog timer.
Refer to **(6) Registers controlling watchdog timer** or **Chapter 11** of *μPD78064, 78064Y Subseries User's Manual*, **Chapter 9** of *μPD78064B Subseries User's Manual*, or **Chapter 11** of *μPD780308, 780308Y Subseries User's Manual* for detailed information.

This section controls the buzzer output function.
Refer to **(8) Registers controlling buzzer output function** or **Chapter 13** of *μPD78064, 78064Y Subseries User's Manual*, **Chapter 11** of *μPD78064B Subseries User's Manual*, or **Chapter 13** of *μPD780308, 780308Y Subseries User's Manual* for detailed information.

TCL24	Watch timer count clock selection		
		MCS = 1	MCS = 0
0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	f_{XT} (32.768 kHz)		

Caution: When rewriting TCL2 to other data, stop the timer operation beforehand.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
f_{XT}: Subsystem clock oscillation frequency
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

Format of Watch Timer Mode Control Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TMC2	0	TMC26	TMC25	TMC24	TMC23	TMC22	TMC21	TMC20	FF4AH	00H	R/W

TMC26	TMC25	TMC24	Prescaler interval time selection		
			f_{XX} = 5.0 MHz operation	f_{XX} = 4.19 MHz operation	f_{XT} = 32.768 kHz operation
0	0	0	$2^4/f_W$ (410 μs)	$2^4/f_W$ (488 μs)	$2^4/f_W$ (488 μs)
0	0	1	$2^5/f_W$ (819 μs)	$2^5/f_W$ (977 μs)	$2^5/f_W$ (977 μs)
0	1	0	$2^6/f_W$ (1.64 ms)	$2^6/f_W$ (1.95 ms)	$2^6/f_W$ (1.95 ms)
0	1	1	$2^7/f_W$ (3.28 ms)	$2^7/f_W$ (3.91 ms)	$2^7/f_W$ (3.91 ms)
1	0	0	$2^8/f_W$ (6.55 ms)	$2^8/f_W$ (7.81 ms)	$2^8/f_W$ (7.81 ms)
1	0	1	$2^9/f_W$ (13.1 ms)	$2^9/f_W$ (15.6 ms)	$2^9/f_W$ (15.6 ms)
Settings other than above are prohibited					

TMC23	Watch flag set time selection		
	f_{XX} = 5.0 MHz operation	f_{XX} = 4.19 MHz operation	f_{XT} = 32.768 kHz operation
0	$2^{14}/f_W$ (0.4 sec)	$2^{14}/f_W$ (0.5 sec)	$2^{14}/f_W$ (0.5 sec)
1	$2^{13}/f_W$ (0.2 sec)	$2^{13}/f_W$ (0.25 sec)	$2^{13}/f_W$ (0.25 sec)

TMC22	5-bit counter operation control
0	Clear after operation stop
1	Operation enable

TMC21	Prescaler operation control
0	Clear after operation stop
1	Operation enable

TMC20	Watch operating mode selection
0	Normal operating mode (flag set at $f_W/2^{14}$)
1	Fast feed operating mode (flag set at $f_W/2^5$)

Caution: When the watch timer is used, the prescaler should not be cleared frequently.

Remarks: f_W: Watch timer clock frequency ($f_{XX}/2^7$ or f_{XT})
f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
f_{XT}: Subsystem clock oscillation frequency

(6) Registers controlling watchdog timer

The following two registers control the watchdog timer:

- Timer clock select register 2 (TCL2)
- Watchdog timer mode register (WDTM)

Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL2	TCL27	TCL26	TCL25	TCL24	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

This section controls the watch timer.
Refer to **(5) Registers controlling watch timer** or **Chapter 10** of *μPD78064, 78064Y Subseries User's Manual*, **Chapter 8** of *μPD78064B Subseries User's Manual*, or **Chapter 10** of *μPD780308, 780308Y Subseries User's Manual* for detailed information.

This section controls the buzzer output function.
Refer to **(8) Registers controlling buzzer output function** or **Chapter 13** of *μPD78064, 78064Y Subseries User's Manual*, **Chapter 11** of *μPD78064B Subseries User's Manual*, or **Chapter 13** of *μPD780308, 780308Y Subseries User's Manual* for detailed information.

TCL22	TCL21	TCL20	Watchdog timer count clock selection		
				MCS = 1	MCS = 0
0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
1	1	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)
1	1	1	$f_{XX}/2^{11}$	$f_X/2^{11}$ (2.4 kHz)	$f_X/2^{12}$ (1.2 kHz)

Caution: When rewriting TCL2 to other data, stop the timer operation beforehand.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz.
This register is also used to control the watch timer and the buzzer.

Format of Watchdog Timer Mode Register

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
WDTM	RUN	0	0	WDTM4	WDTM3	0	0	0	FFF9H	00H	R/W

WDTM4	WDTM3	Watchdog timer operation mode selection Note 1
0	×	Interval timer mode Note 3 (Maskable interrupt request occurs upon generation of an overflow.)
1	0	Watchdog timer mode 2 (Non-maskable interrupt request occurs upon generation of an overflow.)
1	1	Watchdog timer mode 2 (Reset operation is activated upon generation of an overflow.)

RUN	Watchdog timer operation mode selection Note 2
0	Count stop
1	Counter is cleared and counting starts.

Notes: 1. Once set to 1, WDTM3 and WDTM4 cannot be cleared to 0 by software.

2. Once set to 1, RUN cannot be cleared to 0 by software.
   Thus, once counting starts, it can only be stopped by $\overline{\text{RESET}}$ input.

3. The watchdog timer starts operating as an interval timer as soon as RUN has been set to 1.

Cautions: 1. When 1 is set in RUN so that the watchdog timer is cleared, the actual overflow time is up to 0.5% shorter than the time set by timer clock select register 2.

2. To use the watchdog timer modes 1 and 2, confirm that the interrupt request flag (TMIF4) is 0, and then set WDTM4 to 1.
If WDTM4 is set to 1 while TMIF4 is 1, the non-maskable interrupt request occurs regardless of the contents of WDTM3.

Remark: ×: Don't care

(7) Registers controlling clock output function

The following two registers control the clock output function:

- Timer clock select register 0 (TCL0)
- Port mode register 3 (PM3).
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 0

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL0	CLOE	TCL06	TCL05	TCL04	TCL03	TCL02	TCL01	TCL00	FF40H	00H	R/W

This section controls the 16-bit timer.
Refer to **(3) Registers controlling 16-bit timer/event counter** or
Chapter 8 of *μPD78064, 78064Y Subseries User's Manual*,
Chapter 6 of *μPD78064B Subseries User's Manual*, or
Chapter 8 of *μPD780308, 780308Y Subseries User's Manual*
for detailed information.

TCL03	TCL02	TCL01	TCL00	PCL output clock selection		
					MCS = 1	MCS = 0
0	0	0	0	f_{XT} (32.768 kHz)		
0	1	0	1	f_{XX}	f_X (5.0 MHz)	$f_X/2$ (2.5 MHz)
0	1	1	0	$f_{XX}/2$	$f_X/2$ (2.5 MHz)	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
Settings other than above are prohibited						

CLOE	PCL output control
0	Output disable
1	Output enable

Cautions: 1. When enabling PCL output, set TCL00 to TCL03, then set 1 in CLOE with a 1-bit memory manipulation instruction.

2. To write data other than that already written to TCL0, stop the timer operation once.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)

f_X: Main system clock oscillation frequency

f_{XT}: Subsystem clock oscillation frequency

MCS: Bit 0 of oscillation mode select register (OSMS)

Values in parentheses apply to operation with f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

(8) Registers controlling buzzer output function

The following two registers control the buzzer output function:

- Timer clock select register 2 (TCL2)
- Port mode register 3 (PM3).
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL2	TCL27	TCL26	TCL25	TCL24	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

This section controls the watchdog timer.
Refer to **(6) Registers controlling watchdog timer** or **Chapter 11** of *μPD78064, 78064Y Subseries User's Manual*, **Chapter 9** of *μPD78064BY Subseries User's Manual*, or **Chapter 11** of *μPD780308, 780308Y Subseries User's Manual* for detailed information.

This section controls the watch timer.
Refer to **(5) Registers controlling watch timer** or **Chapter 10** of *μPD78064, 78064Y Subseries User's Manual*, **Chapter 8** of *μPD78064B Subseries User's Manual*, or **Chapter 10** of *μPD780308, 780308Y Subseries User's Manual* for detailed information.

TCL27	TCL26	TCL25	Buzzer output frequency selection		
				MCS = 1	MCS = 0
0	×	×	Buzzer output disable		
1	0	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)
1	0	1	$f_{XX}/2^{10}$	$f_X/2^{10}$ (4.9 kHz)	$f_X/2^{11}$ (2.4 kHz)
1	1	0	$f_{XX}/2^{11}$	$f_X/2^{11}$ (2.4 kHz)	$f_X/2^{12}$ (1.2 kHz)
1	1	1	Setting prohibited		

Caution: When rewriting TCL2 to other data, stop the timer operation beforehand.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
×: Don't care
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz.

(9) Registers controlling A/D converter

The following three registers control the A/D converter:

- A/D converter mode register (ADM)
- A/D converter input select register (ADIS)
- External interrupt mode register 1 (INTM1)
  - Refer to section (15) for the register format.

Format of A/D Converter Mode Register

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After Reset	R/W
ADM	CS	TRG	FR1	FR0	ADM3	ADM2	ADM1	HSC	FF80H	01H	R/W

CS	A/D conversion operation control
0	Operation stop
1	Operation start

TRG	External trigger selection
0	No external trigger (software starts)
1	Conversion started by external trigger (hardware starts)

FR1	FR0	HSC	A/D conversion time selection [Note 1]			
			f_X = 5.0 MHz operation		f_X = 4.19 MHz operation	
			MCS = 1	MCS = 0	MCS = 1	MCS = 0
0	0	1	80/f_X (Setting prohibited [Note 2])	160/f_X (32.0 μs)	80/f_X (19.1 μs)	160/f_X (38.1 μs)
0	1	1	40/f_X (Setting prohibited [Note 2])	80/f_X (Setting prohibited [Note 2])	40/f_X (Setting prohibited [Note 2])	80/f_X (19.1 μs)
1	0	0	50/f_X (Setting prohibited [Note 2])	100/f_X (20.0 μs)	50/f_X (Setting prohibited [Note 2])	100/f_X (23.8 μs)
1	0	0	100/f_X (20.0 μs)	200/f_X (40.0 μs)	100/f_X (23.8 μs)	200/f_X (47.7 μs)
1	1	1	Setting prohibited			

ADM3	ADM2	ADM1	Analog input channel selection
0	0	0	ANI0
0	0	1	ANI1
0	1	0	ANI2
0	1	1	ANI3
1	0	0	ANI4
1	0	1	ANI5
1	1	0	ANI6
1	1	1	ANI7

Notes: 1. Set so that the A/D conversion time is 19.1 μs or more.
2. Setting prohibited because A/D conversion time is less than 19.1 μs.

Cautions: 1. The following sequence is recommended for power consumption reduction of A/D converter when the standby function is used: Clear bit 7 (CS) to 0 first to stop the A/D conversion operation, and then execute the HALT or STOP instruction.

2. When restarting the stopped A/D conversion operation, start the A/D conversion operation after clearing the interrupt request flag (ADIF) to 0.

Remarks: f_X: Main system clock oscillation frequency
MCS: Bit 0 of oscillation mode select register (OSMS)

Format of A/D Converter Input Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADIS	0	0	0	0	ADIS3	ADIS2	ADIS1	ADIS0	FF84H	00H	R/W

ADIS3	ADIS2	ADIS1	ADIS0	Number of analog input channel selection
0	0	0	0	No analog input channel (P10 to P17)
0	0	0	1	1 channel (ANI0, P11 to P17)
0	0	1	0	2 channels (ANI0, ANI1, P12 to P17)
0	0	1	1	3 channels (ANI0 to ANI2, P13 to P17)
0	1	0	0	4 channels (ANI0 to ANI3, P14 to P17)
0	1	0	1	5 channels (ANI0 to ANI4, P15 to P17)
0	1	1	0	6 channels (ANI0 to ANI5, P16, P17)
0	1	1	1	7 channels (ANI0 to ANI6, P17)
1	0	0	0	8 channels (ANI0 to ANI7)
Settings other than above are prohibited				

Cautions: 1. Set the analog input channel in the following order:

a. Set the number of analog input channels with ADIS.

b. Using the A/D converter mode register (ADM), select one channel to undergo A/D conversion from among the channels set for analog input with ADIS.

2. No internal pull-up resistor can be used to the channels set for analog input with ADIS, irrespective of the value of bit 1 (PUO1) of the pull-up resistor option register L (PUOL).

(10) Registers controlling serial interface channel 0 (Non-Y Subseries)

The μPD78064 and 78064B are provided with two channels of serial interface, and the μPD780308 Subseries is provided with three channels.

The differences among channels 0, 2, and 3 are as indicated in the table below.

Differences Among Channels 0, 2, and 3

Serial Transfer Mode		Channel 0	Channel 2	Channel 3 Note
3-wire serial I/O	Clock selection	$f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, $f_{XX}/2^8$, external clock, TO2 output	External clock, baud rate generator output	$f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, $f_{XX}/2^8$, external clock
	Transfer method	switchable MSB/LSB first	switchable MSB/LSB first	switchable MSB/LSB first
	Transfer end flag	Serial transfer end interrupt request flag (CSIIF0)	Serial transfer end interrupt request flag (SRIF)	Serial transfer end interrupt request flag (CSIIF3)
SBI (serial bus interface)		Use possible	None	None
2-wire serial I/O				
UART (asynchronous serial interface)		None	Use possible	

Note: Provided for the μPD780308 Subseries only.

The following four registers control serial interface channel 0:

- Timer clock select register 3 (TCL3)
- Serial operation mode register 0 (CSIM0)
- Serial bus interface control register (SBIC)
- Interrupt timing specification register (SINT)
- Port mode register 2 (PM2)
  - Refer to seciton (1) for the register format.

Format of Timer Clock Select Register 3

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL3	1	0	0	0	TCL33	TCL32	TCL31	TCL30	FF43H	88H	R/W

TCL33	TCL32	TCL31	TCL30	Serial interface channel 0 serial clock selection		
					MCS = 1	MCS = 0
0	1	1	0	$f_{XX}/2$	Setting prohibited	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
Settings other than above are prohibited						

Cautions: 1. Be sure to set bits 4 to 6 to 0, and set bit 7 to 1.

2. To write data other than that already written to TCL3, stop the serial transfer operation once.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)

f_X: Main system clock oscillation frequency

MCS: Bit 0 of oscillation mode select register (OSMS)

Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of Serial Operation Mode Register 0

Symbol	<7>	<6>	<5>	4	3	2	1	0	Address	After Reset	R/W
CSIM0	CSIE0	COI	WUP	CSIM04	CSIM03	CSIM02	CSIM01	CSIM00	FF60H	00H	R/W Note 1

R/W	CSIE0	Serial interface channel 0 operation control Note 3
	0	Operation stopped
	1	Operation enable

R	COI	Slave address comparison result flag Notes 1, 2
	0	Slave address register (SVA) not equal to serial I/O shift register 0 (SIO0) data
	1	Slave address register (SVA) equal to serial I/O shift register 0 (SIO0) data

R/W	WUP	Wake-up function control Note 3
	0	Interrupt request signal generation with each serial transfer in any mode
	1	Interrupt request signal generation when the address received after bus release (when CMDD = RELD = 1) matches the slave address register (SVA) data in SBI mode

R/W

CSIM 04	CSIM 03	CSIM 02	PM25	P25	PM26	P26	PM27	P27	Operation mode	Start bit	SIO/SB0/P25 pin function	SO0/SB1/P26 pin function	$\overline{SCK0}$/P27 pin function
0	×	0	Note 4 1	Note 4 ×	0	0	0	1	3-wire serial I/O mode	MSB	SI0 Note 4 (Input)	SO0 (CMOS output)	$\overline{SCK0}$ (CMOS input/output)
		1								LSB			
1	0	0	Note 5 ×	Note 5 ×	0	0	0	1	SBI mode	MSB	P25 (CMOS input/output)	SB1 (N-ch open-drain input/output)	$\overline{SCK0}$ (CMOS input/output)
		1	0	0	Note 5 ×	Note 5 ×	0	1			SB0 (N-ch open-drain input/output)	P26 (CMOS input/output)	
1	1	0	Note 5 ×	Note 5 ×	0	0	0	1	2-wire serial I/O mode	MSB	P25 (CMOS input/output)	SB1 (N-ch open-drain input/output)	$\overline{SCK0}$ (N-ch open-drain input/output)
		1	0	0	Note 5 ×	Note 5 ×	0	1			SB0 (N-ch open-drain input/output)	P26 (CMOS input/output)	

R/W	CSIM01	CSIM00	Serial interface channel 0 clock selection
	0	×	Input clock to $\overline{SCK0}$ pin from off chip
	1	0	8-bit timer register 2 (TM2) output
	1	1	Clock specified with bits 0 to 3 of timer clock select register 3 (TCL3)

Notes: 1. Bit 6 (COI) is a read-only bit.
2. When CSIE = 0, COI becomes 0.
3. Clear bit 5 (SIC) of the interrupt timing specification register (SINT) to 0 when using the wake-up function (WUP = 1).
4. Can be used as P25 (CMOS input/output) when channel 0 is used only for transmission.
5. Can be used freely as a port function for SBI or 2-wire mode.

Caution: Do not change the operation mode (3-wire serial I/O, 2-wire serial I/O, or SBI) while serial interface channel 0 is enabled. To change the operating mode, stop the serial operation once.

Remarks: ×: Don't care
PM××: Port mode register
P××: Port output latch

Format of Serial Bus Interface Control Register (1/2)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
SBIC	BSYE	ACKD	ACKE	ACKT	CMDD	RELD	CMDT	RELT	FF61H	00H	R/W Note 1

R/W

BSYE Note 2	Synchronizing busy signal output control
0	Disables busy signal, which is output in synchronization with the falling edge of $\overline{SCK0}$ clock just after execution of the instruction to be cleared to 0.
1	Outputs busy signal at the falling edge of $\overline{SCK0}$ clock following the acknowledge signal.

R

ACKD	Acknowledge detection	
Clear Conditions (ACKD = 0)		Set Condition (ACKD = 1)
• Falling edge of the $\overline{SCK0}$ immediately after the busy mode is released while executing the transfer start instruction • When CSIE0 = 0 • When $\overline{RESET}$ input is applied		• When the acknowledge signal ($\overline{ACK}$) is detected at the rising edge of the $\overline{SCK0}$ clock after completion of a transfer

R/W

ACKE	Acknowledge signal automatic output control	
0	Acknowledge signal automatic output disable (output with ACKT enable)	
1	Before completion of transfer	Acknowledge signal is output in synchronization with the falling edge of the 9th $\overline{SCK0}$ clock (automatically output when ACKE = 1).
	After completion of transfer	Acknowledge signal is output in synchronization with the falling edge of $\overline{SCK0}$ just after execution of the instruction to be set to 1 (automatically output when ACKE = 1). However, it is not automatically cleared to 0 after acknowledge signal output.

R/W

ACKT	Acknowledge signal is output in synchronization with the falling edge clock of $\overline{SCK0}$ just after execution of the instruction to be set to 1, and after acknowledge signal output, automatically cleared to 0. Used as ACKE = 0. Also cleared to 0 upon start of a serial interface transfer or when CSIE0 = 0.

R

CMDD	Command detection	
Clear Conditions (CMDD = 0)		Set Condition (CMDD = 1)
• When transfer start instruction is executed • When bus release signal (REL) is detected • When CSIE0 = 0 • When $\overline{RESET}$ input is applied		• When command signal (CMD) is detected

Notes: 1. Bits 2, 3, and 6 (RELD, CMDD, and ACKD) are read-only bits.

2. The Busy mode can be canceled by start of a serial interface transfer. However, the BSYE flag is not cleared to 0.

Remarks: Bits 0, 1, and 4 (RELT, CMDT, and ACKT) are 0 when read after data has been set.

CSIE: Bit 7 of serial operation mode register 0 (CSIM0)

Format of Serial Bus Interface Control Register (2/2)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
SBIC	BSYE	ACKD	ACKE	ACKT	CMDD	RELD	CMDT	RELT	FF61H	00H	R/W Note 1

R

RELD	Bus release detection	
	Clear Conditions (RELD = 0)	Set Condition (RELD = 1)
	• When transfer start instruction is executed • If SIO0 and SVA values do not match in address reception • When CSIE0 = 0 • When RESET input is applied	• When bus release signal (REL) is detected

R/W

CMDT	Used for command signal output. When CMDT = 1, SO latch is cleared to 0. After SO latch clearance, automatically cleared to 0. Also cleared to 0 when CSIE0 = 0.

R/W

RELT	Used for bus release signal output. When RELT = 1, SO latch is set to 1. After SO latch setting, automatically cleared to 0. Also cleared to 0 when CSIE0 = 0.

Format of Interrupt Timing Specification Register

Symbol	7	<6>	<5>	<4>	3	2	1	0	Address	After Reset	R/W
SINT	0	CLD	SIC	SVAM	0	0	0	0	FF63H	00H	R/W Note 1

R	CLD	$\overline{SCK0}$ pin level Note 2
	0	Low level
	1	High level

R/W	SIC	INTCSI0 interrupt cause selection Note 3
	0	CSIIF0 is set upon termination of serial interface channel 0 transfer
	1	CSIIF0 is set upon bus release detection or termination of serial interface channel 0 transfer

R/W	SVAM	SVA bit to be used as slave address
	0	Bits 0 to 7
	1	Bits 1 to 7

Notes: 1. Bit 6 (CLD) is a read-only bit.
2. When CSIE0 = 0, CLD becomes 0.
3. When using the wake-up function in the SBI mode, set SIC to 0.

Caution: Be sure to set bits 0 to 3 to 0.

Remarks: SVA: Slave address register
CSIIF0: Interrupt request flag corresponding to INTCSI0
CSIE0: Bit 7 of serial operation mode register 0 (CSIM0)

(11) Registers controlling serial interface channel 0 (Y Subseries)

The μPD78064Y Subseries is provided with two channels of serial interfaces, and the μPD780308Y Subseries is provided with three channels.

The differences among channels 0, 1, and 2 are as indicated in the table below.

Differences Among Channels 0, 2, and 3

Serial Transfer Mode		Channel 0	Channel 2	Channel 3 Note
3-wire serial I/O	Clock selection	$f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, $f_{XX}/2^8$, external clock, TO2 output	External clock, baud rate generator output	$f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, $f_{XX}/2^8$, external clock
	Transfer method	switchable MSB/LSB first	switchable MSB/LSB first	switchable MSB/LSB first
	Transfer end flag	Serial transfer end interrupt request flag (CSIIF0)	Serial transfer end interrupt request flag (SRIF)	Serial transfer end interrupt request flag (CSIIF3)
I^2C bus (inter-IC bus)		Use possible	None	None
2-wire serial I/O				
UART (asynchronous serial interface)		None	Use possible	

Note: Provided for the μPD780308Y Subseries only.

The following four registers control serial interface channel 0:

- Timer clock select register 3 (TCL3)
- Serial operation mode register 0 (CSIM0)
- Serial bus interface control register (SBIC)
- Interrupt timing specification register (SINT)
- Port mode register 2 (PM2)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 3

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL3	1	0	0	0	TCL33	TCL32	TCL31	TCL30	FF43H	88H	R/W

TCL33	TCL32	TCL31	TCL30	Serial interface channel 0 serial clock selection			
				Serial clock I^2C bus mode		Serial clock in 2-wire or 3-wire serial I/O mode	
				MCS = 1	MCS = 0	MCS = 1	MCS = 0
0	1	1	0	Setting prohibited	$f_X/2^6$ (78.1 kHz)	Setting prohibited	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.77 kHz)	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_X/2^9$ (9.77 kHz)	$f_X/2^{10}$ (4.88 kHz)	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_X/2^{10}$ (4.88 kHz)	$f_X/2^{11}$ (2.44 kHz)	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_X/2^{11}$ (2.44 kHz)	$f_X/2^{12}$ (1.22 kHz)	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_X/2^{12}$ (1.22 kHz)	$f_X/2^{13}$ (0.61 kHz)	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
Settings other than above are prohibited							

Cautions: 1. Be sure to set bits 4 to 6 to 0, and set bit 7 to 1.

2. To write data other than that already written to TCL3, stop the serial transfer operation once.

Remarks: f_X: Main system clock oscillation frequency

MCS: Bit 0 of oscillation mode select register (OSMS)

Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of Serial Operation Mode Register 0

Symbol	<7>	<6>	<5>	4	3	2	1	0	Address	After Reset	R/W
CSIM0	CSIE0	COI	WUP	CSIM04	CSIM03	CSIM02	CSIM01	CSIM00	FF60H	00H	R/W Note 1

R/W	CSIE0	Serial interface channel 0 operation control
	0	Operation stopped
	1	Operation enable

R	COI	Slave address comparison result flag Note 2
	0	Slave address register (SVA) not equal to serial I/O shift register 0 (SIO0) data
	1	Slave address register (SVA) equal to serial I/O shift register 0 (SIO0) data

R/W	WUP	Wake-up function control Note 3
	0	Interrupt request signal generation with each serial transfer in any mode
	1	Interrupt request signal generation when the address received after detecting the start condition (when CMDD = 1) matches the slave address register (SVA) data in I^2C bus mode

R/W	CSIM 04	CSIM 03	CSIM 02	PM25	P25	PM26	P26	PM27	P27	Operation mode	Start bit	SI0/SB0/SDA0/ P25 pin function	SO0/SB1/SDA1/ P26 pin function	$\overline{SCK0}$/SCL/P27 pin function
	0	×	0	Note 4 1	Note 4 ×	0	0	0	1	3-wire serial I/O mode	MSB	SI0 Note 3 (Input)	SO0 (CMOS output)	$\overline{SCK0}$ (CMOS input/output)
			1								LSB			
	1	1	0	Note 5 ×	Note 5 ×	0	0	0	1	2-wire serial I/O mode or I^2C bus mode	MSB	P25 (CMOS input/output)	SB1/SDA1 (N-ch open-drain input/output)	$\overline{SCK0}$/SCL (N-ch open-drain input/output)
			1	0	0	Note 5 ×	Note 5 ×	0	1			SB0/SDA0 (N-ch open-drain input/output)	P26 (CMOS input/output)	

R/W	CSIM01	CSIM00	Serial interface channel 0 clock selection
	0	×	Input clock to $\overline{SCK0}$/SCL pin from off chip
	1	0	8-bit timer register 2 (TM2) output Note 6
	1	1	Clock specified with bits 0 to 3 of timer clock select register 3 (TCL3)

Notes: 1. Bit 6 (COI) is a read-only bit.
2. When CSIE0 = 0, COI becomes 0.
3. To use the wake-up function (WUP = 1), set bit 5 (SIC) of the interrupt timing specification register (SINT) to 1. Do not execute an instruction that writes to serial I/O shift register 0 (SIO0) while WUP = 1.
4. Can be used as P25 (CMOS input/output) when channel 0 is used only for transmission.
5. Can be used freely as port function for SBI or 2-wire mode.
6. In I^2C bus mode, the clock frequency becomes 1/16 of that output from TO2.

Caution: Do not change the operation mode (3-wire serial I/O, 2-wire serial I/O, or I^2C bus) while serial interface channel 0 is enabled. To change the operating mode, stop the serial operation once.

Remarks: ×: Don't care
PM××: Port mode register
P××: Port output latch

Format of Serial Bus Interface Control Register (1/2)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
SBIC	BSYE	ACKD	ACKE	ACKT	CMDD	RELD	CMDT	RELT	FF61H	00H	R/W Note 1

R/W

Note 2 BSYE	Control of N-ch open-drain output for transmission in I²C bus mode Note 3
0	Output enabled (transmission)
1	Output disabled (reception)

R

ACKD	Acknowledge detection	
Clear Conditions (ACKD = 0)		Set Condition (ACKD = 1)
• While executing the transfer start instruction • When CSIE0 = 0 • When RESET input is applied		• When the acknowledge signal ($\overline{ACK}$) is detected at the rising edge of the SCL clock after completion of a transfer

R/W

ACKE	Acknowledge signal automatic output control Note 4
0	Disables acknowledge signal automatic output (however, output with ACKT is enabled). Used for reception when an 8-clock wait mode is selected or for transmission Note 5.
1	Enables acknowledge signal automatic output. Outputs acknowledge signal in synchronization with the falling edge of the 9th SCL clock cycle (automatically output when ACKE = 1). However, not automatically cleared to 0 after acknowledge signal output. Used in reception with the 9-clock wait mode selected.

R/W

ACKT	Used to generate the $\overline{ACK}$ signal by software when an 8-clock wait mode is selected. Keeps SDA0 (SDA1) low from set instruction (ACKT = 1) execution to the next falling edge of SCL. Also cleared to 0 upon start of a serial interface transfer or when CSIE0 = 0.

R

CMDD	Start condition detection	
Clear Conditions (CMDD = 0)		Set Condition (CMDD = 1)
• When transfer start instruction is executed • When stop condition signal is detected • When CSIE0 = 0 • When RESET input is applied		• When start condition signal is detected

Notes: 1. Bits 2, 3, and 6 (RELD, CMDD, and ACKD) are read-only bits.
2. The Busy mode can be canceled by start of a serial interface transfer or reception of an address signal. However, the BSYE flag is not cleared to 0.
3. When using the wake-up function, be sure to set BSYE to 1.
4. Setting should be performed before a transfer.
5. If an 8-clock wait mode is selected, the acknowledge signal at reception time must be output using ACKT.

Remarks: Bits 0, 1, and 4 (RELT, CMDT, and ACKT) are 0 when read after data has been set.
CSIE: Bit 7 of serial operation mode register 0 (CSIM0)

Format of Serial Bus Interface Control Register (2/2)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
SBIC	BSYE	ACKD	ACKE	ACKT	CMDD	RELD	CMDT	RELT	FF61H	00H	R/W Note 1

R

RELD	Stop condition detection	
	Clear Conditions (RELD = 0)	Set Condition (RELD = 1)
	• When transfer start instruction is executed • If SIO0 and SVA values do not match in address reception • When CSIE0 = 0 • When $\overline{\text{RESET}}$ input is applied	• When stop condition signal is detected

R/W

CMDT	Used for start condition signal output. When CMDT = 1, SO latch is cleared to 0. After SO latch clearance, automatically cleared to 0. Also cleared to 0 when CSIE0 = 0.

R/W

RELT	Used for stop condition signal output. When RELT = 1, SO latch is set to 1. After SO latch setting, automatically cleared to 0. Also cleared to 0 when CSIE0 = 0.

Remark: CSIE0: Bit 7 of serial operation mode register 0 (CSIM0)

Format of Interrupt Timing Specification Register

Symbol	7	<6>	<5>	<4>	<3>	<2>	1	0	Address	After Reset	R/W
SINT	0	CLD	SIC	SVAM	CLC	WREL	WAT1	WAT0	FF63H	00H	R/W Note 1

R

CLD	$\overline{SCK0}$/SCL pin level Note 2
0	Low level
1	High level

R/W

SIC	INTCSI0 interrupt cause selection Note 3
0	CSIIF0 is set to 1 upon termination of serial interface channel 0 transfer
1	CSIIF0 is set to 1 upon stop condition detection or termination of serial interface channel 0 transfer

R/W

SVAM	SVA bit to be used as slave address
0	Bits 0 to 7
1	Bits 1 to 7

R/W

CLC	Clock level control Note 4
0	Used in I^2C bus mode. Make output level of SCL pin low unless a serial transfer is being performed.
1	Used in I^2C bus mode. Make SCL pin enter a high-impedance state unless a serial transfer is being performed (except for clock line, which is kept high). Used to enable a master device to generate start condition and stop condition signals.

R/W

WREL	Wait state cancellation control
0	Wait state has been canceled.
1	Cancels wait state. Automatically cleared to 0 when the state is canceled. (Used to cancel wait state by means of WAT0 and WAT1.)

R/W

WAT1	WAT0	Wait and interrupt control
0	0	Generates interrupt service request at rising edge of 8th $\overline{SCK0}$ clock cycle (keeping clock output in high impedance)
0	1	Setting prohibited
1	0	Used in I^2C bus mode (8-clock wait) Generates an interrupt service request at rising edge of 8th $\overline{SCK0}$ clock cycle. (In the case of a master device, makes SCL output low to enter wait state after 8 clock pulses are output. In the case of a slave device, makes SCL outputlow to request wait state after 8 clock pulses are input.)
1	1	Used in I^2C bus mode (9-clock wait) Generates interrupt service request at rising edge of 9th $\overline{SCK0}$ clock cycle. (In the case of a master device, makes SCL output low to enter wait state after 9 clock pulses are output. In the case of a slave device, makes SCL outputlow to request wait state after 9 clock pulses are input.)

Notes: 1. Bit 6 (CLD) is a read-only bit.
2. When CSIE0 = 0, CLD becomes 0.
3. When using the wake-up function in the I^2C mode, set SIC to 1.
4. When not using the I^2C mode, clear CLC to 0.

Remarks: SVA: Slave address register
CSIIF0: Interrupt request flag corresponding to INTCSI0
CSIE0: Bit 7 of serial operation mode register 0 (CSIM0)

(12) Registers controlling serial interface channel 2

The following five registers control serial interface channel 2:

- Serial operation mode register 2 (CSIM2)
- Asynchronous serial interface mode register (ASIM)
- Asynchronous serial interface status register (ASIS)
- Baud rate generator control register (BRGC)
- Serial interface pin select register (SIPS) Note
- Port mode register 7 (PM7)
  - Refer to section (1) for the register format.

Note: This register is provided only for μPD780308/308Y Subseries products.

Format of Serial Operation Mode Register 2

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
CSIM2	CSIE2	0	0	0	0	CSIM 22	CSCK	0	FF72H	00H	R/W

CSIE2	Operation control in 3-wire serial I/O mode
0	Operation stopped
1	Operation enabled

CSIM22	First bit specification
0	MSB
1	LSB

CSCK	Clock selection in 3-wire serial I/O mode
0	Input clock from off-chip to $\overline{SCK2}$ pin
1	Dedicated baud rate generator output

Cautions: 1. Ensure that bits 0 and 3 to 6 are set to 0.

2. When UART mode is selected, CSIM2 should be set to 00H.

Format of Asynchronous Serial Interface Mode Register

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After Reset	R/W
ASIM	TXE	RXE	PS1	PS0	CL	SL	ISRM	SCK	FF70H	00H	R/W

TXE	Transmit operation control
0	Transmit operation stopped
1	Transmit operation enabled

RXE	Receive operation control
0	Receive operation stopped
1	Receive operation enabled

PS1	PS0	Parity bit specification
0	0	No parity
0	1	0 parity always added in transmission No parity test in reception (parity error not generated)
1	0	Odd parity
1	1	Even parity

CL	Character length specification
0	7 bits
1	8 bits

SL	Transmit data stop bit length specification
0	1 bit
1	2 bits

ISRM	Control of reception completion interrupt request in case of error generation
0	Reception completion interrupt request generated in case of error generation
1	Reception completion interrupt request not generated in case of error generation

SCK	Clock selection in asynchronous serial interface mode
0	Input clock from off chip to ASCK pin
1	Dedicated baud rate generator output Note

Note: When SCK is set to 1 and the baud rate generator output is selected, the ASCK pin can be used as an input/output port.

Cautions: 1. When the 3-wire serial I/O mode is selected, 00H should be set in ASIM.

2. The serial transmit/receive operation must be stopped before changing the operating mode.

Format of Asynchronous Serial Interface Status Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ASIS	0	0	0	0	0	PE	FE	OVE	FF71H	00H	R

PE	Parity error flag
0	Parity error not generated
1	Parity error generated (when transmit data parity does not match)

FE	Framing error flag
0	Framing error not generated
1	Framing error generated Note 1 (when stop bit is not detected)

OVE	Overrun error flag
0	Overrun error not generated
1	Overrun error generated Note 2 (when next receive operation is completed before data from receive buffer register is read)

Notes: 1. Even if the stop bit length has been set as 2 bits by bit 2 (SL) of the asynchronous serial interface mode register (ASIM), only single stop bit detection is performed during reception.

2. The receive buffer register (RXB) must be read when an overrun error is generated. Overrun errors will continue to be generated until RXB is read.

Format of Baud Rate Generator Control Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
BRGC	TPS3	TPS2	TPS1	TPS0	MDL3	MDL2	MDL1	MDL0	FF73H	00H	R/W

TPS3	TPS2	TPS1	TPS0	Selects source clock of 5-bit counter			n
					MCS = 1	MCS = 0	
0	0	0	0	$f_{XX}/2^{10}$	$f_X/2^{10}$ (4.9 kHz)	$f_X/2^{11}$ (2.4 kHz)	11
0	1	0	1	f_{XX}	f_X (5.0 MHz)	$f_X/2$ (2.5 MHz)	1
0	1	1	0	$f_{XX}/2$	$f_X/2$ (2.5 MHz)	$f_X/2^2$ (1.25 MHz)	2
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)	3
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)	4
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)	5
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)	6
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)	7
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)	8
1	1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)	9
1	1	1	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)	10
Settings other than above are prohibited							

MDL3	MDL2	MDL1	MDL0	Baud rate generator input clock selection	k
0	0	0	0	$f_{SCK}/16$	0
0	0	0	1	$f_{SCK}/17$	1
0	0	1	0	$f_{SCK}/18$	2
0	0	1	1	$f_{SCK}/19$	3
0	1	0	0	$f_{SCK}/20$	4
0	1	0	1	$f_{SCK}/21$	5
0	1	1	0	$f_{SCK}/22$	6
0	1	1	1	$f_{SCK}/23$	7
1	0	0	0	$f_{SCK}/24$	8
1	0	0	1	$f_{SCK}/25$	9
1	0	1	0	$f_{SCK}/26$	10
1	0	1	1	$f_{SCK}/27$	11
1	1	0	0	$f_{SCK}/28$	12
1	1	0	1	$f_{SCK}/29$	13
1	1	1	0	$f_{SCK}/30$	14
1	1	1	1	f_{SCK} Note	

Note: Can only be used in 3-wire serial I/O mode.

Caution: When a write is performed to BRGC during a communication operation, baud rate generator output is disrupted and communication cannot be performed normally. Therefore, BRGC must not be written to during a communication operation.

Remarks: f_X: Main system clock oscillation frequency
f_{XX}: Main system clock frequency (fx or fx/2)
MCS: Bit 0 of oscillation mode selection register (OSMS)
n: Value set in TPS0 to TPS3 ($1 \leq n \leq 11$)
f_{SCK}: 5-bit counter source clock
k: Value set in MDL0 to MDL3 ($0 \leq k \leq 14$)
Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of Serial Interface Pin Select Register (For μPD780308/308Y Subseries Only)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
SIPS	0	0	SIPS21	SIPS20	0	0	0	0	FF75H	00H	R/W

SIPS21	SIPS20	Selects input/output pin of asynchronous serial interface
0	0	Input pin: RxD/SI2/P70 Output pin: TxD/SO2/P71
0	1	Input pin: RxD/P114 Output pin: TxD/SO2/P71
1	0	Input pin: RxD/SI2/P70 Output pin: TxD/P113
1	1	Input pin: RxD/P114 Output pin: TxD/P113

Cautions: 1. Select input/output pins after stopping serial transmission/reception.
2. Port 11 has a falling edge detection function. Do not specify the pin of this port used in a mode other than Port mode to input the falling edge. To set input falling edge, refer to "Format of Key Return Mode Register" in (16) Registers controlling port function.
3. This register is provided only for μPD780308/308Y Subseries products.

(13) Registers controlling serial interface channel 3 (μPD780308/308Y Subseries only)

Serial interface channel 3 is available only in the μPD780308/308Y Subseries.
The following three registers control serial interface channel 3:

- Timer clock select register 4 (TCL4)
- Serial operation mode register 3 (CSIM3)
- Port mode register 11 (PM11)
  - Refer to section (1) for the format of this register.

Format of Timer Clock Select Register 4

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL4	TCL47	TCL46	TCL45	TCL44	1	0	0	0	FF44H	88H	R/W

TCL47	TCL46	TCL45	TCL44	Selects serial clock of serial interface channel 3	
				MCS = 1	MCS = 0
0	1	1	0	Setting prohibited	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
Settings other than above are prohibited					

Cautions: 1. Be sure to set bits 0 to 2 to 0, and set bit 3 to 1.

2. To write data other than that already written to TCL4, stop the serial transfer operation.

Remarks: f_X: Main system clock oscillation frequency
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of Serial Operation Mode Register 3

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
CSIM3	CSIE3	DIR3	Note 1 0	0	0	0	CSIM31	CSIM30	FF6CH	00H	R/W

CSIE3	CSIM31	PM110	P110	PM111	P111	PM112	P112	Controls operation of serial interface channel 3	Controls operation of serial clock counter	SI3/P110 pin functions	SO3/P111 pin functions	$\overline{\text{SCK3}}$/P112 pin functions
0	×	Note 2 ×	Note 2 ×	Note 2 ×	Note 2 ×	Note 2 ×	Note 2 ×	Stops operation	Clear	P110 (CMOS I/O)	P111 (CMOS I/O)	P112 (CMOS I/O)
1	0	Note 2 1	Note 2 ×	0	0	1	×	Enables operation	Count operation	SI3 Note 3 (Input)	SO3 (CMOS output)	$\overline{\text{SCK3}}$ (Input)
	1					0	1					$\overline{\text{SCK3}}$ (CMOS output)

DIR3	First bit	SI3/P110 pin functions	SO3/P111 pin functions
0	MSB	SI3 Note 3 (Input)	SO3 (CMOS output)
1	LSB		

CSIM31	CSIM30	Selects clock of serial interface channel 3
0	×	Input clock to $\overline{\text{SCK3}}$ pin from off chip
1	1	Clock specified by bits 0 through 3 of timer clock select register 4 (TCL4)
Settings other than above are prohibited		

Notes: 1. Be sure to set bit 5 to 0.
2. Can be used freely as port pins.
3. Can be used as P110 (CMOS input/output) when only transmitting data.

Caution: Port 11 has a function to detect the falling edge. To use the SI3/P110, SO3/P111, and $\overline{\text{SCK3}}$/P112 pins as the input/output pins of serial interface channel 3, the falling edge detection function must be disabled by using the key return mode register (KRM). For details, refer to "Format of Key Return Mode Register" in (16) Registers controlling port function.

Remarks: ×: Don't care
PM××: Port mode register
P××: Port output latch

(14) Registers controlling LCD controller/driver

The following two registers control the LCD controller/driver:

- LCD display mode register (LCDM)
- LCD display control register (LCDC)

Format of LCD Display Mode Register

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
LCDM	LCDON	LCDM6	LCDM5	LCDM4	LCDM3 Note 2	LCDM2	LCDM1	LCDM0	FFB0H	00H	R/W

LDON	Enables/disables LCD display
0	Display OFF (all segment outputs are unselected signals)
1	Display ON

LCDM6	LCDM5	LCDM4	Selects LCD clock Note 1		
			f_{XX} = 5.0 MHz	f_{XX} = 4.19 MHz	f_{XT} = 32.768 kHz
0	0	0	$f_W/2^9$ (76 Hz)	$f_W/2^9$ (64 Hz)	$f_W/2^9$ (64 Hz)
0	0	1	$f_W/2^8$ (153 Hz)	$f_W/2^8$ (128 Hz)	$f_W/2^8$ (128 Hz)
0	1	0	$f_W/2^7$ (305 Hz)	$f_W/2^7$ (256 Hz)	$f_W/2^7$ (256 Hz)
0	1	1	$f_W/2^6$ (610 Hz)	$f_W/2^6$ (512 Hz)	$f_W/2^6$ (512 Hz)
Settings other than above are prohibited					

LCDM3 Note 2	Operating mode of LCD controller/driver	Supply voltage of LCD controller/driver		
		Static display mode	1/3 Bias mode	1/2 Bias mode
0	Normal operation	2.0 to 5.5 V	2.5 to 5.5 V	2.7 to 5.5 V
1	Low-voltage operation	2.0 to 3.4 V		

LCDM2	LCDM1	LCDM0	Selects display mode of LCD controller/driver	
			Time division	Bias mode
0	0	0	4 (Quadruplex)	1/3
0	0	1	3 (Triplex)	1/3
0	1	0	2 (Duplex)	1/2
0	1	1	3 (Triplex)	1/2
1	0	0	Static display mode	
Settings other than above are prohibited				

Frame Frequencies (Hz)

LCDCL / Duty	$f_W/2^9$ (Hz)	$f_W/2^8$ (Hz)	$f_W/2^7$ (Hz)	$f_W/2^6$ (Hz)
Static	64	128	256	512
1/2 (Duplex)	32	64	128	256
1/3 (Triplex)	21	43	85	171
1/4 (Quadruplex)	16	32	64	128

Note: LCDM3 is a 0 for the μPD78064 subseries. It is programmable for only the μPD780308 subseries.

Notes: 1. The LCD clock is supplied from the watch timer. When LCD display is performed, 1 should be set in bit 1 (TMC21) of the clock timer mode control register (TMC2). If TMC21 is reset to 0 during LCD display, the LCD clock supply will be stopped and the display will be off.

2. Bit 3 of LCDM (LCDM3) is a 0 for the 7806x, but is present in the 780308. To reduce the power consumption, clear LCDM3 to 0 when LCD display is not performed. Before manipulating LCDM3, be sure to turn off the LCD display. If TMC21 is cleared to 0 during LCD display, the LCD clock supply will be stopped and the display will be off.

Remarks: f_W: Clock timer clock frequency ($f_{XX}/2^7$ or f_XT)
f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
f_{XT}: Subsystem clock oscillation frequency

Format of LCD Display Control Register

Symbol	<7>	6	5	4	3	2	<1>	<0>	Address	After Reset	R/W
LCDC	LCDC7	LCDC6	LCDC5	LCDC4	0	0	LEPS	LIPS	FFB2H	00H	R/W

LCDC7	LCDC6	LCDC5	LCDC4	P80/S39 to P97/S24 pin functions	
				Port pins	Segment pins
0	0	0	0	P80 to P97	None
0	0	0	1	P80 to P95	S24, S25
0	0	1	0	P80 to P93	S24 to S27
0	0	1	1	P80 to P91	S24 to S29
0	1	0	0	P80 to P87	S24 to S31
0	1	0	1	P80 to P85	S24 to S33
0	1	1	0	P80 to P83	S24 to S35
0	1	1	1	P80 to P81	S24 to S37
1	0	0	0	None	S24 to S39
Settings other than above are prohibited					

LEPS	LIPS	LCD driving power supply selection
0	0	Does not supply power to LCD
0	1	Supplies power to LCD from V_{DD} pin
1	0	Supplies power to LCD from BIAS pin (shorts BIAS and V_{LCD} pins internally)
1	1	Setting prohibited

Cautions: 1. Pins that perform segment output cannot be used as output port pins even if 0 is set in the port register.

2. If a pin that performs segment output is read as a port, its value will be 0.

3. Pins set as segment outputs by LCDC cannot have an internal pull-up resistor connected, regardless of the value of bits 0 and 1 (PUO8 and PUO9) of pull-up resistor option register H.

(15) Registers controlling interrupt function

A total of 21 interrupt sources are provided for the (μPD78064/64Y, 78064B, and 780308/308Y Subseries), including non-maskable, maskable, and software interrupts.

Table 6-24. Interrupt Source List

Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address
		Name	Trigger		
Non-maskable	—	RESET	Low voltage level	External	0000H
		INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)		
	1	INTP0	Pin input edge detection	External	0006H
	2	INTP1			0008H
	3	INTP2			000AH
	4	INTP3			000CH
	5	INTP4			000EH
	6	INTP5			0010H
	7	INTCSI0	End of serial interface channel 0 transfer	Internal	0014H
	8	INTSER	Serial interface channel 2 UART reception error generation		0018H
	9	INTSR	End of serial interface channel 2 UART reception		001AH
		INTCSI2	End of serial interface channel 2 3-wire transfer		
	10	INTST	End of serial interface channel 2 UART transmission		001CH
	11	INTTM3	Reference time interval signal from watch timer		001EH
	12	INTTM00	Generation of 16-bit timer register and capture/ compare register 00 (CR00) match signal		0020H
	13	INTTM01	Generation of 16-bit timer register and capture/ compare register 01 (CR01) match signal		0022H
	14	INTTM1	Generation of 8-bit timer/event counter 1 match signal		0024H
	15	INTTM2	Generation of 8-bit timer/event counter 2 match signal		0026H
	16	INTAD	End of A/D converter conversion		0028H
	17 Note 2	INTCSI3	End of serial interface channel 3 transfer		002AH
Software	—	BRK	BRK instruction execution	—	003EH

Notes: 1. Default priorities are intended for two or more simultaneously generated maskable interrupt requests. 0 is the highest priority and 17 is the lowest priority.

2. Interrupt INTCS13 is present in the μPD780308 subseries only.

The following table gives a listing of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 6-25. Interrupt Sources and Flags

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
		Register		Register		Register
INTWDT	TMIF4	IF0L	TMMK4	MK0L	TMPR4	PR0L
INTP0	PIF0		PMK0		PPR0	
INTP1	PIF1		PMK1		PPR1	
INTP2	PIF2		PMK2		PPR2	
INTP3	PIF3		PMK3		PPR3	
INTP4	PIF4		PMK4		PPR4	
INTP5	PIF5		PMK5		PPR5	
INTCSI0	CSIIF0	IF0H	CSIMK0	MK0H	CSIPR0	PR0H
INTSER	SERIF		SERMK		SERPR	
INTSR/INTCSI2	SRIF		SRMK		SRPR	
INTST	STIF		STMK		STPR	
INTTM3	TMIF3		TMMK3		TMPR3	
INTTM00	TMIF00		TMMK00		TMPR00	
INTTM01	TMIF01		TMMK01		TMPR01	
INTTM1	TMIF1	IF1L	TMMK1	MK1L	TMPR1	PR1L
INTTM2	TMIF2		TMMK2		TMPR2	
INTAD	ADIF		ADMK		ADPR	
INTCSI3 Note	CSIIF3 Note		CSIMK3 Note		CSIPR3 Note	

Note: Provided for the μPD780308/308Y Subseries only.

The following six types of registers control the interrupt functions:

- Interrupt request flag registers (IF0L, IF0H, IF1L)
- Interrupt mask flag registers (MK0L, MK0H, MK1L)
- Priority specification flag registers (PR0L, PR0H, PR1L)
- External interrupt mode registers (INTM0, INTM1)
- Sampling clock select register (SCS)
- Program status word (PSW)

Format of Interrupt Request Flag Registers

Symbol	7	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
IF0L	0	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	TMIF4	FFE0H	00H	R/W
	<7>	<6>	<5>	<4>	<3>	<2>	1	<0>			
IF0H	TMIF01	TMIF00	TMIF3	STIF	SRIF	SERIF	0	CSIIF0	FFE1H	00H	R/W
	<7>	6	5	4	<3>	<2>	<1>	<0>			
IF1L	WTIF Note 1	0	0	0	CSIIF3 Notes 2, 3	ADIF	TMIF2	TMIF1	FFE2H	00H	R/W

××IF	Interrupt request flag
0	No interrupt request signal
1	Interrupt request signal is generated; Interrupt request state

Notes: 1. WTIF is a test input flag. A vectored interrupt request is not generated.
2. The CSIIF3 flag is present in the μPD780308 subseries only.
3. Bit 3 of IF1L is a 0 in the μPD78064 subseries.

Cautions: 1. The TMIF4 flag is R/W enabled only when a watchdog timer is used as an interval timer. If a watchdog timer is used in watchdog timer mode 1, set the TMIF4 flag to 0.
2. Always set IF1L bits 4 to 6, IF0L bit 7, and IF0H bit 1 to

Format of Interrupt Mask Flag Registers

Symbol	7	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
MK0L	1	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	TMMK4	FFE4H	FFH	R/W
	<7>	<6>	<5>	<4>	<3>	<2>	1	<0>			
MK0H	TMMK01	TMMK00	TMMK3	STMK	SRMK	SERMK	1	CSIMK0	FFE5H	FFH	R/W
	<7>	6	5	4	<3>	<2>	<1>	<0>			
MK1L	WTMK Note 1	1	1	1	CSIMK3 Note 2	ADMK	TMMK2	TMMK1	FFE6H	FFH	R/W

××MK	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Notes: 1. WTMK controls the Standby mode release enable/disable. It does not control the interrupt function.
2. The CSIMK3 flag (MK1L bit 3) is present in the μPD780308 subseries only. It must be set to a 1 in the μPD78064 subseries.

Cautions: 1. If the TMMK4 flag is read when a watchdog timer is used in watchdog timer mode 1, the MK0 value becomes undefined.
2. Because port 0 has an alternate function as the external interrupt input, when the output level is changed by specifying the output mode of the port function, an interrupt request flag is set. Therefore, 1 should be set in the interrupt mask flag before using the output mode.
3. Always set MK1L bits 4 to 6, MK0L bit 7, and MK0H bit 1 to 1.

Format of Priority Specification Flag Registers

Symbol	7	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
PR0L	1	PPR5	PPR4	PPR3	PPR2	PPR1	PPR0	TMPR4	FFE8H	FFH	R/W
	<7>	<6>	<5>	<4>	<3>	<2>	1	<0>			
PR0H	TMPR01	TMPR00	TMPR3	STPR	SRPR	SERPR	1	CSIPR0	FFE9H	FFH	R/W
	7	6	5	4	<3>	<2>	<1>	<0>			
PR1L	1	1	1	1	CSIPR3 Note 1	ADPR	TMPR2	TMPR1	FFEAH	FFH	R/W

××PR	Priority level selection
0	High priority level
1	Low priority level

Note: The CSIPR3 flag (PR1L bit 3) is present only in the μPD780308 subseries. This bit must be set to a 1 in the μPD78064 subseries.

Cautions: 1. If a watchdog timer is used in watchdog timer mode 1, set the TMPR4 flag to 1.

2. Always set PR1L bits 4 to 7, PR0L bit 7, and PR0H bit 1 to 1.

Format of External Interrupt Mode Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
INTM0	ES31	ES30	ES21	ES20	ES11	ES10	0	0	FFECH	00H	R/W

ES31	ES30	INTP2 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES21	ES20	INTP1 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES11	ES10	INTP0 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

Caution: Before setting the valid edges of the INTP0/P00 pins, stop the timer operation by clearing bits 1 to 3 (TMC01 to TMC03) of the 16-bit timer mode control register (TMC0) to 0.

Format of External Interrupt Mode Register 1

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
INTM1	0	0	ES61	ES60	ES51	ES50	ES41	ES40	FFEDH	00H	R/W

ES61	ES60	INTP5 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES51	ES50	INTP4 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES41	ES40	INTP3 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

Format of Sampling Clock Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
SCS	0	0	0	0	0	0	SCS1	SCS0	FF47H	00H	R/W

SCS1	SCS0	INTP0 sampling clock selection		
			MCS = 1	MCS = 0
0	0	$f_{XX}/2^N$		
0	1	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	0	$f_{XX}/2^5$	$f_X/2^5$ (156.3 kHz)	$f_X/2^6$ (78.1 kHz)
1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)

Caution: $f_{XX}/2^N$ is a clock to be supplied to the CPU and $f_{XX}/2^5$, $f_{XX}/2^6$, and $f_{XX}/2^7$ are clocks to be supplied to the peripheral hardware. $f_{XX}/2^N$ stops in the HALT mode.

Remarks: N: Value (N = 0 to 4) at bits 0 to 2 (PCC0 to PCC2) of processor clock control register

f_{XX}: Main system clock frequency (f_X or $f_X/2$)

f_X: Main system clock oscillation frequency

MCS: Bit 0 of oscillation mode selection register

Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of Program Status Word

	7	6	5	4	3	2	1	0	After Reset
PSW	IE	Z	RBS1	AC	RBS0	0	ISP	CY	02H

Used when a normal instruction is executed

ISP	Priority of interrupt currently being received
0	High-priority interrupt servicing (low-priority interrupt disable)
1	Interrupt request not acknowledged or low-priority interrupt servicing (all-maskable interrupts enable)

IE	Interrupt request acknowledge enable/disable
0	Disable
1	Enable

(16) Registers controlling test function

The following three registers control the test function:

- Interrupt request flag register 1L (IF1L)
  - Refer to section (15) for the register format.
- Interrupt mask flag register 1L (MK1L)
  - Refer to section (15) for the register format.
- Key return mode register (KRM)

The names of the test input flag and test mask flag corresponding to the test input signal name are as follows.

Test Input Sources

Test Input		Test Input Flag	Test Mask Flag	Internal/ External
Name	Trigger			
INTWT	Watch timer overflow	WTIF	WTMK	Internal
INTPT11	Falling edge detection at port 11	KRIF	KRMK	External

Format of Key Return Mode Register

Symbol	7	6	5	4	3	2	<1>	<0>	Address	After Reset	R/W
KRM	0	0	0	0	KRM3	KRM2	KRMK	KRIF	FFB8H	02H	R/W

KRM3	KRM2	Selection of port 11 falling edge input
0	0	P117
0	1	P114 to P117
1	0	P112 to P117
1	1	P110 to P117

KRMK	Standby mode control by key return signal
0	Standby mode release enabled
1	Standby mode release disabled

KRIF	Key return signal detection flag
0	Not detected
1	Detected (port 11 falling edge detection)

Caution: When port 11 falling edge detection is used, be sure to clear KRIF to 0 (it is not cleared to 0 automatically).

(17) Register controlling standby function

The standby function is intended to decrease the power consumption of the system. The following two modes are available: HALT and STOP.

When MCU is released from the STOP mode, a wait time is required for the crystal to resume oscillations. The wait time is controlled by the following register:

- Oscillation stabilization time select register (OSTS)

Format of Oscillation Stabilization Time Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0	FFFAH	04H	R/W

OSTS2	OSTS1	OSTS0	Selection of oscillation stabilization time when STOP mode is released		
				MCS = 1	MCS = 0
0	0	0	$2^{12}/f_{XX}$	$2^{12}/f_X$ (819 μs)	$2^{13}/f_X$ (1.64 ms)
0	0	1	$2^{14}/f_{XX}$	$2^{14}/f_X$ (3.28 ms)	$2^{15}/f_X$ (6.55 ms)
0	1	0	$2^{15}/f_{XX}$	$2^{15}/f_X$ (6.55 ms)	$2^{16}/f_X$ (13.1 ms)
0	1	1	$2^{16}/f_{XX}$	$2^{16}/f_X$ (13.1 ms)	$2^{17}/f_X$ (26.2 ms)
1	0	0	$2^{17}/f_{XX}$	$2^{17}/f_X$ (26.2 ms)	$2^{18}/f_X$ (52.4 ms)
Settings other than above are prohibited					

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)

f_X: Main system clock oscillation frequency

MCS: Bit 0 of oscillation mode select register (OSMS)

Values in parentheses apply to operation with f_X = 5.0 MHz.

The operation status in the HALT mode is described below.

HALT Mode Operating Status

Setting of HALT Mode / Item		HALT Execution during Main System Clock Operation		HALT Execution during Subsystem Clock Operation	
		Without Subsystem Clock Note 1	With Subsystem Clock Note 2	When Main System Clock Continues Oscillation	When Main System Clock Stops Oscillation
Clock generator		Both main system and subsystem clocks can be oscillated. Clock supply to the CPU stops.			
CPU		Operation stops			
Port (output latch)		Status before HALT mode setting is held			
16-bit timer/event counter		Operable			Operable when watch timer output with f_{XT} is selected as count clock and f_{XT} is selected as count clock for watch timer
8-bit timer/event counters 1 and 2		Operable			Operable when TI1 or TI2 is selected as count clock
Watch timer		Operable when $f_{XX}/2^7$ is selected as count clock	Operable		Operable when f_{XT} is selected as count clock
Watchdog timer		Operable		Operation stops	
A/D converter		Operable			Operation stops
Serial interface		Operable			Operable with external SCK
LCD controller/driver		Operable when $f_{XX}/2^7$ is selected as count clock	Operable		Operable when f_{XT} is selected as count clock
External interrupt request	INTP0	Operable when a clock ($f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$) for the peripheral hardware is selected as sampling clock			Operation stops
	INTP1 to INTP5	Operable			

Notes: 1. Including when an external clock is not supplied.

2. Including when an external clock is supplied.

The operation in the STOP mode is described below.

STOP Mode Operating Status

Item \ Setting of STOP Mode		With Subsystem Clock	Without Subsystem Clock
Clock generator		Only main system clock stops oscillation	
CPU		Operation stops	
Port (output latch)		Status before STOP mode setting is held	
16-bit timer/event counter		Operable when watch timer output with f_{XT} is selected as count clock and f_{XT} is selected as count clock for watch timer	Operation stops
8-bit timer/event counters 1 and 2		Operable when TI1 and TI2 are selected for the count clock	
Watch timer		Operable when f_{XT} is selected for the count clock	Operation stops
Watchdog timer		Operation stops	
A/D converter			
Serial interface	Other than UART	Operable when externally supplied clock is specified as the serial clock	
	UART	Operation stops	
LCD controller/driver		Operable when f_{XT} is selected for the count clock	Operation stops
External interrupt request	INTP0	Not operable	
	INTP1 to INTP5	Operable	

Cautions: 1. When the STOP mode is set, the X2 pin is internally connected to V_{DD1} via a pull-up resistor to minimize the leakage current at the crystal oscillator. Thus, do not use the STOP mode in a system where an external CMOS clock is used for the main system clock.

2. Because the interrupt request signal is used to release the Standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the Standby mode is immediately released if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction. After the wait set using the oscillation stabilization time select register (OSTS), the operating mode is set.

(18) Reset function

The following two operations generate a reset signal:

- External reset input via the $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer in Watchdog Timer Mode

Table 6-26. Hardware Status After Reset (1/2)

Hardware		Status After Reset
Program counter (PC) Note 1		Contents of reset vector tables (0000H, 0001H) are set
Stack pointer (SP)		Undefined
Program status word (PSW)		02H
RAM	Data memory	Undefined Note 2
	General-purpose register	Undefined Note 2
Port (output latch)	Ports 0 to 3, Ports 7 to 11 (P0 to P3, P7 to P11)	00H
Port mode registers (PM0 to PM3, PM7 to PM11)		FFH
Pull-up resistor option registers (PUOH, PUOL)		00H
Processor clock control register (PCC)		04H
Oscillation mode select register (OSMS)		00H
Internal memory size switching register (IMS)		**Note 3**
Internal expansion RAM size switching register (IXS) Note 4		0AH
Oscillation stabilization time select register (OSTS)		04H
16-bit timer/event counter	Timer register (TM0)	0000H
	Capture/compare registers (CR00, CR01)	Undefined
	Clock select register (TCL0)	00H
	Mode control register (TMC0)	00H
	Capture/compare control register 0 (CRC0)	04H
	Output control register (TOC0)	00H
8-bit timer/event counters 1 and 2	Timer registers (TM1, TM2)	00H
	Compare registers (CR10, CR20)	Undefined
	Clock select register (TCL1)	00H
	Mode control register (TMC1)	00H
	Output control register (TOC1)	00H
Watch timer	Mode control register (TMC2)	00H
	Clock select register (TCL2)	00H
Watchdog timer	Mode register (WDTM)	00H
Serial interface	Clock select registers (TCL3, TCL4 Note 4)	88H
	Shift registers (SIO0, SIO3 Note 4)	Undefined
	Mode registers (CSIM0, CSIM2, CSIM3 Note 4)	00H
	Serial bus interface control register (SBIC)	00H
	Slave address register (SVA)	Undefined
	Asynchronous serial interface mode register (ASIM)	00H
	Asynchronous serial interface status register (ASIS)	00H
	Baud rate generator control register (BRGC)	00H
	Serial interface pin select register (SIPS) Note 4	00H
	Transmit shift register (TXS)	FFH
	Receive buffer register (RXB)	
	Interrupt timing specification register (SINT)	00H

Table 6-26. Hardware Status After Reset (2/2)

Hardware		Status After Reset
A/D converter	Mode register (ADM)	01H
	Conversion result register (ADCR)	Undefined
	Input select register (ADIS)	00H
LCD controller/ driver	Display mode register (LCDM)	00H
	Display control register (LCDC)	00H
Interrupt	Request flag registers (IF0L, IF0H, IF1L)	00H
	Mask flag registers (MK0L, MK0H, MK1L)	FFH
	Priority specification flag registers (PR0L, PR0H, PR1L)	FFH
	External interrupt mode registers (INTM0, INTM1)	00H
	Key return mode register (KRM)	02H
	Sampling clock select register (SCS)	00H

Notes: 1. During reset input or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. The post-reset status is held in the Standby mode.

3. The value after reset differs depending on the product, as follows:

	μPD78062 μPD78062Y	μPD78063 μPD78063Y	μPD78064 μPD78064Y μPD78P064	μPD78P064Y μPD78064B μPD78P064B	μPD780306 μPD780306Y	μPD780308 μPD780308Y μPD78P0308 μPD78P0308Y
IMS	44H	C6H	C8H		CCH	CFH

4. The following registers are provided for μPD780308/308Y Subseries products only: IXS, TCL4, SIO3, CSIM3, and SIPS.

(19) Register controlling internal memory capacity

The μPD78P064/64Y, 78P064B, and 78P0308/308Y allow users to select the internal memory capacity. The following registers are used to control the internal memory capacity:

- Internal memory size switching register (IMS)
- Internal expansion RAM size switching (IXS)

(a) μPD78P064/64Y and 78P064B Subseries

To map the ROM memory and the internal high-speed memory of the μPD78P064/64Y or 78P064B identically to that of a mask ROM version, the value at the time the mask ROM version is reset must be set.

For the mask ROM version, IMS does not need to be set.

Format of Internal Memory Size Switching Register (μPD78P064/64Y and 78P064B)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	C8H	R/W

RAM2	RAM1	RAM0	Internal high-speed RAM capacity selection
0	1	0	512 bytes Note
1	1	1	1024 bytes
Settings other than above are prohibited			

ROM3	ROM2	ROM1	ROM0	Internal ROM capacity selection
0	1	0	0	16K Note
0	1	1	0	24K Note
1	0	0	0	32K
Settings other than above are prohibited				

Note: Setting prohibited for the μPD78064B Subseries.

The following table shows the set value of IMS to map the memory of the μPD78P064/64Y or 78P064B identically to that of a mask ROM version.

Set Value of Internal Memory Size Switching Register (μPD78P064/64Y and 78P064B)

Target Mask ROM Version	Set Value of IMS
μPD78062/62Y	44H
μPD78063/63Y	C6H
μPD78064/64Y, 78064B	C8H

Caution: When using a mask ROM version, do not set a value to IMS other than those shown in the table above.

(b) μPD78P0308/308Y Subseries

To map the ROM memory and the internal high-speed RAM memory of the μPD78P0308 or 78P0308Y identically to that of a mask ROM version, the value at the time the mask ROM version is reset must be set.

For the mask ROM version, IMS does not need to be set.

Format of Internal Memory Size Switching Register (μPD78P0308/308Y)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

RAM2	RAM1	RAM0	Internal high-speed RAM capacity selection
1	1	0	1024 bytes
Settings other than above are prohibited			

ROM3	ROM2	ROM1	ROM0	Internal ROM capacity selection
1	1	0	0	48K
1	1	1	1	60K
Settings other than above are prohibited				

The following table shows the set value of IMS to map the memory of the μPD78P0308/308Y identically to that of a mask ROM version.

Set Value of Internal Memory Size Switching Register (μPD78P0308/308Y)

Target Mask ROM Version	Set Value of IMS
μPD780306F/306Y	CCH
μPD780308/308Y	CFH

Caution: When using a mask ROM version, do not set a value to IMS other than those shown in the table above.

(20) Register controlling internal expansion RAM capacity (μPD780308/308Y Subseries only)

The μPD78P0308/308Y allow users to select the internal expansion RAM capacity.

The following register is used to control the internal expansion RAM capacity. This register is not in the μPD78064 subseries.

- Internal expansion RAM size switching register (IXS)

Format of Internal Expansion RAM Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IXS	0	0	0	0	IXRAM3	IXRAM2	IXRAM1	IXRAM0	FFF4H	0AH	W

IXRAM3	IXRAM2	IXRAM1	IXRAM0	Internal expansion RAM capacity selection
1	0	1	0	1024 bytes
Settings other than above are prohibited				

The following table shows the set value of IXS to map the internal expansion RAM of the μPD78P0308/308Y identically to that of a mask ROM version.

Set Value of Internal Expansion RAM Size Switching Register

Target Mask ROM Version	Set Value of IXS
μPD780306/306Y	0AH
μPD780308/308Y	

Cautions: 1. For the mask ROM version, IXS does not need to be set.

2. When using a mask ROM version, do not set a value to IXS other than those shown in the table above.

6.7 μPD78078, 78075B, and 78070A Subseries

6.7.1 Documentation Reference Information

Device Series Number	User's Manual Number	Date Published
μPD78078, 78Y	U10641EJ4V0UM00	December 1997
μPD78075B, 75BY	U12560EJ1V0UM00	August 1997
μPD78070A, 70AY	U10200EJ2V0UM00	January 1998

Caution: The user should check the current User's Manual with the information in this section to be sure of having the most up-to-date information.

6.7.2 Device Series Differences

Device Series Number	ROM and RAM Differences		External Bus
	ROM Size	RAM Size	Mode
μPD78078, 78078Y	48K/60K	1K	Multiplexed
μPD78075B, 78075BY	32K/40K/60K		or separate
μPD78070A, 78070AY	None		Separate

General Programmer's Note

The NEC C-compiler and the NEC Assembler are capable of recognizing certain symbolic SFR bit names. These special bit names are identified in the user manual in one of the four ways shown below:

1. <7>
2. (7)
3. ⑦
4. [7]

Example:

	<7>	<6>	<5>	<4>	3	2	1	0
PCC	MCC	FRC	CLS	CSS	0	PCC2	PCC1	PCC0

If a bit number has one of the four symbols around it, the NEC software will recognize the associated symbolic bit name. For example to set bit 7, the user can write the code in two ways:

```
1.    SET1    MCC
2.    SET1    PCC.7
```

Alternatively since bit 2 does not have any of the four symbols around it, the user can only set this bit as follows:

```
1.    SET1    PCC.2
```

Note: The attempt to employ a symbolic name of bit-2 (PCC2) will return an error. Thus the use of instruction

```
SET1    PCC2
```

is improper since neither the NEC C-compiler nor the NEC Assembler recognizes this symbolic name and will generate an error.

6.7.3 Memory Address Space

Each model in the μPD78078/78Y, 78075B/75BY, and 78070A/70AY Subseries can access a memory space of 64 Kbytes. Figures 6-35 through 6-39 show memory maps of the respective models.

Figure 6-35. Memory Map (μPD78070A/70AY)

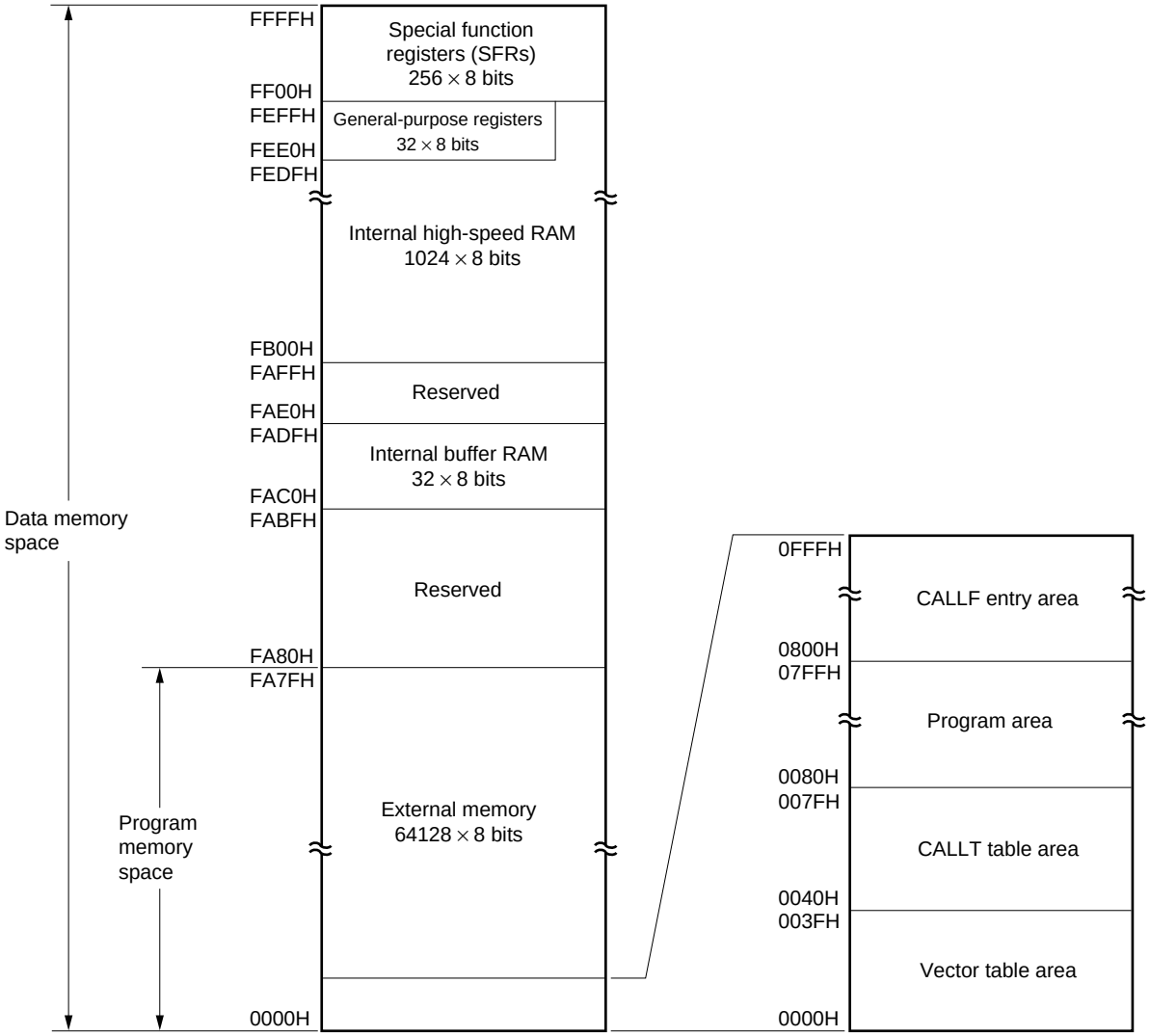


Figure 6-36. Memory Map (μPD78074B/74BY)

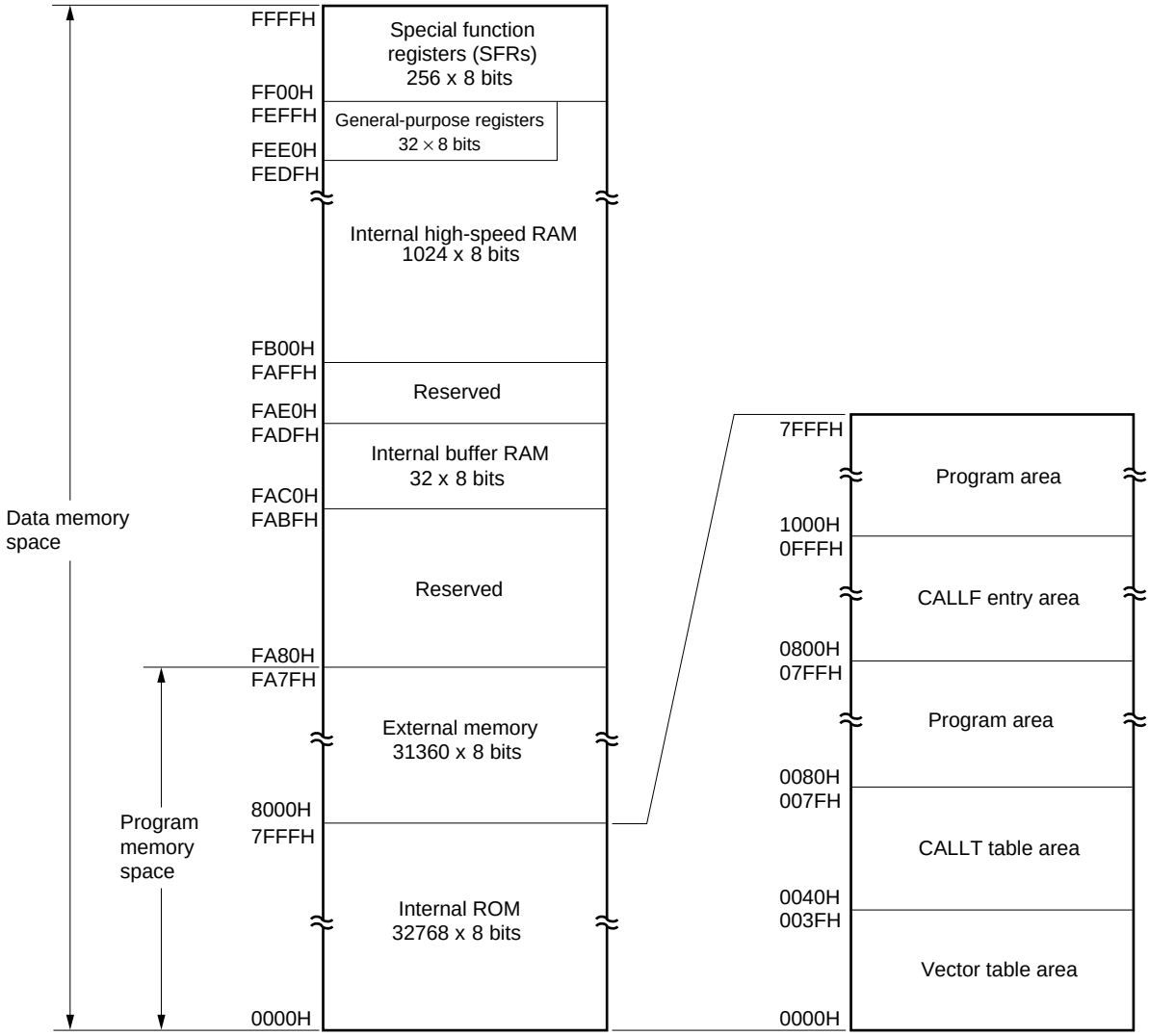


Figure 6-37. Memory Map (μPD78075B/75BY)

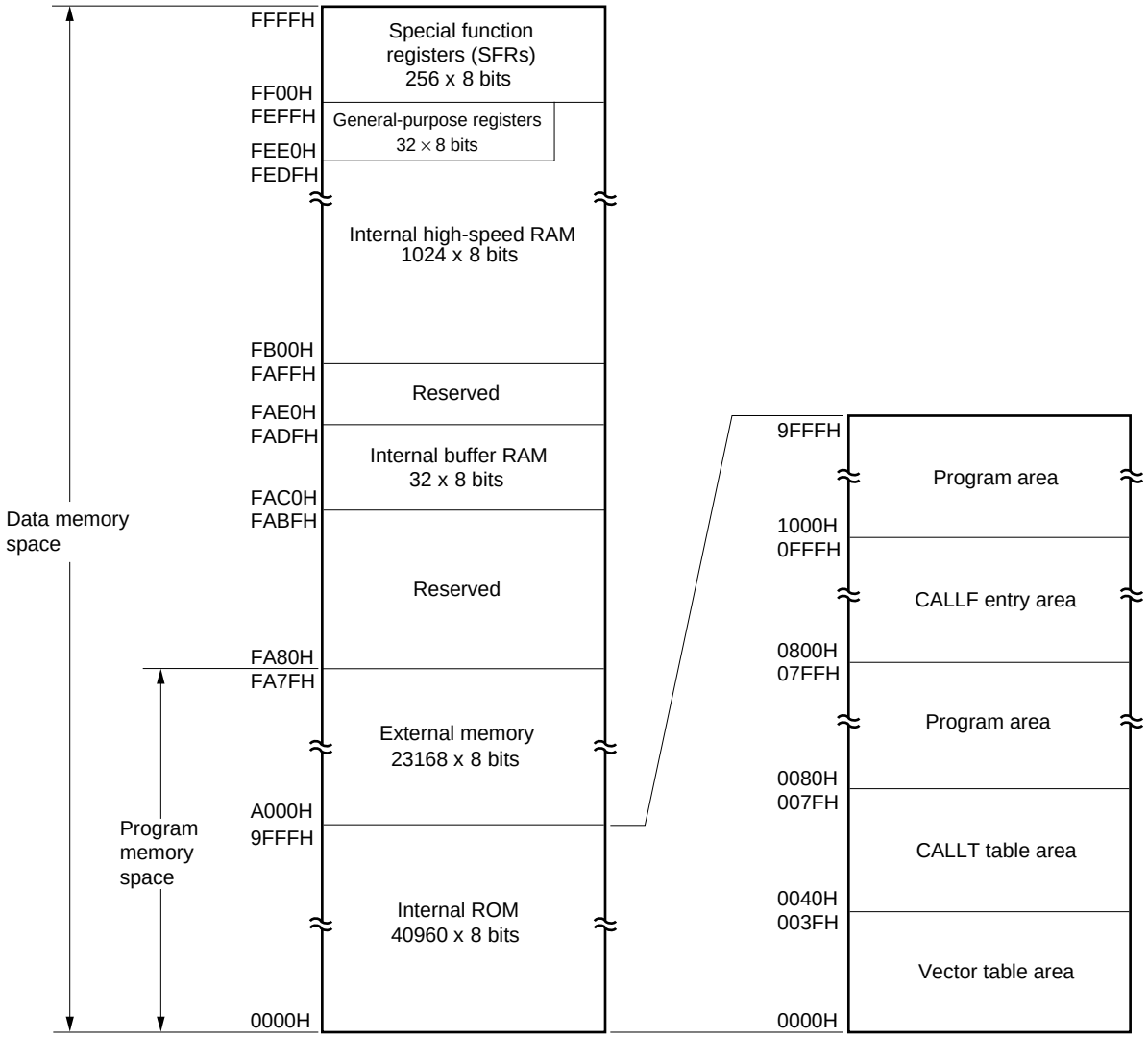


Figure 6-38. Memory Map (μPD78076/76Y)

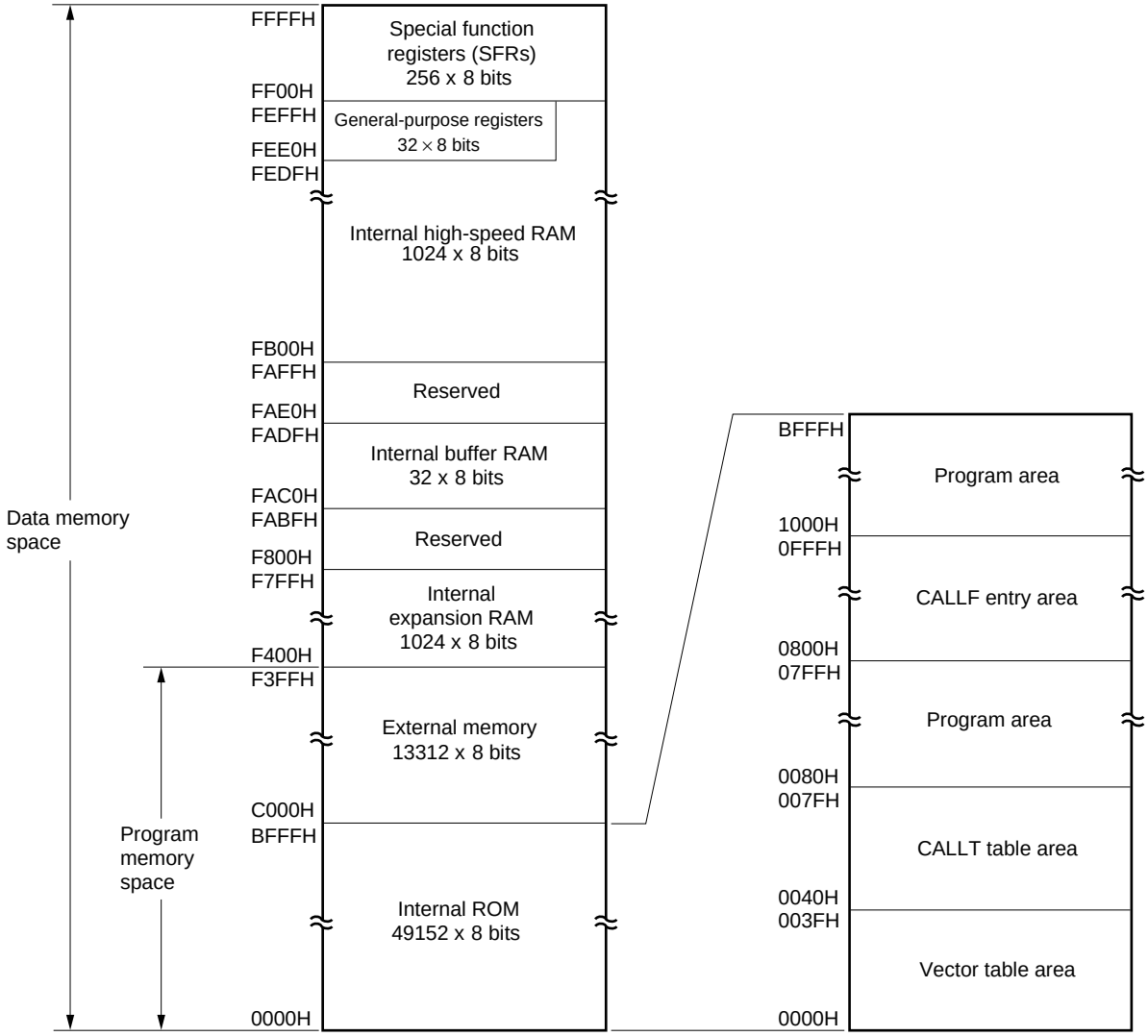
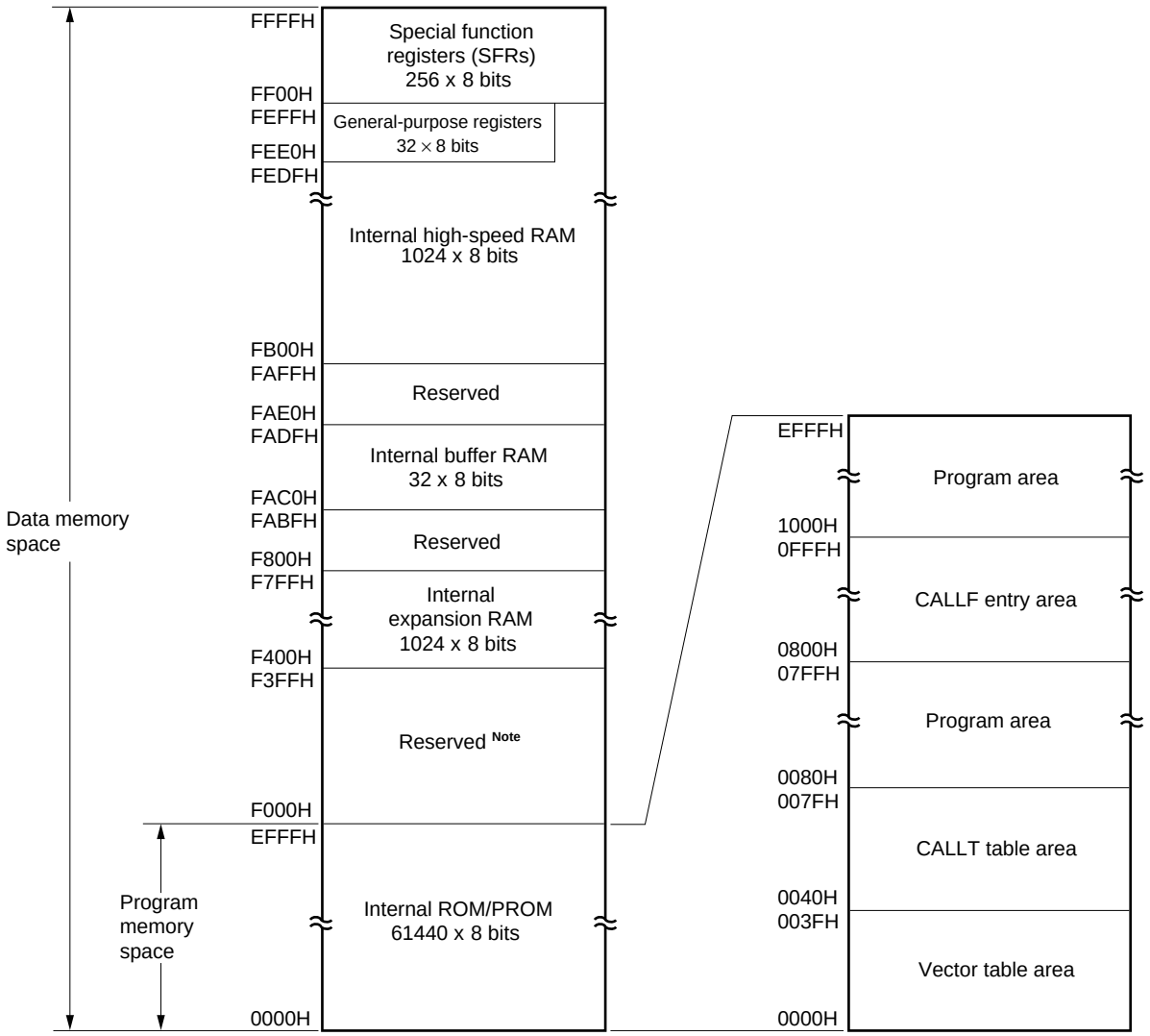


Figure 6-39. Memory Map (μPD78078/78Y, 78P078/78Y)



Note: When the internal ROM or internal PROM size is 60K, the area F000H to F3FFH cannot be used. F000H to F3FFH can be used as external memory by setting the internal ROM size to less than 56K via the internal memory size switching register (IMS).

6.7.4 Special Function Registers (SFRs)

Table 6-27. Special Function Register List (μPD78078/78Y, 78075B/75BY, and 78070A/70AY Subseries) (1/3)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulatable Bit Unit			After Reset
				1 Bit	8 Bits	16 Bits	
FF00H	Port 0	P0	R/W	√	√	–	00H
FF01H	Port 1	P1		√	√	–	
FF02H	Port 2	P2		√	√	–	
FF03H	Port 3	P3		√	√	–	
FF04H	Port 4 Note 1	P4		√	√	–	Undefined
FF05H	Port 5 Note 1	P5		√	√	–	
FF06H	Port 6	P6		√	√	–	
FF07H	Port 7	P7		√	√	–	00H
FF08H	Port 8 Note 1	P8		√	√	–	
FF09H	Port 9	P9		√	√	–	
FF0AH	Port 10	P10		√	√	–	
FF0CH	Port 12	P12		√	√	–	
FF0DH	Port 13	P13		√	√	–	
FF10H FF11H	Capture/compare register 00	CR00		–	–	√	Undefined
FF12H FF13H	Capture/compare register 01	CR01		–	–	√	
FF14H FF15H	16-bit timer register	TM0	R	–	–	√	0000H
FF16H	Compare register 10	CR10	R/W	–	√	–	Undefined
FF17H	Compare register 20	CR20		–	√	–	
FF18H	8-bit timer register 1	TMS TM1	R	–	√	√	00H
FF19H	8-bit timer register 2	TM2		–	√		
FF1AH	Serial I/O shift register 0	SIO0	R/W	–	√	–	Undefined
FF1BH	Serial I/O shift register 1	SIO1		–	√	–	
FF1FH	A/D conversion result register	ADCR	R	–	√	–	
FF20H	Port mode register 0	PM0	R/W	√	√	–	FFH
FF21H	Port mode register 1	PM1		√	√	–	
FF22H	Port mode register 2	PM2		√	√	–	
FF23H	Port mode register 3	PM3		√	√	–	
FF25H	Port mode register 5 Note 1	PM5		√	√	–	
FF26H	Port mode register 6	PM6		√	√	–	
FF27H	Port mode register 7	PM7		√	√	–	
FF28H	Port mode register 8 Note 1	PM8		√	√	–	
FF29H	Port mode register 9	PM9		√	√	–	
FF2AH	Port mode register 10	PM10		√	√	–	
FF2CH	Port mode register 12	PM12		√	√	–	
FF2DH	Port mode register 13	PM13		√	√	–	

Table 6-27. Special Function Register List (μPD78078/78Y, 78075B/75BY, and 78070A/70AY Subseries) (2/3)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulatable Bit Unit			After Reset
				1 Bit	8 Bits	16 Bits	
FF30H	Real-time output buffer register L	RTBL	R/W	–	√	–	00H
FF31H	Real-time output buffer register H	RTBH		–	√	–	
FF34H	Real-time output port mode register	RTPM		√	√	–	
FF36H	Real-time output port control register	RTPC		√	√	–	
FF38H FF39H	Correction address register 0 Note 2	CORAD0		–	–	√	
FF3AH FF3BH	Correction address register 1 Note 2	CORAD1		–	–	√	
FF3FH	External bus type select register	EBTS		–	√	–	
FF40H	Timer clock select register 0	TCL0		√	√	–	
FF41H	Timer clock select register 1	TCL1		–	√	–	
FF42H	Timer clock select register 2	TCL2		–	√	–	
FF43H	Timer clock select register 3	TCL3		–	√	–	88H
FF47H	Sampling clock select register	SCS		–	√	–	00H
FF48H	16-bit timer mode control register	TMC0		√	√	–	
FF49H	8-bit timer mode control register 1	TMC1		√	√	–	
FF4AH	Watch timer mode control register	TMC2		√	√	–	
FF4CH	Capture/compare control register 0	CRC0		√	√	–	04H
FF4EH	16-bit timer output control register	TOC0		√	√	–	00H
FF4FH	8-bit timer output control register	TOC1		√	√	–	
FF50H	Compare register 50	CR50		–	√	–	
FF51H	8-bit timer register 5	TM5	R	–	√	–	
FF52H	Timer clock select register 5	TCL5	R/W	–	√	–	
FF53H	8-bit timer mode control register 5	TMC5		√	√	–	
FF54H	Compare register 60	CR60		–	√	–	
FF55H	8-bit timer register 6	TM6	R	–	√	–	
FF56H	Timer clock select register 6	TCL6	R/W	–	√	–	
FF57H	8-bit timer mode control register 6	TMC6		√	√	–	
FF60H	Serial operation mode register 0	CSIM0		√	√	–	
FF61H	Serial bus interface control register	SBIC		√	√	–	
FF62H	Slave address register	SVA		–	√	–	Undefined
FF63H	Interrupt timing specification register	SINT		√	√	–	00H
FF68H	Serial operation mode register 1	CSIM1		√	√	–	
FF69H	Automatic data transmit/receive control register	ADTC		√	√	–	
FF6AH	Automatic data transmit/receive address pointer	ADTP		–	√	–	
FF6BH	Automatic data transmit/receive interval specification register	ADTI		√	√	–	
FF70H	Asynchronous serial interface mode register	ASIM		√	√	–	
FF71H	Asynchronous serial interface status register	ASIS	R	–	√	–	
FF72H	Serial operation mode register 2	CSIM2	R/W	√	√	–	
FF73H	Baud rate generator control register	BRGC		–	√	–	

Table 6-27. Special Function Register List (μPD78078/78Y, 78075B/75BY, and 78070A/70AY Subseries) (3/3)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulatable Bit Unit			After Reset
					1 Bit	8 Bits	16 Bits	
FF74H	Transmit shift register	TXS	SIO2	W	–	√	–	FFH
	Receive buffer register	RXB		R				
FF80H	A/D converter mode register	ADM		R/W	√	√	–	01H
FF84H	A/D converter input select register	ADIS			–	√	–	00H
FF8AH	Correction control register Note 2	CORCN			√	√	–	
FF90H	D/A conversion value set register 0	DACS0			–	√	–	
FF91H	D/A conversion value set register 1	DACS1			–	√	–	
FF98H	D/A converter mode register	DAM			√	√	–	
FFD0H to FFDFH	External access area Note 3				√	√	–	Undefined
FFE0H	Interrupt request flag register 0L	IF0	IF0L		√	√	√	00H
FFE1H	Interrupt request flag register 0H		IF0H		√	√		
FFE2H	Interrupt request flag register 1L	IF1L			√	√	–	
FFE4H	Interrupt request mask register 0L	MK0	MK0L		√	√	√	FFH
FFE5H	Interrupt request mask register 0H		MK0H		√	√		
FFE6H	Interrupt request mask register 1L	MK1L			√	√	–	
FFE8H	Priority order specification flag register 0L	PR0	PR0L		√	√	√	
FFE9H	Priority order specification flag register 0H		PR0H		√	√		
FFEAH	Priority order specification flag register 1L	PR1L			√	√	–	
FFECH	External interrupt mode register 0	INTM0			–	√	–	00H
FFEDH	External interrupt mode register 1	INTM1			–	√	–	
FFF0H	Internal memory size switching register	IMS			–	√	–	**Note 4**
FFF2H	Oscillation mode select register	OSMS		W	–	√	–	00H
FFF3H	Pull-up resistor option register H	PUOH		R/W	√	√	–	
FFF4H	Internal expansion RAM size switching register Note 1	IXS		W	–	√	–	**Note 5**
FFF6H	Key return mode register Note 1	KRM		R/W	√	√	–	02H
FFF7H	Pull-up resistor option register L	PUOL			√	√	–	00H
FFF8H	Memory expansion mode register	MM			√	√	–	10H
FFF9H	Watchdog timer mode register	WDTM			√	√	–	00H
FFFAH	Oscillation stabilization time select register	OSTS			–	√	–	04H
FFFBH	Processor clock control register	PCC			√	√	–	

Notes: 1. This register is not provided for the μPD78070A/70A Subseries.

2. This register is provided for the μPD78078/78Y Subseries only.

3. The external access area cannot be accessed in SFR addressing. Access the area with direct addressing.

4. The value after reset differs depending on the product, as follows:

	μPD78070A μPD78070AY	μPD78074B μPD78074BY	μPD78075B μPD78075BY	μPD78076 μPD78076Y	μPD78078 μPD78078Y	μPD78P078 μPD78P078Y
IMS	C0H	C8H	CAH	CCH	CFH	

To use a mask ROM version, do not set to IMS a value other than that after reset (except, however, when the external device expansion function is used with the μPD78078/78Y).

5. The value after reset differs depending on the product, as follows:
μPD78078/78Y Subseries products: 0AH
μPD78075B/75BY Subseries products: 0CH
To use a mask ROM version, do not set to IXS a value other than that after reset.

(1) Registers controlling port functions

The following four types of registers control the ports:

- Port mode registers (PM0 to PM3, PM5 to PM10 [Note 1], PM12, PM13)
- Pull-up resistor option registers (PUOH, PUOL)

Notes: 1. The μPD78070A/70AY do not have PM5 and PM8.
2. This register is not provided for the μPD78070A/70AY.

Format of Port Mode Registers (μPD78078/78Y and 78075B/75BY Subseries)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	1	FF20H	FFH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W
PM3	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	FF23H	FFH	R/W
PM5	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	FF25H	FFH	R/W
PM6	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	FF26H	FFH	R/W
PM7	1	1	1	1	1	PM72	PM71	PM70	FF27H	FFH	R/W
PM8	PM87	PM86	PM85	PM84	PM83	PM82	PM81	PM80	FF28H	FFH	R/W
PM9	1	PM96	PM95	PM94	PM93	PM92	PM91	PM90	FF29H	FFH	R/W
PM10	1	1	1	1	PM103	PM102	PM101	PM100	FF2AH	FFH	R/W
PM12	PM127	PM126	PM125	PM124	PM123	PM122	PM121	PM120	FF2CH	FFH	R/W
PM13	1	1	1	1	1	1	PM131	PM130	FF2DH	FFH	R/W

PMmn	Pmn pin input/output mode selection (m = 0 to 3, 5 to 10, 12, 13 : n = 0 to 7)
0	Output mode (output buffer ON)
1	Input mode (output buffer OFF)

Cautions: 1. Pins P00 and P07 are input-only pins.

2. Because port 0 has an alternate function as an external interrupt request input, when the port function output mode is specified and the output level is changed, the interrupt request flag is set. When the output mode is used, therefore, the interrupt mask flag should be set to 1 beforehand.

3. I/O specification of pins P40 to P47 is set by using the memory expansion mode register (MM).

Format of Port Mode Registers (μPD78070A/70AY Subseries)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	1	FF20H	FFH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W
PM3	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	FF23H	FFH	R/W
PM6	1	PM66	1	1	PM63	PM62	PM61	PM60	FF26H	FFH	R/W
PM7	1	1	1	1	1	PM72	PM71	PM70	FF27H	FFH	R/W
PM9	1	PM96	PM95	PM94	PM93	PM92	PM91	PM90	FF29H	FFH	R/W
PM10	1	1	1	1	PM103	PM102	PM101	PM100	FF2AH	FFH	R/W
PM12	PM127	PM126	PM125	PM124	PM123	PM122	PM121	PM120	FF2CH	FFH	R/W
PM13	1	1	1	1	1	1	PM131	PM130	FF2DH	FFH	R/W

PMmn	Pmn pin input/output mode selection (m = 0 to 3, 6, 7, 9, 10, 12, 13 : n = 0 to 7)
0	Output mode (output buffer ON)
1	Input mode (output buffer OFF)

Cautions: 1. Pins P00 and P07 are input-only pins.

2. Because port 0 has an alternate function as an external interrupt request input, when the port function output mode is specified and the output level is changed, the interrupt request flag is set. When the output mode is used, therefore, the interrupt mask flag should be set to 1 beforehand.

Format of Pull-up Resistor Option Registers
(μPD78078/78Y and 78075B/75BY Subseries)

Symbol	7	6	<5>	<4>	3	<2>	<1>	<0>	Address	After Reset	R/W
PUOH	0	0	PUO13	PUO12	0	PUO10	PUO9	PUO8	FFF3H	00H	R/W

	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>			
PUOL	PUO7	PUO6	PUO5	PUO4	PUO3	PUO2	PUO1	PUO0	FFF7H	00H	R/W

PUOm	Pm internal pull-up resistor selection (m = 0 to 10, 12, 13)
0	Internal pull-up resistor not used
1	Internal pull-up resistor used

Cautions: 1. P00 and P07 pins do not incorporate a pull-up resistor.

2. When ports 1, 4, 5, and the P64 to P67 pins, or port 8 pins are used as alternate-function pins, an on-chip pull-up resistor cannot be used even if 1 is set in the PUOm bit of PUOH and PUOL (m = 1, 4 to 6, or 8).

3. Pins P60 to P63 and P90 to 93 can be connected with a pull-up resistor by mask option only for a mask ROM version.

4. Bits 3, 6, and 7 of PUOH should be set to 0.

Format of Pull-up Resistor Option Registers (μPD78070A/70AY Subseries)

Symbol	7	6	<5>	<4>	3	<2>	<1>	<0>	Address	After Reset	R/W
PUOH	0	0	PUO13	PUO12	0	PUO10	PUO9	0	FFF3H	00H	R/W

	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>			
PUOL	PUO7	PUO6	0	0	PUO3	PUO2	PUO1	PUO0	FFF7H	00H	R/W

PUOm	Pm internal pull-up resistor selection (m = 0 to 3, 6, 7, 9, 10, 12, 13)
0	Internal pull-up resistor not used
1	Internal pull-up resistor used

Cautions: 1. P00, P07, P60 to P63, and P90 to P93 pins do not incorporate a pull-up resistor.

2. When port 1 or the P66 pin is used as an alternate function pin, an on-chip pull-up resistor cannot be used even if 1 is set in the PUOm bit of PUOL (m = 1, 6).

3. Bits 0, 3, 6, and 7 of PUOH and bits 4 and 5 of PUOL should be set to 0.

Caution: When the falling edge detection of port 4 is used, KRIF should be cleared to 0 (it is not cleared to 0 automatically).

(2) Registers controlling clock generator

The following two registers control the clock generator:

- Processor clock control register (PCC)
- Oscillation mode select register (OSMS)

Format of Processor Clock Control Register

Symbol	<7>	<6>	<5>	<4>	3	2	1	0	Address	After Reset	R/W
PCC	MCC	FRC	CLS	CSS	0	PCC2	PCC1	PCC0	FFFBH	04H	R/W Note 1

R/W

CSS	PCC2	PCC1	PCC0	CPU clock (f_{CPU}) selection		
					MCS = 1	MCS = 0
0	0	0	0	f_{XX}	f_X	$f_X/2$
	0	0	1	$f_{XX}/2$	$f_X/2$	$f_X/2^2$
	0	1	0	$f_{XX}/2^2$	$f_X/2^2$	$f_X/2^3$
	0	1	1	$f_{XX}/2^3$	$f_X/2^3$	$f_X/2^4$
	1	0	0	$f_{XX}/2^4$	$f_X/2^4$	$f_X/2^5$
1	0	0	0	$f_{XT}/2$		
	0	0	1			
	0	1	0			
	0	1	1			
	1	0	0			
Other than above				Setting prohibited		

R

CLS	CPU clock status
0	Main system clock
1	Subsystem clock

R/W

FRC	Subsystem clock feedback resistor selection
0	Internal feedback resistor used
1	Internal feedback resistor not used

R/W

MCC	Main system clock oscillation control Note 2
0	Oscillation possible
1	Oscillation stopped

Notes: 1. Bit 5 is a read-only bit.
2. When the CPU is operating on the subsystem clock, MCC should be used to stop the main system clock oscillation. A STOP instruction should not be used.

Caution: Bit 3 must be set to 0.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillator frequency
f_{XT}: Subsystem clock oscillator frequency
MCS: Bit 0 of oscillation mode select register (OSMS)

The fastest instruction of the μPD7807x Subseries can be executed in two clocks of the CPU clock. The relationship between the CPU clock (f_{CPU}) and the minimum instruction execution time is shown in the table below.

Relationship between CPU Clock and Minimum Instruction Execution Time

CPU Clock (f_{CPU})	Minimum Instruction Execution Time: $2/f_{CPU}$
f_X	0.4 μs
$f_X/2$	0.8 μs
$f_X/2^2$	1.6 μs
$f_X/2^3$	3.2 μs
$f_X/2^4$	6.4 μs
$f_X/2^5$	12.8 μs
$f_{XT}/2$	122 μs

Remarks: f_X = 5.0 MHz, f_{XT} = 32.768 kHz
f_X: Main system clock oscillation frequency
f_{XT}: Subsystem clock oscillation frequency

Format of Oscillation Mode Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
OSMS	0	0	0	0	0	0	0	MCS	FFF2H	00H	W

MCS	Main system clock scaler control
0	Scaler used
1	Scaler not used

Cautions: 1. Writing data (including same data as previous) to OSMS causes a delay of the main system clock cycle of up to 2/f_x during the write operation. Therefore, if this register is written during the operation, in peripheral hardware that operates with the main system clock a temporary error occurs in the count clock cycle of the timer, etc. In addition, because the oscillation mode is changed by this register, the clocks for the peripheral hardware as well as that for the CPU are switched.

Therefore, writing to OSMS should be performed only immediately after reset signal release and before peripheral hardware operation starts.

2. When writing "1" to MCS, V_{DD} must be 2.7 V or higher before the write execution.

(3) Registers controlling 16-bit timer/event counter

The following seven registers control the 16-bit timer/event counter:

- Timer clock select register 0 (TCL0)
- 16-bit timer mode control register (TMC0)
- Capture/compare control register 0 (CRC0)
- 16-bit timer output control register (TOC0)
- Port mode register 3 (PM3)
  - Refer to section (1) for the register format.
- External interrupt mode register 0 (INTM0)
  - Refer to section (17) for the register format.
- Sampling clock select register (SCS)
  - Refer to section (17) for the register format.

Format of Timer Clock Select Register 0

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL0	CLOE	TCL06	TCL05	TCL04	TCL03	TCL02	TCL01	TCL00	FF40H	00H	R/W

This section controls the clock output circuit.
Refer to **(8) Registers controlling clock output function** or **Chapter 13** of *μPD78078, 78078Y Subseries User's Manual*, **Chapter 13** of *μPD78075B, 78075BY Subseries User's Manual*, or **Chapter 13** of *μPD78070A, 78070AY Subseries User's Manual* for detailed information.

TCL06	TCL05	TCL04	16-bit timer register count clock selection		
				MCS = 1	MCS = 0
0	0	0	TI00 (Valid edge specifiable)		
0	0	1	$2f_{XX}$	Setting prohibited	f_X (5.0 MHz)
0	1	0	f_{XX}	f_X (5.0 MHz)	$f_X/2$ (2.5 MHz)
0	1	1	$f_{XX}/2$	$f_X/2$ (2.5 MHz)	$f_X/2^2$ (1.25 MHz)
1	0	0	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	1	1	Watch timer output (INTTM3)		
Settings other than above are prohibited					

Cautions: 1. External interrupt mode register 0 sets the TI00/INTP0 pin valid edge, and the sampling clock select register selects the sampling clock frequency.

2. To read the count value when TI00 has been specified as the TM0 count clock, the value should be read from TM0, not from capture/compare register 01 (CR01).

3. To write data other than that already written to TCL0, stop the timer operation once.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)

f_X: Main system clock oscillation frequency

TI00: 16-bit timer/event counter input pin

TM0: 16-bit timer register

MCS: Bit 0 of oscillation mode select register (OSMS)

Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of 16-Bit Timer Mode Control Register

Symbol	7	6	5	4	3	2	1	<0>	Address	After Reset	R/W
TMC0	0	0	0	0	TMC03	TMC02	TMC01	OVF0	FF48H	00H	R/W

OVF0	16-bit timer register overflow detection
0	Overflow not detected
1	Overflow detected

TMC03	TMC02	TMC01	Operating mode and Clear mode	TO0 output timing	Interrupt generation
0	0	0	Operation stop (TM0 cleared to 0)	No change	Not generated
0	0	1	PWM mode (free running)	PWM pulse output	Generated when TM0 and CR00 match, or TM0 and CR01 match
0	1	0	Free-running mode	TM0 and CR00 match or TM0 and CR01 match	
0	1	1		TM0 and CR00 match, TM0 and CR01 match, or on TI00 valid edge	
1	0	0	Clear and start on TI00 valid edge	TM0 and CR00 match or TM0 and CR01 match	
1	0	1		TM0 and CR00 match, TM0 and CR01 match, or on TI00 valid edge	
1	1	0	Clear and start when TM0 and CR00 match	TM0 and CR00 match or TM0 and CR01 match	
1	1	1		TM0 and CR00 match, TM0 and CR01 match, or on TI00 valid edge	

Cautions:

1. **The 16-bit timer register (TM0) starts operation when a value other than 0, 0, 0 is set to TMC01 to TMC03 (operation stop mode). To stop the operation, set TMC01 to TMC03 to 0, 0, 0.**
2. **Switch the Clear mode and the T00 output timing after stopping the timer operation (by setting TMC01 to TMC03 to 0, 0, 0).**
3. **Set the valid edge of the TI00/INTP0 pin with external interrupt mode register 0 (INTM0) and select the sampling clock frequency with the sampling clock select register (SCS).**
4. **When using the PWM mode, set the PWM mode and then set data to CR00.**
5. **If the mode is set so that the timer is cleared and starts when TM0 and CR00 match, the OVF0 flag is set to 1 when the TM0 value changes from FFFFH to 0000H with CR00 set to FFFFH.**

Remarks:

TO0: 16-bit timer/event counter output pin
TI00: 16-bit timer/event counter input pin
TM0: 16-bit timer register
CR00: Compare register 00
CR01: Compare register 01

Format of Capture/Compare Control Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
CRC0	0	0	0	0	0	CRC02	CRC01	CRC00	FF4CH	04H	R/W

CRC00	CR00 operating mode selection
0	Operates as compare register
1	Operates as capture register

CRC01	CR00 capture trigger selection
0	Captures on valid edge of TI01
1	Captures on valid edge of TI00

CRC02	CR01 operating mode selection
0	Operates as compare register
1	Operates as capture register

Cautions: 1. Timer operation must be stopped before setting CRC0.

2. When Clear and Start mode on a match between TM0 and CR00 is selected with the 16-bit timer mode control register, CR00 should not be specified as a capture register.

Format of 16-Bit Timer Output Control Register

Symbol	7	<6>	<5>	4	<3>	<2>	1	<0>	Address	After Reset	R/W
TOC0	0	OSPT	OSPE	TOC04	LVS0	LVR0	TOC01	TOE0	FF4EH	00H	R/W

TOE0	16-bit timer/event counter output control
0	Output disabled (Port mode)
1	Output enabled

TOC01	In PWM mode	In other modes
	Active level selection	Timer output F/F control by match of CR00 and TM0
0	Active high	Inversion operation disabled
1	Active low	Inversion operation enabled

LVS0	LVR0	16-bit timer/event counter timer output F/F status setting
0	0	No change
0	1	Timer output F/F reset (0)
1	0	Timer output F/F set (1)
1	1	Setting prohibited

TOC04	Timer output F/F control by match of CR01 and TM0
0	Inversion operation disabled
1	Inversion operation enabled

OSPE	One-shot pulse output control
0	Continuous pulse output
1	One-shot pulse output

OSPT	Control of one-shot pulse output trigger by software
0	No one-shot pulse trigger
1	One-shot pulse trigger used

Cautions: 1. Timer operation must be stopped before setting TOC0 (except, however, OSPT).

2. If LVS0 and LVR0 are read after data is set, they will be 0.

3. OSPT is cleared automatically after data setting, and will therefore be 0 if read.

4. $f_{XX}/2^N$ is the clock supplied to the CPU, and $f_{XX}/2^5$, $f_{XX}/2^6$, and $f_{XX}/2^7$ are clocks supplied to peripheral hardware. $f_{XX}/2^N$ is stopped in HALT mode.

(4) Registers controlling 8-bit timer/event counters 1 and 2

The following four registers control 8-bit timer/event counters 1 and 2:

- Timer clock select register 1 (TCL1)
- 8-bit timer mode control register 1 (TMC1)
- 8-bit timer output control register (TOC1)
- Port mode register 3 (PM3)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 1

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL1	TCL17	TCL16	TCL15	TCL14	TCL13	TCL12	TCL11	TCL10	FF41H	00H	R/W

TCL13	TCL12	TCL11	TCL10	8-bit timer register 1 count clock selection		
					MCS = 1	MCS = 0
0	0	0	0	TI1 falling edge		
0	0	0	1	TI1 rising edge		
0	1	1	0	$f_{XX}/2$	$f_X/2$ (2.5 MHz)	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
1	1	1	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)
1	1	1	1	$f_{XX}/2^{11}$	$f_X/2^{11}$ (2.4 kHz)	$f_X/2^{12}$ (1.2 kHz)
Settings other than above are prohibited						

TCL17	TCL16	TCL15	TCL14	8-bit timer register 2 count clock selection		
					MCS = 1	MCS = 0
0	0	0	0	TI2 falling edge		
0	0	0	1	TI2 rising edge		
0	1	1	0	$f_{XX}/2$	$f_X/2$ (2.5 MHz)	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
1	1	1	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)
1	1	1	1	$f_{XX}/2^{11}$	$f_X/2^{11}$ (2.4 kHz)	$f_X/2^{12}$ (1.2 kHz)
Settings other than above are prohibited						

Caution: To write data other than that already written to TCL1, stop the timer operation once.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
TI1: 8-bit timer register 1 input pin
TI2: 8-bit timer register 2 input pin
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of 8-Bit Timer Mode Control Register 1

Symbol	7	6	5	4	3	2	<1>	<0>	Address	After Reset	R/W
TMC1	0	0	0	0	0	TMC12	TCE2	TCE1	FF49H	00H	R/W

TCE1	8-bit timer register 1 operation control
0	Operation stop (TM1 clear to 0)
1	Operation enable

TCE2	8-bit timer register 2 operation control
0	Operation stop (TM2 clear to 0)
1	Operation enable

TMC12	Operating mode selection
0	8-bit timer register x 2 channel mode (TM1, TM2)
1	16-bit timer register x 1 channel mode (TMS)

Cautions: 1. Stop the timer operation before switching the operating mode.

2. When used as a 16-bit timer register, TCE1 should be used to control the enable/stop function.

Format of 8-Bit Timer Output Control Register

Symbol	<7>	<6>	5	<4>	<3>	<2>	1	<0>	Address	After Reset	R/W
TOC1	LVS2	LVR2	TOC15	TOE2	LVS1	LVR1	TOC11	TOE1	FF4FH	00H	R/W

TOE1	8-bit timer/event counter 1 outptut control
0	Output disable (port mode)
1	Output enable

TOC11	8-bit timer/event counter 1 timer output F/F control
0	Inverted operation disable
1	Inverted operation enable

LVS1	LVR1	8-bit timer/event counter 1 timer output F/F status set
0	0	Unchanged
0	1	Timer output F/F reset (0)
1	0	Timer output F/F set (1)
1	1	Setting prohibited

TOE2	8-bit timer/event counter 2 output control
0	Output disable (Port mode)
1	Output enable

TOC15	8-bit timer/event counter 2 timer output F/F control
0	Inverted operation disable
1	Inverted operation enable

LVS2	LVR2	8-bit timer/event counter 2 timer output F/F status set
0	0	Unchanged
0	1	Timer output F/F reset (0)
1	0	Timer output F/F set (1)
1	1	Setting prohibited

Cautions: 1. Timer operation must be stopped before setting TOC1.

2. After data setting, 0 can be read from LVS1, LVS2, LVR1, and LVR2.

(5) Registers controlling 8-bit timer/event counters 5 and 6

The following three types of registers control 8-bit timer/event counters 5 and 6:

- Timer clock select registers 5 and 6 (TCL5, TCL6)
- 8-bit timer mode control registers 5 and 6 (TMC5, TMC6)
- Port mode register 10 (PM10)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 5

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL5	0	0	0	0	TCL53	TCL52	TCL51	TCL50	FF52H	00H	R/W

TCL53	TCL52	TCL51	TCL50	8-bit timer register 5 count clock selection		
					MCS = 1	MCS = 0
0	0	0	0	TI5 falling edge [Note]		
0	0	0	1	TI5 rising edge [Note]		
0	1	0	0	$2f_{XX}$	(Setting prohibited)	f_X (5.0 MHz)
0	1	0	1	f_{XX}	f_X (5.0 MHz)	$f_X/2$ (2.5 MHz)
0	1	1	0	$f_{XX}/2$	$f_X/2$ (2.5 MHz)	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
1	1	1	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)
1	1	1	1	$f_{XX}/2^{11}$	$f_X/2^{11}$ (2.4 kHz)	$f_X/2^{11}$ (1.2 kHz)
Settings other than above are prohibited						

Note: When a clock is input from the external, timer output (PWM output) cannot be used.

Caution: To write data other than that already set to TCL5, stop the timer operation once.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
TI5: 8-bit timer register 5 input pin
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of Timer Clock Select Register 6

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL6	0	0	0	0	TCL63	TCL62	TCL61	TCL60	FF56H	00H	R/W

TCL63	TCL62	TCL61	TCL60	8-bit timer register 6 count clock selection		
					MCS = 1	MCS = 0
0	0	0	0	TI6 falling edge Note		
0	0	0	1	TI6 rising edge Note		
0	1	0	0	$2f_{XX}$	(Setting prohibited)	f_X (5.0 MHz)
0	1	0	1	f_{XX}	f_X (5.0 MHz)	$f_X/2$ (2.5 MHz)
0	1	1	0	$f_{XX}/2$	$f_X/2$ (2.5 MHz)	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
1	1	1	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)
1	1	1	1	$f_{XX}/2^{11}$	$f_X/2^{11}$ (2.4 kHz)	$f_X/2^{11}$ (1.2 kHz)
Settings other than above are prohibited						

Note: When a clock is input from the external, timer output (PWM output) cannot be used.

Caution: To write data other than that already set to TCL6, stop the timer operation once.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
TI6: 8-bit timer register 6 input pin
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of 8-Bit Timer Output Control Register 5

Symbol	<7>	6	5	4	<3>	<2>	1	<0>	Address	After Reset	R/W
TMC5	TCE5	TMC56	0	0	LVS5	LVR5	TMC51	TOE5	FF53H	00H	R/W

TOE5	8-bit timer/event counter 5 output control
0	Output disabled (Port mode)
1	Output enabled

TMC51	In PWM mode	In other modes
	Active level selection	Timer output F/F1 control
0	Active high	Inversion operation disabled
1	Active low	Inversion operation enabled

LVS5	LVR5	8-bit timer/event counter 5 timer output F/F1 status setting
0	0	No change
0	1	Timer output F/F1 reset (0)
1	0	Timer output F/F1 set (1)
1	1	Setting prohibited

TMC56	8-bit timer/event counter 5 operating mode selection
0	Clear and Start mode on match of TM5 and CR50
1	PWM mode (free running)

TCE5	8-bit timer register 5 operation control
0	Operation stop (TM5 clear to 0)
1	Operation enable

Cautions: 1. Timer operation must be stopped before setting TMC5.

2. If LVS5 and LVR5 are read after data are set, they will be 0.

3. Be sure to set bits 4 and 5 to 0.

Format of 8-Bit Timer Output Control Register 6

Symbol	<7>	6	5	4	<3>	<2>	1	<0>	Address	After Reset	R/W
TMC6	TCE6	TMC66	0	0	LVS6	LVR6	TMC61	TOE6	FF57H	00H	R/W

TOE6	8-bit timer/event counter 6 output control
0	Output disabled (Port mode)
6	Output enabled

TMC61	In PWM mode	In other modes
	Active level selection	Timer output F/F1 control
0	Active high	Inversion operation disabled
1	Active low	Inversion operation enabled

LVS6	LVR6	8-bit timer/event counter 6 timer output F/F1 status setting
0	0	No change
0	1	Timer output F/F1 reset (0)
1	0	Timer output F/F1 set (1)
1	1	Setting prohibited

TMC66	8-bit timer/event counter 6 operating mode selection
0	Clear and Start mode on match of TM6 and CR60
1	PWM mode (free running)

TCE6	8-bit timer register 6 operation control
0	Operation stop (TM6 clear to 0)
1	Operation enable

Cautions: 1. Timer operation must be stopped before setting TMC6.

2. If LVS6 and LVR6 are read after data are set, they will be 0.

3. Be sure to set bits 4 and 5 to 0.

(6) Registers controlling watch timer

The following two registers control the watch timer:

- Timer clock select register 2 (TCL2)
- Watch timer mode control register (TMC2)

Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL2	TCL27	TCL26	TCL25	TCL24	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

This section controls the watchdog timer.
Refer to **(7) Registers controlling watchdog timer** or
Chapter 12 of *μPD78078, 78078Y Subseries User's Manual*,
Chapter 12 of *μPD78075B, 78075BY Subseries User's Manual*, or
Chapter 12 of *μPD78070A, 78070AY Subseries User's Manual*
for detailed information.

This section controls the buzzer output function.
Refer to **(9) Registers controlling buzzer output function** or
Chapter 14 of *μPD78078, 78078Y Subseries User's Manual*,
Chapter 14 of *μPD78075B, 78075BY Subseries User's Manual*, or
Chapter 14 of *μPD78070A, 78070AY Subseries User's Manual*
for detailed information.

TCL24	Watch timer count clock selection		
		MCS = 1	MCS = 0
0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	f_{XT} (32.768 kHz)		

Caution: When rewriting TCL2 to other data, stop the timer operation beforehand.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
f_{XT}: Subsystem clock oscillation frequency
MCS: Bit 0 of oscillation mode select register (OSMS)

Values in parentheses apply to operation with f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

A 0.5 second or 0.25 second interval can be generated either with a 4.19304 MHz main system clock or a 32.768 kHz subsystem clock

Format of Watch Timer Mode Control Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TMC2	0	TMC26	TMC25	TMC24	TMC23	TMC22	TMC21	TMC20	FF4AH	00H	R/W

TMC20	Watch operating mode selection
0	Normal operating mode (flag set at $f_W/2^{14}$)
1	Fast feed operating mode (flag set at $f_W/2^5$)

TMC21	Prescaler operation control
0	Clear after operation stop
1	Operation enable

TMC22	5-bit counter operation control
0	Clear after operation stop
1	Operation enable

TMC23	Watch flag set time selection		
	f_{XX} = 5.0-MHz operation	f_{XX} = 4.19-MHz operation	f_{XT} = 32.768-kHz operation
0	$2^{14}/f_W$ (0.4 sec)	$2^{14}/f_W$ (0.5 sec)	$2^{14}/f_W$ (0.5 sec)
1	$2^{13}/f_W$ (0.2 sec)	$2^{13}/f_W$ (0.25 sec)	$2^{13}/f_W$ (0.25 sec)

TMC26	TMC25	TMC24	Prescaler interval time selection		
			f_{XX} = 5.0-MHz operation	f_{XX} = 4.19-MHz operation	f_{XT} = 32.768-kHz operation
0	0	0	$2^4/f_W$ (410 μs)	$2^4/f_W$ (488 μs)	$2^4/f_W$ (488 μs)
0	0	1	$2^5/f_W$ (819 μs)	$2^5/f_W$ (977 μs)	$2^5/f_W$ (977 μs)
0	1	0	$2^6/f_W$ (1.64 ms)	$2^6/f_W$ (1.95 ms)	$2^6/f_W$ (1.95 ms)
0	1	1	$2^7/f_W$ (3.28 ms)	$2^7/f_W$ (3.91 ms)	$2^7/f_W$ (3.91 ms)
1	0	0	$2^8/f_W$ (6.55 ms)	$2^8/f_W$ (7.81 ms)	$2^8/f_W$ (7.81 ms)
1	0	1	$2^9/f_W$ (13.1 ms)	$2^9/f_W$ (15.6 ms)	$2^9/f_W$ (15.6 ms)
Settings other than above are prohibited					

Caution: When the watch timer is used, the prescaler should not be cleared frequently.

Remarks: f_W: Watch timer clock frequency ($f_{XX}/2^7$ or f_{XT})

f_{XX}: Main system clock frequency (f_X or $f_X/2$)

f_X: Main system clock oscillation frequency

f_{XT}: Subsystem clock oscillation frequency

(7) Registers controlling watchdog timer

The following two registers control the watchdog timer:

- Timer clock select register 2 (TCL2)
- Watchdog timer mode register (WDTM)

Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL2	TCL27	TCL26	TCL25	TCL24	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

This section controls the watch timer.
Refer to **(6) Registers controlling watch timer** or
Chapter 11 of *μPD78078, 78078Y Subseries User's Manual*,
Chapter 11 of *μPD78075B, 78075BY Subseries User's Manual*, or
Chapter 11 of *μPD78070A, 78070AY Subseries User's Manual*
for detailed information.

This section controls the buzzer output function.
Refer to **(9) Registers controlling buzzer output function** or
Chapter 14 of *μPD78078, 78078Y Subseries User's Manual*,
Chapter 14 of *μPD78075B, 78075BY Subseries User's Manual*, or
Chapter 14 of *μPD78070A, 78070AY Subseries User's Manual*
for detailed information.

TCL22	TCL21	TCL20	Watchdog timer count clock selection		
				MCS = 1	MCS = 0
0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
1	1	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)
1	1	1	$f_{XX}/2^{11}$	$f_X/2^{11}$ (2.4 kHz)	$f_X/2^{12}$ (1.2 kHz)

Caution: When rewriting TCL2 to other data, stop the timer operation beforehand.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz.
This register also controls the watch timer and the buzzer.

Format of Watchdog Timer Mode Register

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
WDTM	RUN	0	0	WDTM4	WDTM3	0	0	0	FFF9H	00H	R/W

WDTM4	WDTM3	Watchdog timer operation mode selection Note 1
0	×	Interval timer mode Note 2 (Maskable interrupt request occurs upon generation of an overflow.)
1	0	Watchdog timer mode 1 (Non-maskable interrupt request occurs upon generation of an overflow.)
1	1	Watchdog timer mode 2 (Reset operation is activated upon generation of an overflow.)

RUN	Watchdog timer operation mode selection Note 3
0	Count stop
1	Counter is cleared and counting starts

Notes: 1. Once set to 1, WDTM3 and WDTM4 cannot be cleared to 0 by software.

2. The watchdog timer starts operating as an interval timer as soon as RUN has been set to 1.

3. Once set to 1, RUN cannot be cleared to 0 by software. Thus, once counting starts, counting can only be stopped by $\overline{\text{RESET}}$ input.

Cautions: 1. When 1 is set in RUN so that the watchdog timer is cleared, the actual overflow time is up to 0.5% shorter than the time set by timer clock select register 2 (TCL2).

2. To use watchdog timer modes 1 and 2, make sure that the interrupt request flag (TMIF4) is 0, and then set WDTM4 to 1.

If WDTM4 is set to 1 when TMIF4 is 1, the non-maskable interrupt request occurs, regardless of the contents of WDTM3.

Remark: ×: Don't care

(8) Registers controlling clock output function

The following two registers control the clock output function:

- Timer clock select register 0 (TCL0)
- Port mode register 3 (PM3)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 0

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL0	CLOE	TCL06	TCL05	TCL04	TCL03	TCL02	TCL01	TCL00	FF40H	00H	R/W

This section controls the 16-bit timer.
Refer to **(3) Registers controlling 16-bit timer/event counter** or **Chapter 8** of *µPD78078, 78078Y Subseries User's Manual*, **Chapter 8** of *µPD78075B, 78075BY Subseries User's Manual*, or **Chapter 8** of *µPD78070A, 78070AY Subseries User's Manual* for detailed information.

TCL03	TCL02	TCL01	TCL00	PCL output clock selection		
					MCS = 1	MCS = 0
0	0	0	0	f_{XT} (32.768 kHz)		
0	1	0	1	f_{XX}	f_X (5.0 MHz)	$f_X/2$ (2.5 MHz)
0	1	1	0	$f_{XX}/2$	$f_X/2$ (2.5 MHz)	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
Settings other than above are prohibited						

CLOE	PCL output control
0	Output disable
1	Output enable

Cautions: 1. When enabling PCL output, set TCL00 to TCL03, then set 1 in CLOE with a 1-bit memory manipulation instruction.

2. To write data other than that already written to TCL0, stop the clock operation once.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)

f_X: Main system clock oscillation frequency

f_{XT}: Subsystem clock oscillation frequency

MCS: Bit 0 of oscillation mode select register (OSMS)

Values in parentheses apply to operation with f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

(9) Registers controlling buzzer output function

The following two registers control the buzzer output function:

- Timer clock select register 2 (TCL2)
- Port mode register 3 (PM3)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL2	TCL27	TCL26	TCL25	TCL24	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

This section controls the watchdog timer.
Refer to **(7) Registers controlling watchdog timer** or
Chapter 12 of *μPD78078, 78078Y Subseries User's Manual*,
Chapter 12 of *μPD78075B, 78075BY Subseries User's Manual*, or
Chapter 12 of *μPD78070A, 78070AY Subseries User's Manual*
for detailed information.

This section controls the watch timer.
Refer to **(6) Registers controlling watch timer** or
Chapter 11 of *μPD78078, 78078Y Subseries User's Manual*,
Chapter 11 of *μPD78075B, 78075BY Subseries User's Manual*, or
Chapter 11 of *μPD78070A, 78070AY Subseries User's Manual*
for detailed information.

TCL27	TCL26	TCL25	Buzzer output frequency selection		
				MCS = 1	MCS = 0
0	x	x	Buzzer output disable		
1	0	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)
1	0	1	$f_{XX}/2^{10}$	$f_X/2^{10}$ (4.9 kHz)	$f_X/2^{11}$ (2.4 kHz)
1	1	0	$f_{XX}/2^{11}$	$f_X/2^{11}$ (2.4 kHz)	$f_X/2^{12}$ (1.2 kHz)
1	1	1	Setting prohibited		

Caution: When rewriting TCL2 to other data, stop the timer operation beforehand.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
×: Don't care
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz.

(10) Registers controlling A/D converter

The following three registers control the A/D converter:

- A/D converter mode register (ADM)
- A/D converter input select register (ADIS)
- External interrupt mode register 1 (INTM1)
  - Refer to section (17) for the register format.

Format of A/D Converter Mode Register

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After Reset	R/W
ADM	CS	TRG	FR1	FR0	ADM3	ADM2	ADM1	HSC	FF80H	01H	R/W

ADM3	ADM2	ADM1	Analog input channel selection
0	0	0	ANI0
0	0	1	ANI1
0	1	0	ANI2
0	1	1	ANI3
1	0	0	ANI4
1	0	1	ANI5
1	1	0	ANI6
1	1	1	ANI7

FR1	FR0	HSC	A/D conversion time selection [Note 1]			
			f_X = 5.0-MHz operation		f_X = 4.19-MHz operation	
			MCS = 1	MCS = 0	MCS = 1	MCS = 0
0	0	1	80/f_X (Setting prohibited [Note 2])	160/f_X (32.0 μs)	80/f_X (19.1 μs)	160/f_X (38.1 μs)
0	1	1	40/f_X (Setting prohibited [Note 2])	80/f_X (Setting prohibited [Note 2])	40/f_X (Setting prohibited [Note 2])	80/f_X (19.1 μs)
1	0	0	50/f_X (Setting prohibited [Note 2])	100/f_X (20.0 μs)	50/f_X (Setting prohibited [Note 2])	100/f_X (23.8 μs)
1	0	1	100/f_X (20.0 μs)	200/f_X (40.0 μs)	100/f_X (23.8 μs)	200/f_X (47.7 μs)
Settings other than above are prohibited						

TRG	External trigger selection
0	No external trigger (software starts)
1	Conversion started by external trigger (hardware starts)

CS	A/D conversion operation control
0	Operation stop
1	Operation start

Notes: 1. Set so that the A/D conversion time is 19.1 μs or more.
2. Setting prohibited because A/D conversion time is less than 19.1 μs.

Cautions: 1. The following sequence is recommended for power consumption reduction of the A/D converter when the standby function is used: Clear bit 7 (CS) to 0 first to stop the A/D conversion operation, and then execute the HALT or STOP instruction.

2. When restarting the stopped A/D conversion operation, start the A/D conversion operation after clearing the interrupt request flag (ADIF) to 0.

Remarks: f_X: Main system clock oscillation frequency
MCS: Bit 0 of oscillation mode select register (OSMS)

Format of A/D Converter Input Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADIS	0	0	0	0	ADIS3	ADIS2	ADIS1	ADIS0	FF84H	00H	R/W

ADIS3	ADIS2	ADIS1	ADIS0	Number of analog input channel selection
0	0	0	0	No analog input channel (P10 to P17)
0	0	0	1	1 channel (ANI0, P11 to P17)
0	0	1	0	2 channels (ANI0, ANI1, P12 to P17)
0	0	1	1	3 channels (ANI0 to ANI2, P13 to P17)
0	1	0	0	4 channels (ANI0 to ANI3, P14 to P17)
0	1	0	1	5 channels (ANI0 to ANI4, P15 to P17)
0	1	1	0	6 channels (ANI0 to ANI5, P16, P17)
0	1	1	1	7 channels (ANI0 to ANI6, P17)
1	0	0	0	8 channels (ANI0 to ANI7)
Settings other than above are prohibited				

Cautions: 1. Set the analog input channel in the following order:

a. Set the number of analog input channels with ADIS.

b. Using the A/D converter mode register (ADM), select one channel to undergo A/D conversion from among the channels set for analog input with ADIS.

2. No internal pull-up resistor can be used to the channels set for analog input with ADIS, irrespective of the value of bit 1 (PUO1) of pull-up resistor option register L (PUOL).

(11) Register controlling D/A converter

The following register controls the D/A converter:

- D/A converter mode register (DAM)

Format of D/A Converter Mode Register

Symbol	7	6	5	4	3	2	<1>	<0>	Address	After Reset	R/W
DAM	0	0	DAM5	DAM4	0	0	DACE1	DACE0	FF98H	00H	R/W

DACE0	D/A converter channel 0 control
0	D/A conversion stop
1	D/A conversion enable

DACE1	D/A converter channel 1 control
0	D/A conversion stop
1	D/A conversion enable

DAM4	D/A converter channel 0 operating mode
0	Normal mode
1	Real-time output mode

DAM5	D/A converter channel 1 operating mode
0	Normal mode
1	Real-time output mode

Cautions: 1. When using the D/A converter, an alternate-function port pin should be set to the input mode, and a pull-up resistor should be disconnected.

2. Always set bits 2, 3, 6, and 7 to 0.

3. When D/A conversion is stopped, the output state is high impedance.

4. The output triggers are INTTM1 and INTTM2 for channel 0 and channel 1, respectively, in the real-time output mode.

(12) Registers controlling serial interface channel 0 (Non-Y Subseries)

The μPD78078, 78075B, and 78070A Subseries are provided with three channels of serial interfaces.
The differences among channels 0, 1, and 2 are as indicated in the table below.

Differences Among Channels 0, 1, and 2

Serial Transfer Mode		Channel 0	Channel 1	Channel 2
3-wire serial I/O	Clock selection	$f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, $f_{XX}/2^8$, external clock, TO2 output	$f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, $f_{XX}/2^8$, external clock, TO2 output	External clock, baud rate generator output
	Transfer method	MSB/LSB first switchable	MSB/LSB first switchable Automatic transmit/receive function	MSB/LSB first switchable
	Transfer end flag	Serial transfer end interrupt request flag (CSIIF0)	Serial transfer end interrupt request flag (CSIIF1)	Serial transfer end interrupt request flag (SRIF)
SBI (serial bus interface)		Use possible	None	None
2-wire serial I/O				
UART (asynchronous serial interface)		None		Use possible

The following four registers control serial interface channel 0:

- Timer clock select register 3 (TCL3)
- Serial operation mode register 0 (CSIM0)
- Serial bus interface control register (SBIC)
- Interrupt timing specification register (SINT)
- Port mode register 2 (PM2)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 3

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL3	TCL37	TCL36	TCL35	TCL34	TCL33	TCL32	TCL31	TCL30	FF43H	88H	R/W

This section controls the serial interface channel 1.
Refer to **(14) Registers controlling serial interface channel 1** or **Chapter 19** of *μPD78078, 78078Y Subseries User's Manual*, **Chapter 19** of *μPD78075B, 78075BY Subseries User's Manual*, or **Chapter 19** of *μPD78070A, 78070AY Subseries User's Manual* for detailed information.

TCL33	TCL32	TCL31	TCL30	Serial interface channel 0 serial clock selection		
					MCS = 1	MCS = 0
0	1	1	0	$f_{XX}/2$	Setting prohibited	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
Settings other than above are prohibited						

Caution: To write data other than that already written to TCL3, stop the serial transfer operation once.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of Serial Operation Mode Register 0

Symbol	<7>	<6>	<5>	4	3	2	1	0	Address	After Reset	R/W
CSIM0	CSIE0	COI	WUP	CSIM04	CSIM03	CSIM02	CSIM01	CSIM00	FF60H	00H	R/W Note 1

R/W

CSIM01	CSIM00	Serial interface channel 0 clock selection
0	x	Input clock to $\overline{\text{SCK0}}$ pin from off-chip
1	0	8-bit timer register 2 (TM2) output
1	1	Clock specified with bits 0 to 3 of timer clock select register 3 (TCL3)

R/W

CSIM 04	CSIM 03	CSIM 02	PM25	P25	PM26	P26	PM27	P27	Operation mode	Start bit	SI0/SB0/P25 pin function	SO0/SB1/P26 pin function	$\overline{\text{SCK0}}$/P27 pin function
0	x	0	Note 2 1	Note 2 x	0	0	0	1	3-wire serial I/O mode	MSB	SI0 Note 2 (Input)	SO0 (CMOS output)	$\overline{\text{SCK0}}$ (CMOS input/output)
		1								LSB			
1	0	0	Note 3 x	Note 3 x	0	0	0	1	SBI mode	MSB	P25 (CMOS input/output)	SB1 (N-ch open-drain input/output)	$\overline{\text{SCK0}}$ (CMOS input/output)
		1	0	0	Note 3 x	Note 3 x	0	1			SB0 (N-ch open-drain input/output)	P26 (CMOS input/output)	
1	1	0	Note 3 x	Note 3 x	0	0	0	1	2-wire serial I/O mode	MSB	P25 (CMOS input/output)	SB1 (N-ch open-drain input/output)	$\overline{\text{SCK0}}$ (N-ch open-drain input/output)
		1	0	0	Note 3 x	Note 3 x	0	1			SB0 (N-ch open-drain input/output)	P26 (CMOS input/output)	

R/W

WUP	Wake-up function control Note 4
0	Interrupt request signal generation with each serial transfer in any mode
1	Interrupt request signal generation when the address received after bus release (when CMDD = RELD = 1) matches the slave address register data in SBI mode

R

COI	Slave address comparison result flag Note 5
0	Slave address register not equal to serial I/O shift register 0 data
1	Slave address register equal to serial I/O shift register 0 data

R/W

CSIE0	Serial interface channel 0 operation control
0	Operation stopped
1	Operation enabled

Notes: 1. Bit 6 (COI) is a read-only bit.
2. Can be used as P25 (CMOS input/output) when serial channel used only for transmission.
3. Can be used freely as a port function when not used in SBI or 2-wire mode.
4. When using the wake-up function (WUP = 1), clear bit 5 (SIC) of the interrupt timing specification register (SINT) to 0.
5. When CSIE = 0, COI becomes 0.

Caution: Do not change the operation mode (3-wire serial I/O, 2-wire serial I/O, or SBI) while the operation of serial interface channel 0 is enabled. Stop the serial operation before changing the operation mode.

Remarks: ×: Don't care
PM××: Port mode register
P××: Port output latch

Format of Serial Bus Interface Control Register (1/2)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
SBIC	BSYE	ACKD	ACKE	ACKT	CMDD	RELD	CMDT	RELT	FF61H	00H	R/W Note

R/W

RELT	Used for bus release signal output. When RELT = 1, SO0 latch is set to 1. After SO0 latch setting, automatically cleared to 0. Also cleared to 0 when CSIE0 = 0.

R/W

CMDT	Used for command signal output. When CMDT = 1, SO0 latch is cleared to 0. After SO0 latch clearance, automatically cleared to 0. Also cleared to 0 when CSIE0 = 0.

R

RELD	Bus release detection	
Clear Conditions (RELD = 0)		Set Condition (RELD =1)
• When transfer start instruction is executed • If SIO0 and SVA values do not match in address reception • When CSIE0 = 0 • When $\overline{\text{RESET}}$ input is applied		• When bus release signal (REL) is detected

R

CMDD	Command detection	
Clear Conditions (CMDD = 0)		Set Condition (CMDD = 1)
• When transfer start instruction is executed • When bus release signal (REL) is detected • When CSIE0 = 0 • When $\overline{\text{RESET}}$ input is applied		• When command signal (CMD) is detected

R/W

ACKT	Acknowledge signal is output in synchronization with the falling edge clock of $\overline{\text{SCK0}}$ just after execution of the instruction to be set to 1, and, after acknowledge signal output, automatically cleared to 0. Used as ACKE = 0. Also cleared to 0 upon start of serial interface transfer or when CSIE0 = 0.

Note: Bits 2, 3, and 6 (RELD, CMDD, and ACKD) are read-only bits.

Remarks: Bits 0, 1, and 4 (RELT, CMDT, and ACKT) are 0 when read after data setting.
CSIE0: Bit 7 of serial operation mode register 0 (CSIM0)

Format of Serial Bus Interface Control Register (2/2)

R/W

ACKE	Acknowledge signal output control	
0	Acknowledge signal automatic output disable (output with ACKT enable)	
1	Before completion of transfer	Acknowledge signal is output in synchronization with the 9th clock falling edge of $\overline{SCK0}$ (automatically output when ACKE = 1)
	After completion of transfer	Acknowledge signal is output in synchronization with the falling edge of $\overline{SCK0}$ just after execution of the instruction to be set to 1 (automatically output when ACKE = 1). However, not automatically cleared to 0 after acknowledge signal output.

R

ACKD	Acknowledge detection	
Clear Conditions (ACKD = 0)		Set Condition (ACKD = 1)
• Falling edge of the $\overline{SCK0}$ immediately after the busy mode is released while executing the transfer start instruction • When CSIE0 = 0 • When $\overline{RESET}$ input is applied		• When acknowledge signal ($\overline{ACK}$) is detected at the rising edge of $\overline{SCK0}$ clock after completion of transfer

R/W

BSYE Note	Synchronizing busy signal output control
0	Disables busy signal which is output in synchronization with the falling edge of $\overline{SCK0}$ clock just after execution of the instruction to be cleared to 0
1	Outputs busy signal at the falling edge of $\overline{SCK0}$ clock following the acknowledge signal

Note: The busy mode can be canceled by starting a serial interface transfer. However, the BSYE flag is not cleared to 0.

Remark: CSIE0: Bit 7 of serial operation mode register 0 (CSIM0)

Format of Interrupt Timing Specification Register

Symbol	7	<6>	<5>	<4>	3	2	1	0	Address	After Reset	R/W
SINT	0	CLD	SIC	SVAM	0	0	0	0	FF63H	00H	R/W Note 1

R/W

SVAM	SVA bit to be used as slave address
0	Bits 0 to 7
1	Bits 1 to 7

R/W

SIC	INTCSI0 interrupt cause selection Note 2
0	CSIIF0 is set upon termination of serial interface channel 0 transfer
1	CSIIF0 is set upon bus release detection or termination of serial interface channel 0 transfer

R

CLD	$\overline{SCK0}$/P27 pin level Note 3
0	Low level
1	High level

Notes: 1. Bit 6 (CLD) is a read-only bit.
2. When using the wake-up function in the SBI mode, set SIC to 0.
3. When CSIE0 = 0, CLD becomes 0.

Caution: Be sure to set bits 0 to 3 to 0.

Remarks: SVA: Slave address register
CSIIF0: Interrupt request flag for INTCSI0
CSIE0: Bit 7 of serial operation mode register 0

(13) Registers controlling serial interface channel 0 (Y Subseries)

The μPD78078Y, 78075BY, and 78070AY Subseries are provided with three channels of serial interfaces. The differences among channels 0, 1, and 2 are as indicated in the table below.

Differences Among Channels 0, 1, and 2

Serial Transfer Mode		Channel 0	Channel 1	Channel 2
3-wire serial I/O	Clock selection	$f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, $f_{XX}/2^8$, external clock, TO2 output	$f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, $f_{XX}/2^8$, external clock, TO2 output	External clock, baud rate generator output
	Transfer method	MSB/LSB first switchable	MSB/LSB first switchable Automatic transmit/receive function	MSB/LSB first switchable
	Transfer end flag	Serial transfer end interrupt request flag (CSIIF0)	Serial transfer end interrupt request flag (CSIIF1)	Serial transfer end interrupt request flag (SRIF)
I^2C bus (inter-IC bus)		Use possible	None	None
2-wire serial I/O				
UART (asynchronous serial interface)		None		Use possible

The following four registers control serial interface channel 0:

- Timer clock select register 3 (TCL3)
- Serial operation mode register 0 (CSIM0)
- Serial bus interface control register (SBIC)
- Interrupt timing specification register (SINT)
- Port mode register 2 (PM2)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 3

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL3	TCL37	TCL36	TCL35	TCL34	TCL33	TCL32	TCL31	TCL30	FF43H	88H	R/W

This section controls the serial interface channel 1.
Refer to **(14) Registers controlling serial interface channel 1** or **Chapter 19** of *μPD78078, 78078Y Subseries User's Manual*, **Chapter 19** of *μPD78075B, 78075BY Subseries User's Manual*, or **Chapter 19** of *μPD78070A, 78070AY Subseries User's Manual* for detailed information.

TCL33	TCL32	TCL31	TCL30	Serial interface channel 0 serial clock selection					
				Serial clock in I^2C bus mode			Serial clock in 2-wire or 3-wire serial I/O mode		
					MCS = 1	MCS = 0		MCS = 1	MCS = 0
0	1	1	0	$f_{XX}/2^5$	Setting prohibited	$f_X/2^6$ (78.1 kHz)	$f_{XX}/2$	Setting prohibited	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.77 kHz)	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_{XX}/2^9$	$f_X/2^9$ (9.77 kHz)	$f_X/2^{10}$ (4.88 kHz)	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_{XX}/2^{10}$	$f_X/2^{10}$ (4.88 kHz)	$f_X/2^{11}$ (2.44 kHz)	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_{XX}/2^{11}$	$f_X/2^{11}$ (2.44 kHz)	$f_X/2^{12}$ (1.22 kHz)	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_{XX}/2^{12}$	$f_X/2^{12}$ (1.22 kHz)	$f_X/2^{13}$ (0.61 kHz)	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
Settings other than above are prohibited									

Caution: To write data other than that written to TCL3, stop the serial transfer operation once.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of Serial Operation Mode Register 0

Symbol	<7>	<6>	<5>	4	3	2	1	0	Address	After Reset	R/W
CSIM0	CSIE0	COI	WUP	CSIM04	CSIM03	CSIM02	CSIM01	CSIM00	FF60H	00H	R/W Note 1

R/W

CSIM01	CSIM00	Serial interface channel 0 clock selection
0	x	Input clock to $\overline{SCK0}$/SCL pin from off chip
1	0	8-bit timer register 2 (TM2) output Note 2
1	1	Clock specified with bits 0 to 3 of timer clock select register 3 (TCL3)

R/W

CSIM 04	CSIM 03	CSIM 02	PM25	P25	PM26	P26	PM27	P27	Operation mode	Start bit	SI0/SB0/SDA0/ P25 pin function	SO0/SB1/SDA1/ P26 pin function	$\overline{SCK0}$/SCL/P27 pin function
0	x	0	Note 3 1	Note 3 x	0	0	0	1	3-wire serial I/O mode	MSB	SI0 Note 3 (Input)	SO0 (CMOS output)	$\overline{SCK0}$ (CMOS input/output)
		1								LSB			
1	1	0	Note 4 x	Note 4 x	0	0	0	1	2-wire serial I/O mode or I^2C bus mode	MSB	P25 (CMOS input/output)	SB1/SDA1 (N-ch open-drain input/output)	$\overline{SCK0}$/SCL (N-ch open-drain input/output)
		1	0	0	Note 4 x	Note 4 x	0	1			SB0/SDA0 (N-ch open-drain input/output)	P26 (CMOS input/output)	

R/W

WUP	Wake-up function control Note 5
0	Interrupt request signal generation with each serial transfer in any mode
1	Interrupt request signal generation when the address received after detecting start condition (when CMDD = 1) matches the slave address register (SVA) data in I^2C bus mode

R

COI	Slave address comparison result flag Note 6
0	Slave address register (SVA) not equal to serial I/O shift register 0 (SIO0) data
1	Slave address register (SVA) equal to serial I/O shift register 0 (SIO0) data

R/W

CSIE0	Serial interface channel 0 operation control
0	Operation stopped
1	Operation enabled

Notes: 1. Bit 6 (COI) is a read-only bit.
2. I^2C bus mode, the clock frequency becomes 1/16 of that output from TO2.
3. Can be used as P25 (CMOS input/output) when serial channel used only for transmission.
4. Can be used freely as a port function when not used in SBI or 2-wire mode.
5. When using the wake-up function (WUP = 1), set bit 5 (SIC) of the interrupt timing specification register (SINT) to 1. Do not execute an instruction that writes the serial I/O shift register 0 (SIO0) while WUP = 1.
6. When CSIE0 = 0, COI becomes 0.

Caution: Do not change the operation mode (3-wire serial I/O, 2-wire serial I/O, or I^2C bus) while the operation of serial interface channel 0 is enabled. Stop the serial operation before changing the operation mode.

Remark: ×: Don't care

Format of Serial Bus Interface Control Register (1/2)

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
SBIC	BSYE	ACKD	ACKE	ACKT	CMDD	RELD	CMDT	RELT	FF61H	00H	R/W Note

R/W

RELT	Used for stop condition signal output. When RELT = 1, SO0 latch is set to 1. After SO0 latch setting, automatically cleared to 0. Also cleared to 0 when CSIE0 = 0.

R/W

CMDT	Used for start condition signal output. When CMDT = 1, SO0 latch is cleared to 0. After SO0 latch clearance, automatically cleared to 0. Also cleared to 0 when CSIE0 = 0.

R

RELD	Stop condition detection	
Clear Conditions (RELD = 0)		Set Condition (RELD = 1)
• When transfer start instruction is executed • If SIO0 and SVA values do not match in address reception • When CSIE0 = 0 • When $\overline{\text{RESET}}$ input is applied		• When stop condition signal is detected

R

CMDD	Start condition detection	
Clear Conditions (CMDD = 0)		Set Condition (CMDD = 1)
• When transfer start instruction is executed • When stop condition signal is detected • When CSIE0 = 0 • When $\overline{\text{RESET}}$ input is applied		• When start condition signal is detected

R/W

ACKT	Used to generate the $\overline{\text{ACK}}$ signal by software when the 8-clock wait mode is selected. Keeps SDA0 (SDA1) low from set instruction (ACKT = 1) execution to the next falling edge of SCL. Also cleared to 0 upon start of a serial interface transfer or when CSIE0 = 0.

Note: Bits 2, 3, and 6 (RELD, CMDD, and ACKD) are read-only bits.

Remark: CSIE0: Bit 7 of serial operation mode register 0 (CSIM0)

Format of Serial Bus Interface Control Register (2/2)

R/W

ACKE	Acknowledge signal output control [Note 1]
0	Disables acknowledge signal automatic output (however, output with ACKT is enabled). Used for reception when the 8-clock wait mode is selected or for transmission. [Note 2]
1	Enables acknowledge signal automatic output. Outputs acknowledge signal in synchronization with the falling edge of the 9th SCL clock cycle (automatically output when ACKE = 1). However, not automatically cleared to 0 after acknowledge signal output. Used in reception with the 9-clock wait mode selected.

R

ACKD	Acknowledge detection	
Clear Conditions (ACKD = 0)		Set Condition (ACKD = 1)
• While executing the transfer start instruction • When CSIE0 = 0 • When $\overline{\text{RESET}}$ input is applied		• When acknowledge signal ($\overline{\text{ACK}}$) is detected at the rising edge of SCL clock after completion of transfer

R/W

BSYE [Note 3]	Control of N-ch open-drain output for transmission in I^2C bus mode [Note 4]
0	Output enabled (transmission)
1	Output disabled (reception)

Notes: 1. Setting should be performed before transfer.

2. If an 8-clock wait mode is selected, the acknowledge signal at reception time must be output using ACKT.
3. The busy mode can be canceled by start of a serial interface transfer or reception of an address signal. However, the BSYE flag is not cleared to 0.
4. When using the wake-up function, be sure to set the BSYE to 1.

Remark: CSIE0: Bit 7 of serial operation mode register 0 (CSIM0)

Format of Interrupt Timing Specification Register (1/2)

Symbol	7	<6>	<5>	<4>	<3>	<2>	1	0	Address	After Reset	R/W
SINT	0	CLD	SIC	SVAM	CLC	WREL	WAT1	WAT0	FF63H	00H	R/W Note 1

R/W

WAT1	WAT0	Wait and interrupt control
0	0	Generates interrupt service request at the rising edge of the 8th $\overline{SCK0}$ clock cycle (keeping clock output in high impedance)
0	1	Setting prohibited
1	0	Used in I^2C bus mode (8-clock wait). Generates interrupt service request at the rising edge of the 8th $\overline{SCK0}$ clock cycle. (In the case of a master device, makes SCL output low to enter the wait state after 8 clock pulses are output. In the case of a slave device, makes SCL output low to request a wait state after 8 clock pulses are input.)
1	1	Used in I^2C bus mode (9-clock wait). Generates an interrupt service request at the rising edge of the 9th $\overline{SCK0}$ clock cycle. (In the case of a master device, makes SCL output low to enter the wait state after 9 clock pulses are output. In the case of a slave device, makes SCL output low to request a wait state after 9 clock pulses are input.)

R/W

WREL	Wait state cancellation control
0	Wait state has been canceled.
1	Cancels wait state. Automatically cleared to 0 when the state is canceled. (Used to cancel wait state by means of WAT0 and WAT1.)

R/W

CLC	Clock level control Note 2
0	Used in I^2C bus mode. Make output level of SCL pin low unless serial transfer is being performed.
1	Used in I^2C bus mode. Make SCL pin enter high-impedance state unless serial transfer is being performed (except for clock line, which is kept high). Used to enable master device to generate start condition and stop condition signals.

Notes: 1. Bit 6 (CLD) is a read-only bit.
2. When not using the I^2C mode, set CLC to 0.

Format of Interrupt Timing Specification Register (2/2)

R/W

SVAM	SVA bit to be used as slave address
0	Bits 0 to 7
1	Bits 1 to 7

R/W

SIC	INTCSI0 interrupt cause selection Note 1
0	CSIIF0 is set to 1 upon termination of serial interface channel 0 transfer
1	CSIIF0 is set to 1 upon stop condition detection or termination of serial interface channel 0 transfer

R

CLD	$\overline{\text{SCK0}}$/SCL pin level Note 2
0	Low level
1	High level

Notes: 1. When using wake-up function in the I^2C mode, set SIC to 0.

2. When CSIE = 0, CLD becomes 0.

Remarks: SVA: Slave address register

CSIIF0: Interrupt request flag for INTCSI0

CSIE0: Bit 7 of serial operation mode register 0 (CSIM0)

(14) Registers controlling serial interface channel 1

The following four registers control serial interface channel 1:

- Timer clock select register 3 (TCL3)
- Serial operation mode register 1 (CSIM1)
- Automatic data transmit/receive control register (ADTC)
- Automatic data transmit/receive time interval specification register (ADTI)

Format of Timer Clock Select Register 3

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL3	TCL37	TCL36	TCL35	TCL34	TCL33	TCL32	TCL31	TCL30	FF43H	88H	R/W

This section controls the serial interface channel 0.
Refer to **(12) Registers controlling serial interface channel 0 (Non-Y Subseries)**, **(13) Registers controlling serial interface channel 0 (Y Subseries)** or
Chapters 17 and 18 of *μPD78078, 78078Y Subseries User's Manual*,
Chapters 17 and 18 of *μPD78075B, 78075BY Subseries User's Manual*, or
Chapters 17 and 18 of *μPD78070A, 78070AY Subseries User's Manual*
for detailed information.

TCL37	TCL36	TCL35	TCL34	Serial interface channel 1 serial clock selection		
					MCS = 1	MCS = 0
0	1	1	0	$f_{XX}/2$	Setting prohibited	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
Settings other than above are prohibited						

Caution: When rewriting TCL3 to other data, stop the serial transfer operation beforehand.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of Serial Operation Mode Register 1

Symbol	<7>	6	<5>	4	3	2	1	0	Address	After Reset	R/W
CSIM1	CSIE1	DIR	ATE	0	0	0	CSIM11	CSIM10	FF68H	00H	R/W

CSIM11	CSIM10	Serial interface channel 1 clock selection
0	x	Clock externally input to $\overline{\text{SCK1}}$ pin Note 1
1	0	8-bit timer register 2 (TM2) output
1	1	Clock specified with bits 4 to 7 of timer clock select register 3 (TCL3)

ATE	Serial interface channel 1 operating mode selection
0	3-wire serial I/O mode
1	3-wire serial I/O mode with automatic transmit/receive function

DIR	Start bit	SI1 pin function	SO1 pin function
0	MSB	SI1/P20 (Input)	SO1 (CMOS output)
1	LSB		

CSIE1	CSIM11	PM20	P20	PM21	P21	PM22	P22	Shift register 1 operation	Serial clock counter operation control	SI1/P20 pin function	SO1/P21 pin function	$\overline{\text{SCK1}}$/P22 pin function
0	x	Note 2 x	Note 2 x	Note 2 x	Note 2 x	Note 2 x	Note 2 x	Operation stop	Clear	P20 (CMOS input/output)	P21 (CMOS input/output)	P22 (CMOS input/output)
1	0	Note 3 1	Note 3 x	0	0	1	x	Operation enable	Count operation	SI1 Note 3 (Input)	SO1 (CMOS output)	$\overline{\text{SCK1}}$ (Input)
	1					0	1					$\overline{\text{SCK1}}$ (CMOS output)

Notes: 1. If the external clock input has been selected with CSIM11 set to 0, set bit 1 (BUSY1) and bit 2 (STRB) of the automatic data transmit/receive control register (ADTC) to 0, 0.

2. Can be used freely as a port function if input or output modes are not used by the serial port.
3. Can be used as P20 (CMOS input/output) when serial channel performs transmission only (clear bit 7 (RE) of ADTC to 0).

Remarks: ×: Don't care
PM××: Port mode register
P××: Port output latch

Format of Automatic Data Transmit/Receive Control Register

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
ADTC	RE	ARLD	ERCE	ERR	TRF	STRB	BUSY1	BUSY0	FF69H	00H	R/W Note 1

R/W

BUSY1	BUSY0	Busy input control
0	x	Not using busy input
1	0	Busy input enable (active high)
1	1	Busy input enable (active low)

R/W

STRB	Strobe output control
0	Strobe output disable
1	Strobe output enable

R

TRF	Status in automatic transmit/receive function Note 2
0	Detection of termination of automatic transmission/ reception. (This bit is set to 0 upon suspension of automatic transmission/reception or when ARLD = 0.)
1	During automatic transmission/reception. (This bit is set to 1 when data is written to SIO1.)

R

ERR	Error detection in automatic transmit/receive function
0	No error (set to 0 when data is written to SIO1)
1	Error occurred

R/W

ERCE	Error check in automatic transmit/receive function
0	Error check disable
1	Error check enable (only when BUSY1 = 1)

R/W

ARLD	Operating mode for automatic transmit/receive function
0	Single operating mode
1	Repetitive operating mode

R/W

RE	Receive operation in automatic transmit/receive function
0	Receive disable
1	Receive enable

Notes: 1. Bits 3 and 4 (TRF and ERR) are read-only bits.

2. The termination of automatic transmission/reception should be judged by using TRF, not CSIIF1 (interrupt request flag).

Caution: When an external clock input is selected by setting bit 1 (CSIM11) of serial operating mode register 1 (CSIM1) to 0, set STRB and BUSY1 of ADTC to 0, 0.

Remark: ×: Don't care

Format of Automatic Data Transmit/Receive Interval Time Specification Register (1/4)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADTI	ADTI7	0	0	ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	FF6BH	00H	R/W

ADTI7	Data transfer interval control
0	No control of interval by ADTI Note 1
1	Control of interval by ADTI (ADTI0 to ADTI4)

ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	Data transfer interval specification (f_{XX} = 5.0-MHz operation)	
					Minimum Note 2	Maximum Note 2
0	0	0	0	0	18.4 μs + 0.5/f_{SCK}	20.0 μs + 1.5/f_{SCK}
0	0	0	0	1	31.2 μs + 0.5/f_{SCK}	32.8 μs + 1.5/f_{SCK}
0	0	0	1	0	44.0 μs + 0.5/f_{SCK}	45.6 μs + 1.5/f_{SCK}
0	0	0	1	1	56.8 μs + 0.5/f_{SCK}	58.4 μs + 1.5/f_{SCK}
0	0	1	0	0	69.6 μs + 0.5/f_{SCK}	71.2 μs + 1.5/f_{SCK}
0	0	1	0	1	82.4 μs + 0.5/f_{SCK}	84.0 μs + 1.5/f_{SCK}
0	0	1	1	0	95.2 μs + 0.5/f_{SCK}	96.8 μs + 1.5/f_{SCK}
0	0	1	1	1	108.0 μs + 0.5/f_{SCK}	109.6 μs + 1.5/f_{SCK}
0	1	0	0	0	120.8 μs + 0.5/f_{SCK}	122.4 μs + 1.5/f_{SCK}
0	1	0	0	1	133.6 μs + 0.5/f_{SCK}	135.2 μs + 1.5/f_{SCK}
0	1	0	1	0	146.4 μs + 0.5/f_{SCK}	148.0 μs + 1.5/f_{SCK}
0	1	0	1	1	159.2 μs + 0.5/f_{SCK}	160.8 μs + 1.5/f_{SCK}
0	1	1	0	0	172.0 μs + 0.5/f_{SCK}	173.6 μs + 1.5/f_{SCK}
0	1	1	0	1	184.8 μs + 0.5/f_{SCK}	186.4 μs + 1.5/f_{SCK}
0	1	1	1	0	197.6 μs + 0.5/f_{SCK}	199.2 μs + 1.5/f_{SCK}
0	1	1	1	1	210.4 μs + 0.5/f_{SCK}	212.0 μs + 1.5/f_{SCK}

Notes: 1. The interval is dependent only on CPU processing.

2. The data transfer interval includes an error. The data transfer minimum and maximum intervals are found from the following expressions (n: Value set in ADTI0 to ADTI4). However, if a minimum calculated by the following expressions is smaller than 2/f_{SCK}, the minimum interval time is 2/f_{SCK}.

$$\text{Minimum} = (n + 1) \times \frac{2^6}{f_{XX}} + \frac{28}{f_{XX}} + \frac{0.5}{f_{SCK}}$$

$$\text{Maximum} = (n + 1) \times \frac{2^6}{f_{XX}} + \frac{36}{f_{XX}} + \frac{1.5}{f_{SCK}}$$

Cautions: 1. Do not write data to ADTI during operation of the automatic data transmit/receive function.

2. Be sure to set bits 5 and 6 to 0.

3. While ADTI is used to control the interval time for data transfer by the automatic data transmit/receive function, busy control is invalid.

Remarks: f_{XX}: Main system clock frequency (f_X or f_X/2)

f_X: Main system clock oscillation frequency

f_{SCK}: Serial clock frequency

Format of Automatic Data Transmit/Receive Interval Time Specification Register (2/4)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADTI	ADTI7	0	0	ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	FF6BH	00H	R/W

ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	Data transfer interval specification (f_{XX} = 5.0-MHz operation)	
					Minimum Note	Maximum Note
1	0	0	0	0	223.2 μs + 0.5/f_{SCK}	224.8 μs + 1.5/f_{SCK}
1	0	0	0	1	236.0 μs + 0.5/f_{SCK}	237.6 μs + 1.5/f_{SCK}
1	0	0	1	0	248.8 μs + 0.5/f_{SCK}	250.4 μs + 1.5/f_{SCK}
1	0	0	1	1	261.6 μs + 0.5/f_{SCK}	263.2 μs + 1.5/f_{SCK}
1	0	1	0	0	274.4 μs + 0.5/f_{SCK}	276.0 μs + 1.5/f_{SCK}
1	0	1	0	1	287.2 μs + 0.5/f_{SCK}	288.8 μs + 1.5/f_{SCK}
1	0	1	1	0	300.0 μs + 0.5/f_{SCK}	301.6 μs + 1.5/f_{SCK}
1	0	1	1	1	312.8 μs + 0.5/f_{SCK}	314.4 μs + 1.5/f_{SCK}
1	1	0	0	0	325.6 μs + 0.5/f_{SCK}	327.2 μs + 1.5/f_{SCK}
1	1	0	0	1	338.4 μs + 0.5/f_{SCK}	340.0 μs + 1.5/f_{SCK}
1	1	0	1	0	351.2 μs + 0.5/f_{SCK}	352.8 μs + 1.5/f_{SCK}
1	1	0	1	1	364.0 μs + 0.5/f_{SCK}	365.6 μs + 1.5/f_{SCK}
1	1	1	0	0	376.8 μs + 0.5/f_{SCK}	378.4 μs + 1.5/f_{SCK}
1	1	1	0	1	389.6 μs + 0.5/f_{SCK}	391.2 μs + 1.5/f_{SCK}
1	1	1	1	0	402.4 μs + 0.5/f_{SCK}	404.0 μs + 1.5/f_{SCK}
1	1	1	1	1	415.2 μs + 0.5/f_{SCK}	416.8 μs + 1.5/f_{SCK}

Note: The data transfer interval includes an error. The data transfer minimum and maximum intervals are found from the following expressions (n: Value set in ADTI0 to ADTI4). However, if a minimum calculated by the following expressions is smaller than 2/f_{SCK}, the minimum interval time is 2/f_{SCK}.

$$\text{Minimum} = (n + 1) \times \frac{2^6}{f_{XX}} + \frac{28}{f_{XX}} + \frac{0.5}{f_{SCK}}$$

$$\text{Maximum} = (n + 1) \times \frac{2^6}{f_{XX}} + \frac{36}{f_{XX}} + \frac{1.5}{f_{SCK}}$$

Cautions: 1. Do not write data to ADTI during operation of the automatic data transmit/receive function.

2. Be sure to set bits 5 and 6 to 0.

3. While ADTI is used to control the interval time for data transfer by the automatic data transmit/receive function, busy control is invalid.

Remarks: f_{XX}: Main system clock frequency (f_X or f_X/2)

f_X: Main system clock oscillation frequency

f_{SCK}: Serial clock frequency

Format of Automatic Data Transmit/Receive Interval Time Specification Register (3/4)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADTI	ADTI7	0	0	ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	FF6BH	00H	R/W

ADTI7	Data transfer interval control
0	No control of interval by ADTI Note 1
1	Control of interval by ADTI (ADTI0 to ADTI4)

ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	Data transfer interval specification (f_{XX} = 2.5-MHz operation)	
					Minimum Note 2	Maximum Note 2
0	0	0	0	0	36.8 μs + 0.5/f_{SCK}	40.0 μs + 1.5/f_{SCK}
0	0	0	0	1	62.4 μs + 0.5/f_{SCK}	65.6 μs + 1.5/f_{SCK}
0	0	0	1	0	88.0 μs + 0.5/f_{SCK}	91.2 μs + 1.5/f_{SCK}
0	0	0	1	1	113.6 μs + 0.5/f_{SCK}	116.8 μs + 1.5/f_{SCK}
0	0	1	0	0	139.2 μs + 0.5/f_{SCK}	142.4 μs + 1.5/f_{SCK}
0	0	1	0	1	164.8 μs + 0.5/f_{SCK}	168.0 μs + 1.5/f_{SCK}
0	0	1	1	0	190.4 μs + 0.5/f_{SCK}	193.6 μs + 1.5/f_{SCK}
0	0	1	1	1	216.0 μs + 0.5/f_{SCK}	219.2 μs + 1.5/f_{SCK}
0	1	0	0	0	241.6 μs + 0.5/f_{SCK}	244.8 μs + 1.5/f_{SCK}
0	1	0	0	1	267.2 μs + 0.5/f_{SCK}	270.4 μs + 1.5/f_{SCK}
0	1	0	1	0	292.8 μs + 0.5/f_{SCK}	296.0 μs + 1.5/f_{SCK}
0	1	0	1	1	318.4 μs + 0.5/f_{SCK}	321.6 μs + 1.5/f_{SCK}
0	1	1	0	0	344.0 μs + 0.5/f_{SCK}	347.2 μs + 1.5/f_{SCK}
0	1	1	0	1	369.6 μs + 0.5/f_{SCK}	372.8 μs + 1.5/f_{SCK}
0	1	1	1	0	395.2 μs + 0.5/f_{SCK}	398.4 μs + 1.5/f_{SCK}
0	1	1	1	1	420.8 μs + 0.5/f_{SCK}	424.0 μs + 1.5/f_{SCK}

Notes: 1. The interval is dependent only on CPU processing.

2. The data transfer interval includes an error. The data transfer minimum and maximum intervals are found from the following expressions (n: Value set in ADTI0 to ADTI4). However, if a minimum calculated by the following expressions is smaller than 2/f_{SCK}, the minimum interval time is 2/f_{SCK}.

$$\text{Minimum} = (n+1) \times \frac{2^6}{f_{XX}} + \frac{28}{f_{XX}} + \frac{0.5}{f_{SCK}}, \quad \text{Maximum} = (n+1) \times \frac{2^6}{f_{XX}} + \frac{36}{f_{XX}} + \frac{1.5}{f_{SCK}}$$

Cautions: 1. Do not write data to ADTI during operation of the automatic data transmit/receive function.

2. Be sure to set bits 5 and 6 to 0.

3. While ADTI is used to control the interval time for data transfer by the automatic data transmit/receive function, busy control is invalid.

Remarks: f_{XX}: Main system clock frequency (f_X or f_X/2)

f_X: Main system clock oscillation frequency

f_{SCK}: Serial clock frequency

Format of Automatic Data Transmit/Receive Interval Time Specification Register (4/4)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADTI	ADTI7	0	0	ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	FF6BH	00H	R/W

ADTI4	ADTI3	ADTI2	ADTI1	ADTI0	Data transfer interval specification (f_{XX} = 2.5-MHz operation)	
					Minimum [Note]	Maximum [Note]
1	0	0	0	0	446.4 μs + 0.5/f_{SCK}	449.6 μs + 1.5/f_{SCK}
1	0	0	0	1	472.0 μs + 0.5/f_{SCK}	475.2 μs + 1.5/f_{SCK}
1	0	0	1	0	497.6 μs + 0.5/f_{SCK}	500.8 μs + 1.5/f_{SCK}
1	0	0	1	1	523.2 μs + 0.5/f_{SCK}	526.4 μs + 1.5/f_{SCK}
1	0	1	0	0	548.8 μs + 0.5/f_{SCK}	552.0 μs + 1.5/f_{SCK}
1	0	1	0	1	574.4 μs + 0.5/f_{SCK}	577.6 μs + 1.5/f_{SCK}
1	0	1	1	0	600.0 μs + 0.5/f_{SCK}	603.2 μs + 1.5/f_{SCK}
1	0	1	1	1	625.6 μs + 0.5/f_{SCK}	628.8 μs + 1.5/f_{SCK}
1	1	0	0	0	651.2 μs + 0.5/f_{SCK}	654.4 μs + 1.5/f_{SCK}
1	1	0	0	1	676.8 μs + 0.5/f_{SCK}	680.0 μs + 1.5/f_{SCK}
1	1	0	1	0	702.4 μs + 0.5/f_{SCK}	705.6 μs + 1.5/f_{SCK}
1	1	0	1	1	728.0 μs + 0.5/f_{SCK}	731.2 μs + 1.5/f_{SCK}
1	1	1	0	0	753.6 μs + 0.5/f_{SCK}	756.8 μs + 1.5/f_{SCK}
1	1	1	0	1	779.2 μs + 0.5/f_{SCK}	782.4 μs + 1.5/f_{SCK}
1	1	1	1	0	804.8 μs + 0.5/f_{SCK}	808.0 μs + 1.5/f_{SCK}
1	1	1	1	1	830.4 μs + 0.5/f_{SCK}	833.6 μs + 1.5/f_{SCK}

Note: The data transfer interval includes an error. The data transfer minimum and maximum intervals are found from the following expressions (n: Value set in ADTI0 to ADTI4). However, if a minimum calculated by the following expressions is smaller than 2/f_{SCK}, the minimum interval time is 2/f_{SCK}.

$$\text{Minimum} = (n + 1) \times \frac{2^6}{f_{XX}} + \frac{28}{f_{XX}} + \frac{0.5}{f_{SCK}}$$

$$\text{Maximum} = (n + 1) \times \frac{2^6}{f_{XX}} + \frac{36}{f_{XX}} + \frac{1.5}{f_{SCK}}$$

Cautions: 1. Do not write data to ADTI during operation of the automatic data transmit/receive function.

2. Be sure to set bits 5 and 6 to 0.

3. While ADTI is used to control the interval time for data transfer by the automatic data transmit/receive function, busy control is invalid.

Remarks: f_{XX}: Main system clock frequency (f_X or f_X/2)

f_X: Main system clock oscillation frequency

f_{SCK}: Serial clock frequency

(15) Registers controlling serial interface channel 2

The following four registers control serial interface channel 2:

- Serial operation mode register 2 (CSIM2)
- Asynchronous serial interface mode register (ASIM)
- Asynchronous serial interface status register (ASIS)
- Baud rate generator control register (BRGC)
- Port mode register 7 (PM7)
  - Refer to section (1) for the register format.

Format of Serial Operation Mode Register 2

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
CSIM2	CSIE2	0	0	0	0	CSIM22	CSCK	0	FF72H	00H	R/W

CSCK	Clock selection in 3-wire serial I/O mode
0	Input clock from off-chip to $\overline{SCK2}$ pin
1	Dedicated baud rate generator output

CSIM22	First bit specification
0	MSB
1	LSB

CSIE2	Operation control in 3-wire serial I/O mode
0	Operation stopped
1	Operation enabled

Cautions: 1. Ensure that bits 0 and 3 through 6 are set to 0.

2. When UART mode is selected, CSIM2 should be set to 00H.

Format of Asynchronous Serial Interface Mode Register

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After Reset	R/W
ASIM	TXE	RXE	PS1	PS0	CL	SL	ISRM	SCK	FF70H	00H	R/W

SCK	Clock in asynchronous serial interface mode
0	Input clock from off chip to ASCK pin
1	Dedicated baud rate generator output Note

ISRM	Control of reception completion interrupt in case of error generation
0	Reception completion interrupt request generated in case of error generation
1	Reception completion interrupt request not generated in case of error generation

SL	Transmit data stop bit length specification
0	1 bit
1	2 bits

CL	Character length specification
0	7 bits
1	8 bits

PS1	PS0	Parity bit specification
0	0	No parity
0	1	0 parity always added in transmission. No parity test in reception (parity error not generated).
1	0	Odd parity
1	1	Even parity

RXE	Receive operation control
0	Receive operation stopped
1	Receive operation enabled

TXE	Transmit operation control
0	Transmit operation stopped
1	Transmit operation enabled

Note: When SCK is set to 1 and the baud rate generator output is selected, the ASCK pin can be used as an input/output port.

Cautions: 1. When the 3-wire serial I/O mode is selected, 00H should be set in ASIM.

2. The serial transmit/receive operation must be stopped before changing the operating mode.

Format of Asynchronous Serial Interface Status Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ASIS	0	0	0	0	0	PE	FE	OVE	FF71H	00H	R

OVE	Overrun error flag
0	Overrun error not generated
1	Overrun error generated Note 1 (When next receive operation is completed before data from receive buffer register is read)

FE	Framing error flag
0	Framing error not generated
1	Framing error generated Note 2 (When stop bit is not detected)

PE	Parity error flag
0	Parity error not generated
1	Parity error generated (When transmit data parity does not match)

Notes: 1. The receive buffer register (RXB) must be read when an overrun error is generated. Overrun errors will continue to be generated until RXB is read.

2. Even if the stop bit length has been set as 2 bits by bit 2 (SL) of the asynchronous serial interface mode register (ASIM), only single stop bit detection is performed during reception.

Format of Baud Rate Generator Control Register (1/2)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
BRGC	TPS3	TPS2	TPS1	TPS0	MDL3	MDL2	MDL1	MDL0	FF73H	00H	R/W

MDL3	MDL2	MDL1	MDL0	Baud rate generator input clock selection	k
0	0	0	0	$f_{SCK}/16$	0
0	0	0	1	$f_{SCK}/17$	1
0	0	1	0	$f_{SCK}/18$	2
0	0	1	1	$f_{SCK}/19$	3
0	1	0	0	$f_{SCK}/20$	4
0	1	0	1	$f_{SCK}/21$	5
0	1	1	0	$f_{SCK}/22$	6
0	1	1	1	$f_{SCK}/23$	7
1	0	0	0	$f_{SCK}/24$	8
1	0	0	1	$f_{SCK}/25$	9
1	0	1	0	$f_{SCK}/26$	10
1	0	1	1	$f_{SCK}/27$	11
1	1	0	0	$f_{SCK}/28$	12
1	1	0	1	$f_{SCK}/29$	13
1	1	1	0	$f_{SCK}/30$	14
1	1	1	1	f_{SCK} **Note**	

Note: Can only be used in 3-wire serial I/O mode.

Remarks: f_{SCK}: 5-bit counter source clock
k: Value set in MDL0 to MDL3 ($0 \leq k \leq 14$)

Format of Baud Rate Generator Control Register (2/2)

TPS3	TPS2	TPS1	TPS0	5-bit counter source clock selection			n
					MCS = 1	MCS = 0	
0	0	0	0	$f_{XX}/2^{10}$	$f_{XX}/2^{10}$ (4.9 kHz)	$f_X/2^{11}$ (2.4 kHz)	11
0	1	0	1	f_{XX}	f_X (5.0 MHz)	$f_X/2$ (2.5 MHz)	1
0	1	1	0	$f_{XX}/2$	$f_X/2$ (2.5 MHz)	$f_X/2^2$ (1.25 MHz)	2
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)	3
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)	4
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)	5
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)	6
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)	7
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)	8
1	1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)	9
1	1	1	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)	10
Settings other than above are prohibited							

Caution: When a write is performed to BRGC during a communication operation, baud rate generator output is disrupted and communication cannot be performed normally. Therefore, BRGC must not be written to during a communication operation.

Remarks: f_X: Main system clock oscillation frequency

f_{XX}: Main system clock frequency (f_X or $f_X/2$)

MCS: Bit 0 of oscillation mode select register (OSMS)

n: Value set in TPS0 to TPS3 ($1 \leq n \leq 11$)

Values in parentheses apply to operation with f_X = 5.0 MHz.

(16) Registers controlling real-time output port

The following three registers control the real-time output port:

- Port mode register 12 (PM12)
  - Refer to section (1) for the register format.
- Real-time output port mode register (RTPM)
- Real-time output port control register (RTPC)

Format of Real-Time Output Port Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
RTPM	RTPM7	RTPM6	RTPM5	RTPM4	RTPM3	RTPM2	RTPM1	RTPM0	FF34H	00H	R/W

RTPMn	Real-time output port selection (n = 0 to 7)
0	Port mode
1	Real-time output port mode

Cautions: 1. When using these bits as a real-time output port, set the ports to which real-time output is performed to the output mode (clear the corresponding bit of port mode register 12 (PM12) to 0).

2. In the port specified as a real-time output port, data cannot be set to the output latch. Therefore, when setting an initial value, data should be set to the output latch before setting the real-time output mode.

Format of Real-Time Output Port Control Register

Symbol	7	6	5	4	3	2	<1>	<0>	Address	After Reset	R/W
RTPC	0	0	0	0	0	0	BYTE	EXTR	FF36H	00H	R/W

EXTR	Real-time output control by INTP2
0	INTP2 not specified as real-time output trigger
1	INTP2 specified as real-time output trigger

BYTE	Real-time output port operating mode
0	4 bits x 2 channels
1	8 bits x 1 channel

(17) Registers controlling interrupt function

A total of 24 interrupt sources are provided for the μPD7807x Subseries, including non-maskable, maskable, and software interrupts.

Table 6-28. Interrupt Source List

Interrupt Type	Default Priority[Note]	Interrupt Source		Internal/ External	Vector Table Address
		Name	Trigger		
Non-maskable	—	RESET	Low voltage level	External	0000H
		INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)		
	1	INTP0	Pin input edge detection	External	0006H
	2	INTP1			0008H
	3	INTP2			000AH
	4	INTP3			000CH
	5	INTP4			000EH
	6	INTP5			0010H
	7	INTP6			0012H
	8	INTCSI0	End of serial interface channel 0 transfer	Internal	0014H
	9	INTCSI1	End of serial interface channel 1 transfer		0016H
	10	INTSER	Serial interface channel 2 UART reception error generation		0018H
	11	INTSR	End of serial interface channel 2 UART reception		001AH
		INTCSI2	End of serial interface channel 2 3-wire transfer		
	12	INTST	End of serial interface channel 2 UART transmission		001CH
	13	INTTM3	Reference time interval signal from watch timer		001EH
	14	INTTM00	Generation of 16-bit timer register and capture/ compare register 00 (CR00) match signal		0020H
	15	INTTM01	Generation of 16-bit timer register and capture/ compare register 01 (CR01) match signal		0022H
	16	INTTM1	Generation of 8-bit timer/event counter 1 match signal		0024H
	17	INTTM2	Generation of 8-bit timer/event counter 2 match signal		0026H
	18	INTAD	End of A/D converter conversion		0028H
	19	INTTM5	Generation of 8-bit timer/event counter 5 match signal		002AH
	20	INTTM6	Generation of 8-bit timer/event counter 6 match signal		002CH
Software	—	BRK	BRK instruction execution	—	003EH

Note: Default priorities are intended for two or more simultaneously generated maskable interrupt requests. 0 is the highest priority and 20 is the lowest priority.

The following table gives a listing of the interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 6-29. Interrupt Sources and Flags

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
		Register		Register		Register
INTWDT	TMIF4	IF0L	TMMK4	MK0L	TMPR4	PR0L
INTP0	PIF0		PMK0		PPR0	
INTP1	PIF1		PMK1		PPR1	
INTP2	PIF2		PMK2		PPR2	
INTP3	PIF3		PMK3		PPR3	
INTP4	PIF4		PMK4		PPR4	
INTP5	PIF5		PMK5		PPR5	
INTP6	PIF6		PMK6		PPR6	
INTCSI0	CSIIF0	IF0H	CSIMK0	MK0H	CSIPR0	PR0H
INTCSI1	CSIIF1		CSIMK1		CSIPR1	
INTSER	SERIF		SERMK		SERPR	
INTSR/INTCSI2	SRIF		SRMK		SRPR	
INTST	STIF		STMK		STPR	
INTTM3	TMIF3		TMMK3		TMPR3	
INTTM00	TMIF00		TMMK00		TMPR00	
INTTM01	TMIF01		TMMK01		TMPR01	
INTTM1	TMIF1	IF1L	TMMK1	MK1L	TMPR1	PR1L
INTTM2	TMIF2		TMMK2		TMPR2	
INTAD	ADIF		ADMK		ADPR0	
INTTM5	TMIF5		TMMK5		TMPR5	
INTTM6	TMIF6		TMMK6		TMPR6	

The following six types of registers control the interrupt functions:

- Interrupt request flag registers (IF0L, IF0H, IF1L)
- Interrupt mask flag registers (MK0L, MK0H, MK1L)
- Priority specification flag registers (PR0L, PR0H, PR1L)
- External interrupt mode registers (INTM0, INTM1)
- Sampling clock select register (SCS)
- Program status word (PSW)

Format of Interrupt Request Flag Registers

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
IF0L	PIF6	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	TMIF4	FFE0H	00H	R/W
IF0H	TMIF01	TMIF00	TMIF3	STIF	SRIF	SERIF	CSIIF1	CSIIF0	FFE1H	00H	R/W
IF1L	WTIF[Note]	0	0	TMIF6	TMIF5	ADIF	TMIF2	TMIF1	FFE2H	00H	R/W

xxIFx	Interrupt request flag
0	No interrupt request signal
1	Interrupt request signal is generated; interrupt request state

Note: WTIF is a test input flag. A vectored interrupt request is not generated.

Cautions: 1. The TMIF4 flag is R/W enabled only when a watchdog timer is used as an interval timer. If a watchdog timer is used in watchdog timer mode 1, set the TMIF4 flag to 0.

2. Always set IF1L bits 5 and 6 to 0.

Format of Interrupt Mask Flag Registers

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
MK0L	PMK6	PMK5	PMK4	PMK3	PMK2	PMK	PMK	TMMK4	FFE4H	FFH	R/W
MK0H	TMMK01	TMMK00	TMMK3	STMK	SRMK	SERMK	CSIMK1	CSIMK0	FFE5H	FFH	R/W
MK1L	WTMK[Note]	1	1	TMMK6	TMMK5	ADMK	TMMK2	TMMK1	FFE6H	FFH	R/W

xxMKx	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Note: WTMK controls standby mode release enable/disable. It does not control the interrupt function.

Cautions: 1. If the TMIF4 flag is read when a watchdog timer is used in watchdog timer mode 1, the MK0 value becomes undefined.

2. Because port 0 has an alternate function as the external interrupt input, when the output level is changed by specifying the output mode of the port function, an interrupt request flag is set. Therefore, 1 should be set in the interrupt mask flag before using the output mode.

3. Always set MK1L bits 5 and 6 to 1.

Format of Priority Specification Flag Registers

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
PR0L	PPR6	PPR5	PPR4	PPR3	PPR2	PPR1	PPR0	TMPR4	FFE8H	FFH	R/W
	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>			
PR0H	TMPR01	TMPR00	TMPR3	STPR	SRPR	SERPR	CSIPR1	CSIPR0	FFE9H	FFH	R/W
	7	6	5	<4>	<3>	<2>	<1>	<0>			
PR1L	1	1	1	TMPR6	TMPR5	ADPR	TMPR2	TMPR1	FFEAH	FFH	R/W

xxPRx	Priority level selection
0	High priority level
1	Low priority level

Cautions: 1. If a watchdog timer is used in watchdog timer mode 1, set the TMPR4 flag to 1.

2. Always set PR1L bits 5 to 7 to 1.

Format of External Interrupt Mode Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
INTM0	ES31	ES30	ES21	ES20	ES11	ES10	0	0	FFECH	00H	R/W

ES11	ES10	INTP0 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES21	ES20	INTP1 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES31	ES30	INTP2 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

Caution: Before setting the valid edge of the INTP0/TIO0/P00 pin, stop the timer operation by clearing bits 1 to 3 (TMC01 to TMC03) of the 16-bit timer mode control register to 0, 0, 0.

Format of External Interrupt Mode Register 1

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
INTM1	ES71	ES70	ES61	ES60	ES51	ES50	ES41	ES40	FFEDH	00H	R/W

ES41	ES40	INTP3 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES51	ES50	INTP4 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES61	ES60	INTP5 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES71	ES70	INTP6 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

Format of Sampling Clock Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
SCS	0	0	0	0	0	0	SCS1	SCS0	FF47H	00H	R/W

SCS1	SCS0	INTP0 sampling clock selection		
			MCS = 1	MCS = 0
0	0	$f_{XX}/2^N$		
0	1	$f_{XX}/2^7$	$f_X/2^7$(39.1 kHz)	$f_X/2^8$(19.5 kHz)
1	0	$f_{XX}/2^5$	$f_X/2^5$(156.3 kHz)	$f_X/2^6$(78.1 kHz)
1	1	$f_{XX}/2^6$	$f_X/2^6$(78.1 kHz)	$f_X/2^7$(39.1 kHz)

Caution: $f_{XX}/2^N$ is a clock to be supplied to the CPU and $f_{XX}/2^5$, $f_{XX}/2^6$, and $f_{XX}/2^7$ are clocks to be supplied to the peripheral hardware. $f_{XX}/2^N$ stops in the HALT mode.

Remarks: N: Value (N = 0 to 4) at bits 0 to 2 (PCC0 to PCC2) of processor clock control register

f_{XX}: Main system clock frequency (f_X or $f_X/2$)

f_X: Main system clock oscillation frequency

MCS: Bit 0 of oscillation mode select register

Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of Program Status Word

	7	6	5	4	3	2	1	0	After Reset
PSW	IE	Z	RBS1	AC	RBS0	0	ISP	CY	02H

Used when a normal instruction is executed

ISP	Priority of interrupt currently being received
0	High-priority interrupt servicing (low-priority interrupt disable)
1	Interrupt request not acknowledged or low-priority interrupt servicing (all maskable interrupts enable)

IE	Interrupt request acknowledge enable/disable
0	Disable
1	Enable

(18) Registers controlling test function

The names of the test input flag and test mask flag corresponding to the test input signal name are as follows.

Test Input Sources

Test Input		Test Input Flag	Test Mask Flag	Internal/
Name	Trigger			External
INTWT	Watch timer overflow	WTIF	WTMK	Internal
INTPT4 Note	Falling edge detection at port 4	KRIF	KRMK	External

Note: Not provided for the μPD78070A/70AY Subseries.

The following three registers control the test function:

- Interrupt request flag register 1L (IF1L)
- Interrupt mask flag register 1L (MK1L)
- Key return mode register (KRM) Note

Note: This register is not provided for the μPD78070A/70AY Subseries.

Format of Interrupt Request Flag Register 1L

Symbol	<7>	6	5	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
IF1L	WTIF	0	0	TMIF6	TMIF5	ADIF	TMIF2	TMIF1	FFE2H	00H	R/W

WTIF	Clock timer overflow detection flag
0	Not detected
1	Detected

Caution: Be sure to clear bits 5 and 6 to 0.

Format of Interrupt Mask Flag Register 1L

Symbol	<7>	6	5	<4>	<3>	<2>	<1>	<0>	Address	After Reset	R/W
MK1L	WTMK	1	1	TMMK6	TMMK5	ADMK	TMMK2	TMMK1	FFE6H	FFH	R/W

WTMK	Standby mode control by clock timer
0	Enables releasing the standby mode
1	Disables releasing the standby mode

Caution: Be sure to set bits 5 and 6 to 1.

Format of Key Return Mode Register (μPD78078/78Y and 78075B/75BY Subseries Only)

Symbol	7	6	5	4	3	2	<1>	<0>	Address	After Reset	R/W
KRM	0	0	0	0	0	0	KRMK	KRIF	FFF6H	02H	R/W

KRIF	Key return signal
0	Not detected
1	Detected (port 4 rising edge detection)

KRMK	Standby mode control by key return signal
0	Standby mode release enabled
1	Standby mode release disabled

Caution: When port 4 falling edge detection is used, be sure to clear KRIF to 0 (it is not cleared to 0 automatically).

(19) Registers controlling external device expansion function

The following three registers control the external device expansion function:

- Memory expansion mode register (MM)
- Internal memory size switching register (IMS)
- External bus type select register (EBTS)

Format of Memory Expansion Mode Register (For μPD78078/78Y and 78075B/75BY Subseries)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
MM	0	0	PW1	PW0	0	MM2	MM1	MM0	FFF8H	10H	R/W

MM2	MM1	MM0	Single-chip/ memory expansion mode selection		P40 to P47, P50 to P57, P64 to P67, P80 to P87 pin state					
					P40 to P47	P80 to P87	P50 to P53	P54, P55	P56, P57	P64 to P67
0	0	0	Single-chip mode		Port mode: Input	Port mode				
0	0	1			Port mode: Output					
0	1	1	Memory expansion mode	256-byte mode	AD0 to AD7	A0 to A7 (**Note 1**)	Port mode			P64 = $\overline{RD}$ P65 = $\overline{WR}$ P66 = $\overline{WAIT}$ P67 = ASTB
1	0	0		4K mode			A8 to A11	Port mode		
1	0	1		16K mode				A12, A13	Port mode	
1	1	1		Full address mode Note 2					A14, A15	
Other than above			Setting prohibited							

PW1	PW0	Wait control
0	0	No wait
0	1	Wait (one wait state insertion)
1	0	Setting prohibited
1	1	Wait control by external wait pin

Notes: 1. This can be used only in the separate bus mode. In the multiplexed bus mode, these pins enter the port mode.

2. The full address mode allows external expansion to the entire 64K address space except for the internal ROM (or PROM), RAM, and SFR areas, and the reserved areas.

Remark: P60 to P63 are used as port pins without regard to the mode (single-chip mode or memory expansion mode).

Format of Memory Expansion Mode Register (For μPD78070A/70AY Subseries)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
MM	0	0	PW1	PW0	0	0	0	0	FFF8H	10H	R/W

PW1	PW0	Wait control
0	0	No wait
0	1	Wait (one wait state insertion)
1	0	Setting prohibited
1	1	Wait control by external wait pin

Caution: Ensure that 0 is set to bits 0 to 3.

Format of Internal Memory Size Switching Register
(For μPD78078/78Y and 78075B/75BY Subseries)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	**Note 1**	R/W

ROM3	ROM2	ROM1	ROM0	Internal ROM size selection
1	0	0	0	32 Kbytes
1	0	1	0	40 Kbytes
1	1	0	0	48 Kbytes
1	1	1	0	56 Kbytes Note 2
1	1	1	1	60 Kbytes
Settings other than above are prohibited				

RAM2	RAM1	RAM0	Internal high-speed RAM size selection
1	1	0	1024 bytes
Settings other than above are prohibited			

Notes: 1. The value of this register after reset differs depending on the product (refer to the table below).
2. When the external device expansion function of the μPD78078/78Y or 78P078/78Y is used, be sure to set the internal ROM capacity to 56K or less.

Value of Internal Memory Size Switching Register After Reset
(μPD78078/78Y and 78075B/75BY Subseries)

Part Number	Value After Reset
μPD78074B/74BY	C8H
μPD78075B/75BY	CAH
μPD78076/76Y	CCH
μPD78078/78Y, 78P078/78Y	CFH

Caution: When using the mask ROM versions, do not set IMS to values other than those shown in the table above, except for cases in which the external device expansion function is used in the μPD78078/78Y.

Remark: IMS should be set according to the internal ROM capacity.

Format of Internal Memory Size Switching Register (For μPD78070A/70AY Subseries)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	0	0	0	0	FFF0H	C0H	R/W

RAM2	RAM1	RAM0	Internal high-speed RAM size selection
1	1	0	1024 bytes
Other than above			Setting prohibited

Caution: Although IMS is a register that specifies the internal high-speed RAM capacity, the memory size of the μPD78070A/70AY cannot be changed. Do not set IMS with a value other than those used for resetting.

Format of External Bus Type Select Register (For μPD78078/78Y and 78075B/75BY Subseries)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
EBTS	0	0	0	0	0	0	0	EBTS0	FF3FH	00H	R/W

EBTS0	Sets operation mode of external device expansion function
0	Multiplexed bus mode
1	Separate bus mode

Format of External Bus Type Select Register (For μPD78070A/70AY Subseries)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
EBTS	0	0	0	0	0	0	0	EBTS0	FF3FH	01H	R/W

EBTS0	Sets operation mode of external device expansion function
0	Multiplexed bus mode (setting prohibited)
1	Separate bus mode

Caution: In the μPD78070A/70AY, this register is fixed to 01H (a separate mode). Do not set EBTS with a value other than those used for resetting.

(20) Register controlling standby function

The standby function is intended to decrease the power consumption of the system. The following two modes are available: HALT and STOP.

When MCU is released from the STOP mode, a wait time is required for the crystal to resume oscillations. The wait time is controlled by the following register:

- Oscillation stabilization time select register (OSTS)

Format of Oscillation Stabilization Time Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0	FFFAH	04H	R/W

OSTS2	OSTS1	OSTS0	Selection of oscillation stabilization time when STOP mode is released		
				MCS = 1	MCS = 0
0	0	0	$2^{12}/f_{xx}$	$2^{12}/f_x$ (819 μs)	$2^{13}/f_x$ (1.64 ms)
0	0	1	$2^{14}/f_{xx}$	$2^{14}/f_x$ (3.28 ms)	$2^{15}/f_x$ (6.55 ms)
0	1	0	$2^{15}/f_{xx}$	$2^{15}/f_x$ (6.55 ms)	$2^{16}/f_x$ (13.1 ms)
0	1	1	$2^{16}/f_{xx}$	$2^{16}/f_x$ (13.1 ms)	$2^{17}/f_x$ (26.2 ms)
1	0	0	$2^{17}/f_{xx}$	$2^{17}/f_x$ (26.2 ms)	$2^{18}/f_x$ (52.4 ms)
Settings other than above are prohibited					

Remarks: f_{xx}: Main system clock frequency (f_x or $f_x/2$)

f_x: Main system clock oscillation frequency

MCS: Bit 0 of oscillation mode select register (OSMS)

Values in parentheses apply to operation with f_x = 5.0 MHz.

$\overline{\text{RESET}}$ input sets OSTS to 04H. However, it takes $2^{17}/fx$, not $2^{18}/fx$, until the STOP Mode is cleared.

The operation status in the HALT mode is described below.

HALT Mode Operating Status

Setting of HALT Mode / Item		On Execution of HALT Instruction during Main System Clock Operation		On Execution of HALT Instruction during Subsystem Clock Operation	
		Without Subsystem Clock Note 1	With Subsystem Clock Note 2	When Main System Clock Continues Oscillation	When Main System Clock Clock Stops Oscillation
Clock generator		Both main system and subsystem clocks can be oscillated. Clock supply to the CPU stops.			
CPU		Operation stops			
Port (output latch)		Status before HALT mode setting is held			
16-bit timer/event counter		Operable			Operable when watch timer output is selected as count clock (f_{XT} is selected as count clock of watch timer)
8-bit timer/event counters 1 and 2		Operable			Operable when TI1 or TI2 is selected as count clock
8-bit timer/event counters 5 and 6		Operable			Operable when TI5 or TI6 is selected as count clock
Watch timer		Operable when $f_{XX}/2^7$ is selected as count clock	Operable		Operable when f_{XT} is selected as count clock
Watchdog timer		Operable		Operation stops	
A/D converter		Operable			Operation stops
D/A converter		Operable			
Real-time output port		Operable			
Serial interface	Other than automatic transmit/receive function	Operable			Operable when external SCK is used
	Automatic transmit/receive function	Operation stops			
External interrupt request	INTP0	INTP0 is operable when a clock ($f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$) supplied for the peripheral hardware is selected as the sampling clock.			Operation stops
	INTP1 to INTP6	Operable			
Bus line for external expansion	AD0 to AD7	High impedance			
	A0 to A15	Status before HALT mode setting is held			
	ASTB	Low level			
	$\overline{WR}$, $\overline{RD}$	High level			
	$\overline{WAIT}$	High impedance			

Notes: 1. Including when an external clock is not supplied.
2. Including when an external clock is supplied.

The operation status in the STOP mode is described below.

STOP Mode Operating Status

Item \ Setting of STOP Mode		With Subsystem Clock	Without Subsystem Clock
Clock generator		Only main system clock stops oscillation	
CPU		Operation stops	
Port (output latch)		Status before STOP mode setting is held	
16-bit timer/event counter		Operable when watch timer output is selected as count clock (f_{XT} is selected as count clock of watch timer)	Operation stops
8-bit timer/event counters 1 and 2		Operable when TI1 or TI2 is selected for the count clock	
8-bit timer/event counters 5 and 6		Operable when TI5 or TI6 is selected for the count clock	
Watch timer		Operable when f_{XT} is selected for the count clock	Operation stops
Watchdog timer		Operation stops	
A/D converter			
D/A converter		Operable	
Real-time output port		Operable when external trigger is used or TI1 or TI2 is selected for the 8-bit timer/event counter 1 or 2 count clock	
Serial interface	Other than automatic transmit/receive function and UART	Operable when externally supplied clock is specified as the serial clock	
	Automatic transmit/receive function and UART	Operation stops	
External interrupt request	INTP0	Not operable	
	INTP1 to INTP6	Operable	
Bus line for external expansion	AD0 to AD7	High impedance	
	A0 to A15	Status before STOP mode setting is held	
	ASTB	Low level	
	$\overline{WR}$, $\overline{RD}$	High level	
	$\overline{WAIT}$	High impedance	

Cautions: 1. When the STOP mode is set, the X2 pin is internally connected to V_{DD1} via a pull-up resistor to minimize the leakage current at the crystal oscillator. Thus, do not use the STOP mode in a system where an external clock is used for the main system clock.

2. Because the interrupt request signal is used to release the Standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the Standby mode is immediately released if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction. After the wait set using the oscillation stabilization time select register (OSTS), the operating mode is set.

(21) Reset function

The following two operations can generate a reset signal:

- External reset input via the $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer in the Watchdog Timer mode

Table 6-30. Hardware Status After Reset (1/2)

Hardware		Status After Reset
Program counter (PC) Note 1		Contents of reset vector tables (0000H, 0001H) are set
Stack pointer (SP)		Undefined
Program status word (PSW)		02H
RAM	Data memory	Undefined Note 2
	General-purpose register	Undefined Note 2
Port (output latch)	Ports 0 to 3, Ports 7, 9, 10, 12, 13 (P0 to P3, P7, P9, P10, P12, P13)	00H
	Ports 4 to 6, port 8 (P4 to P6, P8) Note 3	Undefined
Port mode registers (PM0 to PM3, PM5 to PM10, PM12, PM13) Note 3		FFH
Pull-up resistor option registers (PUOH, PUOL)		00H
Processor clock control register (PCC)		04H
Oscillation mode select register (OSMS)		00H
Internal memory size switching register (IMS)		**Note 4**
Internal expansion RAM size switching register (IXS) Note 5		**Note 6**
External bus type select register (EBTS)		00H
Memory expansion mode register (MM)		10H
Oscillation stabilization time select register (OSTS)		04H
16-bit timer/event counter	Timer register (TM0)	00H
	Capture/compare registers (CR00, CR01)	Undefined
	Clock select register (TCL0)	00H
	Mode control register (TMC0)	00H
	Capture/compare control register 0 (CRC0)	04H
	Output control register (TOC0)	00H
8-bit timer/event counters 1 and 2	Timer registers (TM1, TM2)	00H
	Compare registers (CR10, CR20)	Undefined
	Clock select register (TCL1)	00H
	Mode control register (TMC1)	00H
	Output control register (TOC1)	00H
8-bit timer/event counters 5 and 6	Timer registers (TM5, TM6)	00H
	Compare registers (CR50, CR60)	00H
	Clock select registers (TCL5, TCL6)	00H
	Mode control registers (TMC5, TMC6)	00H
Watch timer	Mode control register (TMC2)	00H
	Clock select register (TCL2)	00H
Watchdog timer	Mode register (WDTM)	00H

Table 6-30. Hardware Status After Reset (2/2)

Hardware		Status After Reset
Serial interface	Clock select register (TCL3)	88H
	Shift registers (SIO0, SIO1)	Undefined
	Mode registers (CSIM0, CSIM1, CSIM2)	00H
	Serial bus interface control register (SBIC)	00H
	Slave address register (SVA)	Undefined
	Automatic data transmit/receive control register (ADTC)	00H
	Automatic data transmit/receive address pointer (ADTP)	00H
	Automatic data transmit/receive interval specification register (ADTI)	00H
	Asynchronous serial interface mode register (ASIM)	00H
	Asynchronous serial interface status register (ASIS)	00H
	Baud rate generator control register (BRGC)	00H
	Transmit shift register (TXS)	FFH
	Receive buffer register (RXB)	
	Interrupt timing specification register (SINT)	00H
A/D converter	Mode register (ADM)	01H
	Conversion result register (ADCR)	Undefined
	Input select register (ADIS)	00H
D/A converter	Mode register (DAM)	00H
	Conversion value setting registers (DACS0, DACS1)	00H
Real-time output port	Mode register (RTPM)	00H
	Control register (RTPC)	00H
	Buffer registers (RTBL, RTBH)	00H
ROM correction **Note 7**	Correction address registers (CORAD0, CORAD1)	0000H
	Correction control register (CORCN)	00H
Interrupt	Request flag registers (IF0L, IF0H, IF1L)	00H
	Mask flag registers (MK0L, MK0H, MK1L)	FFH
	Priority specification flag registers (PR0L, PR0H, PR1L)	FFH
	External interrupt mode registers (INTM0, INTM1)	00H
	Key return mode register (KRM) Note 5	02H
	Sampling clock select register (SCS)	00H

Notes: 1. During reset input or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. If the reset signal is input in the Standby mode, the status before reset is retained even after reset.
3. The μPD78070A/70AY Subseries do not have ports 4, 5, 8, and PM5, PM8.
4. The value after reset differs depending on the product, as follows:

	μPD78070 μPD78070Y	μPD78074B μPD78074BY	μPD78075B μPD78075BY	μPD78076 μPD78076Y	μPD78078 μPD78078Y	μPD78P078 μPD78P078Y
IMS	C0H	C6H	C8H	CCH	CFH	

5. This register is not provided for the μPD78070A/70AY Subseries.
6. The value after reset differs depending on the product, as follows:

	μPD78076 μPD78076Y	μPD78078 μPD78078Y	μPD78P078 μPD78P078Y	μPD78074B μPD78074BY	μPD78075B μPD78075BY
IXS	0AH			0CH	

7. This register is provided only for the μPD78078/78Y Subseries.

(22) Registers controlling ROM correction (μPD78078/78Y Subseries only)

The following two types of registers control the ROM correction:

- Correction address registers 0 and 1 (CORAD0 and CORAD1)
- Correction control register (CORCN)

Format of Correction Address Registers 0 and 1

Symbol	15	0	Address	After Reset	R/W
CORAD0			FF38H/FF39H	0000H	R/W
CORAD1			FF3AH/FF3BH	0000H	R/W

Cautions: 1. Set CORAD0 and CORAD1 when bits 1 (COREN0) and 3 (COREN1) of the correction control register (CORCN: refer to the figure below) are 0.

2. Only addresses where operation codes are stored can be set in CORAD0 and CORAD1.

3. Do not set the following addresses to CORAD0 and CORAD1:

- **Address value in table area of table reference instruction (CALLT instruction): 0040H to 007FH**
- **Address value in vector table area: 0000H to 003FH**

Format of Correction Control Register

Symbol	7	6	5	4	<3>	<2>	<1>	<0>	Address	After Reset	R/W
CORCN	0	0	0	0	COREN1	CORST1	COREN0	CORST0	FF8AH	00H	R/W Note

R

CORST0	Correction address register 0 and fetch address match detection
0	Not detected
1	Detected

R/W

COREN0	Correction address register 0 and fetch address match detection control
0	Disabled
1	Enabled

R

CORST1	Correction address register 1 and fetch address match detection
0	Not detected
1	Detected

R/W

COREN1	Correction address register 1 and fetch address match detection control
0	Disabled
1	Enabled

Note: Bits 0 and 2 are read-only bits.

(23) Register controlling internal memory capacity

The μPD78P078 and 78P078Y allow users to select the internal memory capacity.
The following register is used to control the internal memory capacity:

- Internal memory size switching register (IMS)

To map the memory of the μPD78P078 or 78P078Y identically to that of a mask ROM version, the value at the time the mask ROM version is reset must be set.
For the mask ROM version, IMS does not need to be set.

Format of Internal Memory Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

ROM3	ROM2	ROM1	ROM0	Internal ROM size selection
1	0	0	0	32K
1	0	1	0	40K
1	1	0	0	48K
1	1	1	0	56K Note
1	1	1	1	60K
Settings other than above are prohibited				

RAM2	RAM1	RAM0	Internal high-speed RAM size selection
1	1	0	1024 bytes
Settings other than above are prohibited			

Note: When the external device expansion function of the μPD78P078/78Y is used, set the internal PROM capacity to 56K or less.

The following table shows the set value of IMS to map the memory of the μPD78P078/78Y identically to that of a mask ROM version.

Set Value of Internal Memory Size Switching Register

Target Mask ROM Version	Set Value of IMS
μPD78074B/74BY	C8H
μPD78075B/75BY	CAH
μPD78076/76Y	CCH
μPD78078/78Y	CFH

Caution: When using a mask ROM version, do not set IMS to a value other than those shown in the table above, except when the external device expansion function of the μPD78078/78Y is used.

(24) Register controlling internal expansion RAM capacity

The μPD78P078/78Y allow users to select the internal expansion RAM capacity.
The following register is used to control the internal expansion RAM capacity:

- Internal expansion RAM size switching register (IXS)

Remark: This register is not provided for the μPD78070A/70AY.

Format of Internal Expansion RAM Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IXS	0	0	0	0	IX RAM3	IX RAM2	IX RAM1	IX RAM0	FFF4H	0AH	W

IX RAM3	IX RAM2	IX RAM1	IX RAM0	Selects internal expansion RAM capacity
1	1	0	0	0 bytes
1	0	1	0	1024 bytes
Settings other than above are prohibited				

The following table shows the set value of IXS to map the internal expansion RAM of the μPD78P078/78Y identically to that of a mask ROM version.

Set Value of Internal Expansion RAM Size Switching Register

Target Mask ROM Version	Set Value of IXS
μPD78076/76Y	0AH
μPD78078/78Y	
μPD78074B/74BY	0CH
μPD78075B/75BY	

Cautions: 1. For the mask ROM version, IXS does not need to be set.

2. When using a mask ROM version, do not set IXS to a value other than those shown in the table above.

[MEMO]

6.8 μPD78083 Subseries

6.8.1 Documentation Reference Information

Device Series Number	User's Manual Number	Date Published
μPD78083	U12176EJ2V0UM00	May 1997

Caution: The user should check the current User's Manual with the information in this section to be sure of having the most up-to-date information.

General Programmer's Note

The NEC C-compiler and the NEC Assembler are capable of recognizing certain symbolic SFR bit names. These special bit names are identified in the user manual in one of the four ways shown below:

1. <7>
2. (7)
3. ⑦
4. 7

Example:

	<7>	<6>	<5>	<4>	3	2	1	0
PCC	MCC	FRC	CLS	CSS	0	PCC2	PCC1	PCC0

If a bit number has one of the four symbols around it, the NEC software will recognize the associated symbolic bit name. For example to set bit 7, the user can write the code in two ways:

```
1.    SET1    MCC
2.    SET1    PCC.7
```

Alternatively since bit 2 does not have any of the four symbols around it, the user can only set this bit as follows:

```
1.    SET1    PCC.2
```

Note: The attempt to employ a symbolic name of bit-2 (PCC2) will return an error. Thus the use of instruction

```
SET1    PCC2
```

is improper since neither the NEC C-compiler nor the NEC Assembler recognizes this symbolic name and will generate an error.

6.8.2 Memory Address Space

Each model in the μPD78083 Subseries can access a memory space of 64K. Figures 6-40 through 6-42 show memory maps of the respective models.

Figure 6-40. Memory Map (μPD78081)

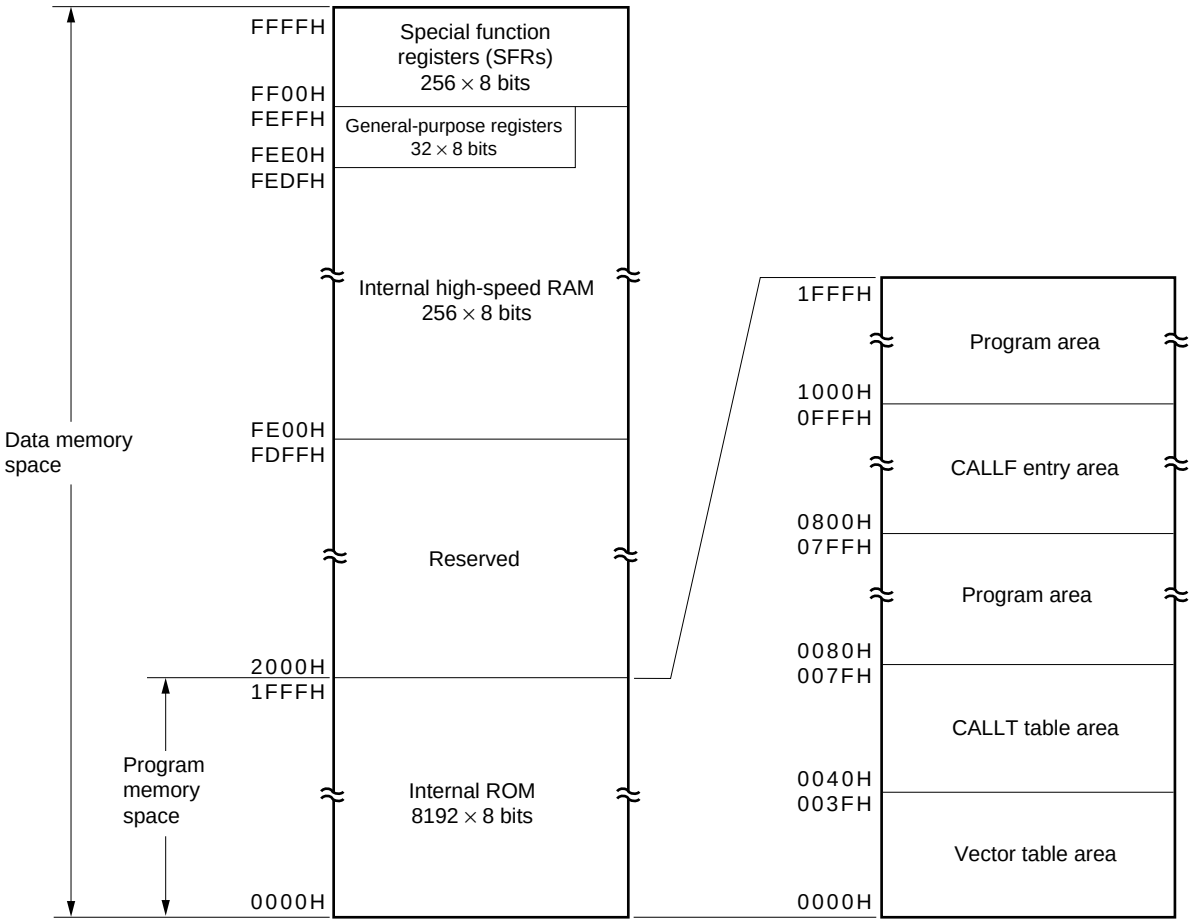


Figure 6-41. Memory Map (μPD78082)

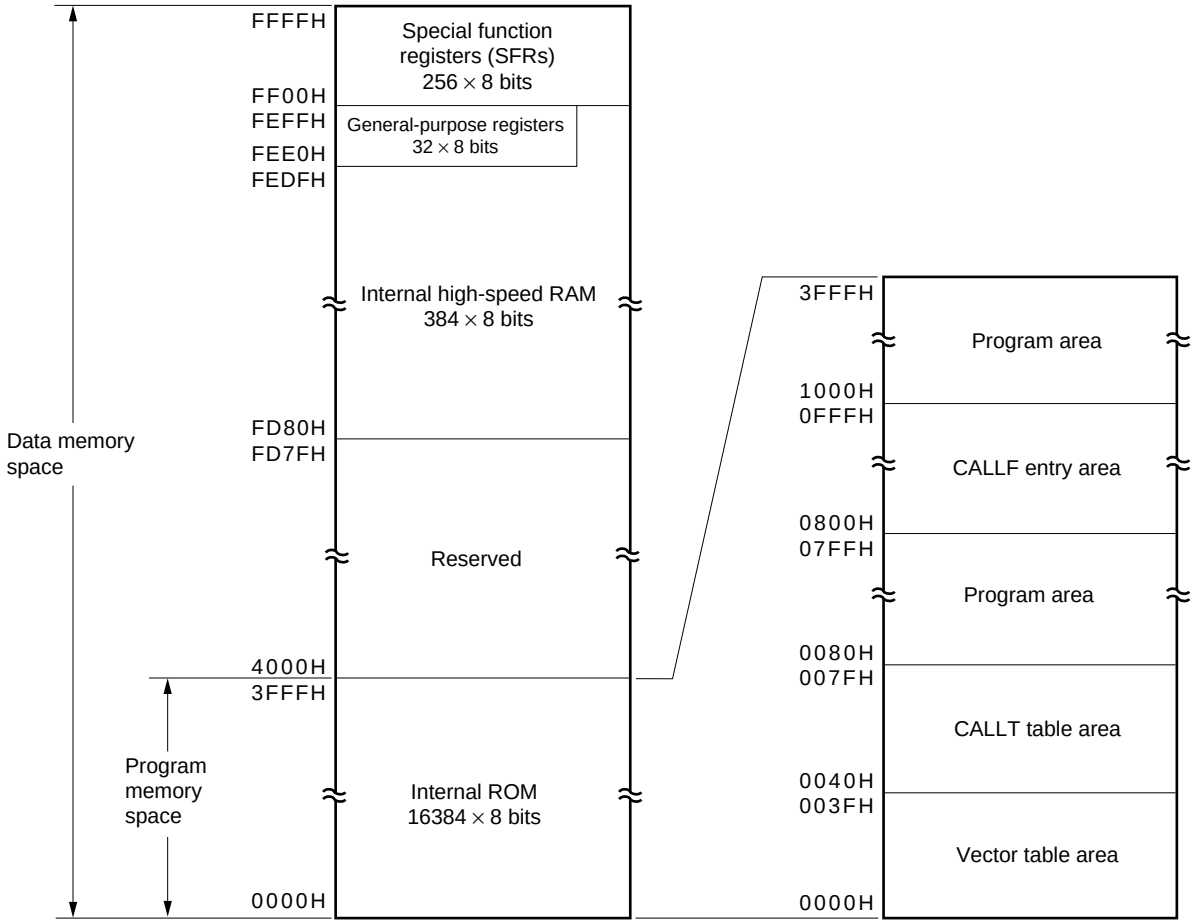
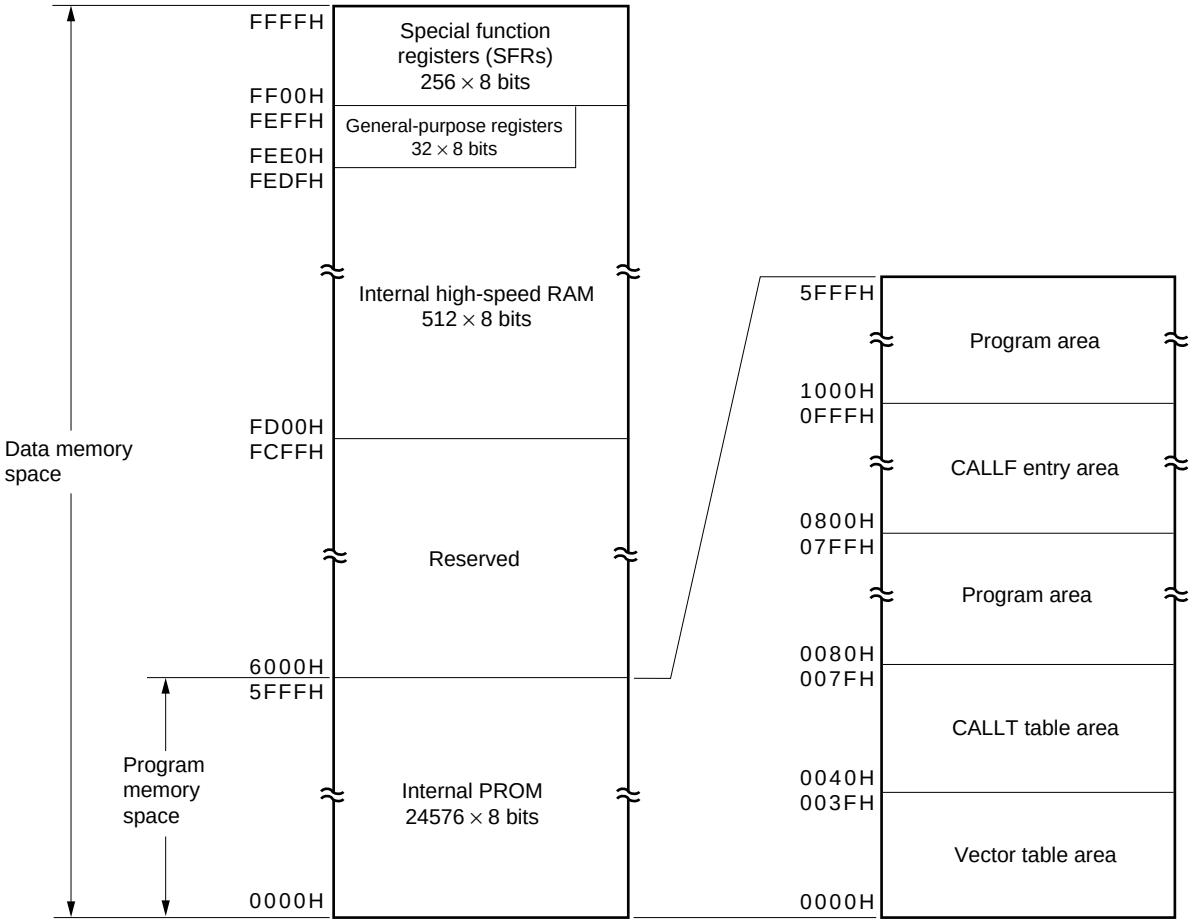


Figure 6-42. Memory Map (μPD78P083)



6.8.3 Special Function Registers (SFRs)

Table 6-31. Special Function Register List (μPD78083 Subseries) (1/2)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulatable Bit Unit			After Reset
				1 Bit	8 Bits	16 Bits	
FF00H	Port 0	P0	R/W	√	√	–	00H
FF01H	Port 1	P1		√	√	–	
FF03H	Port 3	P3		√	√	–	
FF05H	Port 5	P5		√	√	–	
FF07H	Port 7	P7		√	√	–	
FF0AH	Port 10	P10		√	√	–	
FF1FH	A/D conversion result register	ADCR	R	–	√	–	Undefined
FF20H	Port mode register 0	PM0	R/W	√	√	–	FFH
FF21H	Port mode register 1	PM1		√	√	–	
FF23H	Port mode register 3	PM3		√	√	–	
FF25H	Port mode register 5	PM5		√	√	–	
FF27H	Port mode register 7	PM7		√	√	–	
FF2AH	Port mode register 10	PM10		√	√	–	
FF40H	Timer clock select register 0	TCL0		√	√	–	00H
FF42H	Timer clock select register 2	TCL2		–	√	–	
FF50H	Compare register 50	CR50		–	√	–	
FF51H	8-bit timer register 5	TM5	R	–	√	–	
FF52H	Timer clock select register 5	TCL5	R/W	–	√	–	
FF53H	8-bit timer mode control register 5	TMC5		√	√	–	
FF54H	Compare register 60	CR60		–	√	–	
FF55H	8-bit timer register 6	TM6	R	–	√	–	
FF56H	Timer clock select register 6	TCL6	R/W	–	√	–	
FF57H	8-bit timer mode control register 6	TMC6		√	√	–	
FF70H	Asynchronous serial interface mode register	ASIM		√	√	–	
FF71H	Asynchronous serial interface status register	ASIS	R	√	√	–	
FF72H	Serial operation mode register 2	CSIM2	R/W	√	√	–	
FF73H	Baud rate generator control register	BRGC		–	√	–	
FF74H	Transmit shift register	TXS, SIO2	W	–	√	–	FFH
	Receive buffer register	RXB	R				
FF80H	A/D converter mode register	ADM	R/W	√	√	–	01H
FF84H	A/D converter input select register	ADIS		–	√	–	00H
FFE0H	Interrupt request flag register 0L	IF0, IF0L		√	√	√	
FFE1H	Interrupt request flag register 0H	IF0H		√	√		
FFE2H	Interrupt request flag register 1L	IF1L		√	√	–	
FFE4H	Interrupt mask flag register 0L	MK0, MK0L		√	√	√	FFH
FFE5H	Interrupt mask flag register 0H	MK0H		√	√		
FFE6H	Interrupt mask flag register 1L	MK1L		√	√	–	

Table 6-31. Special Function Register List (μPD78083 Subseries) (2/2)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulatable Bit Unit			After Reset
					1 Bit	8 Bits	16 Bits	
FFE8H	Priority order specification flag register 0L	PR0	PR0L	R/W	√	√	√	FFH
FFE9H	Priority order specification flag register 0H		PR0H		√	√		
FFEAH	Priority order specification flag register 1L	PR1L			√	√	–	
FFECH	External interrupt mode register 0	INTM0			–	√	–	00H
FFEDH	External interrupt mode register 1	INTM1			–	√	–	
FFF0H	Internal memory size switching register	IMS			–	√	–	**Note**
FFF2H	Oscillation mode select register	OSMS		W	–	√	–	00H
FFF3H	Pull-up resistor option register H	PUOH		R/W	√	√	–	
FFF7H	Pull-up resistor option register L	PUOL			√	√	–	
FFF9H	Watchdog timer mode register	WDTM			√	√	–	
FFFAH	Oscillation stabilization time select register	OSTS			–	√	–	04H
FFFBH	Processor clock control register	PCC			√	√	–	

Note: The value after reset depends on products:
μPD78081: 82H, μPD78082: 64H, μPD78P083: 46H.

(1) Registers controlling port functions

The following two types of registers control the ports:

- Port mode registers (PM0, PM1, PM3, PM5, PM7, PM10)
- Pull-up resistor option registers (PUOH, PUOL)

Format of Port Mode Registers

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PM0	1	1	1	1	PM03	PM02	PM01	1	FF20H	FFH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FF21H	FFH	R/W
PM3	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	FF23H	FFH	R/W
PM5	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	FF25H	FFH	R/W
PM7	1	1	1	1	1	PM72	PM71	PM70	FF27H	FFH	R/W
PM10	1	1	1	1	1	1	PM101	PM100	FF2AH	FFH	R/W

PMmn	Pmn pin input/output mode selection (m = 0, 1, 3, 5, 7, 10 : n = 0 to 7)
0	Output mode (output buffer ON)
1	Input mode (output buffer OFF)

Caution: Be sure to set bits 0 and 4 to 7 of PM0, bits 3 to 7 of PM7, and bits 2 to 7 of PM10 to 1.

Format of Pull-up Resistor Option Registers

Symbol	7	6	5	4	3	<2>	1	0	Address	After Reset	R/W
PUOH	0	0	0	0	0	PUO10	0	0	FFF3H	00H	R/W
	<7>	6	<5>	4	<3>	2	<1>	<0>			
PUOL	PUO7	0	PUO5	0	PUO3	0	PUO1	PUO0	FFF7H	00H	R/W

PUOm	Pm internal pull-up resistor selection (m = 0, 1, 3, 5, 7, 10)
0	Internal pull-up resistor not used
1	Internal pull-up resistor used

Cautions: 1. Be sure to set bits 0, 1 and 3 through 7 of PUOH and bits 2, 4, and 6 of PUOL to 0.

2. P00 pin does not incorporate a pull-up resistor.

3. When a pin of port 1 is used as an alternate function pin, an on-chip pull-up resistor cannot be used even if 1 is set in PUOL bit 1 (PUO1).

(2) Registers controlling clock generator

The following two registers control the clock generator:

- Processor clock control register (PCC)
- Oscillation mode select register (OSMS)

Format of Processor Clock Control Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PCC	0	0	0	0	0	PCC2	PCC1	PCC0	FFFBH	04H	R/W

PCC2	PCC1	PCC0	CPU clock selection (f_{CPU})		
				MCS = 1	MCS = 0
0	0	0	f_{XX}	f_X (0.4 μs)	f_X/2 (0.8 μs)
0	0	1	$f_{XX}/2$	$f_X/2$ (0.8 μs)	$f_X/2^2$ (1.6 μs)
0	1	0	$f_{XX}/2^2$	$f_X/2^2$ (1.6 μs)	$f_X/2^3$ (3.2 μs)
0	1	1	$f_{XX}/2^3$	$f_X/2^3$ (3.2 μs)	$f_X/2^4$ (6.4 μs)
1	0	0	$f_{XX}/2^4$	$f_X/2^4$ (6.4 μs)	$f_X/2^5$ (12.8 μs)
Settings other than above are prohibited					

Caution: Be sure to clear bits 3 to 7 to 0.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillator frequency
MCS: Bit 0 of oscillation mode select register (OSMS)

Values in parentheses indicate a minimum instruction execution time of $2f_{CPU}$ when operating at f_X = 5.0 MHz.

Format of Oscillation Mode Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
OSMS	0	0	0	0	0	0	0	MCS	FFF2H	00H	W

MCS	Main system clock scaler control
0	Scaler used
1	Scaler not used

Cautions: 1. Writing data (including the same data as previous) to OSMS causes a delay of the main system clock cycle of up to 2/f_x during the write operation. Therefore, if this register is written during the operation, in peripheral hardware that operates with the main system clock, a temporary error occurs in the count clock cycle of the timer, etc. In addition, because the oscillation mode is changed by this register, the clocks for peripheral hardware as well as that for the CPU are switched.

Therefore, writing to OSMS should be performed only immediately after reset signal release and before peripheral hardware operation starts.

2. When writing "1" to MCS, V_{DD} must be 2.7 V or higher before the write execution.

(3) Registers controlling 8-bit timer/event counters 5 and 6

The following three types of registers control 8-bit timer/event counters 5 and 6:

- Timer clock select registers 5 and 6 (TCL5, TCL6)
- 8-bit timer mode control registers 5 and 6 (TMC5, TMC6)
- Port mode register 10 (PM10)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register n (n = 5 or 6)

Symbol	7	6	5	4	3	2	1	0
TCLn	0	0	0	0	TCLn3	TCLn2	TCLn1	TCLn0

	Address	After Reset	R/W
TCL5	FF52H	00H	R/W
TCL6	FF56H	00H	R/W

TCLn3	TCLn2	TCLn1	TCLn0	8-bit timer register n count clock selection		
					MCS = 1	MCS = 0
0	0	0	0	TIn falling edge Note		
0	0	0	1	TIn rising edge Note		
0	1	0	0	$2f_{XX}$	Setting prohibited	f_X (5.0 MHz)
0	1	0	1	f_{XX}	f_X (5.0 MHz)	$f_X/2$ (2.5 MHz)
0	1	1	0	$f_{XX}/2$	$f_X/2$ (2.5 MHz)	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
1	1	1	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)
1	1	1	1	$f_{XX}/2^{11}$	$f_X/2^{11}$ (2.4 kHz)	$f_X/2^{12}$ (1.2 kHz)
Settings other than above are prohibited						

Note: When the clock is input from the external, timer output (PWM output) cannot be used.

Caution: To write data other than that already set to TCLn (n = 5 or 6), stop the timer operation once.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
TIn: 8-bit timer register n input pin (n = 5 or 6)
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz.

Format of 8-Bit Timer Output Control Register n (n = 5 or 6)

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
TMCn	TCEn	TMCn6	0	0	LVSn	LVRn	TMCn1	TOEn

	Address	After Reset	R/W
TMC5	FF53H	00H	R/W
TMC6	FF57H	00H	R/W

TOEn	8-bit timer/event counter n output control
0	Output disabled (Port mode)
1	Output enabled

TMCn1	In PWM mode	In other modes
	Active level selection	Timer output F/F1 control
0	Active high	Inversion operation disabled
1	Active low	Inversion operation enabled

LVSn	LVRn	8-bit timer/event counter n timer output F/F1 status setting
0	0	No change
0	1	Timer output F/F1 reset (0)
1	0	Timer output F/F1 set (1)
1	1	Setting prohibited

TMCn6	8-bit timer/event counter n operating mode selection
0	Clear and Start mode on match of TMn and CRn0
1	PWM mode (free running)

TCEn	8-bit timer register n operation control
0	Operation stop (TMn clear to 0)
1	Operation enable

Cautions: 1. Timer operation must be stopped before setting TMCn (n = 5 or 6).

2. If LVSn and LVRn (n = 5 or 6) are read after data are set, they will be 0.

3. Be sure to set bits 4 and 5 to 0.

(4) Registers controlling watchdog timer

The following two registers control the watchdog timer:

- Timer clock select register 2 (TCL2)
- Watchdog timer mode register (WDTM)

Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL2	TCL27	TCL26	TCL25	0	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

This section controls the buzzer output function.
Refer to **(6) Registers controlling buzzer output function** or **Chapter 9** of *μPD78083 Subseries User's Manual* for detailed information.

TCL22	TCL21	TCL20	Watchdog timer count clock selection		
				MCS = 1	MCS = 0
0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)
1	1	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)
1	1	1	$f_{XX}/2^{11}$	$f_X/2^{11}$ (2.4 kHz)	$f_X/2^{12}$ (1.2 kHz)

Cautions: 1. When rewriting TCL2 to other data, stop the timer operation beforehand.

2. Be sure to set bits 3 and 4 to 0.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)

f_X: Main system clock oscillation frequency

MCS: Bit 0 of oscillation mode select register (OSMS)

Values in parentheses apply to operation with f_X = 5.0 MHz.

This register also controls the buzzer.

Format of Watchdog Timer Mode Register

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
WDTM	RUN	0	0	WDTM4	WDTM3	0	0	0	FFF9H	00H	R/W

WDTM4	WDTM3	Watchdog timer operation mode selection Note 1
0	×	Interval timer mode Note 2 (Maskable interrupt occurs upon generation of an overflow.)
1	0	Watchdog timer mode 1 (Non-maskable interrupt occurs upon generation of an overflow.)
1	1	Watchdog timer mode 2 (Reset operation is activated upon generation of an overflow.)

RUN	Watchdog timer operation mode selection Note 3
0	Count stop
1	Counter is cleared and counting starts

Notes: 1. Once set to 1, WDTM3 and WDTM4 cannot be cleared to 0 by software.

2. The watchdog timer starts operating as an interval timer as soon as RUN has been set to 1.

3. Once set to 1, RUN cannot be cleared to 0 by software.
Thus, once counting starts, counting can only be stopped by $\overline{\text{RESET}}$ input.

Cautions: 1. When 1 is set in RUN so that the watchdog timer is cleared, the actual overflow time is up to 0.5% shorter than the time set by timer clock select register 2 (TCL2).

2. To use watchdog timer modes 1 and 2, make sure that the interrupt request flag (TMIF4) is 0, and then set WDTM4 to 1.
If WDTM4 is set to 1 when TMIF4 is 1, the non-maskable interrupt request occurs, regardless of the contents of WDTM3.

Remark: ×: Don't care

(5) Registers controlling clock output function

The following two registers control the clock output function:

- Timer clock select register 0 (TCL0)
- Port mode register 3 (PM3)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 0

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL0	CLOE	0	0	0	TCL03	TCL02	TCL01	TCL00	FF40H	00H	R/W

TCL03	TCL02	TCL01	TCL00	PCL output clock selection		
					MCS = 1	MCS = 0
0	1	0	1	f_{XX}	f_X (5.0 MHz)	$f_X/2$ (2.5 MHz)
0	1	1	0	$f_{XX}/2$	$f_X/2$ (2.5 MHz)	$f_X/2^2$ (1.25 MHz)
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2^5$ (156 kHz)
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)
Settings other than above are prohibited						

CLOE	PCL output control
0	Output disable
1	Output enable

Cautions:
1. **When enabling PCL output, set TCL00 to TCL03, then set 1 in CLOE with a 1-bit memory manipulation instruction.**
2. **To write data other than that already written to TCL0, stop the clock operation once.**
3. **Be sure to set bits 4 to 6 to 0.**

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_X = 5.0 MHz.

(6) Registers controlling buzzer output function

The following two registers control the buzzer output function:

- Timer clock select register 2 (TCL2)
- Port mode register 3 (PM3)
  - Refer to section (1) for the register format.

Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
TCL2	TCL27	TCL26	TCL25	0	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

This section controls the watchdog timer output function. Refer to **(4) Registers controlling watchdog timer** or **Chapter 7** of *μPD78083 Subseries User's Manual* for detailed information.

TCL27	TCL26	TCL25	Buzzer output frequency selection		
				MCS = 1	MCS = 0
0	×	×	Buzzer output disable		
1	0	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)
1	0	1	$f_{XX}/2^{10}$	$f_X/2^{10}$ (4.9 kHz)	$f_X/2^{11}$ (2.4 kHz)
1	1	0	$f_{XX}/2^{11}$	$f_X/2^{11}$ (2.4 kHz)	$f_X/2^{12}$ (1.2 kHz)
1	1	1	Setting prohibited		

Cautions: 1. When rewriting TCL2 to other data, stop the timer operation beforehand.

2. Be sure to set bits 3 and 4 to 0.

Remarks: f_{XX}: Main system clock frequency (f_X or $f_X/2$)

f_X: Main system clock oscillation frequency

×: Don't care

MCS: Bit 0 of oscillation mode select register (OSMS)

Values in parentheses apply to operation with f_X = 5.0 MHz.

(7) Registers controlling A/D converter

The following three registers control the A/D converter:

- A/D converter mode register (ADM)
- A/D converter input select register (ADIS)
- External interrupt mode register 1 (INTM1)
  - Refer to section (19) for the register format.

Format of A/D Converter Mode Register

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After Reset	R/W
ADM	CS	TRG	FR1	FR0	ADM3	ADM2	ADM1	HSC	FF80H	01H	R/W

ADM3	ADM2	ADM1	Analog input channel selection
0	0	0	ANI0
0	0	1	ANI1
0	1	0	ANI2
0	1	1	ANI3
1	0	0	ANI4
1	0	1	ANI5
1	1	0	ANI6
1	1	1	ANI7

FR1	FR0	HSC	A/D conversion time selection Note 1			
			f_X = 5.0-MHz operation		f_X = 4.19-MHz operation	
			MCS = 1	MCS = 0	MCS = 1	MCS = 0
0	0	1	80/f_X (Setting prohibited Note 2)	160/f_X (32.0 μs)	80/f_X (19.1 μs)	160/f_X (38.1 μs)
0	1	1	40/f_X (Setting prohibited Note 2)	80/f_X (Setting prohibited Note 2)	40/f_X (Setting prohibited Note 2)	80/f_X (19.1 μs)
1	0	0	50/f_X (Setting prohibited Note 2)	100/f_X (20.0 μs)	50/f_X (Setting prohibited Note 2)	100/f_X (23.8 μs)
1	0	1	100/f_X (20.0 μs)	200/f_X (40.0 μs)	100/f_X (23.8 μs)	200/f_X (47.7 μs)
Settings other than above are prohibited						

TRG	External trigger selection
0	No external trigger (software starts)
1	Conversion started by external trigger (hardware starts)

CS	A/D conversion operation control
0	Operation stop
1	Operation start

Notes: 1. Set so that the A/D conversion time is 19.1 μs or more.
2. Setting prohibited because the A/D conversion time is less than 19.1 μs.

Cautions: 1. The following sequence is recommended for power consumption reduction of the A/D converter when the standby function is used: Clear bit 7 (CS) to 0 first to stop the A/D conversion operation, and then execute the HALT or STOP instruction.

2. When restarting the stopped A/D conversion operation, start the A/D conversion operation after clearing the interrupt request flag (ADIF) to 0.

Remarks: f_X: Main system clock oscillation frequency
MCS: Bit 0 of oscillation mode select register (OSMS)

Format of A/D Converter Input Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ADIS	0	0	0	0	ADIS3	ADIS2	ADIS1	ADIS0	FF84H	00H	R/W

ADIS3	ADIS2	ADIS1	ADIS0	Number of analog input channel selection
0	0	0	0	No analog input channel (P10 to P17)
0	0	0	1	1 channel (ANI0, P11 to P17)
0	0	1	0	2 channels (ANI0, ANI1, P12 to P17)
0	0	1	1	3 channels (ANI0 to ANI2, P13 to P17)
0	1	0	0	4 channels (ANI0 to ANI3, P14 to P17)
0	1	0	1	5 channels (ANI0 to ANI4, P15 to P17)
0	1	1	0	6 channels (ANI0 to ANI5, P16, P17)
0	1	1	1	7 channels (ANI0 to ANI6, P17)
1	0	0	0	8 channels (ANI0 to ANI7)
Settings other than above are prohibited				

Cautions: 1. Set the analog input channel in the following order:

a. Set the number of analog input channels with ADIS.

b. Using the A/D converter mode register (ADM), select one channel to undergo A/D conversion from among the channels set for analog input with ADIS.

2. No internal pull-up resistor can be used to the channels set for analog input with ADIS, irrespective of the value of bit 1 (PUO1) of pull-up resistor option register L (PUOL).

(8) Registers controlling serial interface channel 2

The following four registers control serial interface channel 2:

- Serial operation mode register 2 (CSIM2)
- Asynchronous serial interface mode register (ASIM)
- Asynchronous serial interface status register (ASIS)
- Baud rate generator control register (BRGC)

Format of Serial Operation Mode Register 2

Symbol	<7>	6	5	4	3	2	1	0	Address	After Reset	R/W
CSIM2	CSIE2	0	0	0	0	CSIM22	CSCK	0	FF72H	00H	R/W

CSCK	Clock selection in 3-wire serial I/O mode
0	Input clock from off-chip to $\overline{SCK2}$ pin
1	Dedicated baud rate generator output

CSIM22	First bit specification
0	MSB
1	LSB

CSIE2	Operation control in 3-wire serial I/O mode
0	Operation stopped
1	Operation enabled

Cautions: 1. Be sure to set bits 0 and 3 to 6 to 0.

2. When UART mode is selected, CSIM2 should be set to 00H.

Format of Asynchronous Serial Interface Mode Register

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After Reset	R/W
ASIM	TXE	RXE	PS1	PS0	CL	SL	ISRM	SCK	FF70H	00H	R/W

SCK	Clock selection in asynchronous serial interface mode
0	Input clock from off-chip to ASCK pin
1	Dedicated baud rate generator output Note

ISRM	Control of reception completion interrupt in case of error generation
0	Reception completion interrupt generated in case of error generation
1	Reception completion interrupt not generated in case of error generation

SL	Transmit data stop bit length specification
0	1 bit
1	2 bits

CL	Character length specification
0	7 bits
1	8 bits

PS1	PS0	Parity bit specification
0	0	No parity
0	1	0 parity always added in transmission No parity test in reception (parity error not generated)
1	0	Odd parity
1	1	Even parity

RXE	Receive operation control
0	Receive operation stopped
1	Receive operation enabled

TXE	Transmit operation control
0	Transmit operation stopped
1	Transmit operation enabled

Note: When SCK is set to 1 and the baud rate generator output is selected, the ASCK pin can be used as an input/output port.

Cautions: 1. When the 3-wire serial I/O mode is selected, 00H should be set in ASIM.

2. The serial transmit/receive operation must be stopped before changing the operating mode.

Format of Asynchronous Serial Interface Status Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
ASIS	0	0	0	0	0	PE	FE	OVE	FF71H	00H	R

OVE	Overrun error flag
0	Overrun error not generated
1	Overrun error generated Note 1 (when next receive operation is completed before data from receive buffer register is read)

FE	Framing error flag
0	Framing error not generated
1	Framing error generated Note 2 (when stop bit is not detected)

PE	Parity error flag
0	Parity error not generated
1	Parity error generated (when transmit data parity does not match)

Notes: 1. The receive buffer register (RXB) must be read when an overrun error is generated. Overrun errors will continue to be generated until RXB is read.

2. Even if the stop bit length has been set as 2 bits by bit 2 (SL) of the asynchronous serial interface mode register (ASIM), only single stop bit detection is performed during reception.

Format of Baud Rate Generator Control Register (1/2)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
BRGC	TPS3	TPS2	TPS1	TPS0	MDL3	MDL2	MDL1	MDL0	FF73H	00H	R/W

MDL3	MDL2	MDL1	MDL0	Baud rate generator input clock selection	k
0	0	0	0	$f_{SCK}/16$	0
0	0	0	1	$f_{SCK}/17$	1
0	0	1	0	$f_{SCK}/18$	2
0	0	1	1	$f_{SCK}/19$	3
0	1	0	0	$f_{SCK}/20$	4
0	1	0	1	$f_{SCK}/21$	5
0	1	1	0	$f_{SCK}/22$	6
0	1	1	1	$f_{SCK}/23$	7
1	0	0	0	$f_{SCK}/24$	8
1	0	0	1	$f_{SCK}/25$	9
1	0	1	0	$f_{SCK}/26$	10
1	0	1	1	$f_{SCK}/27$	11
1	1	0	0	$f_{SCK}/28$	12
1	1	0	1	$f_{SCK}/29$	13
1	1	1	0	$f_{SCK}/30$	14
1	1	1	1	f_{SCK} **Note**	

Note: Can only be used in 3-wire serial I/O mode.

Remarks: f_{SCK}: 5-bit counter source clock

k: Value set in MDL0 to MDL3 ($0 \leq k \leq 14$)

Format of Baud Rate Generator Control Register (2/2)

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
BRGC	TPS3	TPS2	TPS1	TPS0	MDL3	MDL2	MDL1	MDL0	FF73H	00H	R/W

TPS3	TPS2	TPS1	TPS0	5-bit counter source clock selection			n
					MCS = 1	MCS = 0	
0	0	0	0	$f_{XX}/2^{10}$	$f_{XX}/2^{10}$ (4.9 kHz)	$f_X/2^{11}$ (2.4 kHz)	11
0	1	0	1	f_{XX}	f_X (5.0 MHz)	$f_X/2$ (2.5 MHz)	1
0	1	1	0	$f_{XX}/2$	$f_X/2$ (2.5 MHz)	$f_X/2^2$ (1.25 MHz)	2
0	1	1	1	$f_{XX}/2^2$	$f_X/2^2$ (1.25 MHz)	$f_X/2^3$ (625 kHz)	3
1	0	0	0	$f_{XX}/2^3$	$f_X/2^3$ (625 kHz)	$f_X/2^4$ (313 kHz)	4
1	0	0	1	$f_{XX}/2^4$	$f_X/2^4$ (313 kHz)	$f_X/2$ (156 kHz)	5
1	0	1	0	$f_{XX}/2^5$	$f_X/2^5$ (156 kHz)	$f_X/2^6$ (78.1 kHz)	6
1	0	1	1	$f_{XX}/2^6$	$f_X/2^6$ (78.1 kHz)	$f_X/2^7$ (39.1 kHz)	7
1	1	0	0	$f_{XX}/2^7$	$f_X/2^7$ (39.1 kHz)	$f_X/2^8$ (19.5 kHz)	8
1	1	0	1	$f_{XX}/2^8$	$f_X/2^8$ (19.5 kHz)	$f_X/2^9$ (9.8 kHz)	9
1	1	1	0	$f_{XX}/2^9$	$f_X/2^9$ (9.8 kHz)	$f_X/2^{10}$ (4.9 kHz)	10
Settings other than above are prohibited							

Caution: When a write is performed to BRGC during a communication operation, baud rate generator output is disrupted and communication cannot be performed normally. Therefore, BRGC must not be written to during a communication operation.

Remarks: f_X: Main system clock oscillation frequency

f_{XX}: Main system clock frequency (f_X or $f_X/2$)

MCS: Bit 0 of oscillation mode select register (OSMS)

n: Value set in TPS0 to TPS3 ($1 \leq n \leq 11$)

Values in parentheses apply to operation with f_X = 5.0 MHz.

(9) Registers controlling interrupt function

A total of 12 interrupt sources are provided for the μPD78083 Subseries, including non-maskable, maskable, and software interrupts.

Table 6-32. Interrupt Source List

Interrupt Type	Default Priority Note	Interrupt Source		Internal/ External	Vector Table Address
		Name	Trigger		
Non-maskable	—	RESET	Low voltage level	External	0000H
		INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)		
	1	INTP1	Pin input edge detection	External	0008H
	2	INTP2			000AH
	3	INTP3			000CH
	4	INTSER	Serial interface channel 2 UART reception error generation	Internal	0018H
	5	INTSR	End of serial interface channel 2 UART reception		001AH
		INTCSI2	End of serial interface channel 2 3-wire transfer		
	6	INTST	End of serial interface channel 2 UART transmission		001CH
	7	INTAD	End of A/D converter conversion		0028H
	8	INTTM5	Generation of 8-bit timer/event counter 5 match signal		002AH
	9	INTTM6	Generation of 8-bit timer/event counter 6 match signal		002CH
Software	—	BRK	BRK instruction execution	—	003EH

Note: Default priorities are intended for two or more simultaneously generated maskable interrupt requests. 0 is the highest priority and 9 is the lowest priority.

The following table gives a listing of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 6-33. Interrupt Sources and Flags

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
		Register		Register		Register
INTWDT	TMIF4	IF0L	TMMK4	MK0L	TMPR4	PR0L
INTP1	PIF1		PMK1		PPR1	
INTP2	PIF2		PMK2		PPR2	
INTP3	PIF3		PMK3		PPR3	
INTSER	SERIF	IF0H	SERMK	MK0H	SERPR	PR0H
INTSR/INTCSI2	SRIF		SRMK		SRPR	
INTST	STIF		STMK		STPR	
INTAD	ADIF	IF1L	ADMK	MK1L	ADPR0	PR1L
INTTM5	TMIF5		TMMK5		TMPR5	
INTTM6	TMIF6		TMMK6		TMPR6	

The following five types of registers control the interrupt functions:

- Interrupt request flag registers (IF0L, IF0H, IF1L)
- Interrupt mask flag registers (MK0L, MK0H, MK1L)
- Priority specification flag registers (PR0L, PR0H, PR1L)
- External interrupt mode registers (INTM0, INTM1)
- Program status word (PSW)

Format of Interrupt Request Flag Registers

Symbol	7	6	5	<4>	<3>	<2>	1	<0>	Address	After Reset	R/W
IF0L	0	0	0	PIF3	PIF2	PIF1	0	TMIF4	FFE0H	00H	R/W
	7	6	5	<4>	<3>	<2>	1	0			
IF0H	0	0	0	STIF	SRIF	SERIF	0	0	FFE1H	00H	R/W
	7	6	5	<4>	<3>	<2>	1	0			
IF1L	0	0	0	TMIF6	TMIF5	ADIF	0	0	FFE2H	00H	R/W

××IF×	Interrupt request flag
0	No interrupt request signal
1	Interrupt request signal is generated; interrupt request state

Cautions: 1. The TMIF4 flag is R/W enabled only when a watchdog timer is used as an interval timer. If a watchdog timer is used in watchdog timer mode 1, set the TMIF4 flag to 0.

2. Be sure to set bits 1 and 5 through 7 of IF0L and bits 0, 1, and 5 to 7 of IF0H and IF1L to 0.

Format of Interrupt Mask Flag Registers

Symbol	7	6	5	<4>	<3>	<2>	1	<0>	Address	After Reset	R/W
MK0L	1	1	1	PMK3	PMK2	PMK	1	TMMK4	FFE4H	FFH	R/W
	7	6	5	<4>	<3>	<2>	1	0			
MK0H	1	1	1	STMK	SRMK	SERMK	1	1	FFE5H	FFH	R/W
	7	6	5	<4>	<3>	<2>	1	0			
MK1L	1	1	1	TMMK6	TMMK5	ADMK	1	1	FFE6H	FFH	R/W

××MK×	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Cautions: 1. If the TMIF4 flag is read when a watchdog timer is used in watchdog timer mode 1, the MK0 value becomes undefined.

2. Because port 0 has an alternate function as the external interrupt request input, when the output level is changed by specifying the output mode of the port function, an interrupt request flag is set. Therefore, 1 should be set in the interrupt mask flag before using the output mode.

3. Be sure to set bits 1 and 5 through 7 of MK0L and bits 0, 1, and 5 to 7 of MK0H and MK1L to 1.

Format of Priority Specification Flag Registers

Symbol	7	6	5	<4>	<3>	<2>	1	<0>	Address	After Reset	R/W
PR0L	1	1	1	PPR3	PPR2	PPR1	1	TMPR4	FFE8H	FFH	R/W
	7	6	5	<4>	<3>	<2>	1	0			
PR0H	1	1	1	STPR	SRPR	SERPR	1	1	FFE9H	FFH	R/W
	7	6	5	<4>	<3>	<2>	1	0			
PR1L	1	1	1	TMPR6	TMPR5	ADPR	1	1	FFEAH	FFH	R/W

××PR×	Priority level selection
0	High priority level
1	Low priority level

Cautions: 1. If a watchdog timer is used in watchdog timer mode 1, set the TMPR4 flag to 1.

2. Be sure to set bits 1 and 5 to 7 of PR0L and bits 0, 1, and 5 to 7 of PR0H and PR1L to 1.

Format of External Interrupt Mode Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
INTM0	ES31	ES30	ES21	ES20	0	0	0	0	FFECH	00H	R/W

ES21	ES20	INTP1 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES31	ES30	INTP2 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

Caution: Be sure to set bits 0 to 3 to 0.

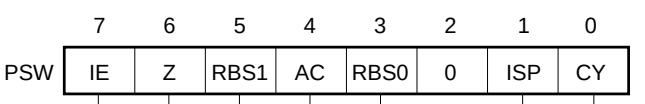
Format of External Interrupt Mode Register 1

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
INTM1	0	0	0	0	0	0	ES41	ES40	FFEDH	00H	R/W

ES41	ES40	INTP3 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

Caution: Be sure to set bits 2 through 7 to 0.

Format of Program Status Word



After Reset: 02H

Used when a normal instruction is executed

ISP	Priority of interrupt currently being received
0	High-priority interrupt servicing (low-priority interrupt disable)
1	Interrupt not acknowledged or low-priority interrupt request servicing (all maskable interrupts enable)

IE	Interrupt request acknowledge enable/disable
0	Disable
1	Enable

(10) Register controlling standby function

The standby function is intended to decrease power consumption of the system. The following two modes are available: HALT and STOP.

When MCU is released from the STOP mode, the wait time is required for crystal to resume oscillations. The wait time is controlled by the following register:

- Oscillation stabilization time select register (OSTS)

Format of Oscillation Stabilization Time Select Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0	FFFAH	04H	R/W

OSTS2	OSTS1	OSTS0	Selection of oscillation stabilization time when STOP mode is released		
				MCS = 1	MCS = 0
0	0	0	$2^{12}/f_{xx}$	$2^{12}/f_x$ (819 μs)	$2^{13}/f_x$ (1.64 ms)
0	0	1	$2^{14}/f_{xx}$	$2^{14}/f_x$ (3.28 ms)	$2^{15}/f_x$ (6.55 ms)
0	1	0	$2^{15}/f_{xx}$	$2^{15}/f_x$ (6.55 ms)	$2^{16}/f_x$ (13.1 ms)
0	1	1	$2^{16}/f_{xx}$	$2^{16}/f_x$ (13.1 ms)	$2^{17}/f_x$ (26.2 ms)
1	0	0	$2^{17}/f_{xx}$	$2^{17}/f_x$ (26.2 ms)	$2^{18}/f_x$ (52.4 ms)
Settings other than above are prohibited					

Remarks: f_{xx}: Main system clock frequency (f_x or $f_x/2$)
f_x: Main system clock oscillation frequency
MCS: Bit 0 of oscillation mode select register (OSMS)
Values in parentheses apply to operation with f_x = 5.0 MHz.

The operation status in HALT mode and STOP mode is described below.

HALT Mode Operating Status

Item	HALT Mode Operating Status
Clock generator	Can be oscillated. Clock supply to the CPU is stopped.
CPU	Operation stops
Port	Status before HALT mode setting is held
8-bit timer/event counters 5 and 6	Operable
Watchdog timer	
A/D converter	
Serial interface	
External interrupt request	

STOP Mode Operating Status

Item	STOP Mode Operating Status
Clock generator	Operation stops
CPU	Operation stops
Port	Status before HALT mode setting is held
8-bit timer/event counters 5 and 6	Operable when TI5 or TI6 is selected for the count clock
Watchdog timer	Operation stops
A/D converter	
Serial interface	3-wire serial I/O is operable when the external input clock is selected as the serial clock. UART operation stops.
External interrupt request	Operable

Cautions: 1. When the STOP mode is set, the X2 pin is internally connected to V_{DD} via a pull-up resistor to minimize the leakage current at the crystal oscillator. Thus, do not use the STOP mode in a system where an external clock is used for the main system clock.

2. Because the interrupt request signal is used to release the Standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the Standby mode is immediately released if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction. After the wait set using the oscillation stabilization time select register (OSTS), the operating mode is set.

(11) Reset function

The following two operations can be used to generate a reset signal:

- External reset input via the $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer in the Watchdog Timer mode

Table 6-34. Hardware Status After Reset

Hardware		Status After Reset
Program counter (PC) Note 1		Contents of reset vector tables (0000H, 0001H) are set
Stack pointer (SP)		Undefined
Program status word (PSW)		02H
RAM	Data memory	Undefined Note 2
	General-purpose register	Undefined Note 2
Port (output latch)	Ports 0, 1, 3, 5, 7, 10 (P0, P1, P3, P5, P7, P10)	00H
Port mode registers (PM0, PM1, PM3, PM5, PM7, PM10)		FFH
Pull-up resistor option registers (PUOH, PUOL)		00H
Processor clock control register (PCC)		04H
Oscillation mode select register (OSMS)		00H
Internal memory size switching register (IMS)		**Note 3**
Oscillation stabilization time select register (OSTS)		04H
Timer clock select register 0 (TCL0)		00H
8-bit timer/event counters 5 and 6	Timer registers (TM5, TM6)	00H
	Compare registers (CR50, CR60)	00H
	Clock select registers (TCL5, TCL6)	00H
	Mode control registers (TMC5, TMC6)	00H
Watchdog timer	Clock select register (TCL2)	00H
	Mode register (WDTM)	00H
Serial interface	Mode register (CSIM2)	00H
	Asynchronous serial interface mode register (ASIM)	00H
	Asynchronous serial interface status register (ASIS)	00H
	Baud rate generator control register (BRGC)	00H
	Transmit shift register (TXS)	FFH
	Receive buffer register (RXB)	
A/D converter	Mode register (ADM)	01H
	Conversion result register (ADCR)	Undefined
	Input select register (ADIS)	00H
Interrupt	Request flag registers (IF0L, IF0H, IF1L)	00H
	Mask flag registers (MK0L, MK0H, MK1L)	FFH
	Priority specification flag registers (PR0L, PR0H, PR1L)	FFH
	External interrupt mode registers (INTM0, INTM1)	00H

Notes: 1. During reset input or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. If the reset signal is input in the Standby mode, the status before reset is retained even after reset.

3. The value after reset differs depending on the product:
μPD78081: 82H, μPD78082: 64H, μPD78P083: 46H.

(12) Register controlling internal memory capacity

The μPD78P083 allows users to select the internal memory capacity.
The following register is used to control the internal memory capacity:

- Internal memory size switching register (IMS)

To map the memory of the μPD78P083 identical to that of a mask ROM version, the value at the time the mask ROM version is reset must be set.

Format of Internal Memory Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	46H	R/W

ROM3	ROM2	ROM1	ROM0	Internal ROM capacity selection
0	0	1	0	8K
0	1	0	0	16K
0	1	1	0	24K
Settings other than above are prohibited				

RAM2	RAM1	RAM0	Internal high-speed RAM capacity selection
0	1	0	512 bytes
0	1	1	384 bytes
1	0	0	256 bytes
Settings other than above are prohibited			

Caution: When using a mask ROM version, do not set a value to IMS other than those shown in the table below.

The following table shows the set value of IMS to map the memory of the μPD78P083 identically to that of a mask ROM version.

Set Value of Internal Memory Size Switching Register

Target Mask ROM Version	Set Value of IMS
μPD78081	82H
μPD78082	64H

[MEMO]

APPENDIX A INDEX (ARCHITECTURE)

A

Addressing Modes 23
Data Memory Addressing 23
Instruction Address Addressing 25
Immediate addressing 26
Register addressing 28
Relative addressing 25
Table indirect addressing 27
Operand Address Addressing 29
Based addressing 34
Based indexed addressing 35
Direct addressing 31
Implied addressing 29
Register addressing 30
Register indirect addressing 34
Short direct addressing 32
Special function register (SFR) addressing 33
Stack addressing 35

G

General Purpose Registers 37

I

Instruction Set 41
Instructions Listed by Addressing Type 51
16-bit instructions 53
8-bit instructions 51
Bit manipulation instructions 53
Call instructions/branch instructions 54
Other instructions 54
Operand Descriptions 41
Description of “Flag” column 42
Operation List 43

P

Processor Registers 38
Program counter (PC) 38
Program status word (PSW) 38
Auxiliary carry flag (AC) 39
Carry flag (CY) 39
In-service priority flag (ISP) 39
Interrupt enable flag (IE) 38
Register bank select flags (RBS0 and RBS1) 38

Zero flag (Z) 38
Stack pointer (SP) 39

S

Sample Program 55
Stack Operation 39

APPENDIX B REGISTER INDEX

B.1 μPD78014/14Y, 78014H, and 78018F/18FY Subseries

(i) Register Name

A

A/D Converter Input Select Register (ADIS) 96
A/D Converter Mode Register (ADM) 95
Automatic Data Transmit/Receive Control Register (ADTC) 112
Automatic Data Transmit/Receive Interval Time Specification Register (ADTI) 113

C

Correction Address Register 0 (CORAD0) 131
Correction Address Register 1 (CORAD1) 131
Correction Control Register (CORCN) 131

E

8-Bit Timer Mode Control Register (TMC1) 87
8-Bit Timer Output Control Register (TOC1) 88
External Interrupt Mode Register (INTM0) 84, 118

I

Internal Expansion RAM Size Switching Register (IXS) 134
Internal Memory Size Switching Register (IMS) 123, 133
Interrupt Mask Flag Register 0H (MK0H) 117, 120
Interrupt Mask Flag Register 0L (MK0L) 117
Interrupt Request Flag Register 0H (IF0H) 117, 120
Interrupt Request Flag Register 0L (IF0L) 117
Interrupt Timing Specification Register (SINT) 102, 108

K

Key Return Mode Register (KRM) 121

M

Memory Expansion Mode Register (MM) 122

O

Oscillation Stabilization Time Select Register (OSTS) 124

P

Port Mode Register n (PMn) (n = 0 to 3, 5, 6) 78
Priority Specification Flag Register 0H (PR0H) 118
Priority Specification Flag Register 0L (PR0L) 118
Processor Clock Control Register (PCC) 79
Program Status Word (PSW) 119
Pull-up Resistor Option Register (PUO) 78

S

Sampling Clock Select Register (SCS) 84, 119
Serial Bus Interface Control Register (SBIC) 100, 106

Serial Operation Mode Register 0 (CSIM0) 99, 105
Serial Operation Mode Register 1 (CSIM1) 111
16-Bit Timer Mode Control Register (TMC0) 82
16-Bit Timer Output Control Register (TOC0) 83

T

Timer Clock Select Register 0 (TCL0) 81, 93
Timer Clock Select Register 1 (TCL1) 86
Timer Clock Select Register 2 (TCL2) 89, 91, 94
Timer Clock Select Register 3 (TCL3) 98, 104, 110

W

Watch Timer Mode Control Register (TMC2) 90
Watchdog Timer Mode Register (WDTM) 92

(ii) Register Symbol

A

ADIS: A/D Converter Input Select Register 96
ADM: A/D Converter Mode Register 95
ADTC: Automatic Data Transmit/Receive Control Register 112
ADTI: Automatic Data Transmit/Receive Interval Time Specification Register 113

C

CORAD0: Correction Address Register 0 131
CORAD1: Correction Address Register 1 131
CORCN: Correction Control Register 131
CSIM0: Serial Operation Mode Register 0 ..... 99, 105
CSIM1: Serial Operation Mode Register 1 111

I

IF0H: Interrupt Request Flag Register 0H 117, 120
IF0L: Interrupt Request Flag Register 0L 117, 123
IMS: Internal Memory Size Switching Register 123, 133
INTM0: External Interrupt Mode Register 84, 118
IXS: Internal Expansion RAM Size Switching Register 134

K

KRM: Key Return Mode Register 121

M

MK0H: Interrupt Mask Flag Register 0H 117, 120
MK0L: Interrupt Mask Flag Register 0L 117
MM: Memory Expansion Mode Register 122

O

OSTS: Oscillation Stabilization Time Select Register 124

P

PCC: Processor Clock Control Register 79
PMn: Port Mode Register n (n = 0 to 3, 5, 6) 78
PR0H: Priority Specification Flag Register 0H 118
PR0L: Priority Specification Flag Register 0L 118
PSW: Program Status Word 119
PUO: Pull-up Resistor Option Register 78

S

SBIC: Serial Bus Interface Control Register 100, 106
SCS: Sampling Clock Select Register 84, 119
SINT: Interrupt Timing Specification Register 102, 108

T

TCL0: Timer Clock Select Register 0 ..... 81, 93
TCL1: Timer Clock Select Register 1 86
TCL2: Timer Clock Select Register 2 ..... 89, 91, 94
TCL3: Timer Clock Select Register 3 ..... 98, 104, 110
TMC1: 8-Bit Timer Mode Control Register 87
TMC0: 16-Bit Timer Mode Control Register 82
TMC2: Watch Timer Mode Control Register 90
TOC0: 16-Bit Timer Output Control Register 83
TOC1: 8-Bit Timer Output Control Register 88

W

WDTM: Watchdog Timer Mode Register (WDTM) 92

B.2 μPD780208 Subseries

(i) Register Name

A

A/D Converter Mode Register (ADM) 163
A/D Converter Input Select Register (ADIS) 164
Automatic Data Transmit/Receive Control Register (ADTC) 172
Automatic Data Transmit/Receive Interval Specification Register (ADTI) 173

D

Display Mode Register 0 (DSPM0) 145, 175
Display Mode Register 1 (DSPM1) 147, 177
Display Mode Register 2 (DSPM2) 178

E

8-Bit Timer Mode Control Register (TMC1) 154
8-Bit Timer Output Control Register (TOC1) 155
External Interrupt Mode Register (INTM0) 182

I

Internal Expansion RAM Size Switching Register (IXS) 192
Internal Memory Size Switching Register (IMS) 191
Interrupt Mask Flag Register 0H (MK0H) 181, 184
Interrupt Mask Flag Register 0L (MK0L) 181
Interrupt Request Flag Register 0H (IF0H) 181, 184
Interrupt Request Flag Register 0L (IF0L) 181
Interrupt Timing Specification Register (SINT) 169

O

Oscillation Stabilization Time Select Register (OSTS) 185

P

Port Mode Register n (PMn) (n = 0 to 3, 7, 10 to 12) 143
Priority Specification Flag Register 0H (PR0H) 182
Priority Specification Flag Register 0L (PR0L) 182
Processor Clock Control Register (PCC) 144
Program Status Word (PSW) 183
Pull-up Resistor Option Register (PUO) 143

S

Sampling Clock Select Register (SCS) 183
Serial Bus Interface Control Register (SBIC) 167
Serial Operation Mode Register 0 (CSIM0) 166
Serial Operation Mode Register 1 (CSIM1) 171
16-Bit Timer Mode Control Register (TMC0) 150
16-Bit Timer Output Control Register (TOC0) 151

T

Timer Clock Select Register 0 (TCL0) 149, 160
Timer Clock Select Register 1 (TCL1) 153
Timer Clock Select Register 2 (TCL2) 156, 158, 161
Timer Clock Select Register 3 (TCL3) 165, 170

W

Watch Timer Mode Control Register (TMC2) 157
Watchdog Timer Mode Register (WDTM) 159

(ii) Register Symbol

A

ADIS: A/D Converter Input Select Register 164
ADM: A/D Converter Mode Register 163
ADTC: Automatic Data Transmit/Receive Control Register 172
ADTI: Automatic Data Transmit/Receive Interval Specification Register 173

C

CSIM0: Serial Operation Mode Register 0 166
CSIM1: Serial Operation Mode Register 1 171

D

DSPM0: Display Mode Register 0 ..... 145, 175
DSPM1: Display Mode Register 1 ..... 147, 177
DSPM2: Display Mode Register 2 178

I

IF0H: Interrupt Request Flag Register 0H 181, 184
IF0L: Interrupt Request Flag Register 0L 181
IMS: Internal Memory Size Switching Register 191
INTM0: External Interrupt Mode Register 182
IXS: Internal Expansion RAM Size Switching Register 192

M

MK0H: Interrupt Mask Flag Register 0H 181, 184
MK0L: Interrupt Mask Flag Register 0L 181

O

OSTS: Oscillation Stabilization Time Select Register 185

P

PCC: Processor Clock Control Register 144
PMn: Port Mode Register n (n = 0 to 3, 7, 10 to 12) 143
PR0H: Priority Specification Flag Register 0H 182
PR0L: Priority Specification Flag Register 0L 182
PSW: Program Status Word 183
PUO: Pull-up Resistor Option Register 143

S

SBIC: Serial Bus Interface Control Register 167
SCS: Sampling Clock Select Register 183
SINT: Interrupt Timing Specification Register 169

T

TCL0: Timer Clock Select Register 0 ..... 149, 160
TCL1: Timer Clock Select Register 1 153
TCL2: Timer Clock Select Register 2 ..... 156, 158, 161
TCL3: Timer Clock Select Register 3 ..... 165, 170
TMC0: 16-Bit Timer Mode Control Register 150
TMC1: 8-Bit Timer Mode Control Register 154
TMC2: Watch Timer Mode Control Register 157
TOC0: 16-Bit Timer Output Control Register 151
TOC1: 8-Bit Timer Output Control Register 155

W

WDTM: Watchdog Timer Mode Register 159

B.3 μPD780024/24Y and 780034/34Y Subseries

(i) Register Name

A

A/D Converter Mode Register (ADM0) 215
Analog Input Channel Specification Register (ADS0) 216
Asynchronous Serial Interface Mode Register (ASIM0) 218
Asynchronous Serial Interface Status Register (ASIS0) 219

B

Baud Rate Generator Control Register (BRGC0) 220

C

Capture/Compare Control Register 0 (CRC0) 205
Clock Output Selection Register (CKS) 214

E

8-Bit Timer Mode Control Register 5n (TMC5n) (n = 0, 1) 210
External Interrupt Falling Edge Enable Register (EGN) 236
External Interrupt Rising Edge Enable Register (EGP) 236

I

I^2C Shift Register (IIC0) 230
IIC Clock Select Register (IICCL0) 229
IIC Control Register (IICC0) 223
IIC Status Register (IICS0) 226
Internal Memory Size Switching Register (IMS) 244
Interrupt Mask Flag Register 0H (MK0H) 234
Interrupt Mask Flag Register 0L (MK0L) 234
Interrupt Mask Flag Register 1L (MK1L) 234
Interrupt Request Flag Register 0H (IF0H) 233
Interrupt Request Flag Register 0L (IF0L) 233
Interrupt Request Flag Register 1L (IF1L) 233

M

Memory Expansion Mode Register (MEM) 237
Memory Expansion Wait Setting Register (MM) 237

O

Oscillation Stabilization Time Select Register (OSTS) 238

P

Port Mode Register n (PMn) (n = 0, 2 to 7) 201
Prescaler Mode Register 0 (PRM0) 207
Priority Specification Flag Register 0H (PR0H) 235
Priority Specification Flag Register 0L (PR0L) 235
Priority Specification Flag Register 1L (PR1L) 235
Processor Clock Control Register (PCC) 203
Program Status Word (PSW) 236

Pull-Up Resistor Option Register n (PUn) (n = 0, 2 to 7) 202

S

Serial Operation Mode Register 30 (CSIM30) 221
16-Bit Timer Mode Control Register (TMC0) 204
16-Bit Timer Output Control Register (TOC0) 206
Slave Address Register (SVA0) 230

T

Timer Clock Select Register 50 208
Timer Clock Select Register 51 209

W

Watch Timer Mode Control Register (WTM) 211
Watchdog Timer Clock Select Register (WDCS) 212
Watchdog Timer Mode Register (WDTM) 213

(ii) Register Symbol

A

ADM0: A/D Converter Mode Register 215
ADS0: Analog Input Channel Specification Register 216
ASIM0: Asynchronous Serial Interface Mode Register 218
ASIS0: Asynchronous Serial Interface Status Register 219

B

BRGC0: Baud Rate Generator Control Register 220

C

CKS: Clock Output Selection Register 214
CRC0: Capture/Compare Control Register 0 205
CSIM30: Serial Operation Mode Register 30 221

E

EGN: External Interrupt Falling Edge Enable Register 236
EGP: External Interrupt Rising Edge Enable Register 236

I

IF0H: Interrupt Request Flag Register 0H 233
IF0L: Interrupt Request Flag Register 0L 233
IF1L: Interrupt Request Flag Register 1L 233
IIC0: I^2C Shift Register 230
IICC0: IIC Control Register 223
IICCL0: IIC Clock Select Register 229
IICS0: IIC Status Register 226
IMS: Internal Memory Size Switching Register 244

M

MEM: Memory Expansion Mode Register 237
MK0H: Interrupt Mask Flag Register 0H 234
MK0L: Interrupt Mask Flag Register 0L 234
MK1L: Interrupt Mask Flag Register 1L 234
MM: Memory Expansion Wait Setting Register 237

O

OSTS: Oscillation Stabilization Time Select Register 238

P

PCC: Processor Clock Control Register 203
PMn: Port Mode Register n (n = 0, 2 to 7) 201
PR0H: Priority Specification Flag Register 0H 235
PR0L: Priority Specification Flag Register 0L 235
PR1L: Priority Specification Flag Register 1L 235
PRM0: Prescaler Mode Register 0 207
PSW: Program Status Word 236
PUn: Pull-Up Resistor Option Register n (n = 0, 2 to 7) 202

S

SVA0: Slave Address Register 230

T

TCL50: Timer Clock Select Register 50 208
TCL51: Timer Clock Select Register 51 209
TMC0: 16-Bit Timer Mode Control Register 204
TMC5n: 8-Bit Timer Mode Control Register 5n (n = 0, 1) 210
TOC0: 16-Bit Timer Output Control Register 206

W

WDCS: Watchdog Timer Clock Select Register 212
WDTM: Watchdog Timer Mode Register 213
WTM: Watch Timer Mode Control Register 211

B.4 μPD78044F and 78044H Subseries

(i) Register Name

A

A/D Converter Input Select Register (ADIS) 279
A/D Converter Mode Register (ADM) 278
Automatic Data Transmit/Receive Control Register (ADTC) 289
Automatic Data Transmit/Receive Interval Specification Register (ADTI) 290

D

Display Mode Register 0 (DSPM0) 261, 292
Display Mode Register 1 (DSPM1) 262, 293

E

8-Bit Timer Mode Control Register (TMC1) 268
8-Bit Timer Output Control Register (TOC1) 269
External Interrupt Mode Register (INTM0) 300

I

Internal Expansion RAM Size Switching Register (IXS) 313
Internal Memory Size Switching Register (IMS) 312
Interrupt Mask Flag Register 0H (MK0H) 298, 302
Interrupt Mask Flag Register 0L (MK0L) 298
Interrupt Request Flag Register 0H (IF0H) 297, 302
Interrupt Request Flag Register 0L (IF0L) 297
Interrupt Timing Specification Register (SINT) 284

O

Oscillation Stabilization Time Select Register (OSTS) 303

P

Port Mode Register n (PMn) (n = 0 to 3, 7, 11, 12) 258
Priority Specification Flag Register 0H (PR0H) 299
Priority Specification Flag Register 0L (PR0L) 299
Processor Clock Control Register (PCC) 260
Program Status Word (PSW) 301
Pull-Up Resistor Option Register (PUO) 259

S

Sampling Clock Select Register (SCS) 301
Serial Bus Interface Control Register (SBIC) 282
Serial Operation Mode Register 0 (CSIM0) 281
Serial Operation Mode Register 1 (CSIM1) 287, 288
6-Bit Up/Down Counter Mode Register (UDM) 274
16-Bit Timer Mode Control Register (TMC0) 264
16-Bit Timer Output Control Register (TOC0) 265

T

Timer Clock Select Register 0 (TCL0) 263, 275
Timer Clock Select Register 1 (TCL1) 267
Timer Clock Select Register 2 (TCL2) 270, 272, 276

Timer Clock Select Register 3 (TCL3) 280, 285, 286

W

Watch Timer Mode Control Register (TMC2) 271
Watchdog Timer Mode Register (WDTM) 273

(ii) Register Symbol

A

ADIS: A/D Converter Input Select Register 279
ADM: A/D Converter Mode Register 278
ADTC: Automatic Data Transmit/Receive Control Register 289
ADTI: Automatic Data Transmit/Receive Interval Specification Register 290

C

CSIM0: Serial Operation Mode Register 0 281
CSIM1: Serial Operation Mode Register 1 ..... 287, 288

D

DSPM0: Display Mode Register 0 ..... 261, 292
DSPM1: Display Mode Register 1 ..... 262, 293

I

IF0H: Interrupt Request Flag Register 0H 297, 302
IF0L: Interrupt Request Flag Register 0L 297
IMS: Internal Memory Size Switching Register 312
INTM0: External Interrupt Mode Register 300
IXS: Internal Expansion RAM Size Switching Register 313

M

MK0H: Interrupt Mask Flag Register 0H 298, 302
MK0L: Interrupt Mask Flag Register 0L 298

O

OSTS: Oscillation Stabilization Time Select Register 303

P

PCC: Processor Clock Control Register 260
PMn: Port Mode Register n (n = 0 to 3, 7, 11, 12) 258
PR0H: Priority Specification Flag Register 0H 299
PR0L: Priority Specification Flag Register 0L 299
PSW: Program Status Word 301
PUO: Pull-Up Resistor Option Register 259

S

SBIC: Serial Bus Interface Control Register 282
SCS: Sampling Clock Select Register 301
SINT: Interrupt Timing Specification Register 284

T

TCL0: Timer Clock Select Register 0 ..... 263, 275
TCL1: Timer Clock Select Register 1 267
TCL2: Timer Clock Select Register 2 ..... 270, 272, 276
TCL3: Timer Clock Select Register 3 ..... 280, 285, 286
TMC0: 16-Bit Timer Mode Control Register 264
TMC1: 8-Bit Timer Mode Control Register 268
TMC2: Watch Timer Mode Control Register 271
TOC0: 16-Bit Timer Output Control Register 265
TOC1: 8-Bit Timer Output Control Register 269

U

UDM: 6-Bit Up/Down Counter Mode Register 274

W

WDTM: Watchdog Timer Mode Register 273

B.5 μPD78054/54Y, 78058F/58FY, 780058/58Y Subseries

(i) Register Name

A

A/D Converter Input Select Register (ADIS) 348
A/D Converter Mode Register (ADM) 347
Asynchronous Serial Interface Mode Register (ASIM) 374
Asynchronous Serial Interface Status Register (ASIS) 375
Automatic Data Transmit/Receive Control Register (ADTC) 366
Automatic Data Transmit/Receive Interval Time Specification Register (ADTI) 368

B

Baud Rate Generator Control Register (BRGC) 376

C

Capture/Compare Control Register 0 (CRC0) 333
Correction Address Register 0 (CORAD0) 400
Correction Address Register 1 (CORAD1) 400
Correction Control Register (CORCN) 400

D

D/A Converter Mode Register (DAM) 349

E

8-Bit Timer Mode Control Register 1 (TMC1) 337
8-Bit Timer Output Control Register (TOC1) 338
External Interrupt Mode Register 0 (INTM0) 386
External Interrupt Mode Register 1 (INTM1) 387, 388

I

Internal Expansion RAM Size Switching Register (IXS) 406
Internal Memory Size Switching Register (IMS) 393, 402, 403, 404, 405
Interrupt Mask Flag Register 0H (MK0H) 384
Interrupt Mask Flag Register 0L (MK0L) 384
Interrupt Mask Flag Register 1L (MK1L) 384, 390
Interrupt Request Flag Register 0H (IF0H) 383
Interrupt Request Flag Register 0L (IF0L) 383
Interrupt Request Flag Register 1L (IF1L) 383, 390
Interrupt Timing Specification Register (SINT) 356, 362

K

Key Return Mode Register (KRM) 391

M

Memory Expansion Mode Register (MM) 392

O

Oscillation Mode Select Register (OSMS) 330
Oscillation Stabilization Time Select Register (OSTS) 394

P

Port Mode Register n (PMn) (n = 0 to 7, 12, 13) 326, 327
Priority Specification Flag Register 0H (PR0H) 385
Priority Specification Flag Register 0L (PR0L) 385
Priority Specification Flag Register 1L (PR1L) 385
Processor Clock Control Register (PCC) 329
Program Status Word (PSW) 389
Pull-up Resistor Option Register H (PUOH) 328
Pull-up Resistor Option Register L (PUOL) 328

R

Real-Time Output Port Control Register (RTPC) 379
Real-Time Output Port Mode Register (RTPM) 379

S

Sampling Clock Select Register (SCS) 389
Serial Bus Interface Control Register (SBIC) 354, 360
Serial Interface Pin Select Register (SIPS) 378
Serial Operation Mode Register 0 (CSIM0) 352, 359
Serial Operation Mode Register 1 (CSIM1) 365
Serial Operation Mode Register 2 (CSIM2) 373
16-Bit Timer Mode Control Register (TMC0) 332
16-Bit Timer Output Control Register (TOC0) 334

T

Timer Clock Select Register 0 (TCL0) 331, 344
Timer Clock Select Register 1 (TCL1) 336
Timer Clock Select Register 2 (TCL2) 339, 341, 345
Timer Clock Select Register 3 (TCL3) 351, 358, 364

W

Watch Timer Mode Control Register (TMC2) 340
Watchdog Timer Mode Register (WDTM) 342

(ii) Register Symbol

A

ADIS: A/D Converter Input Select Register 348
ADM: A/D Converter Mode Register 347
ADTC: Automatic Data Transmit/Receive Control Register 366
ADTI: Automatic Data Transmit/Receive Interval Time Specification Register 368
ASIM: Asynchronous Serial Interface Mode Register 374
ASIS: Asynchronous Serial Interface Status Register 375

B

BRGC: Baud Rate Generator Control Register 376

C

CORAD0: Correction Address Register 0 400
CORAD1: Correction Address Register 1 400
CORCN: Correction Control Register 400
CRC0: Capture/Compare Control Register 0 333
CSIM0: Serial Operation Mode Register 0 ..... 352, 359
CSIM1: Serial Operation Mode Register 1 365
CSIM2: Serial Operation Mode Register 2 373

D

DAM: D/A Converter Mode Register 349

I

IF0H: Interrupt Request Flag Register 0H 383
IF0L: Interrupt Request Flag Register 0L 383
IF1L: Interrupt Request Flag Register 1L 383, 390
IMS: Internal Memory Size Switching Register 393, 402, 403, 404, 405
INTM0: External Interrupt Mode Register 0 386
INTM1: External Interrupt Mode Register 1 ..... 387, 388
IXS: Internal Expansion RAM Size Switching Register 406

K

KRM: Key Return Mode Register 391

M

MK0H: Interrupt Mask Flag Register 0H 384
MK0L: Interrupt Mask Flag Register 0L 384
MK1L: Interrupt Mask Flag Register 1L 384, 390
MM: Memory Expansion Mode Register 392

O

OSMS: Oscillation Mode Select Register 330
OSTS: Oscillation Stabilization Time Select Register 394

P

PCC: Processor Clock Control Register 329
PMn: Port Mode Register n (n = 0 to 7, 12, 13) 326, 327
PR0H: Priority Specification Flag Register 0H 385
PR0L: Priority Specification Flag Register 0L 385
PR1L: Priority Specification Flag Register 1L 385
PSW: Program Status Word 389
PUOH: Pull-up Resistor Option Register H 328
PUOL: Pull-up Resistor Option Register L 328

R

RTPC: Real-Time Output Port Control Register 379
RTPM: Real-Time Output Port Mode Register 379

S

SBIC: Serial Bus Interface Control Register 354, 360
SCS: Sampling Clock Select Register 389
SINT: Interrupt Timing Specification Register 356, 362

SIPS: Serial Interface Pin Select Register 378

T

TCL0: Timer Clock Select Register 0 ..... 331, 344
TCL1: Timer Clock Select Register 1 336
TCL2: Timer Clock Select Register 2 ..... 339, 341, 345
TCL3: Timer Clock Select Register 3 ..... 351,358, 364
TMC0: 16-Bit Timer Mode Control Register 332
TMC1: 8-Bit Timer Mode Control Register 1 337
TMC2: Watch Timer Mode Control Register 340
TOC0: 16-Bit Timer Output Control Register 334
TOC1: 8-Bit Timer Output Control Register 338

W

WDTM: Watchdog Timer Mode Register 342

B.6 μPD78064/64Y, 78064B, and 780308/308Y Subseries

(i) Register Name

A

A/D Converter Input Select Register (ADIS) 440
A/D Converter Mode Register (ADM) 439
Asynchronous Serial Interface Mode Register (ASIM) 456
Asynchronous Serial Interface Status Register (ASIS) 457

B

Baud Rate Generator Control Register (BRGC) 458

C

Capture/Compare Control Register 0 (CRC0) 425

E

8-Bit Timer Mode Control Register 1 (TMC1) 429
8-Bit Timer Output Control Register (TOC1) 430
External Interrupt Mode Register 0 (INTM0) 470
External Interrupt Mode Register 1 (INTM1) 471

I

Internal Expansion RAM Size Switching Register (IXS) 484
Internal Memory Size Switching Register (IMS) 482, 483
Interrupt Mask Flag Register 0H (MK0H) 468
Interrupt Mask Flag Register 0L (MK0L) 468
Interrupt Mask Flag Register 1L (MK1L) 468
Interrupt Request Flag Register 0H (IF0H) 467
Interrupt Request Flag Register 0L (IF0L) 467
Interrupt Request Flag Register 1L (IF1L) 467
Interrupt Timing Specification Register (SINT) 447, 453

K

Key Return Mode Register (KRM) 474

L

LCD Display Control Register (LCDC) 464
LCD Display Mode Register (LCDM) 463

O

Oscillation Mode Select Register (OSMS) 421
Oscillation Stabilization Time Select Register (OSTS) 475

P

Port Mode Register n (PMn) (n = 0 to 3, 7 to 11) 417
Priority Specification Flag Register 0H (PR0H) 469
Priority Specification Flag Register 0L (PR0L) 469
Priority Specification Flag Register 1L (PR1L) 469
Processor Clock Control Register (PCC) 420
Program Status Word (PSW) 472
Pull-Up Resistor Option Register H (PUOH) 418

Pull-Up Resistor Option Register L (PUOL) 418

S

Sampling Clock Select Register (SCS) 472
Serial Bus Interface Control Register (SBIC) 445, 451
Serial Interface Pin Select Register (SIPS) 459
Serial Operation Mode Register 0 (CSIM0) 443, 450
Serial Operation Mode Register 2 (CSIM2) 455
Serial Operation Mode Register 3 (CSIM3) 461
16-Bit Timer Mode Control Register (TMC0) 423
16-Bit Timer Output Control Register (TOC0) 426

T

Timer Clock Select Register 0 (TCL0) 422, 435
Timer Clock Select Register 1 (TCL1) 428
Timer Clock Select Register 2 (TCL2) 431, 433, 437
Timer Clock Select Register 3 (TCL3) 442, 449
Timer Clock Select Register 4 (TCL4) 460

W

Watch Timer Mode Control Register (TMC2) 432
Watchdog Timer Mode Register (WDTM) 434

(ii) Register Symbol

A

ADIS: A/D Converter Input Select Register 440
ADM: A/D Converter Mode Register 439
ASIM: Asynchronous Serial Interface Mode Register 456
ASIS: Asynchronous Serial Interface Status Register 457

B

BRGC: Baud Rate Generator Control Register 458

C

CRC0: Capture/Compare Control Register 0 425
CSIM0: Serial Operation Mode Register 0 ..... 443, 450
CSIM2: Serial Operation Mode Register 2 455
CSIM3: Serial Operation Mode Register 3 461

I

IF0H: Interrupt Request Flag Register 0H 467
IF0L: Interrupt Request Flag Register 0L 467
IF1L: Interrupt Request Flag Register 1L 467
IMS: Internal Memory Size Switching Register 482, 483
INTM0: External Interrupt Mode Register 0 470
INTM1: External Interrupt Mode Register 1 471
IXS: Internal Expansion RAM Size Switching Register 484

K

KRM: Key Return Mode Register 474

L

LCDC: LCD Display Control Register 464
LCDM: LCD Display Mode Register 463

M

MK0H: Interrupt Mask Flag Register 0H 468
MK0L: Interrupt Mask Flag Register 0L 468
MK1L: Interrupt Mask Flag Register 1L 468

O

OSMS: Oscillation Mode Select Register 421
OSTS: Oscillation Stabilization Time Select Register 475

P

PCC: Processor Clock Control Register 420
PMn: Port Mode Register n (n = 0 to 3, 7 to 11) 417
PR0H: Priority Specification Flag Register 0H 469
PR0L: Priority Specification Flag Register 0L 469
PR1L: Priority Specification Flag Register 1L 469
PSW: Program Status Word 472
PUOH: Pull-Up Resistor Option Register H 418
PUOL: Pull-Up Resistor Option Register L 418

S

SBIC: Serial Bus Interface Control Register 445, 451
SCS: Sampling Clock Select Register 472
SINT: Interrupt Timing Specification Register 447, 453
SIPS: Serial Interface Pin Select Register 459

T

TCL0: Timer Clock Select Register 0 ..... 422, 435
TCL1: Timer Clock Select Register 1 428
TCL2: Timer Clock Select Register 2 ..... 431, 433, 437
TCL3: Timer Clock Select Register 3 ..... 442, 449
TCL4: Timer Clock Select Register 4 460
TMC0: 16-Bit Timer Mode Control Register 423
TMC1: 8-Bit Timer Mode Control Register 1 429
TMC2: Watch Timer Mode Control Register 432
TOC0: 16-Bit Timer Output Control Register 426
TOC1: 8-Bit Timer Output Control Register 430

W

WDTM: Watchdog Timer Mode Register 434

B.7 μPD78078/78Y, 78075B/75BY, and 78070A/70AY Subseries

(i) Register Name

A

A/D Converter Input Select Register (ADIS) 524
A/D Converter Mode Register (ADM) 523
Asynchronous Serial Interface Mode Register (ASIM) 547
Asynchronous Serial Interface Status Register (ASIS) 548
Automatic Data Transmit/Receive Control Register (ADTC) 541
Automatic Data Transmit/Receive Interval Time Specification Register (ADTI) 542

B

Baud Rate Generator Control Register (BRGC) 549

C

Capture/Compare Control Register 0 (CRC0) 505
Correction Address Register 0 (CORAD0) 571
Correction Address Register 1 (CORAD1) 571
Correction Control Register (CORCN) 571

D

D/A Converter Mode Register (DAM) 525

E

8-Bit Timer Mode Control Register 1 (TMC1) 509
8-Bit Timer Output Control Register (TOC1) 510
8-Bit Timer Output Control Register 5 (TMC5) 513
8-Bit Timer Output Control Register 6 (TMC6) 514
External Bus Type Select Register (EBTS) 563
External Interrupt Mode Register 0 (INTM0) 555
External Interrupt Mode Register 1 (INTM1) 556

I

Internal Expansion RAM Size Switching Register (IXS) 573
Internal Memory Size Switching Register (IMS) 562, 563, 572
Interrupt Mask Flag Register 0H (MK0H) 554
Interrupt Mask Flag Register 0L (MK0L) 554
Interrupt Mask Flag Register 1L (MK1L) 554, 558
Interrupt Request Flag Register 0H (IF0H) 554
Interrupt Request Flag Register 0L (IF0L) 554
Interrupt Request Flag Register 1L (IF1L) 554, 558
Interrupt Timing Specification Register (SINT) 531, 537

K

Key Return Mode Register (KRM) 559

M

Memory Expansion Mode Register (MM) 561

O

Oscillation Mode Select Register (OSMS) 501
Oscillation Stabilization Time Select Register (OSTS) 564

P

Port Mode Register n (PMn) (n = 0 to 3, 5 to 10, 12, 13) 496
Port Mode Register n (PMn) (n = 0 to 3, 6, 7, 9, 10, 12, 13) 497
Priority Specification Flag Register 0H (PR0H) 555
Priority Specification Flag Register 0L (PR0L) 555
Priority Specification Flag Register 1L (PR1L) 555
Processor Clock Control Register (PCC) 499
Program Status Word (PSW) 557
Pull-up Resistor Option Register H (PUOH) 498
Pull-up Resistor Option Register L (PUOL) 498

R

Real-Time Output Port Control Register (RTPC) 551
Real-Time Output Port Mode Register (RTPM) 551

S

Sampling Clock Select Register (SCS) 557
Serial Bus Interface Control Register (SBIC) 529, 535
Serial Operation Mode Register 0 (CSIM0) 528, 534
Serial Operation Mode Register 1 (CSIM1) 540
Serial Operation Mode Register 2 (CSIM2) 546
16-Bit Timer Mode Control Register (TMC0) 504
16-Bit Timer Output Control Register (TOC0) 506

T

Timer Clock Select Register 0 (TCL0) 503, 520
Timer Clock Select Register 1 (TCL1) 508
Timer Clock Select Register 2 (TCL2) 515, 517, 521
Timer Clock Select Register 3 (TCL3) 527, 533, 539
Timer Clock Select Register 5 (TCL5) 511
Timer Clock Select Register 6 (TCL6) 512

W

Watch Timer Mode Control Register (TMC2) 516
Watchdog Timer Mode Register (WDTM) 518

(ii) Register Symbol

A

ADIS: A/D Converter Input Select Register 524
ADM: A/D Converter Mode Register 523
ADTC: Automatic Data Transmit/Receive Control Register 541
ADTI: Automatic Data Transmit/Receive Interval Time Specification Register 542
ASIM: Asynchronous Serial Interface Mode Register 547
ASIS: Asynchronous Serial Interface Status Register 548

B

BRGC: Baud Rate Generator Control Register 549

C

CORAD0: Correction Address Register 0 571
CORAD1: Correction Address Register 1 571
CORCN: Correction Control Register 571
CRC0: Capture/Compare Control Register 0 505
CSIM0: Serial Operation Mode Register 0 ..... 528, 534
CSIM1: Serial Operation Mode Register 1 540
CSIM2: Serial Operation Mode Register 2 546

D

DAM: D/A Converter Mode Register 525

E

EBTS: External Bus Type Select Register 563

I

IF0H: Interrupt Request Flag Register 0H 554
IF0L: Interrupt Request Flag Register 0L 554
IF1L: Interrupt Request Flag Register 1L 554, 558
IMS: Internal Memory Size Switching Register 562, 563, 572
INTM0: External Interrupt Mode Register 0 555
INTM1: External Interrupt Mode Register 1 556
IXS: Internal Expansion RAM Size Switching Register 573

K

KRM: Key Return Mode Register 559

M

MK0H: Interrupt Mask Flag Register 0H 554
MK0L: Interrupt Mask Flag Register 0L 554
MK1L: Interrupt Mask Flag Register 1L 554, 558
MM: Memory Expansion Mode Register 561

O

OSMS: Oscillation Mode Select Register 501
OSTS: Oscillation Stabilization Time Select Register 564

P

PCC: Processor Clock Control Register 499
PMn: Port Mode Register n (n = 0 to 3, 5 to 10, 12, 13) 496
PMn: Port Mode Register n (n = 0 to 3, 6, 7, 9, 10, 12, 13) 497
PR0H: Priority Specification Flag Register 0H 555
PR0L: Priority Specification Flag Register 0L 555
PR1L: Priority Specification Flag Register 1L 555
PSW: Program Status Word 557
PUOH: Pull-up Resistor Option Register H 498
PUOL: Pull-up Resistor Option Register L 498

R

RTPC: Real-Time Output Port Control Register 551
RTPM: Real-Time Output Port Mode Register 551

S

SBIC: Serial Bus Interface Control Register 529, 535
SCS: Sampling Clock Select Register 557
SINT: Interrupt Timing Specification Register 531, 537

T

TCL0: Timer Clock Select Register 0 ..... 503, 520
TCL1: Timer Clock Select Register 1 508
TCL2: Timer Clock Select Register 2 ..... 515, 517, 521
TCL3: Timer Clock Select Register 3 ..... 527, 533, 539
TCL5: Timer Clock Select Register 5 511
TCL6: Timer Clock Select Register 6 512
TMC0: 16-Bit Timer Mode Control Register 504
TMC1: 8-Bit Timer Mode Control Register 1 509
TMC2: Watch Timer Mode Control Register 516
TMC5: 8-Bit Timer Output Control Register 5 513
TMC6: 8-Bit Timer Output Control Register 6 514
TOC0: 16-Bit Timer Output Control Register 506
TOC1: 8-Bit Timer Output Control Register 510

W

WDTM: Watchdog Timer Mode Register 518

B.8 μPD78083 Subseries

(i) Register Name

A

A/D Converter Input Select Register (ADIS) 593
A/D Converter Mode Register (ADM) 592
Asynchronous Serial Interface Mode Register (ASIM) 595
Asynchronous Serial Interface Status Register (ASIS) 596

B

Baud Rate Generator Control Register (BRGC) 597

E

8-Bit Timer Output Control Register n (TMCn) (n = 5, 6) 586
External Interrupt Mode Register 0 (INTM0) 603
External Interrupt Mode Register 1 (INTM1) 603

I

Internal Memory Size Switching Register (IMS) 609
Interrupt Mask Flag Register 0H (MK0H) 601
Interrupt Mask Flag Register 0L (MK0L) 601
Interrupt Mask Flag Register 1L (MK1L) 601
Interrupt Request Flag Register 0H (IF0H) 601
Interrupt Request Flag Register 0L (IF0L) 601
Interrupt Request Flag Register 1L (IF1L) 601

O

Oscillation Mode Select Register (OSMS) 584
Oscillation Stabilization Time Select Register (OSTS) 605

P

Port Mode Register n (PMn) (n = 0, 1, 3, 5, 7, 10) 582
Priority Specification Flag Register 0H (PR0H) 602
Priority Specification Flag Register 0L (PR0L) 602
Priority Specification Flag Register 1L (PR1L) 602
Processor Clock Control Register (PCC) 583
Program Status Word (PSW) 604
Pull-up Resistor Option Register H (PUOH) 582
Pull-up Resistor Option Register L (PUOL) 582

S

Serial Operation Mode Register 2 (CSIM2) 594

T

Timer Clock Select Register 0 (TCL0) 589
Timer Clock Select Register 2 (TCL2) 587, 590
Timer Clock Select Register n (TCLn) (n = 5, 6) 585

W

Watchdog Timer Mode Register (WDTM) 588

(ii) Register Symbol

A

ADIS: A/D Converter Input Select Register 593
ADM: A/D Converter Mode Register 592
ASIM: Asynchronous Serial Interface Mode Register 595
ASIS: Asynchronous Serial Interface Status Register 596

B

BRGC: Baud Rate Generator Control Register 597

C

CSIM2: Serial Operation Mode Register 2 594

I

IF0H: Interrupt Request Flag Register 0H 601
IF0L: Interrupt Request Flag Register 0L 601
IF1L: Interrupt Request Flag Register 1L 601
IMS: Internal Memory Size Switching Register 609
INTM0: External Interrupt Mode Register 0 603
INTM1: External Interrupt Mode Register 1 603

M

MK0H: Interrupt Mask Flag Register 0H 601
MK0L: Interrupt Mask Flag Register 0L 601
MK1L: Interrupt Mask Flag Register 1L 601

O

OSMS: Oscillation Mode Select Register 584
OSTS: Oscillation Stabilization Time Select Register 605

P

PCC: Processor Clock Control Register 583
PMn: Port Mode Register n (n = 0, 1, 3, 5, 7, 10) 582
PR0H: Priority Specification Flag Register 0H 602
PR0L: Priority Specification Flag Register 0L 602
PR1L: Priority Specification Flag Register 1L 602
PSW: Program Status Word 604
PUOH: Pull-up Resistor Option Register H 582
PUOL: Pull-up Resistor Option Register L 582

T

TCL0: Timer Clock Select Register 0 589
TCL2: Timer Clock Select Register 2 ..... 587, 590
TCLn: Timer Clock Select Register n (n = 5, 6) 585
TMCn: 8-Bit Timer Output Control Register n (n = 5, 6) 586

W

WDTM: Watchdog Timer Mode Register 588

[MEMO]