

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Phase-out/Discontinued
 μ PA1500
**N-CHANNEL POWER MOS FET ARRAY
SWITCHING USE**
DESCRIPTION

The μ PA1500 is N-channel Power MOS FET Array that built in 4 circuits and surge absorber designed for solenoid, motor and lamp driver.

FEATURES

- 4 V driving is possible
- Low On-state Resistance
 $R_{DS(on)} \leq 0.18 \Omega$ MAX. ($V_{GS} = 10$ V, $I_D = 2$ A)
 $R_{DS(on)} \leq 0.24 \Omega$ MAX. ($V_{GS} = 4$ V, $I_D = 2$ A)
- Surge Absorber, built in.

ORDERING INFORMATION

Part Number	Package
μ PA1500H	12-Pin SIP

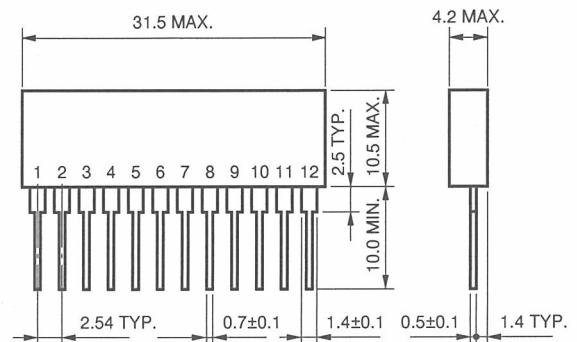
ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	$V_{GSS(AC)}$	+20, -10	V
Drain Current (DC)	$I_{D(DC)}$	± 3.0	A/unit
Drain Current (pulse)	$I_{D(pulse)^*}$	± 12	A/unit
Repetitive Peak Reverse Voltage	V_{RRM}	65	V
Diode Forward Current	$I_{F(av)}$	3.0	A/unit
Total Power Dissipation	P_T^{**}	4.0	W
Channel Temperature	T_{CH}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

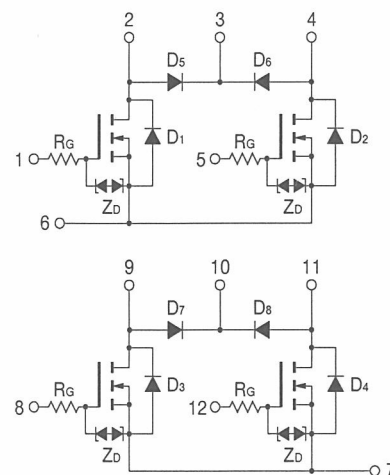
* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

** 4 circuits, $T_A = 25^\circ\text{C}$

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

**PACKAGE DIMENSIONS
(in millimeters)**

ELECTRODE CONNECTION

- 1, 5, 8, 12 GATE
 2, 4, 9, 11 DRAIN, ANODE
 6, 7 SOURCE
 3, 10 CATHODE

CONNECTION DIAGRAM


- D_1 to D_4 : Body Diode
 D_5 to D_8 : Surge Absorber
 Z_D : Gate to Source Protection Diode
 R_G : Gate Input Resistance 450 Ω TYP.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Leakage Current	I _{oss}	V _{DS} = 60 V, V _{GS} = 0			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = +20, -10 V, V _{DS} = 0			±10	μA
Gate to Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0		2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 2 A	2.4			S
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 2 A		0.13	0.18	Ω
	R _{DS(on)2}	V _{GS} = 4 V, I _D = 2 A		0.17	0.24	Ω
Input Capacitance	C _{iss}	V _{DS} = 10 V		550		pF
Output Capacitance	C _{oss}	V _{GS} = 0		220		pF
Reverse Transfer Capacitance	C _{rss}	f = 1.0 MHz		25		pF
Turn-On Delay Time	t _{d(on)}	I _D = 2 A		80		ns
Rise Time	t _r	V _{GS} = 10 V		170		ns
Turn-Off Delay Time	t _{d(off)}	V _{DD} = 30 V		1 200		ns
Fall Time	t _f	R _L = 15 Ω		380		ns
Total Gate Charge	Q _G	See Fig. 1				
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		13		nC
Gate to Drain Charge	Q _{GD}	I _D = 3 A		2		nC
		V _{DD} = 48 V		4		nC
Diode Forward Voltage	V _{F(S-D)}	See Fig. 2				
		I _D = 3 A, V _{GS} = 0		1.2		V

SURGE ABSORBER (Diode, built in) 1 Unit

Repetitive Peak Reverse Current	I _{RRM}	V _R = 65 V			10	μA
Diode Forward Voltage	V _F	I _F = 3 A		1.2	1.5	V

Phase-out/Discontinued

Fig.1 Switching Test Circuit

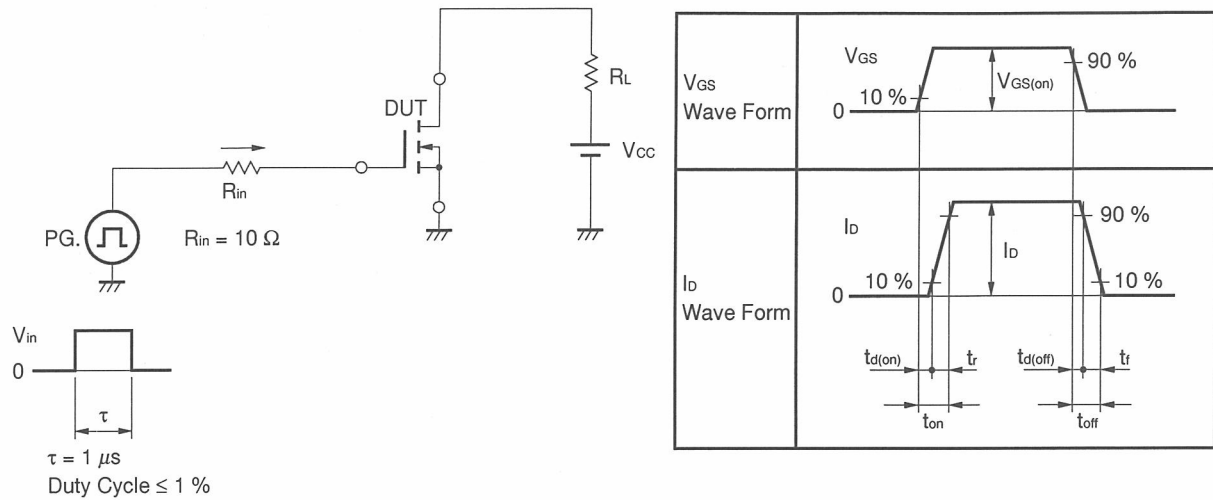
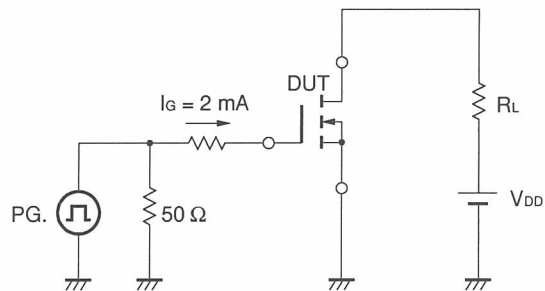
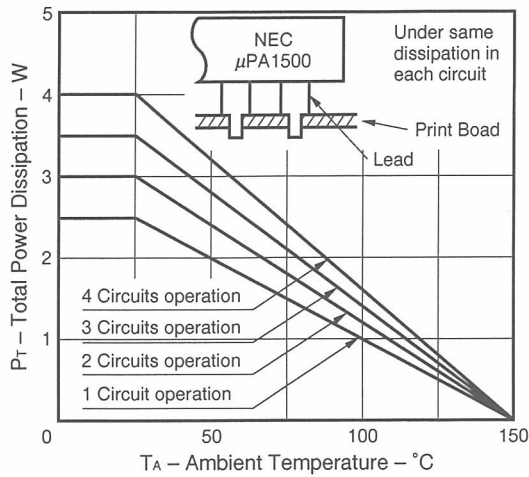


Fig. 2 Gate Charge Test Circuit

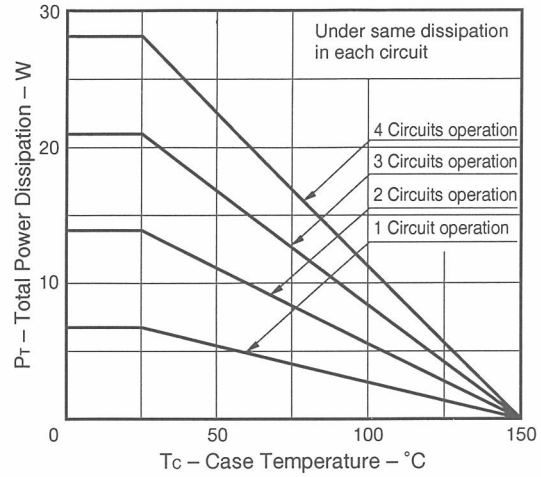


TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$)

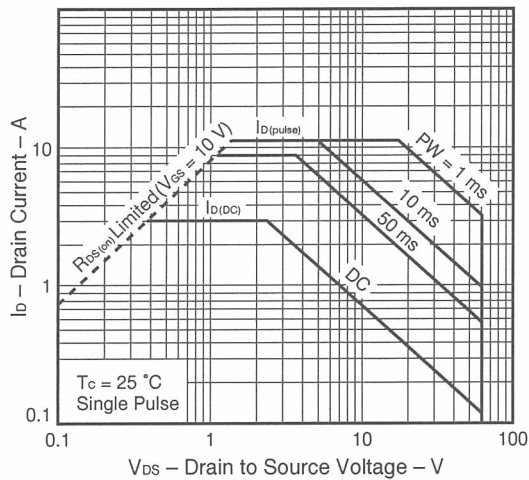
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



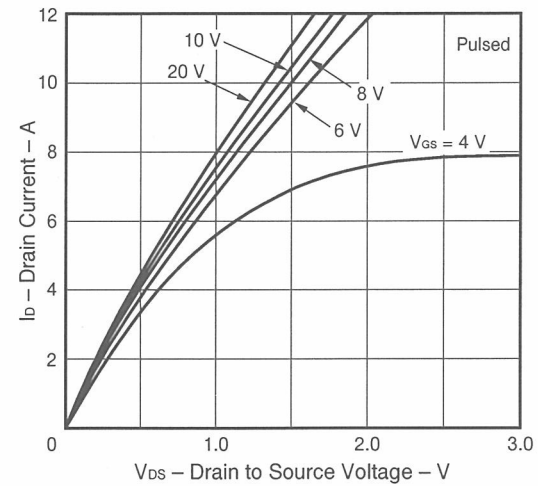
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



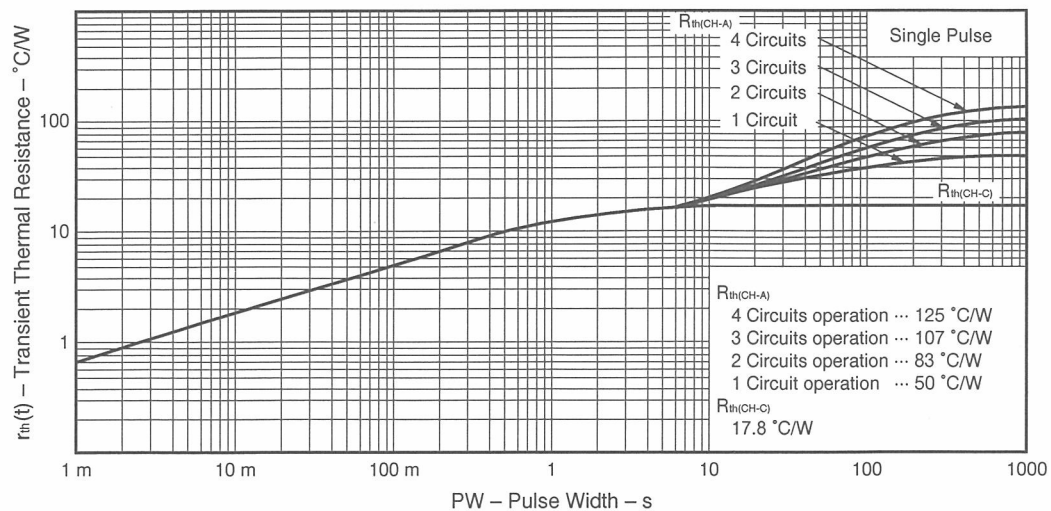
FORWARD BIAS SAFE OPERATING AREA



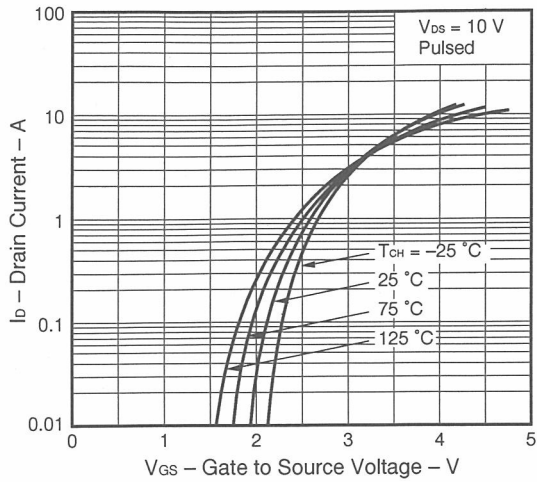
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



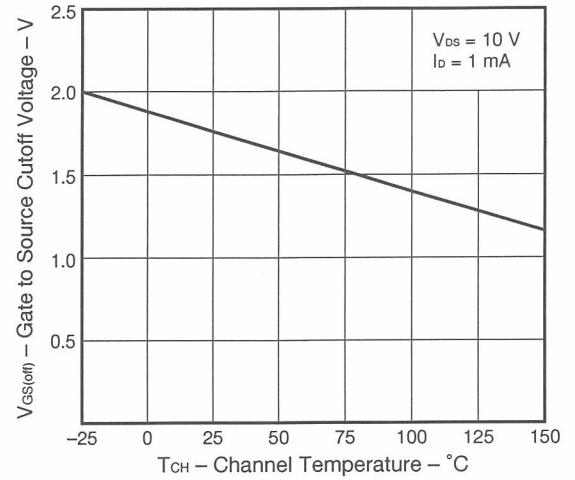
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



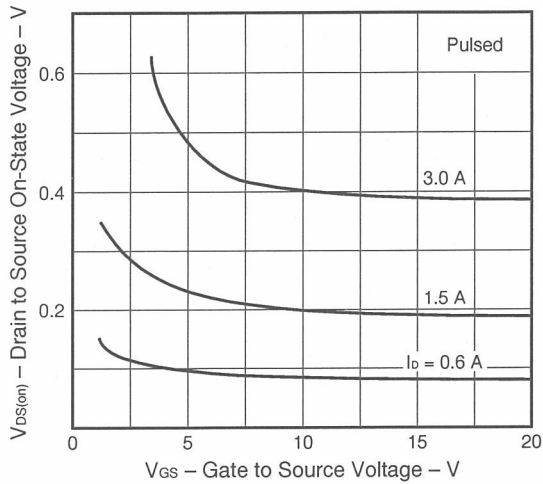
TRANSFER CHARACTERISTIC



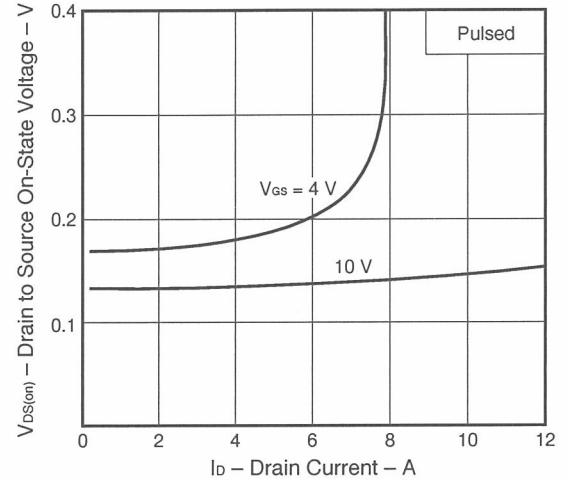
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



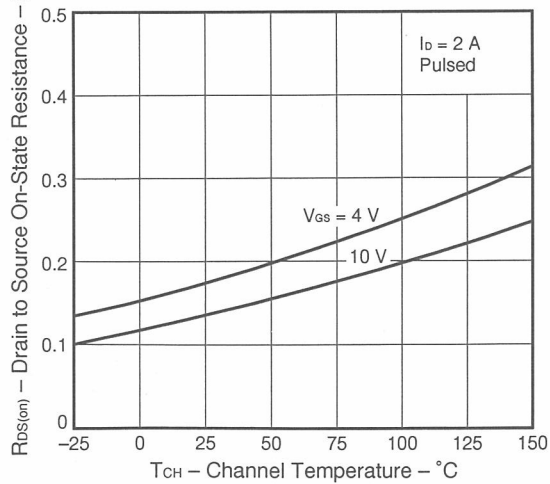
DRAIN TO SOURCE ON-STATE VOLTAGE vs. GATE TO SOURCE VOLTAGE



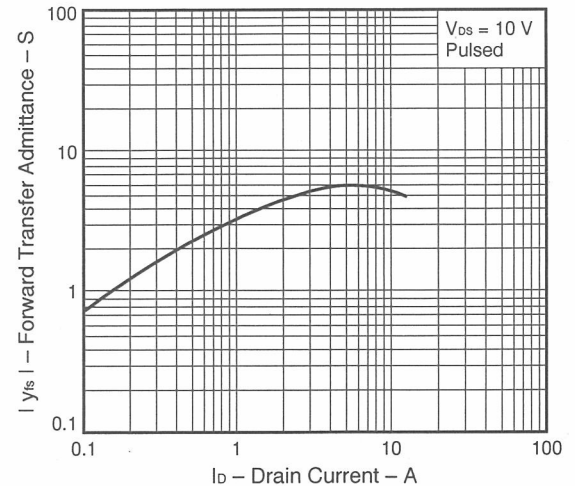
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



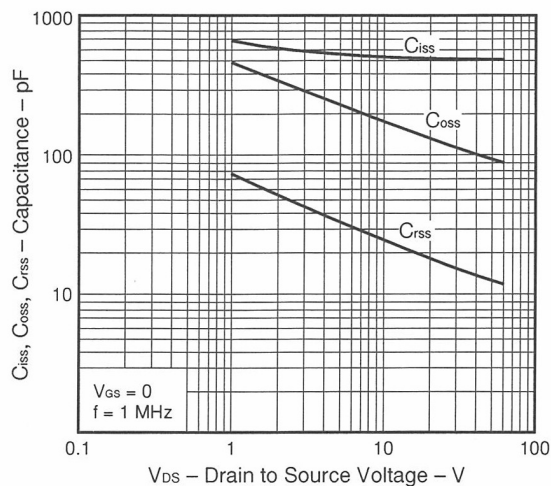
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



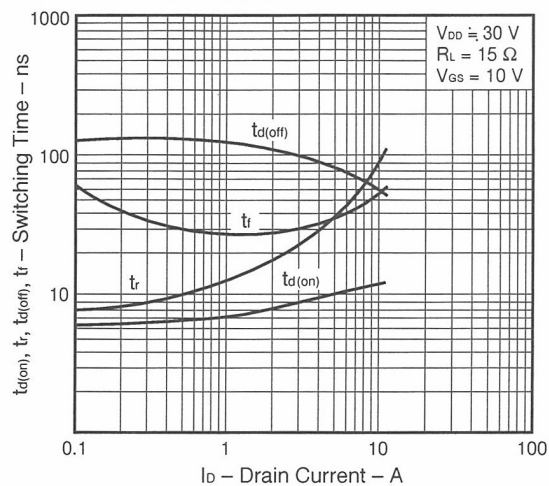
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



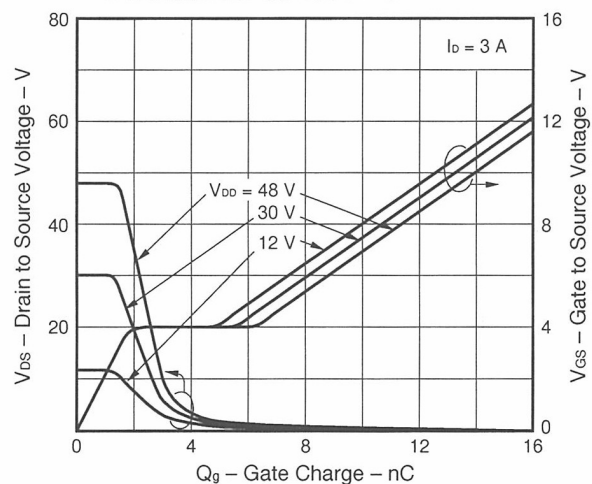
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



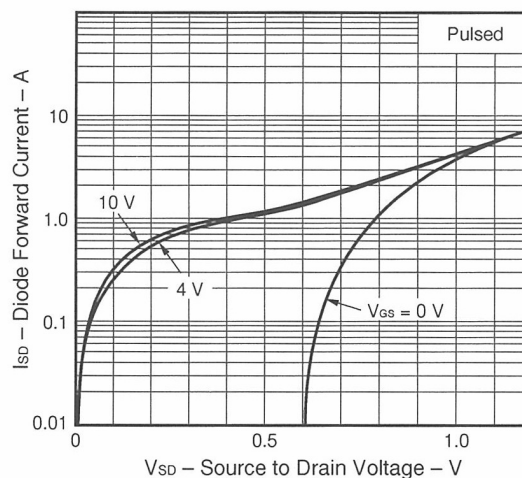
SWITCHING TIME vs. DRAIN CURRENT



DYNAMIC INPUT CHARACTERISTIC



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	IEI-1207
Semiconductor device package manual	IEI-1213
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	MF-1134
Power MOS FET features and application switching power supply	TEA-1034
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

Phase-out/Discontinued

[MEMO]

[MEMO]

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Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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