DESCRIPTION

This document describes the specifications for the F0502 600MHz to 1000MHz dual path Sampling IF (SIF) Receiver used in Multi-mode, Multi-carrier BaseStation Receivers. Refer to the Part Number# Matrix below describing the frequency coverage of the complete series. This series is offered with high side or low side LO injection options for all UTRA bands and offers significantly better Noise and Distortion performance than currently available solutions. IF frequencies from 60MHz to 275MHz are supported.

The F0502 SIF provides 28.2dB gain and offers 47dB gain adjustment in 1dB steps and is designed to operate with a single 5V supply. Nominally, the device offers +44dBm Output IP3 using 480mA of I_{CC}. Alternately one can configure the device in low current (LC) mode to reduce power consumption to less than 1.95 watts.

This device is packaged in a 10x10 68-pin TQFN with 50Ω single-ended RF input and 200Ω differential IF output impedances for ease of integration into the receiver lineup. The 200Ω differential IF output can easily be matched to 100Ω differential per the application drawing.

COMPETITIVE ADVANTAGE

Renesas' Zero-Distortion™ mixer in combination with interstage filtering and Renesas' proprietary FlatNoise™ DVGA improves system SNR to the point where the external SAW filter can be eliminated. Both $IP3_O$ and NF are kept virtually flat while gain is backed off, enhancing SNR significantly under high level interferer conditions, and greatly benefiting 2G/3G/4G Multi-Carrier IF sampling receivers. In addition, total power consumption is reduced by 35% compared to conventional solutions.

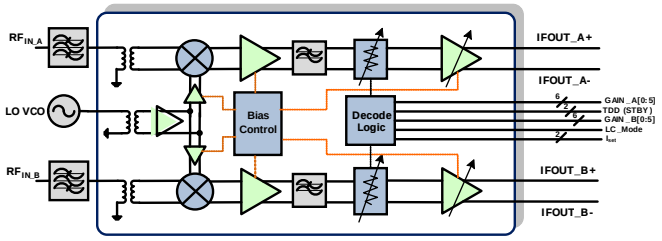
- ✓ No external SAW is needed
- ✓ Reduced Power Consumption by 35%
- ✓ NF and OIP3 virtually flat for first 13dB gain reduction

The fast-settling, parallel mode gain step of 1.0 dB coupled with the excellent differential non-linearity allow for SNR to be maximized further by targeting the minimum necessary gain in small, accurate increments. The matched output does not require a terminating resistor, thus the gain and distortion performance are preserved when driving Bandpass Anti-Alias filters.

FEATURES

- Dual Channel for Diversity / MIMO Systems
- Combines FlatNoise™ and Zero- Distortion™ technology
- 28.2dB Total Power Gain
- 47dB gain control range
- 1dB Gain Steps
- Ultra linear +44dBm $IP3_O$
- Low NF: 9.6dB at G_{MAX}
- 50Ω input impedance
- Matched 100Ω differential output impedance
- Ultra high +20.2dBm P1dBo
- Independent path standby mode
- Constant LO impedance in STBY mode
- 6 bit parallel control
- 60MHz to 275MHz IF frequency range
- Excellent 2nd Harmonic Rejection
- I_{CC} = 480mA STD Mode, 390mA LC Mode
- 10 x 10 mm 68-pin VFQFPN package

DEVICE BLOCK DIAGRAM



PART NUMBER# MATRIX

Part#	RF Freq Range (MHz)	UTRA bands	IF Freq Range (MHz)	Typ. Gain (dB)	Injection
F0502	600 - 1000	5,6,8,12,13,14,17 18,19,20	60 - 275	28.2	Low & High Side
F0552	1710 - 2050	1,2,3,4,9,10,23, 25,33,34,35,36, 37,39	60 – 450	29	Low & High Side
F0562	2300 – 2700	7,38,40,41	60 – 450	29	Low & High Side

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ABSOLUTE MAXIMUM RATINGS

Parameter / Condition	Symbol	Min	Max	Unit
Vcc to GND	Vcc	-0.3	+5.5	V
A[5:0], B[5:0], TDD_A, TDD_B, LCMode	V_{CNTL}	-0.3	Vcc + 0.25	V
MX_IFA+, MX_IFA-, MX_IFB+, MX_IFB-	V_{MX}	-0.3	Vcc + 0.25	V
IFOUT_A+, IFOUT_A-, IFOUT_B+, IFOUT_B-	V_{IF}	+1	Vcc + 0.3	V
LO1_ADJ	V_{LO1ADJ}	+1	+3	V
LO2_ADJ	V_{LO2ADJ}	+2.1	+4	V
MX_IF_BiasA, MX_IF_BiasB	V_{BIAS}	-0.3	+0.3	V
ISET_A, ISET_B to GND	V_{ISET}	-0.3	+2.2	V
LO_IN, RFIN_A, RFIN_B	V_{RF}	-0.3	+0.3	V
RF Input Power (RFIN_A, RFIN_B)	P_{RFMAX}		+20	dBm
LO Input Power (LO_IN)	P_{LOMAX}		+20	dBm
Continuous Power Dissipation	P_{DISS}		3	W
Operating Case Temperature (Tc)	T_{OP}	-40	+105	°C
Maximum Junction Temperature	T_{Jmax}		+150	°C
Storage Temperature Range	T_{ST}	-65	+150	°C
Lead Temperature (soldering, 10s)	T_{LEAD}		+260	°C
ESD Voltage– HBM (Per JESD22-A114)	V_{ESDHBM}		Class 1C (1000V)	
ESD Voltage – CDM (Per JESD22-C101)	V_{ESDCDM}		Class III (500V)	

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL AND MOISTURE CHARACTERISTICS

θ_{JA} (Junction – Ambient)	25°C/W
θ_{JC} (Junction – Case) The Case is defined as the exposed paddle	3°C /W
Moisture Sensitivity Rating (Per J-STD-020)	MSL 3

Truth Table – Channel A & B

Gain Set Target	Gain CodeWord	Code Name	Gain Set Target	Gain CodeWord	Code Name	Gain Set Target	Gain CodeWord	Code Name
27	000000	G_{27}	5	010110	G_{5}	-17	101100	G_{-17}
26	000001	G_{26}	4	010111	G_{4}	-18	101101	G_{-18}
25	000010	G_{25}	3	011000	G_{3}	-19	101110	G_{-19}
24	000011	G_{24}	2	011001	G_{2}	-20	101111	G_{-20}
23	000100	G_{23}	1	011010	G_{1}	-20	110000	G_{-20}
22	000101	G_{22}	0	011011	G_{0}	-20	110001	G_{-20}
21	000110	G_{21}	-1	011100	G_{-1}	-20	110010	G_{-20}
20	000111	G_{20}	-2	011101	G_{-2}	-20	110011	G_{-20}
19	001000	G_{19}	-3	011110	G_{-3}	-20	110100	G_{-20}
18	001001	G_{18}	-4	011111	G_{-4}	-20	110101	G_{-20}
17	001010	G_{17}	-5	100000	G_{-5}	-20	110110	G_{-20}
16	001011	G_{16}	-6	100001	G_{-6}	-20	110111	G_{-20}
15	001100	G_{15}	-7	100010	G_{-7}	-20	111000	G_{-20}
14	001101	G_{14}	-8	100011	G_{-8}	-20	111001	G_{-20}
13	001110	G_{13}	-9	100100	G_{-9}	-20	111010	G_{-20}
12	001111	G_{12}	-10	100101	G_{-10}	-20	111011	G_{-20}
11	010000	G_{11}	-11	100110	G_{-11}	-20	111100	G_{-20}
10	010001	G_{10}	-12	100111	G_{-12}	-20	111101	G_{-20}
9	010010	G_{9}	-13	101000	G_{-13}	-20	111110	G_{-20}
8	010011	G_{8}	-14	101001	G_{-14}	-20	111111	G_{-20}
7	010100	G_{7}	-15	101010	G_{-15}			
6	010101	G_{6}	-16	101011	G_{-16}			

F0502 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CC}	All V_{CC} pins	4.75		5.25	V
LO Power	P_{LO}		-3		+3	dBm
Operating Temperature Range	T_{CASE}	Case Temperature	-40		+105	°C
RF Frequency Range	F_{RF}		600		1000	MHz
LO Frequency Range	F_{LO}		600		1225	
IF Frequency Range	F_{IF}		60		275	

F0502 SPECIFICATION

F0502 Typical Application Circuit, when operated as a Sampling IF Receiver, V_{CC} = +5.00V, T_C = +25°C, F_{RF} = 850MHz, F_{IF} = 184MHz, F_{LO} = 1034MHz, P_{LO} = 0 dBm, Max gain setting, IF output power = +3dBm per tone, TDD_ = LOW, STD Mode, unless otherwise stated. EVkit PCB, connector and IF transformer losses are de-embedded unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Logic Input High	V_{IH}	For all control pins	***1.07***			V
Logic Input Low	V_{IL}	For all control pins			***0.68***	V
Logic Current	I_{IH}, I_{IL}	For all control pins	***-150***		***10***	µA
Total Supply Current	I_{cc}	**STD Mode**		480	***545***[1]	mA
		LC Mode		390	***440***	
		Standby Mode STBY = V_{IH}		26	***36***	
Conversion Power Gain	G	**STD Mode**	***26.2***	28.2	***30.2***	dB
		LC Mode	***26.2***	28.2	***30.2***	
		STD Mode Max attenuation		-18.8		
Gain Control Range	G_{RANGE}			47		dB
Step Size	G_{STEP}			1		dB
Differential Gain Error	DNL	Between any two adjacent 1dB steps		0.1	0.2[2]	dB
Integral Gain Error	INL	Error vs. line (G_{27} Ref)		0.2	***0.8***	dB
Phase Error	IPE	Maximum phase change between G_{MAX} and any state down to G_{-14}		2		deg
Noise Figure	NF	**STD Mode**		9.6	10.6	dB
		STD Mode at G_{MAX} – 10dB		9.6	10.6	
		LC Mode		9.3	10.3	
		LC Mode at G_{MAX} – 10dB		9.3	10.3	
Noise Figure with Blocker	NF_{BLK}	Desired RF = 800MHz Blocker = 700MHz LO = 984MHz P_{IN} = +4dBm Gain = -1dB		17.5	19	dB

F0502 SPECIFICATION (CONTINUED)

F0502 Typical Application Circuit, when operated as a Sampling IF Receiver, V_{CC} = +5.00V, T_C = +25°C, F_{RF} = 850MHz, F_{IF} = 184MHz, F_{LO} = 1034MHz, P_{LO} = 0 dBm, Max gain setting, IF output power = +3dBm per tone, TDD_ = LOW, STD Mode, unless otherwise stated. EVkit PCB, connector and IF transformer losses are de-embedded unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Turn-on time	T_{SETT1}	Gate STBY from V_{IH} to V_{IL} Time for IF Signal to settle to within 0.1 dB of final value			0.17	0.20	µs
Attenuator Adjustment Settling Time	T_{1dB}	Any two Adjacent 1dB Steps +/-0.10 dB Pout settling			17.5	25	ns
Output IP3	OIP3	**STD Mode** 800 KHz Tone Separation		***40***	44		dBm
		STD Mode Gain = G_{MAX} – 10dB, Pout = +1dBm per tone 800 KHz Tone Separation -40C ≤ Tcase ≤ +105C IF = 138MHz, LO = 988MHz IF = 184MHz, LO = 1034MHz IF = 276MHz, LO = 1126MHz		40	44		
		LC Mode 800 KHz Tone Separation		40	44		
Input IP3	IIP3	**STD Mode** Gain = G_{MAX} – 22dB, Pin = - 5dBm/tone 800 KHz Tone Separation		21	25		dBm
		LC Mode Gain = G_{MAX} – 22dB, Pin = -10dBm/tone 800 KHz Tone Separation			21		
1 dB Output Compression	OP1dB	**STD Mode**		***17.5***	20.2		dBm
		LC Mode		***17.5***	20.2		
1 dB Input Compression	IP1dB	Gain = G_{MAX} – 30dB	**STD Mode**	7.7	8.7		dBm
			LC Mode	6.5	7		

F0502 SPECIFICATION (CONTINUED)

F0502 Typical Application Circuit, when operated as a Sampling IF Receiver, V_{CC} = +5.00V, T_C = +25°C, F_{RF} = 850MHz, F_{IF} = 184MHz, F_{LO} = 1034MHz, P_{LO} = 0 dBm, Max gain setting, IF output power = +3dBm per tone, TDD_ = LOW, STD Mode, unless otherwise stated. EVkit PCB, connector and IF transformer losses are de-embedded unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units
2LO – 2RF Rejection		**STD Mode** Frequency = F_{RF} + ½ F_{IF} P_{RF} = -27dBm			-75	-65	dBc
		STD Mode, Gain = G_{MAX} – 22dB, Frequency = F_{RF} + ½ F_{IF} P_{RF} = -5dBm			-69	-60	
		LC Mode Frequency = F_{RF} + ½ F_{IF} P_{RF} = -27dBm			-73	-60	
		LC Mode, Gain = G_{MAX} – 22dB, Frequency = F_{RF} + ½ F_{IF} P_{RF} = -27dBm			-69	-60	
2nd Harmonic	HD2	P_{RF} = -27 dBm	**STD Mode**		-81	-70	dBc
			LC Mode		-80	-70	
3rd Harmonic	HD3	P_{RF} = -27 dBm	**STD Mode**		-94	-80	dBc
			LC Mode		-94	-80	
Channel Isolation	ISO_C	RFIN_A applied, IFOUT_A compared with IFOUT_B	**STD Mode**	45	50		dB
			LC Mode	45	50		
LO to IF Leakage	ISO_{LI}	**STD Mode**			-60	-55	dBm
		LC Mode			-60	-55	
RF to IF leakage	ISO_{RI}	**STD Mode**			-80	-70	dBm
		LC Mode			-80	-70	
LO to RF leakage	ISO_{LR}				-44		dBm
RFIN Impedance	Z_{RFIN}	Single Ended			50		Ω
LO Port Impedance	Z_{LO}	Single Ended			50		
IF Output Impedance	Z_{IF}	Differential			200		

1 – Items in min/max columns in ***bold italics*** are Guaranteed by Test using BOM1 components supporting 4:1 output impedance transformation to 50Ω

2 – Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization using BOM2 components supporting 2:1 output impedance transformation to 100□

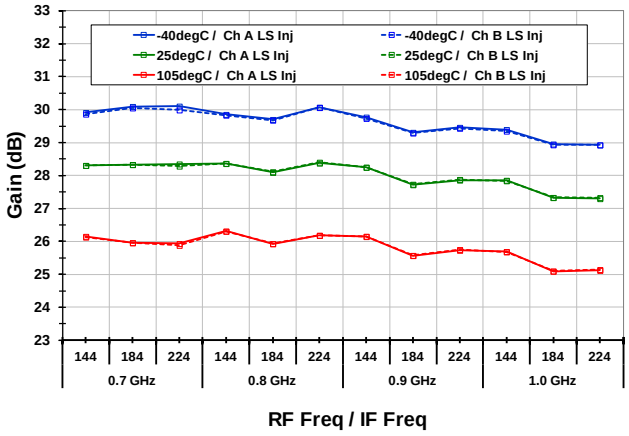
TYPICAL OPERATING CONDITIONS (184 MHZ IF CENTER)

Unless otherwise noted, the following conditions apply:

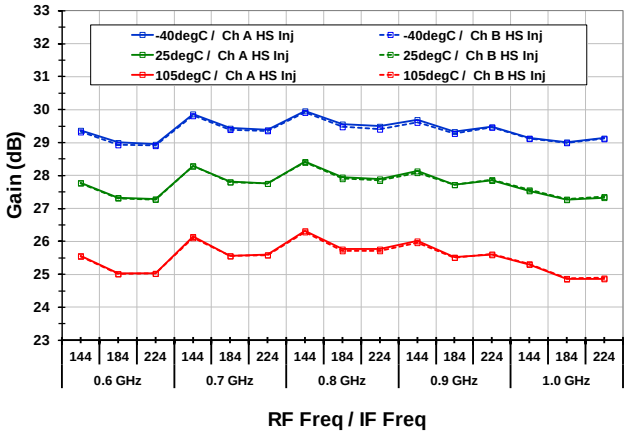
- Applications circuit for 100□ differential load with 184MHz +/- 40MHz BW into 2:1 transformer. See schematic in BOM section.
- Pout ~ +3dBm
- Measurement on Channel A
- P_{IN} from -27dBm to -5dBm per tone (Gain Setting Adjusted to yield Pout ~ +3dBm)
- Tone Spacing = 800KHz
- Device configured in Standard Mode with High Side Injection
- T_{CASE} = 25C, V_{CC} = 5.00V, LO Power = 0dBm
- RF Frequency: 915MHz
- IF Frequency: 184MHz
- IF Transformer losses are de-embedded
- Input RF trace and connector losses are de-embedded
- Listed Temperatures are Case Temperature (T_C = Case Temperature)
- Where noted, T_A or T_{AMB} = Ambient Temperature

TOCs [MAX GAIN, STD MODE, IF = 184MHZ +/- 40MHZ] GAIN, OIP3, OIP2 (-1-)

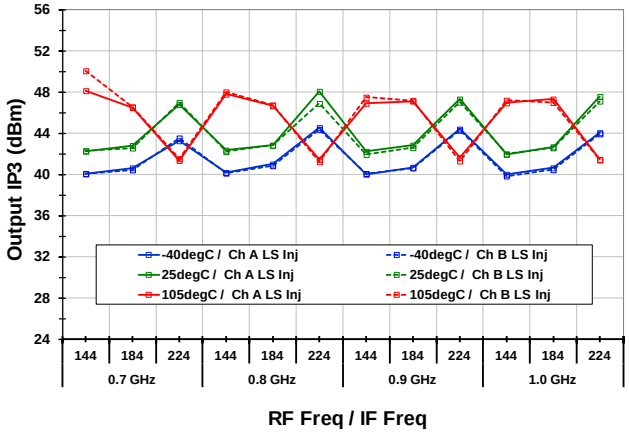
RF Gain vs. T_{CASE} [low side inj.]



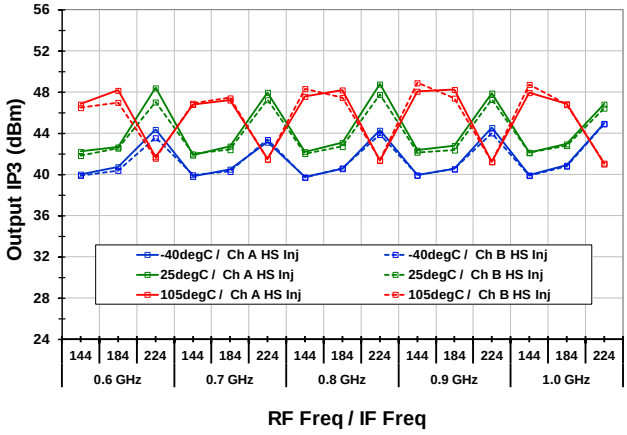
RF Gain vs. T_{CASE} [high side inj.]



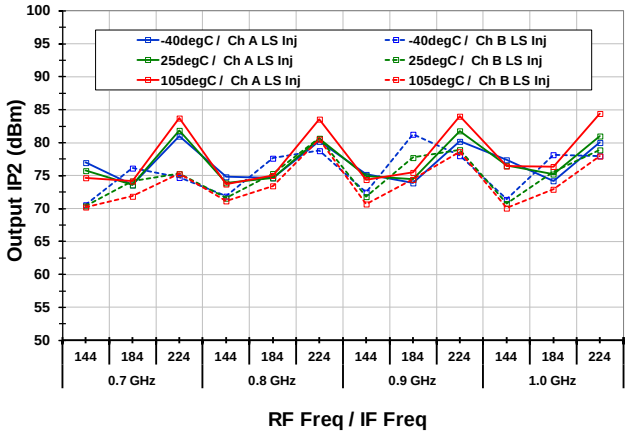
Output IP3 vs. T_{CASE} [low side inj.]



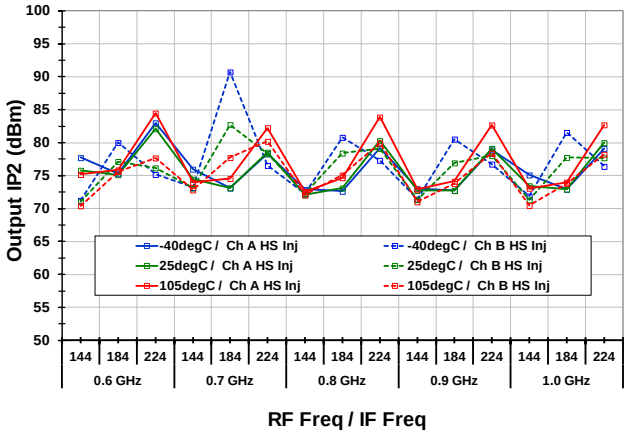
Output IP3 vs. T_{CASE} [high side inj.]



Output IP2 vs. T_{CASE} [low side inj.]

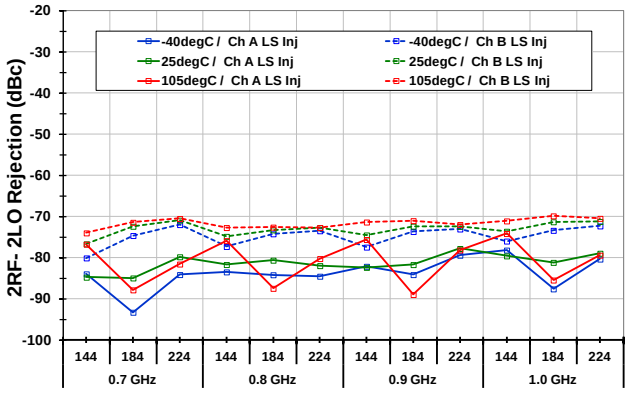


Output IP2 vs. T_{CASE} [high side inj.]

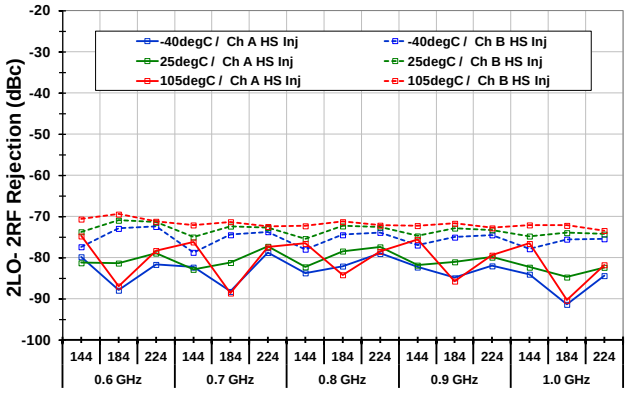


TOCs [Max Gain, STD Mode, IF = 184MHz +/- 40MHz] 2x2, L-I, DC Current (-2-)

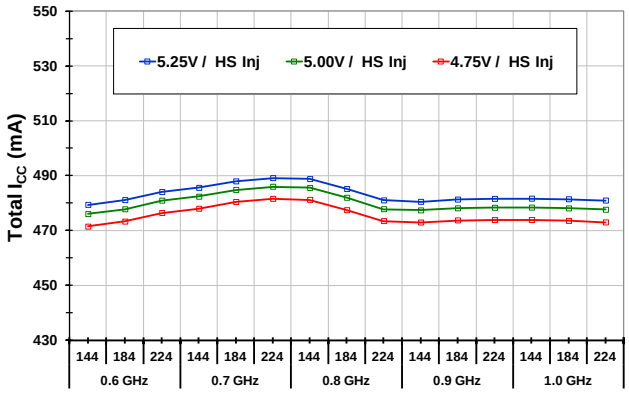
2RF-2LO vs. TCASE [low side inj.]



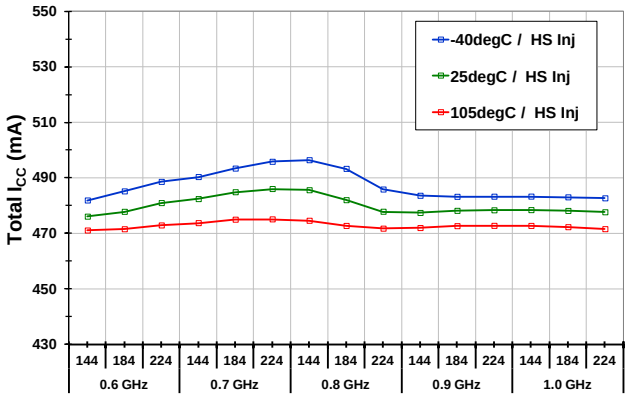
2LO-2RF vs. TCASE [high side inj.]



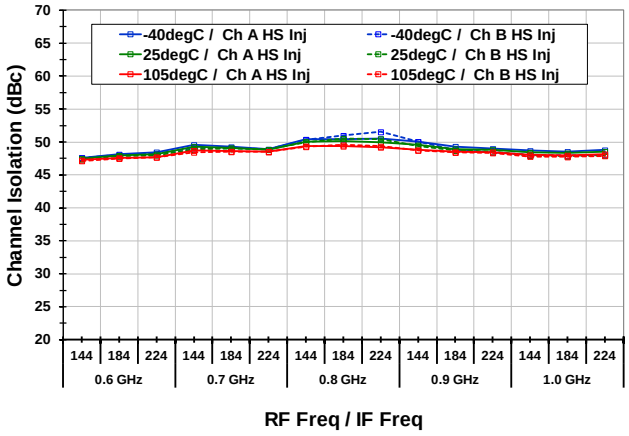
Total Current Drain [v VSUPPLY, high side inj.]



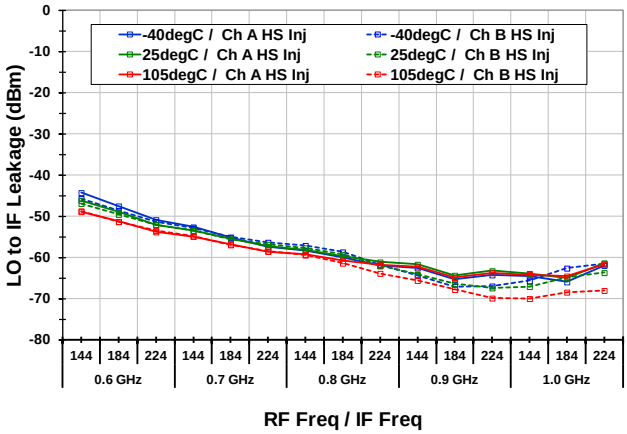
Total Current Drain [v Temp, high side inj.]



Channel Isolation [high side inj.]

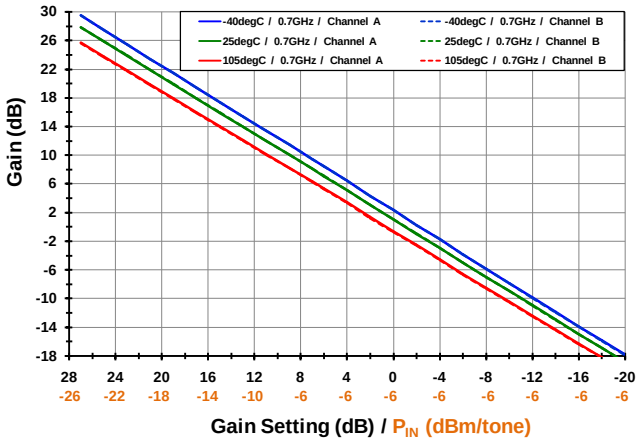


LO to IF Leakage [high side inj.]

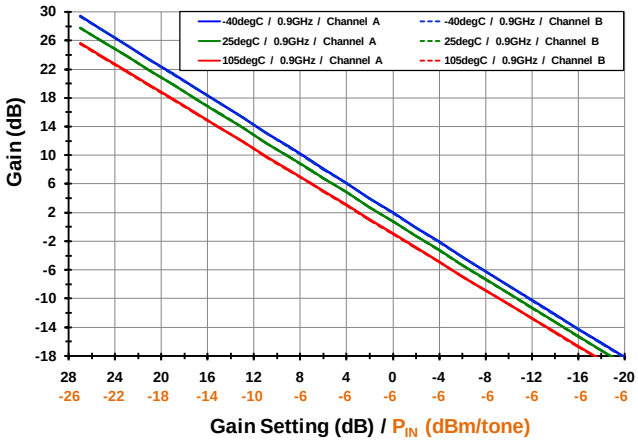


TOCs [Swept Gain, STD Mode, IF = 184MHz, HS Injection] Gain, OIP3, IIP3 (-3-)

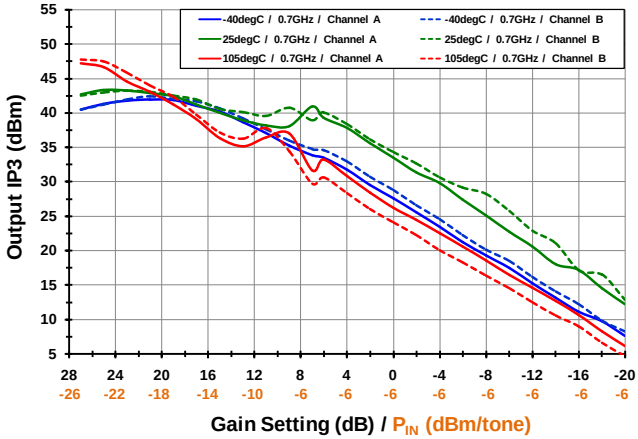
RF Gain [RF=0.7 GHz]



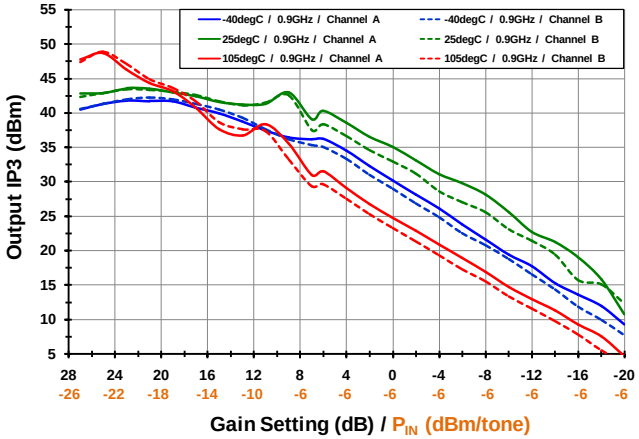
RF Gain [RF=0.9 GHz]



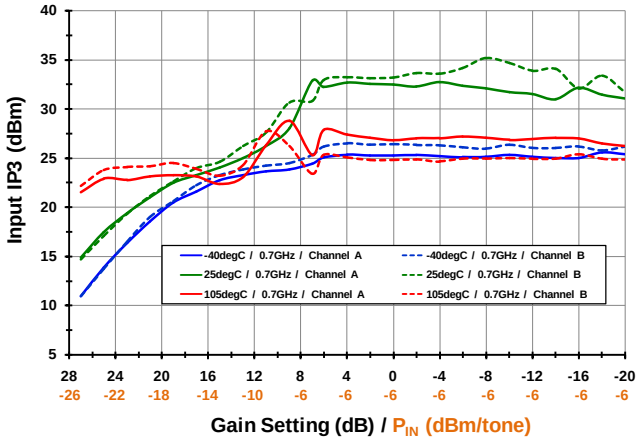
Output IP3 [RF=0.7 GHz]



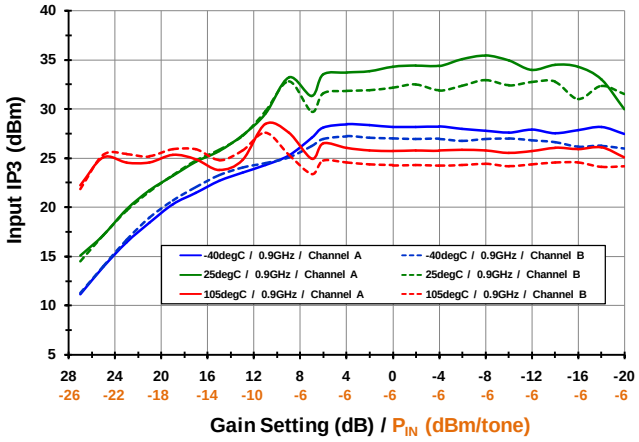
Output IP3 [RF=0.9 GHz]



Input IP3 [RF=0.7 GHz]

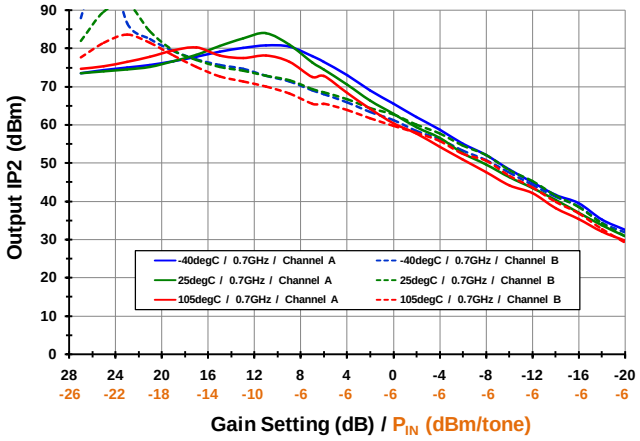


Input IP3 [RF=0.9 GHz]

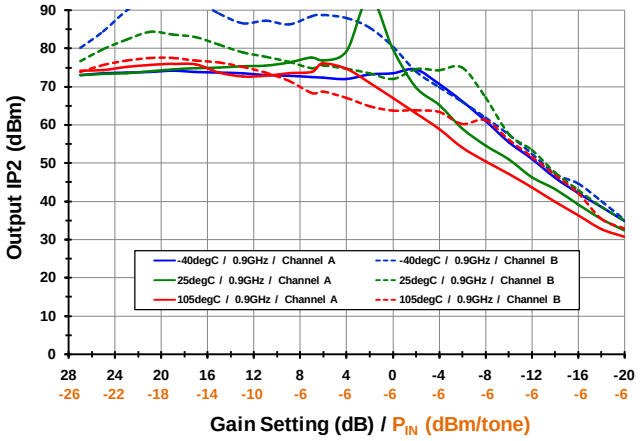


TOCs [Swept Gain, STD Mode, IF = 184MHz, HS Injection] OIP2, IIP2, 2x2 (-4-)

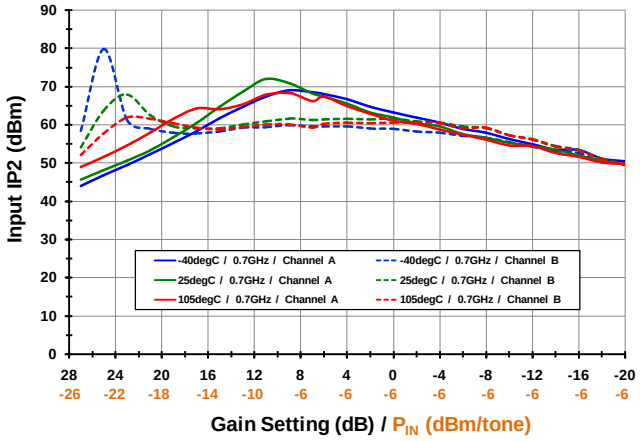
Output IP2 [RF=0.7 GHz]



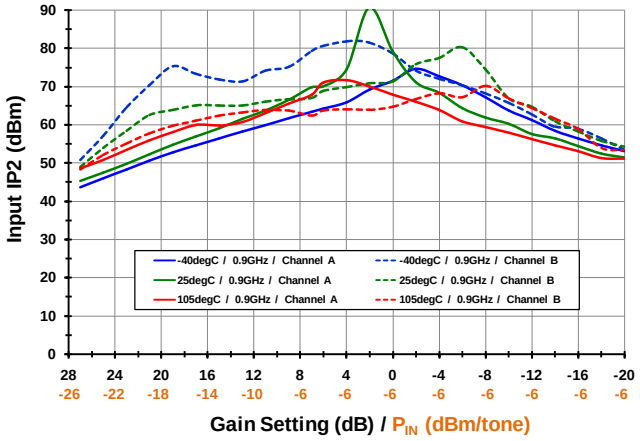
Output IP2 [RF=0.9 GHz]



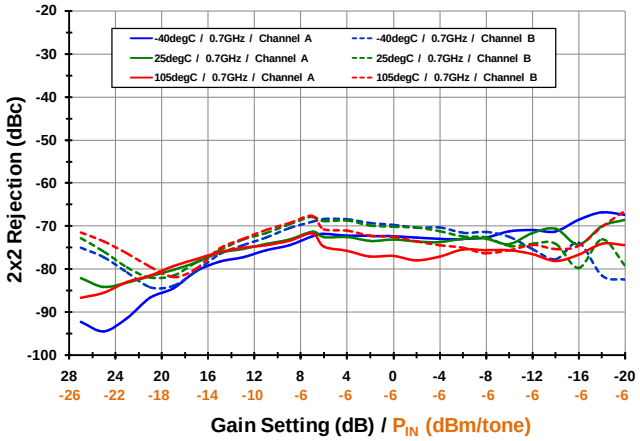
Input IP2 [RF=0.7 GHz]



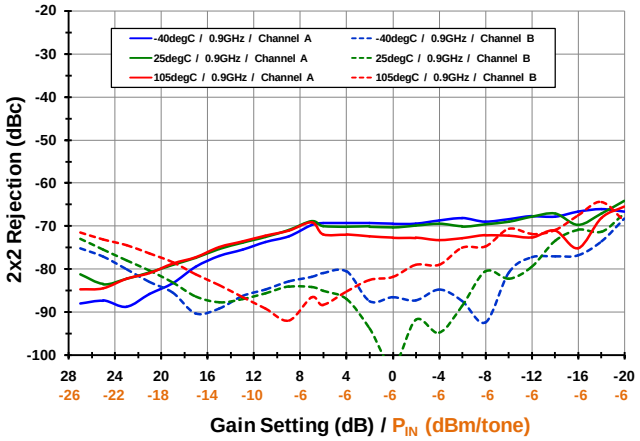
Input IP2 [RF=0.9 GHz]



2LO-2RF Rejection [RF=0.7 GHz]

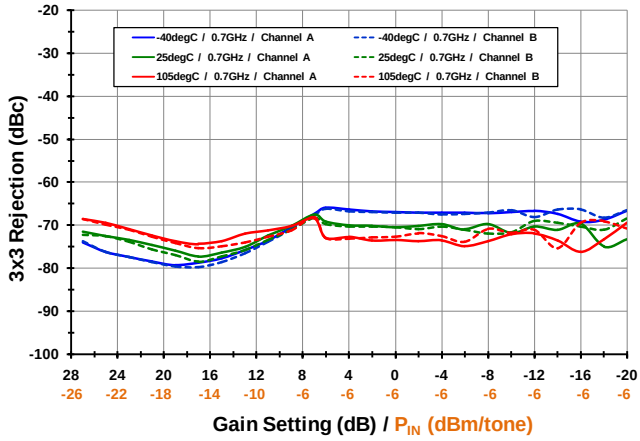


2LO-2RF Rejection [RF=0.9 GHz]

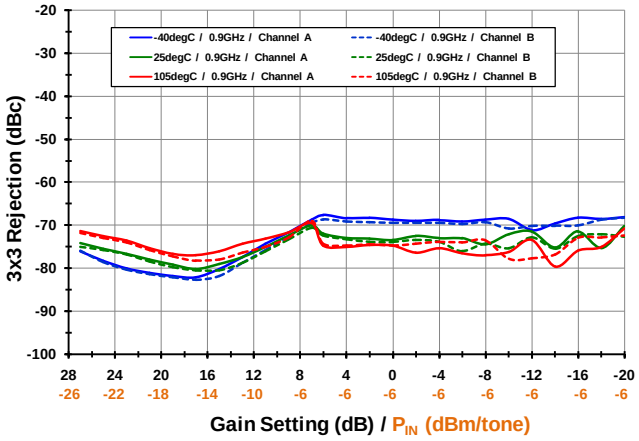


TOCs [Swept Gain, STD Mode, IF = 184MHz, HS Injection] 3x3, L-I, R-I (-5-)

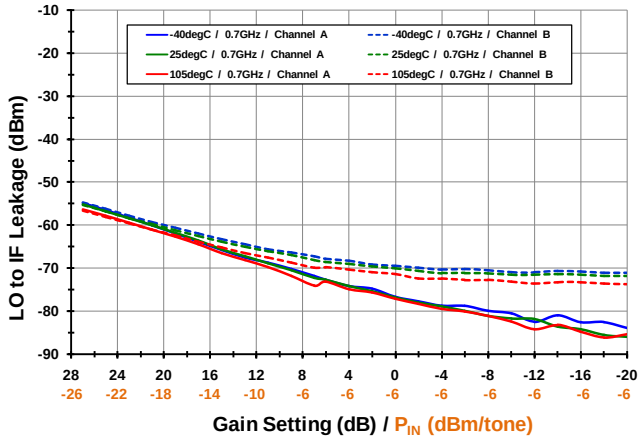
3LO-3RF Rejection [RF=0.7 GHz]



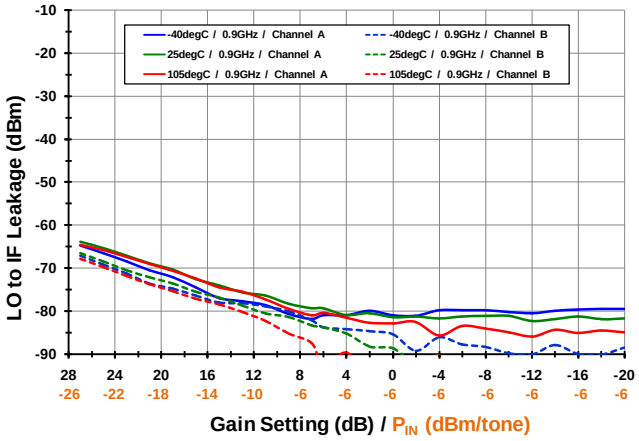
3LO-3RF Rejection [RF=0.9 GHz]



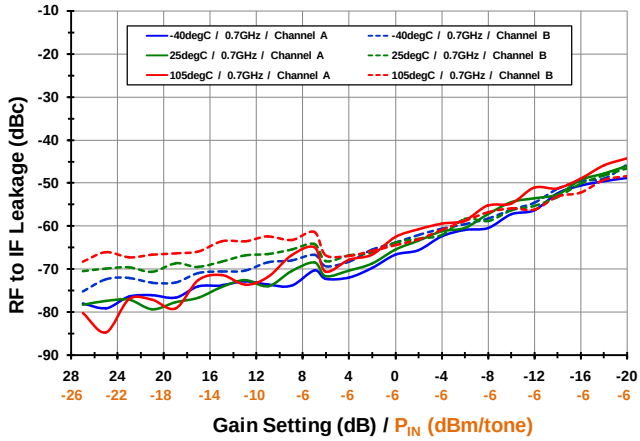
LO to IF Leakage [RF=0.7 GHz]



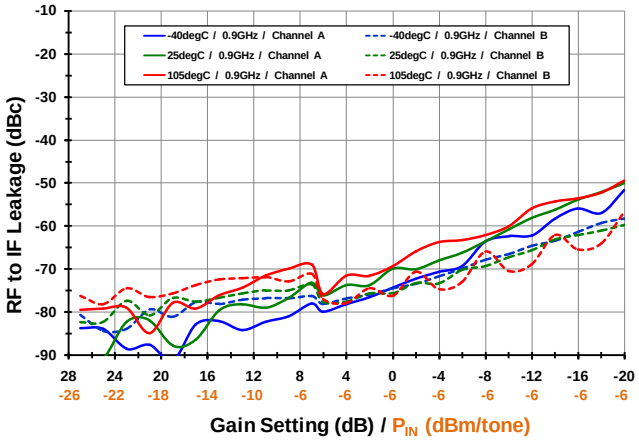
LO to IF Leakage [RF=0.9 GHz]



RF to IF Leakage [RF=0.7 GHz]

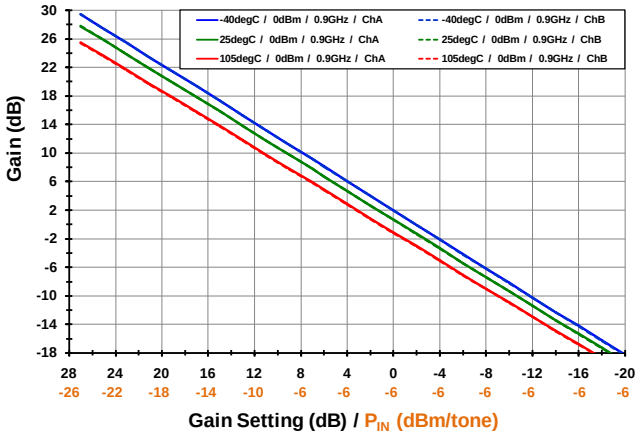


RF to IF Leakage [RF=0.9 GHz]

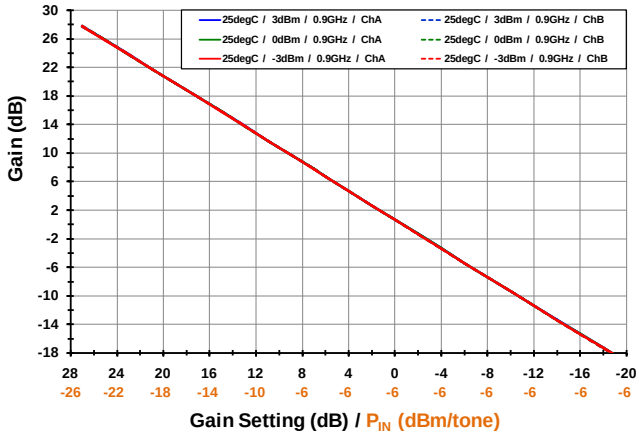


TOCs [Swept Gain, *LC Mode*, RF=900MHz, IF = 184MHz, HS Injection] Gain, OIP3, IIP3 (-6-)

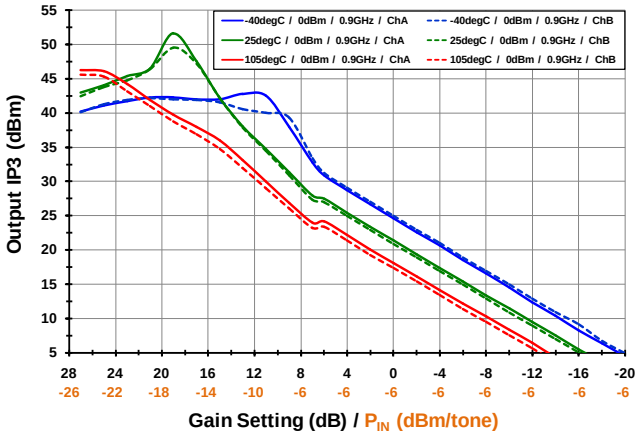
RF Gain [v Temp]



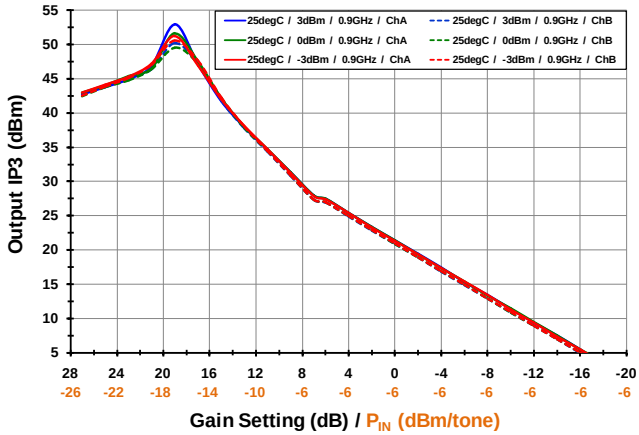
RF Gain [v LO Power]



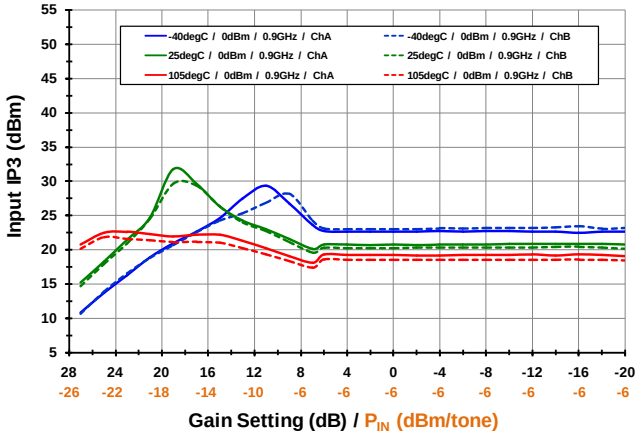
Output IP3 [v Temp]



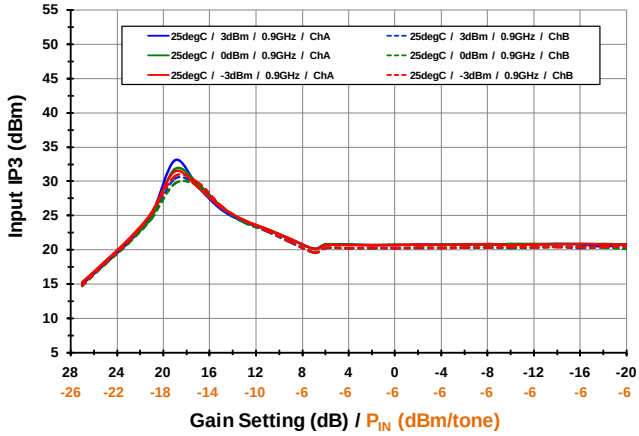
Output IP3 [v LO Power]



Input IP3 [v Temp]

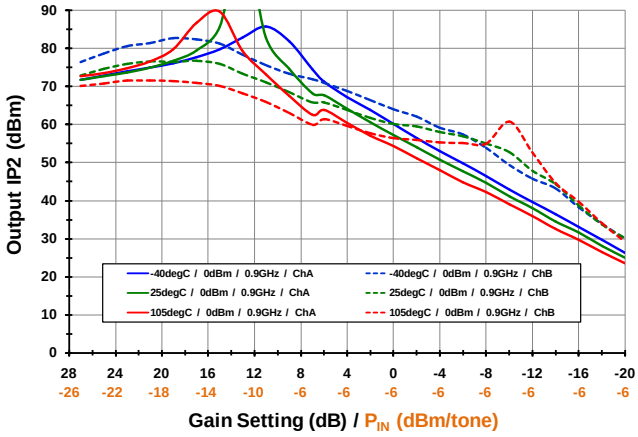


Input IP3 [v LO Power]

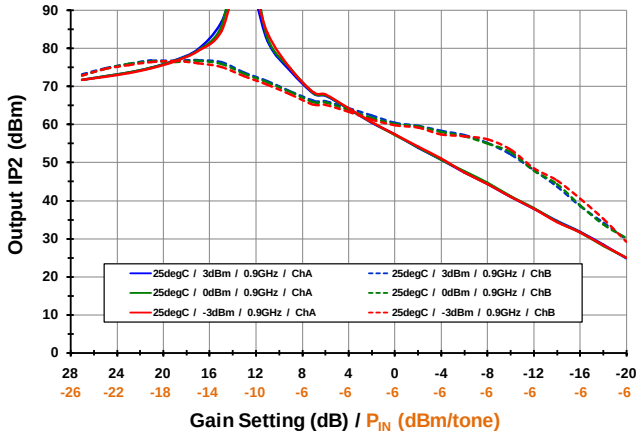


TOCs [Swept Gain, *LC Mode*, RF=900MHz, IF = 184MHz, HS Injection] OIP2, Chan Iso, 2x2 (-7-)

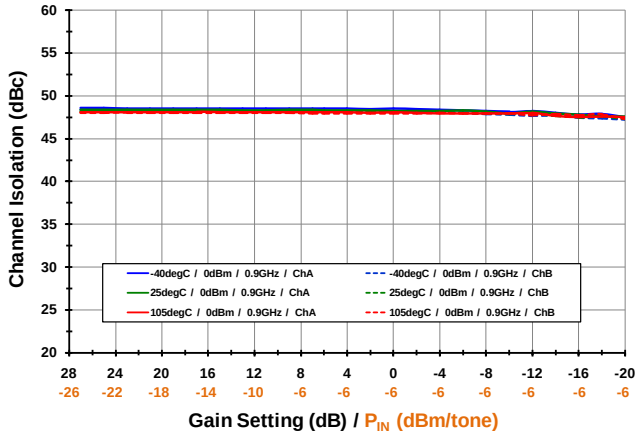
Output IP2 [v Temp]



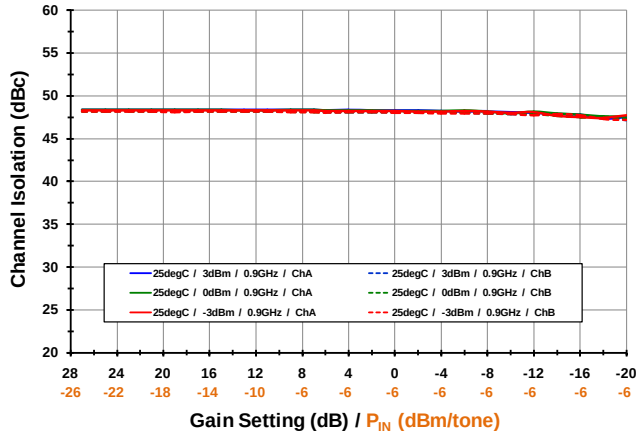
Output IP2 [v LO Power]



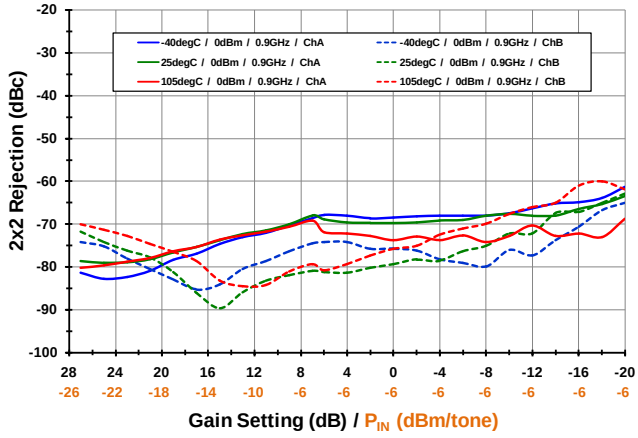
Channel Isolation [v Temp]



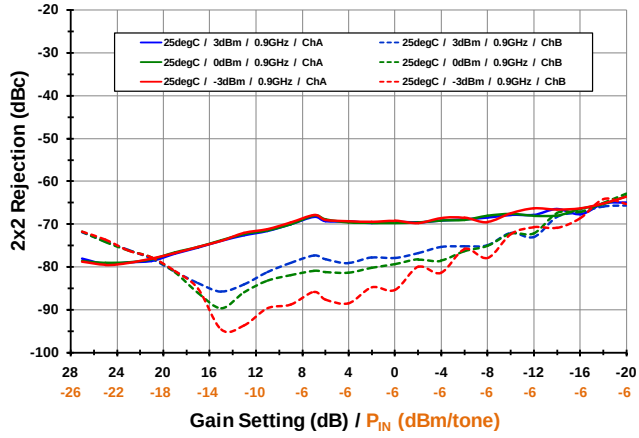
Channel Isolation [v LO Power]



2LO-2RF Rejection [v Temp]

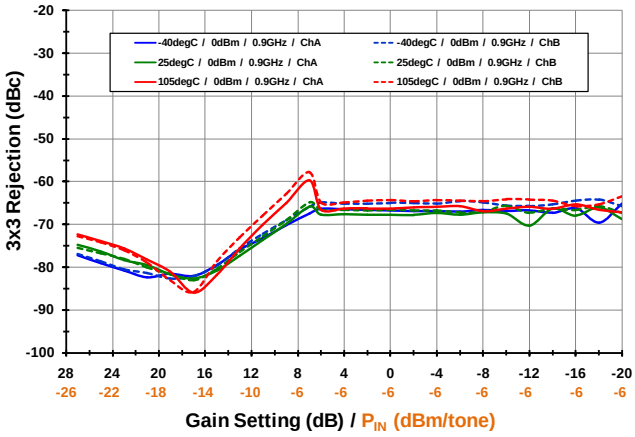


2LO-2RF Rejection [v LO Power]

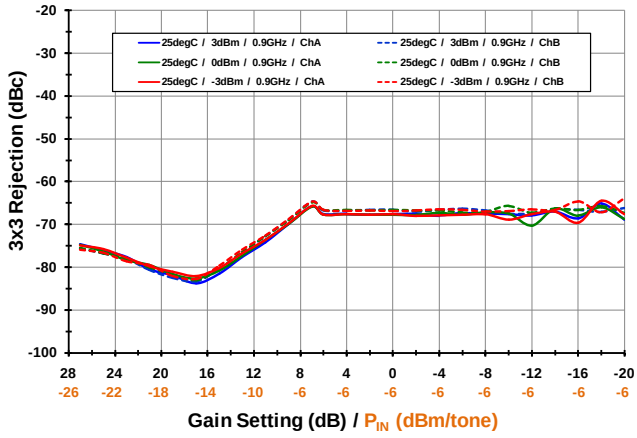


TOCs [Swept Gain, *LC Mode*, RF=900MHz, IF = 184MHz, HS Inj] 3x3, L-I, DC Current, R-I (-8-)

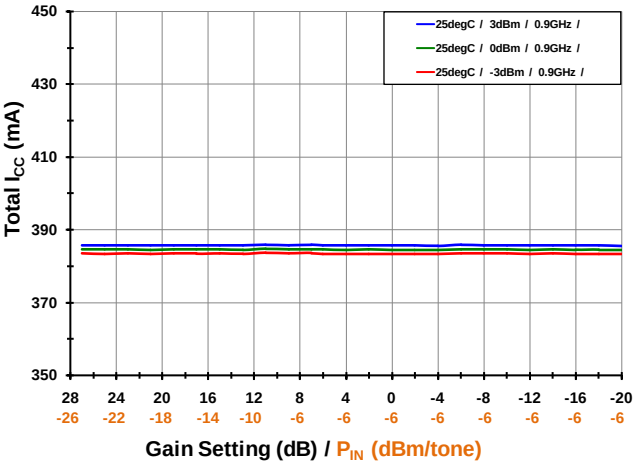
3LO-3RF Rejection [v Temp]



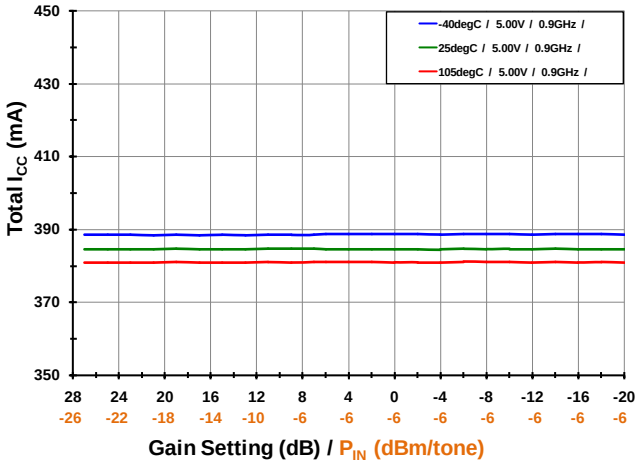
3LO-3RF Rejection [v LO Power]



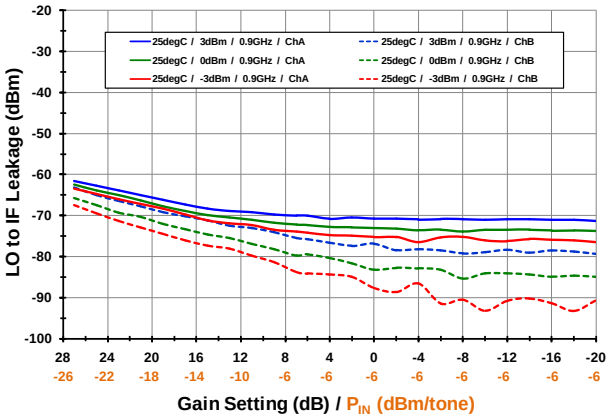
Total I_{CC} [v LO Power]



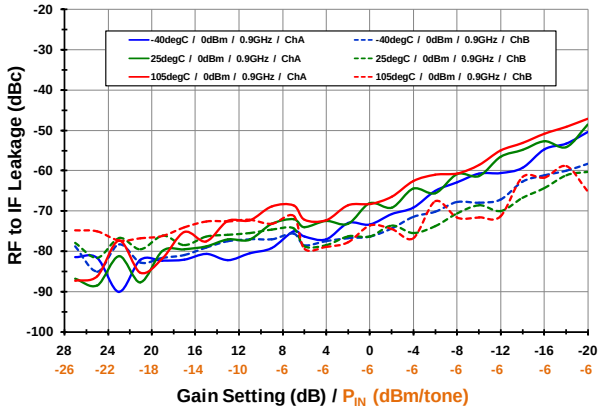
Total I_{CC} [v Temp]



LO to IF Leakage [v LO Power]



RF to IF Leakage [v Temp]



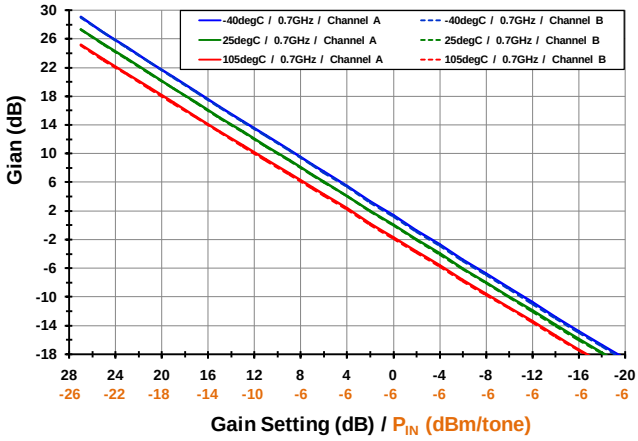
TYPICAL OPERATING CONDITIONS [276 MHZ IF CENTER]

Unless otherwise noted, the following conditions apply:

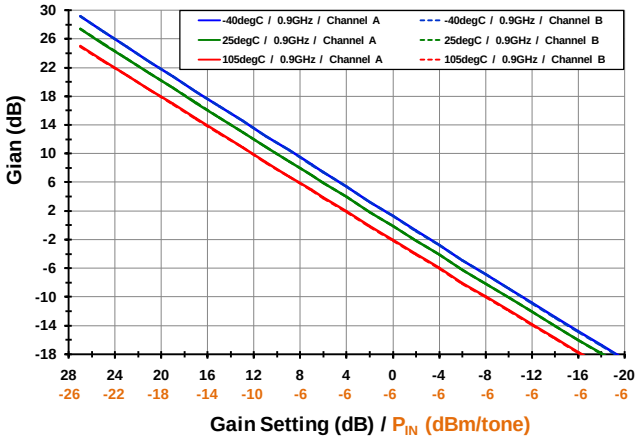
- Applications circuit for 100Ω differential load with 276MHz +/- 40MHz BW into 2:1 transformer. See schematic in BOM section.
- Pout ~ +3dBm
- Measurement on Channel A
- P_{IN} from -27dBm to -6dBm per tone (Gain Setting Adjusted to yield Pout ~ +3dBm)
- Tone Spacing = 800KHz
- Device configured in Standard Mode with High Side Injection
- T_{CASE} = 25C, V_{CC} = 5.00V, LO Power = 0dBm
- RF Frequency: 915MHz
- IF Frequency: 276MHz
- IF Transformer Losses are de-embedded
- Input RF trace and connector losses are de-embedded
- Listed Temperatures are Case Temperature (T_C = Case Temperature)
- Where noted, T_A or T_{AMB} = Ambient Temperature

TOCs [Swept Gain, STD Mode, IF = 276MHz, HS Injection] Gain, OIP3, OIP2 (-9-)

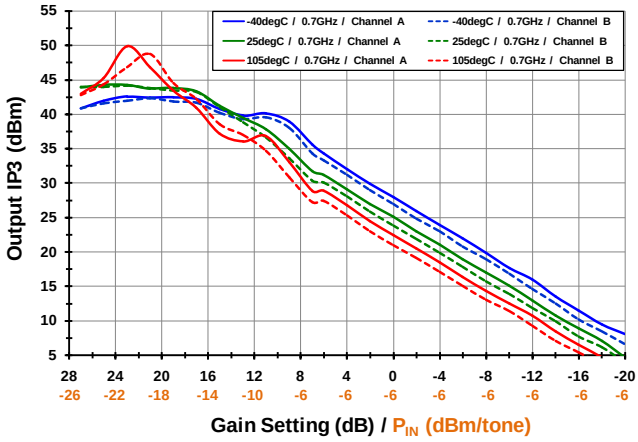
RF Gain [RF=0.7 GHz]



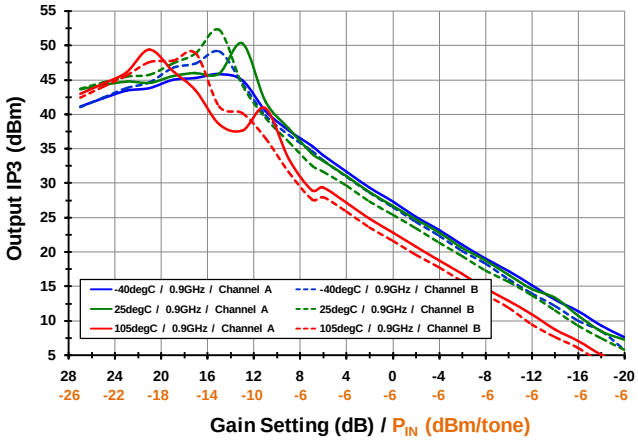
RF Gain [RF=0.9 GHz]



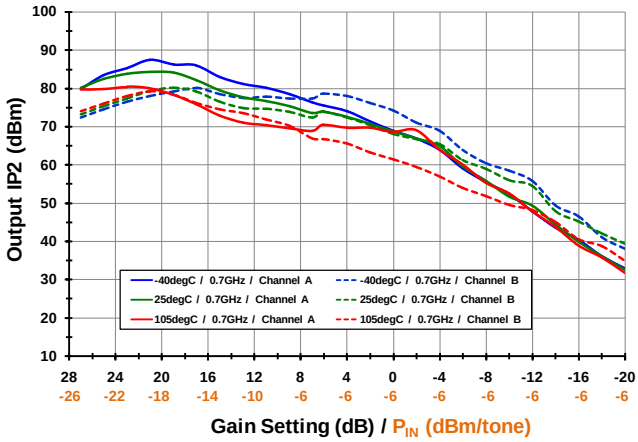
Output IP3 [RF=0.7 GHz]



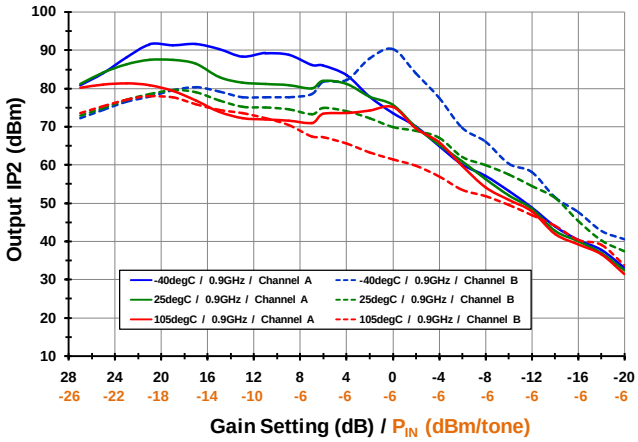
Output IP3 [RF=0.9 GHz]



Output IP2 [RF=0.7 GHz]

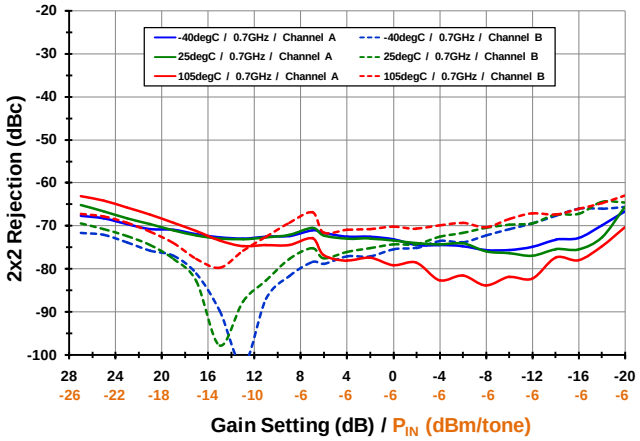


Output IP2 [RF=0.9 GHz]

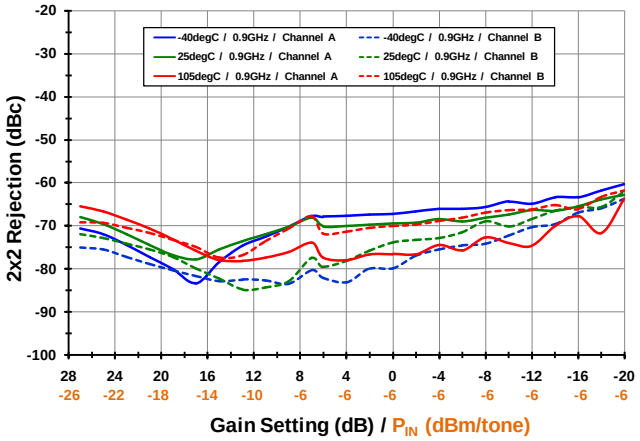


TOCs [Swept Gain, STD Mode, IF = 276MHz, HS Injection] 2x2, 3x3, Current, R-I, ISO (-10-)

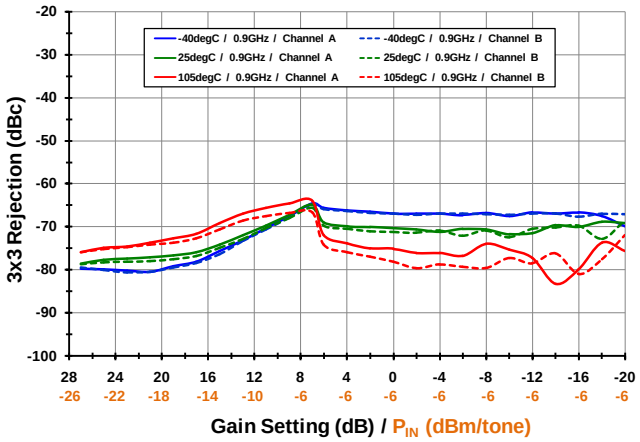
2x2 Rejection [RF=0.7 GHz]



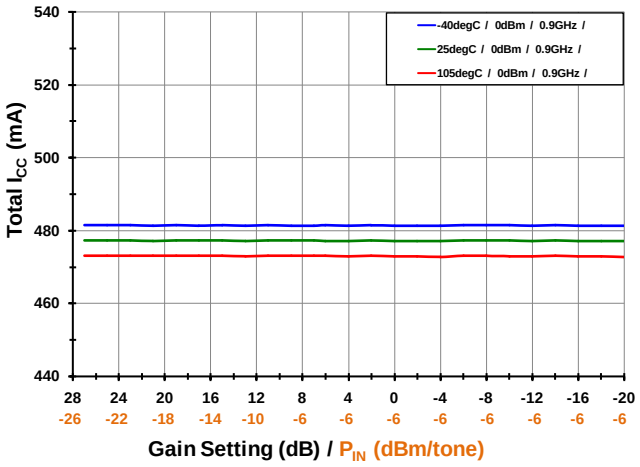
2x2 Rejection [RF=0.9 GHz]



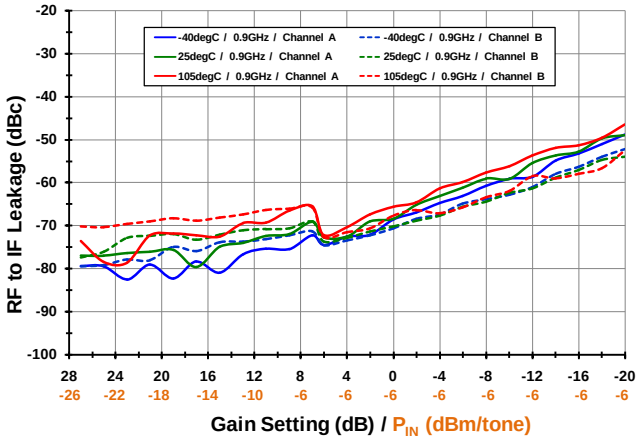
3x3 Rejection [RF=0.9 GHz]



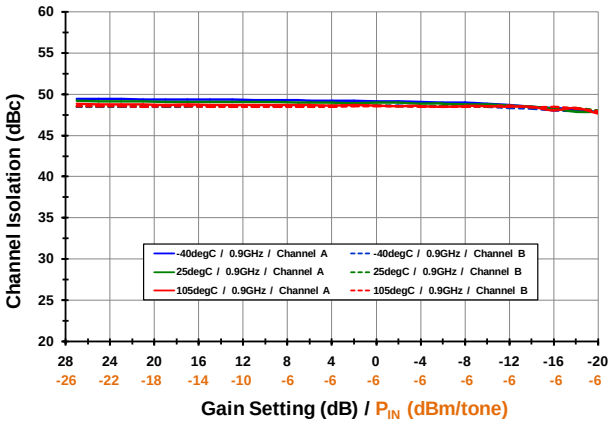
Total I_{CC} [RF=0.9 GHz]



RF to IF Leakage [RF=0.9 GHz]



Channel Isolation [RF=0.9 GHz]



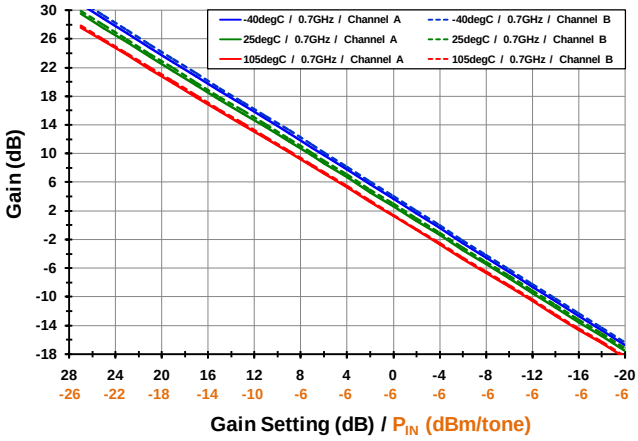
TYPICAL OPERATING CONDITIONS (80 MHZ IF CENTER)

Unless otherwise noted, the following conditions apply:

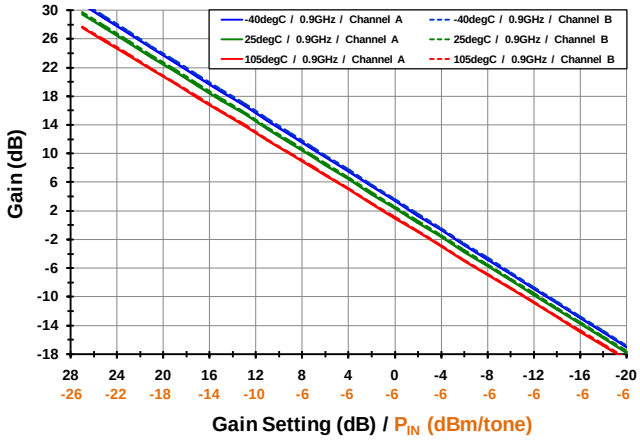
- Applications circuit for 100Ω differential load with 80MHz +/- 40MHz BW into 2:1 transformer. See schematic in BOM section.
- Pout ~ +3dBm
- Measurement on Channel A
- P_{IN} from -27dBm to -5dBm per tone (Gain Setting Adjusted to yield Pout ~ +3dBm)
- Tone Spacing = 800KHz
- Device configured in Standard Mode with High Side Injection
- T_{CASE} = 25C, V_{CC} = 5.00V, LO Power = 0dBm
- RF Frequency: 915MHz
- IF Frequency: 80MHz
- IF Transformer Losses are de-embedded
- Input RF trace and connectors losses are de-embedded
- Listed Temperatures are Case Temperature (T_C = Case Temperature)
- Where noted, T_A or T_{AMB} = Ambient Temperature

TOCs [Swept Gain, STD Mode, IF = 80MHz, HS Injection] Gain, OIP3, OIP2 (-11-)

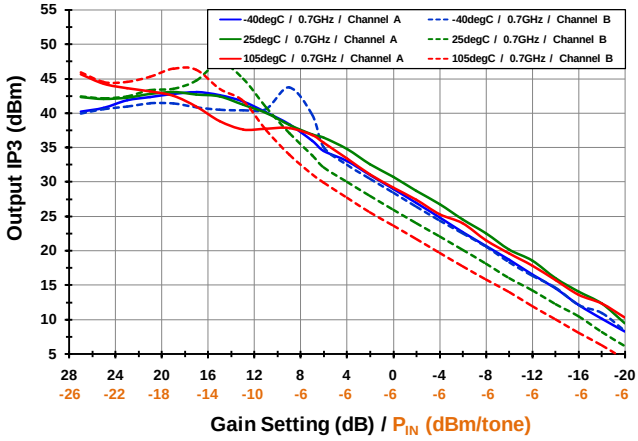
RF Gain [RF=0.7 GHz]



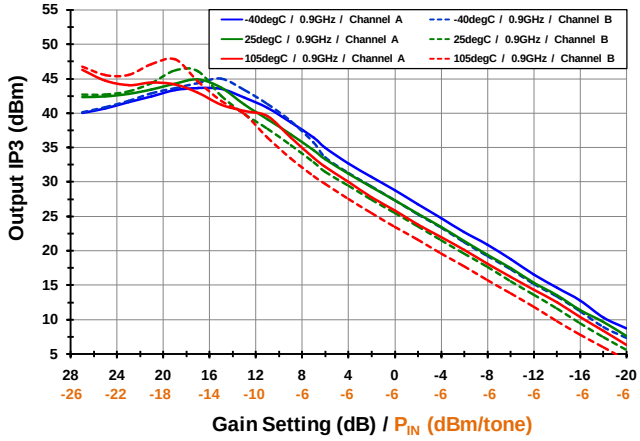
RF Gain [RF=0.9 GHz]



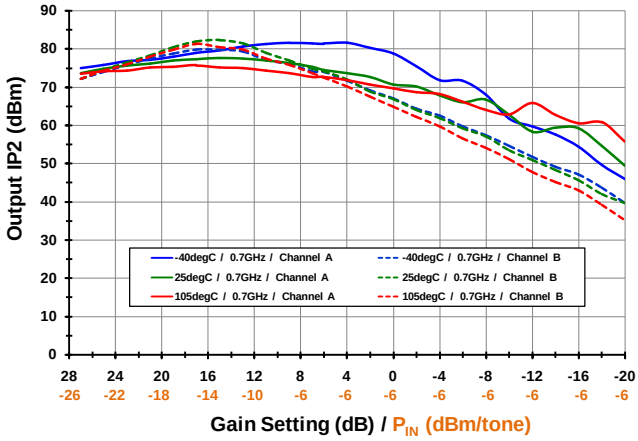
Output IP3 [RF=0.7 GHz]



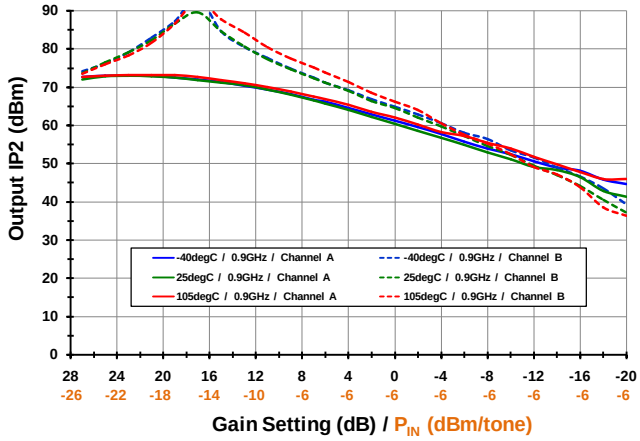
Output IP3 [RF=0.9 GHz]



Output IP2 [RF=0.7 GHz]

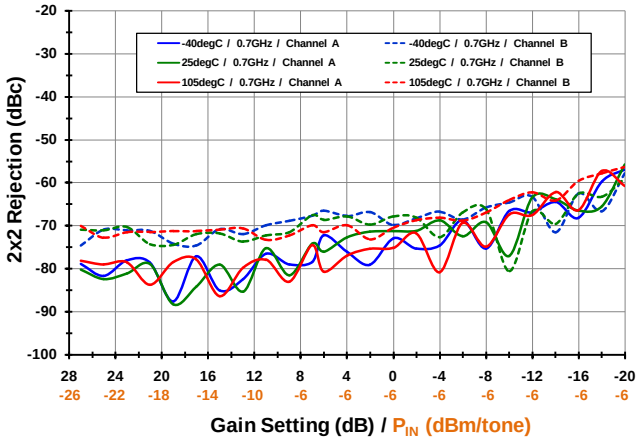


Output IP2 [RF=0.9 GHz]

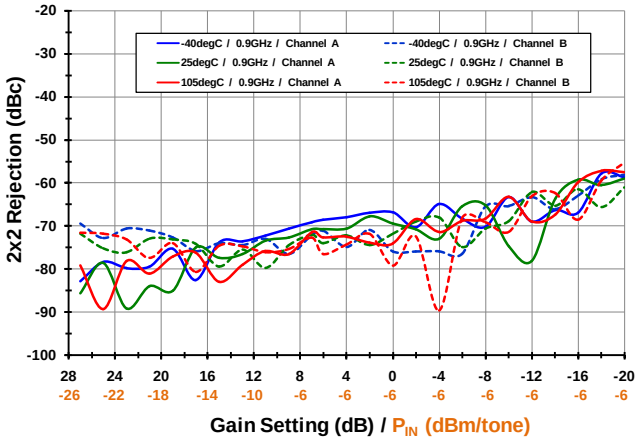


TOCs [Swept Gain, STD Mode, IF = 80MHz, HS Injection] 2x2, 3x3, Current, R-I, ISO (-12-)

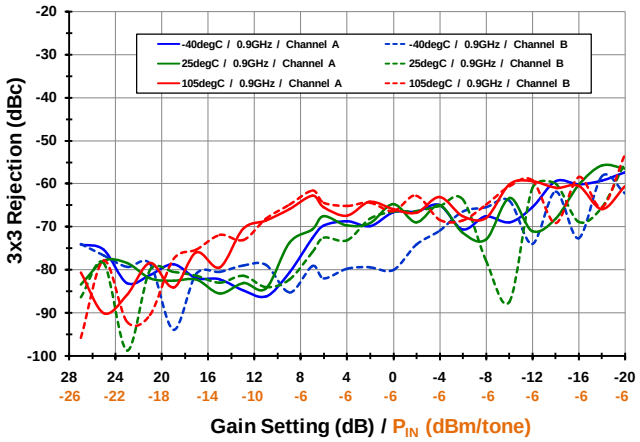
2LO-2RF Rejection [RF=0.7 GHz]



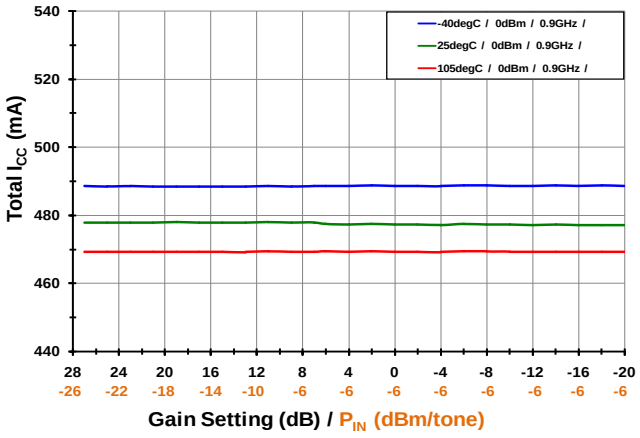
2LO-2RF Rejection [RF=0.9 GHz]



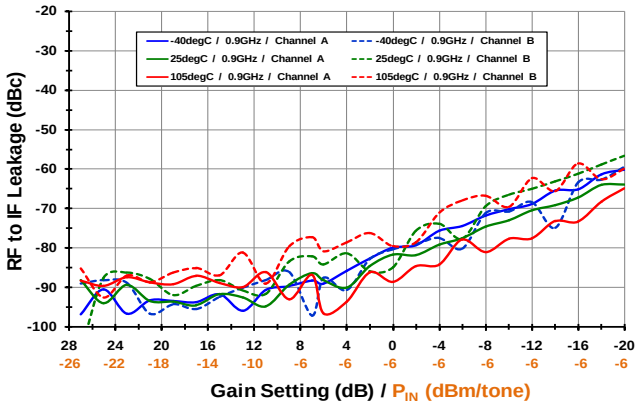
3LO-3RF Rejection [RF=0.9 GHz]



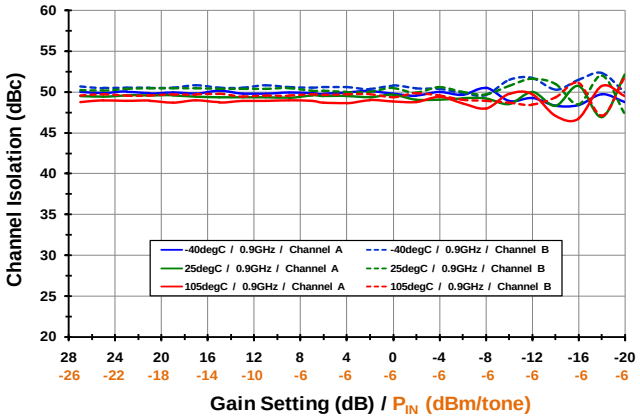
Total I_{CC} [RF=0.9 GHz]



RF to IF Leakage [RF=0.9 GHz]

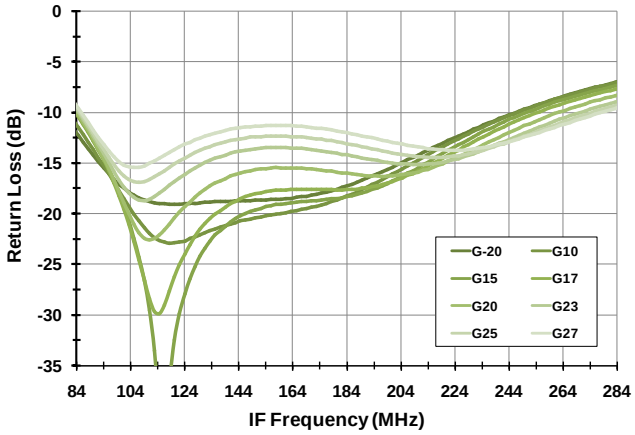


Channel Isolation [RF=0.9 GHz]

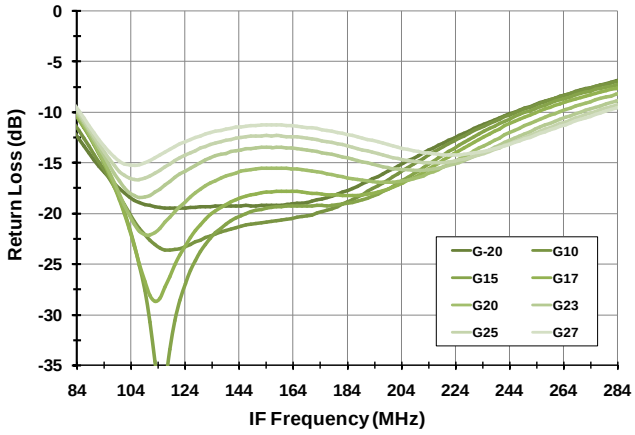


TOCs Return Loss [STD Mode] (-13-)

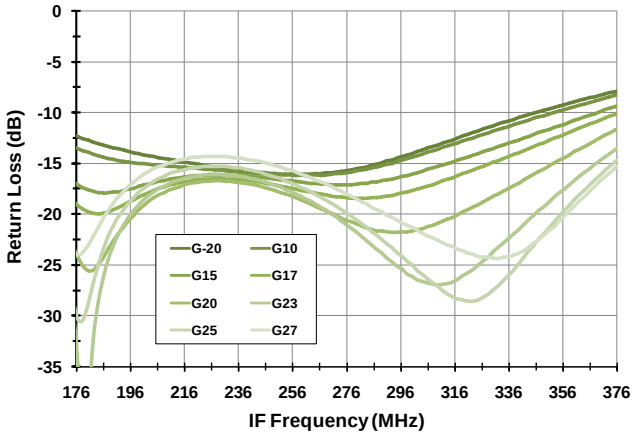
IF_A Output Return Loss 184MHz match



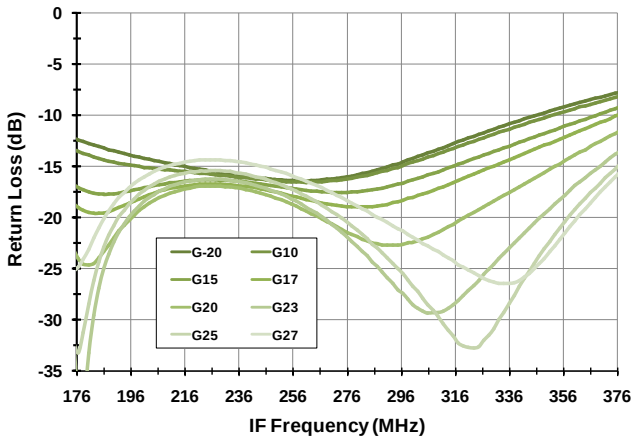
IF_B Output Return Loss 184MHz match



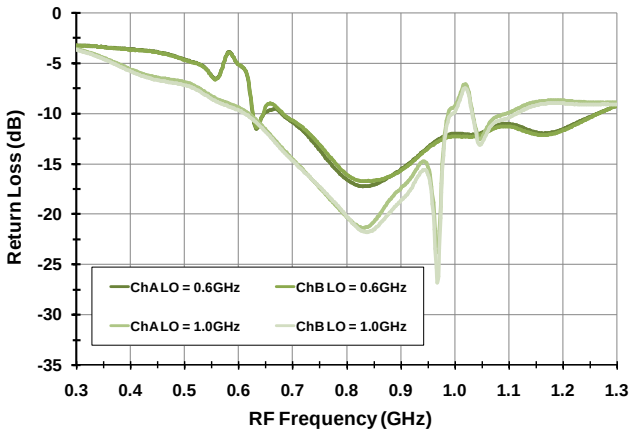
IF_A Output Return Loss 276MHz match



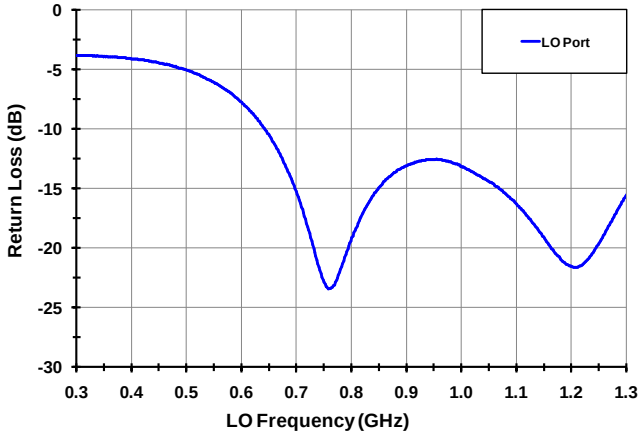
IF_B Output Return Loss 276MHz match



RF Port Return Loss

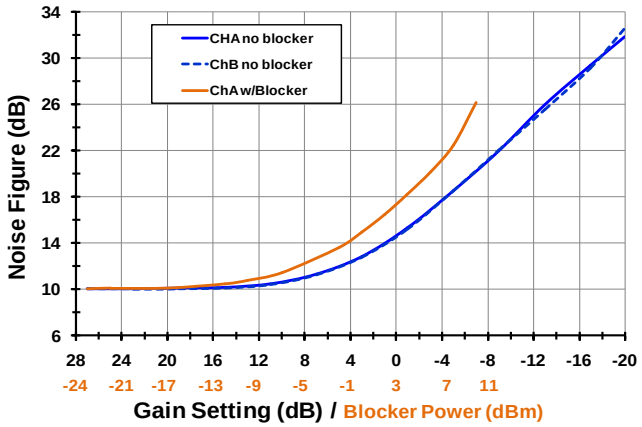


LO Port Return Loss

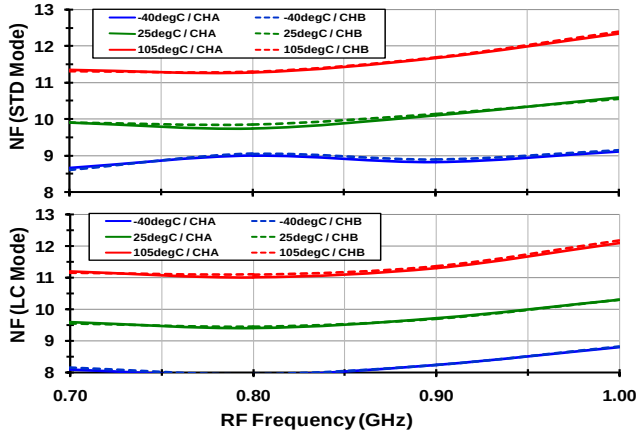


TOCs Noise Figure, Gain Accuracy, P1dB [STD Mode] (-14-)

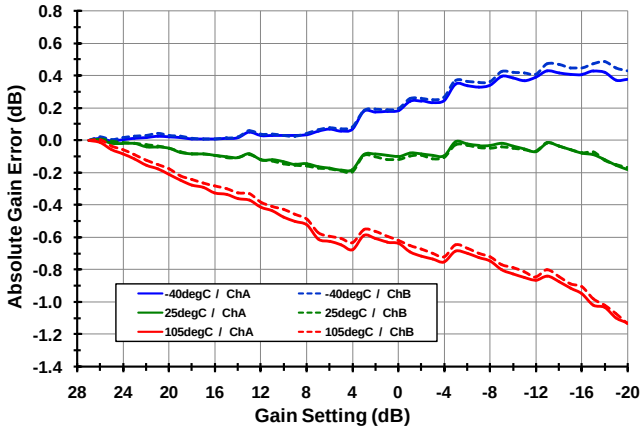
NF v Gain [RF=915M, IF=184M, HS Injection]



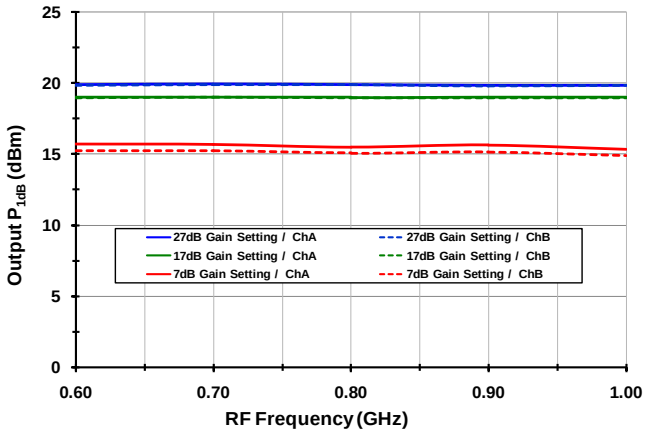
NF v Temp [RF=915M, IF=184M, HS Injection]



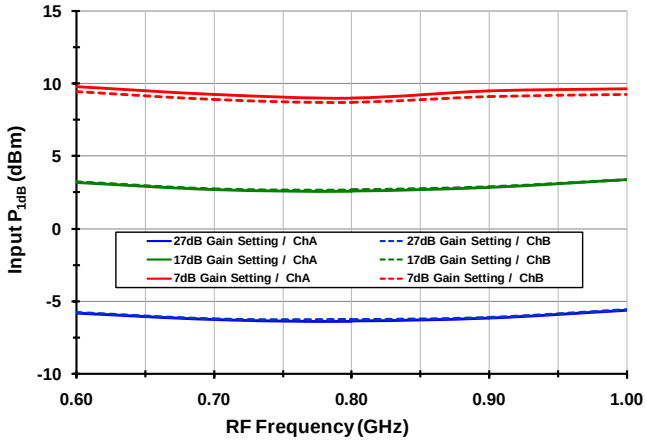
Gain Accuracy [RF =915M, IF=184M, HS Injection]



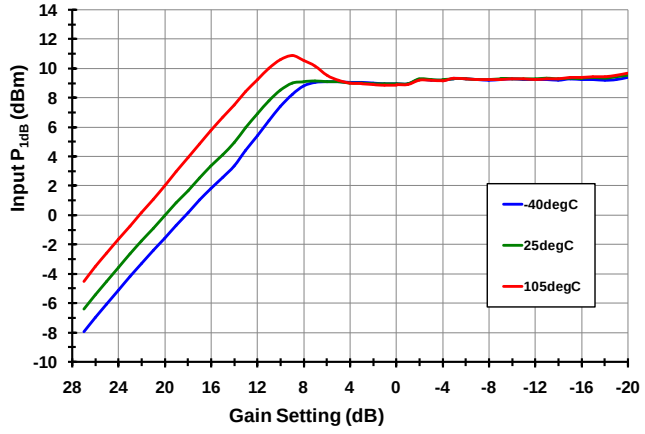
Output P1dB [IF = 184 MHz, High Side Injection]



Input P1dB [IF =184 MHz, High Side Injection]

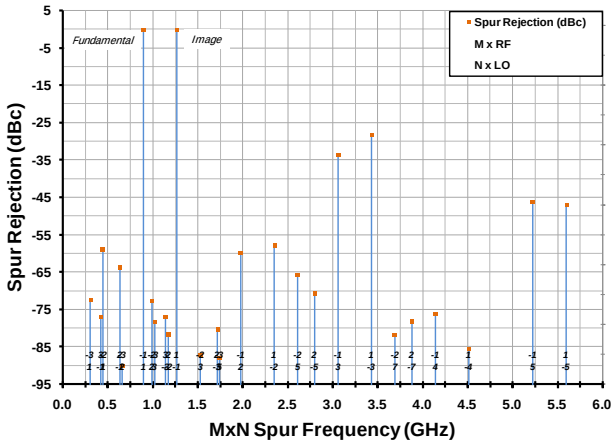


Input P1dB [RF = 915M, IF = 184M, High Side Inj.]

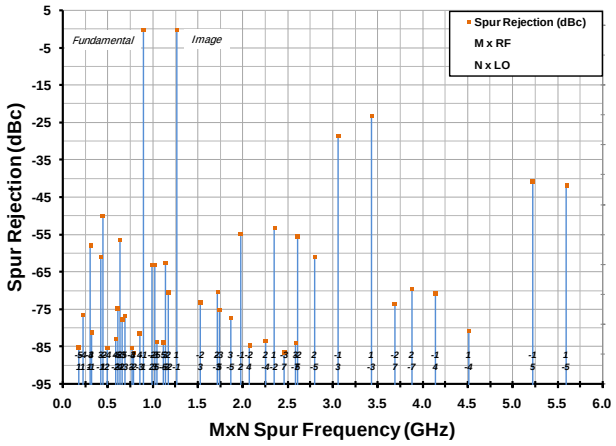


TOCs M x N Spurs [LO = 1.08182 GHz, T_{CASE} = 25C, > -90 dBc] (-15-)

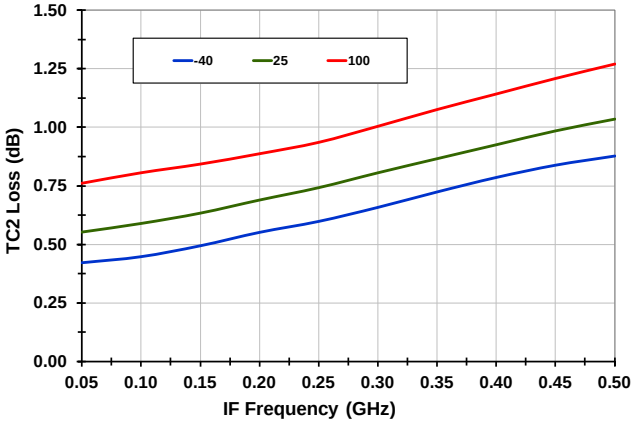
Spur Rejection [ChA, Spur P_{IN} = -5 dBm]

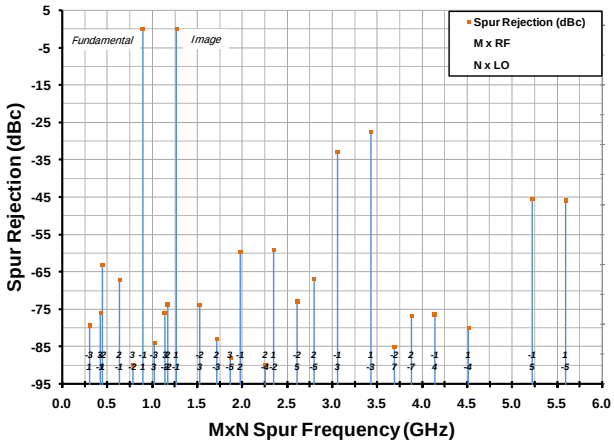


Spur Rejection [ChA, Spur P_{IN} = 0 dBm]

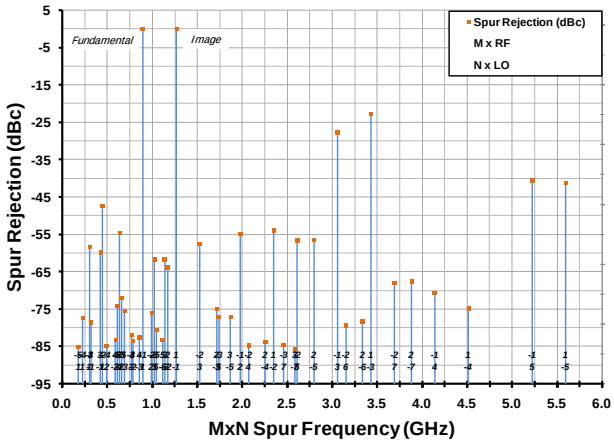


Transformer TC2-7T Loss vs. Temperature



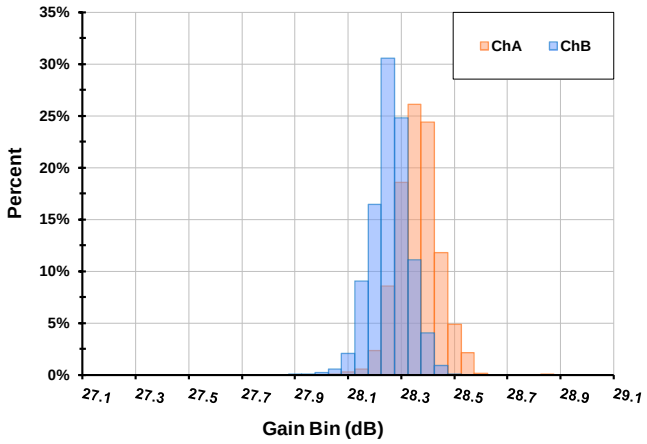


Spur Rejection [ChB, Spur P_{IN} = 0 dBm]

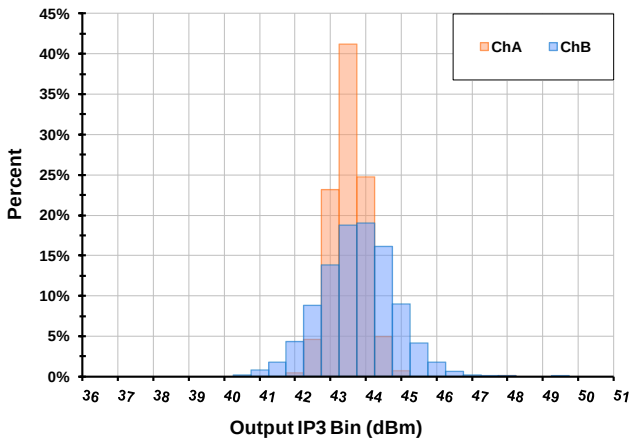


TOCs Histograms [N= 4584, T_{CASE} = 25C] (-16-)

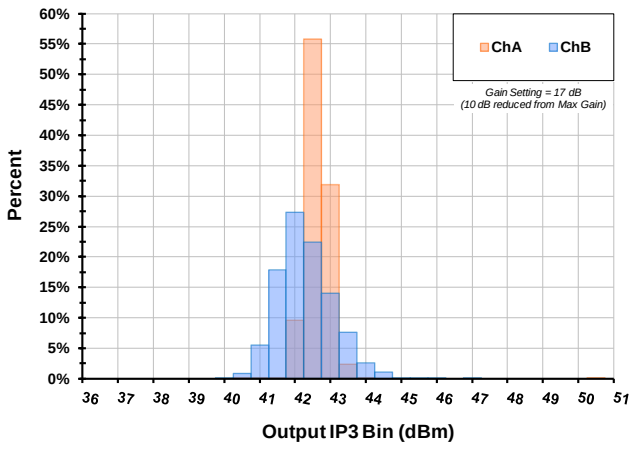
Gain [RF = 850MHz, G_{MAX}]



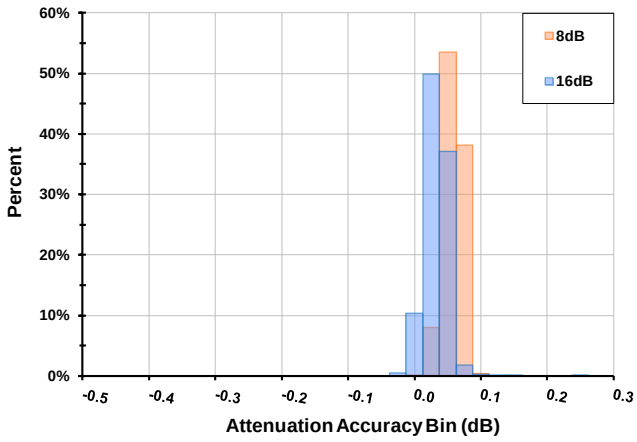
Output IP3 [RF = 850MHz, G_{MAX}]



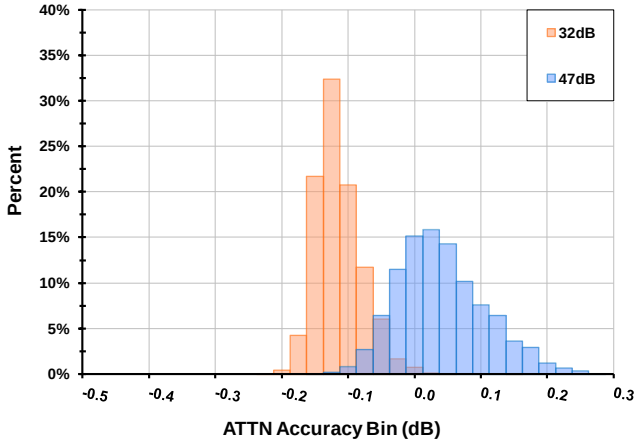
Output IP3 [RF = 850MHz, G_{17}]



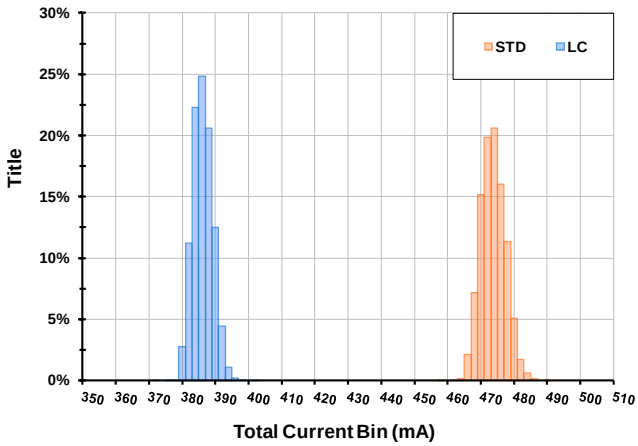
ATTN Accuracy1 [RF = 850MHz, ChB]



ATTN Accuracy2 [RF = 850MHz, ChB]



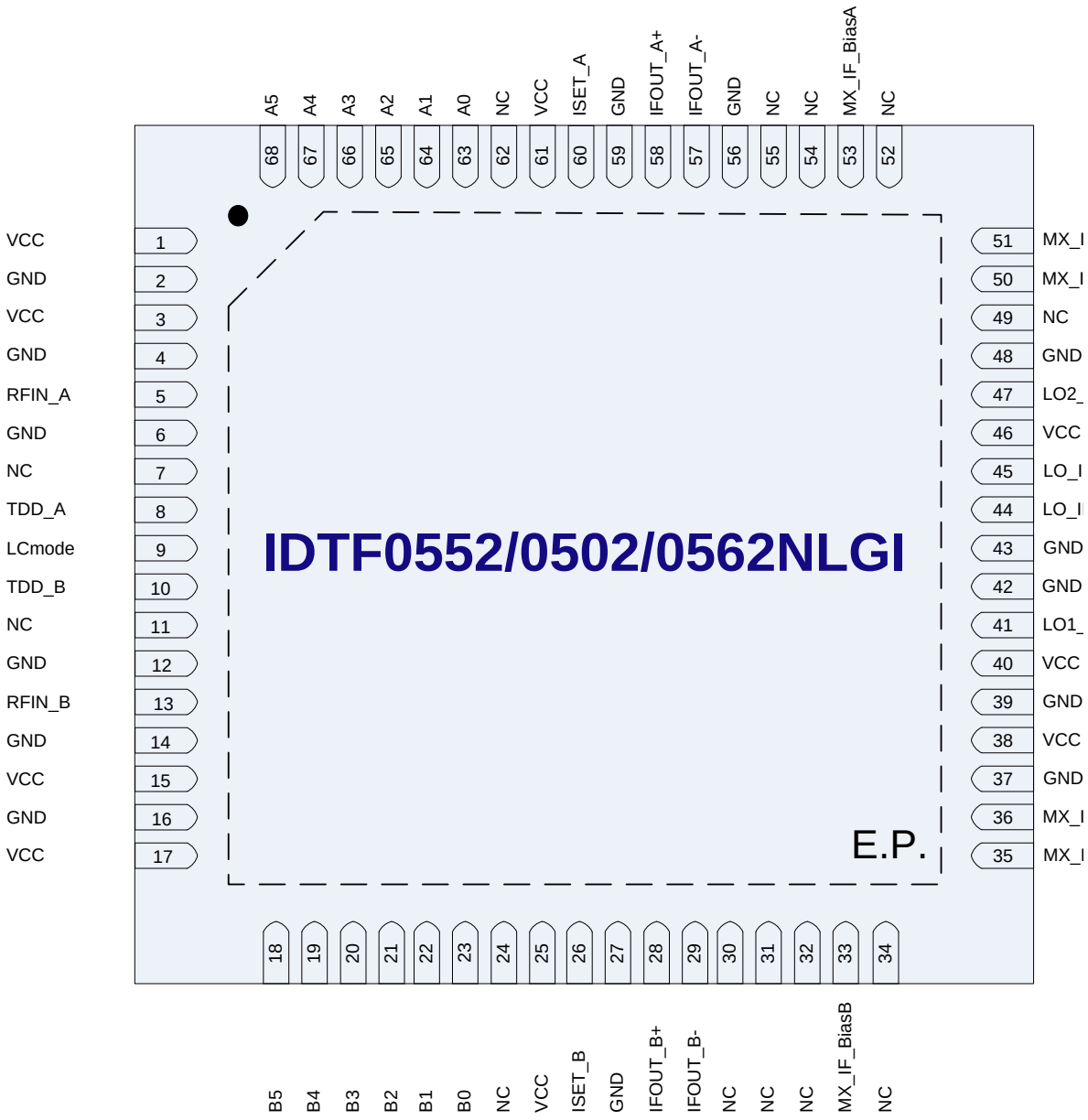
Total I_{CC} [LO = 1034MHz, V_{CC} = 5.00 V]



PACKAGE OUTLINE DRAWINGS

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

PIN DIAGRAM



PIN DESCRIPTION

Pin	Name	Function
1, 3, 15, 17, 25, 38, 40, 46, 61	VCC	Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.
2, 4, 6, 12, 14, 16, 27, 37, 39, 42, 43, 48, 56, 59	GND	Ground these pins. These pins are internally tied to the exposed paddle.
5	RFIN_A	Main Channel RF Input. Internally matched to 50Ω. **DO NOT apply DC to this pin**,
7, 11, 24, 30, 31, 32, 34, 49, 52, 54, 55, 62	NC	No Connection. Not internally connected. OK to connect to VCC, or GND
8	TDD_A	Standby control for Channel A. Includes an internal pull-up resistor so leave as NC for Standby mode. Set this pin to low or GND for normal operation.
9	LCmode	Low_Current Mode. Includes an internal pull-up resistor so leave as NC for LC mode. Set this pin to low or GND for STD mode.
10	TDD_B	Standby control for Channel B. Includes an internal pull-up resistor so leave as NC for Standby mode. Set this pin to low or GND for normal operation.
13	RFIN_B	Diversity Channel RF Input. Internally matched to 50Ω. **DO NOT apply DC to this pin**,
18	B5	Parallel Gain Control Input - MSB
19	B4	Parallel Gain Control Input
20	B3	Parallel Gain Control Input
21	B2	Parallel Gain Control Input
22	B1	Parallel Gain Control Input
23	B0	Parallel Gain Control Input – LSB (1 dB step)
26	ISET_B	ChB VGA Icc set: Recommended resistor value = 3.48kΩ
28	IFOUT_B+	Channel B Differential Output +. Pull up to Vcc through an inductor
29	IFOUT_B-	Channel B Differential Output -. Pull up to Vcc through an inductor
33	MX_IF_BiasB	Connect the specified resistor for either Standard mode (40.2Ω) or LC mode (62Ω) from this pin to ground to set the bias for the Diversity IF amplifier. This is NOT a current set resistor.
35	MX_IFB+	Diversity Mixer Differential IF (+) Output. Connect a pullup inductor from this pin to VCC.
36	MX_IFB-	Diversity Mixer Differential IF (-) Output. Connect a pullup inductor from this pin to VCC.

PIN DESCRIPTION (CONTINUED)

41	LO1_ADJ	Connect the specified resistor for either Standard mode (91Ω) or LC mode (180Ω) from this pin to ground to set the LO common buffer Icc.
44	LO_IN	Local Oscillator Input. Connect the LO to this port through the recommended coupling capacitor.
45	LO_IN_RTN	Transformer ground return. Ground this pin close to the device
47	LO2_ADJ	Connect the specified resistor for either Standard mode (1.21kΩ) or LC mode (1.91kΩ) from this pin to ground to set the LO drive buffers Icc.
50	MX_IFA-	Diversity Mixer Differential IF (-) Output. Connect a pullup inductor from this pin to VCC.
51	MX_IFA+	Diversity Mixer Differential IF (+) Output. Connect a pullup inductor from this pin to VCC.
53	MX_IF_BiasA	Connect the specified resistor for either Standard mode (40.2Ω) or LC mode (62Ω) from this pin to ground to set the bias for the Diversity IF amplifier. This is NOT a current set resistor.
57	IFOUT_A-	Channel A Differential Output -. Pull up to Vcc through an inductor
58	IFOUT_A+	Channel A Differential Output +. Pull up to Vcc through an inductor
60	ISET_A	ChA VGA Icc set: Recommended resistor value = 3.48kΩ
63	A0	Parallel Gain Control Input – LSB (1dB step)
64	A1	Parallel Gain Control Input
65	A2	Parallel Gain Control Input
66	A3	Parallel Gain Control Input
67	A4	Parallel Gain Control Input
68	A5	Parallel Gain Control Input - MSB
69	EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the noted RF performance.

DIGITAL PIN VOLTAGE AND RESISTANCE VALUES

The following table provides open-circuit DC voltage referenced to ground and resistance values for each of the control pins listed.

Pin	Name	DC Voltage (volts)	Resistance (ohms)
8	TDD_A	**5V**	**50kΩ to Vcc**
9	LCmode	**5V**	**50kΩ to Vcc**
10	TDD_B	**5V**	**50kΩ to Vcc**
18 – 23	B5-B0	**5V**	**50kΩ to Vcc**
63 - 68	A0-A5	**5V**	**50kΩ to Vcc**

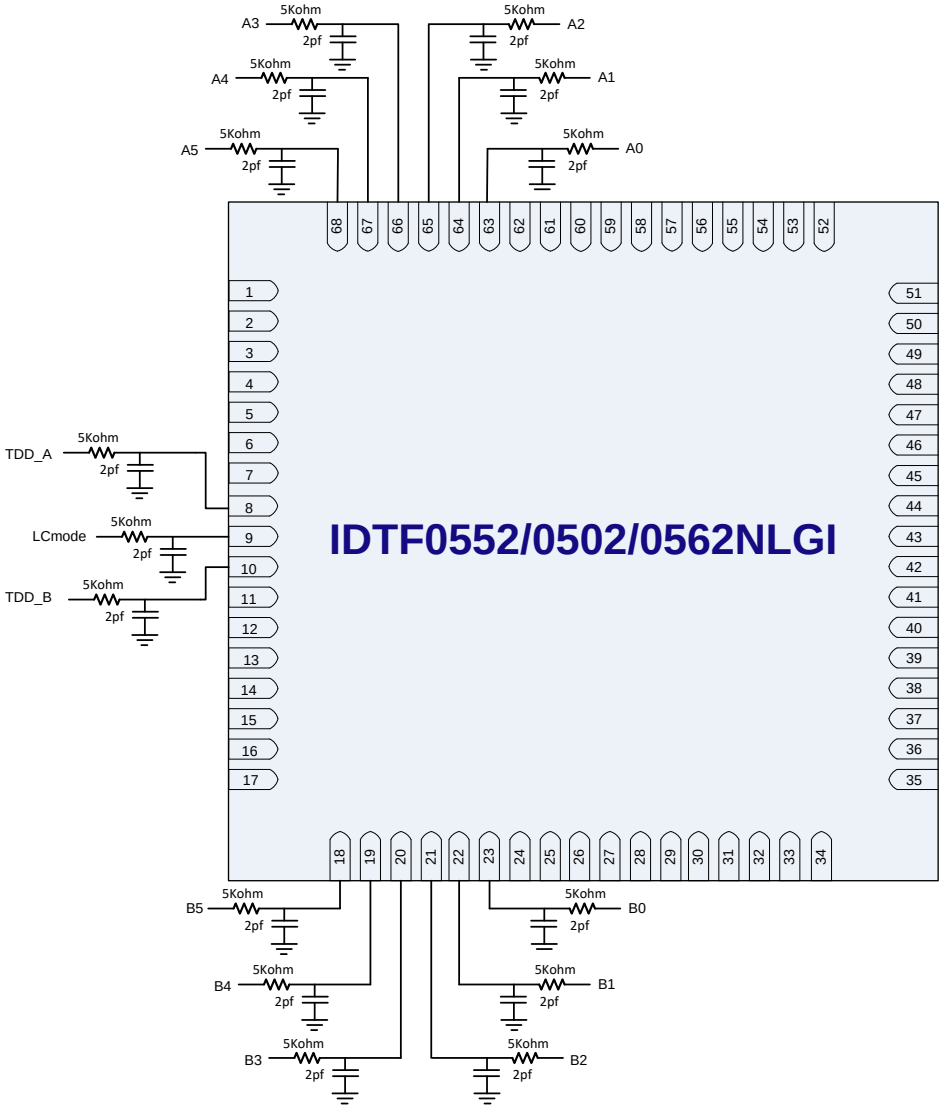
APPLICATIONS INFORMATION

Power Supplies

A common VCC power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20µs. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.

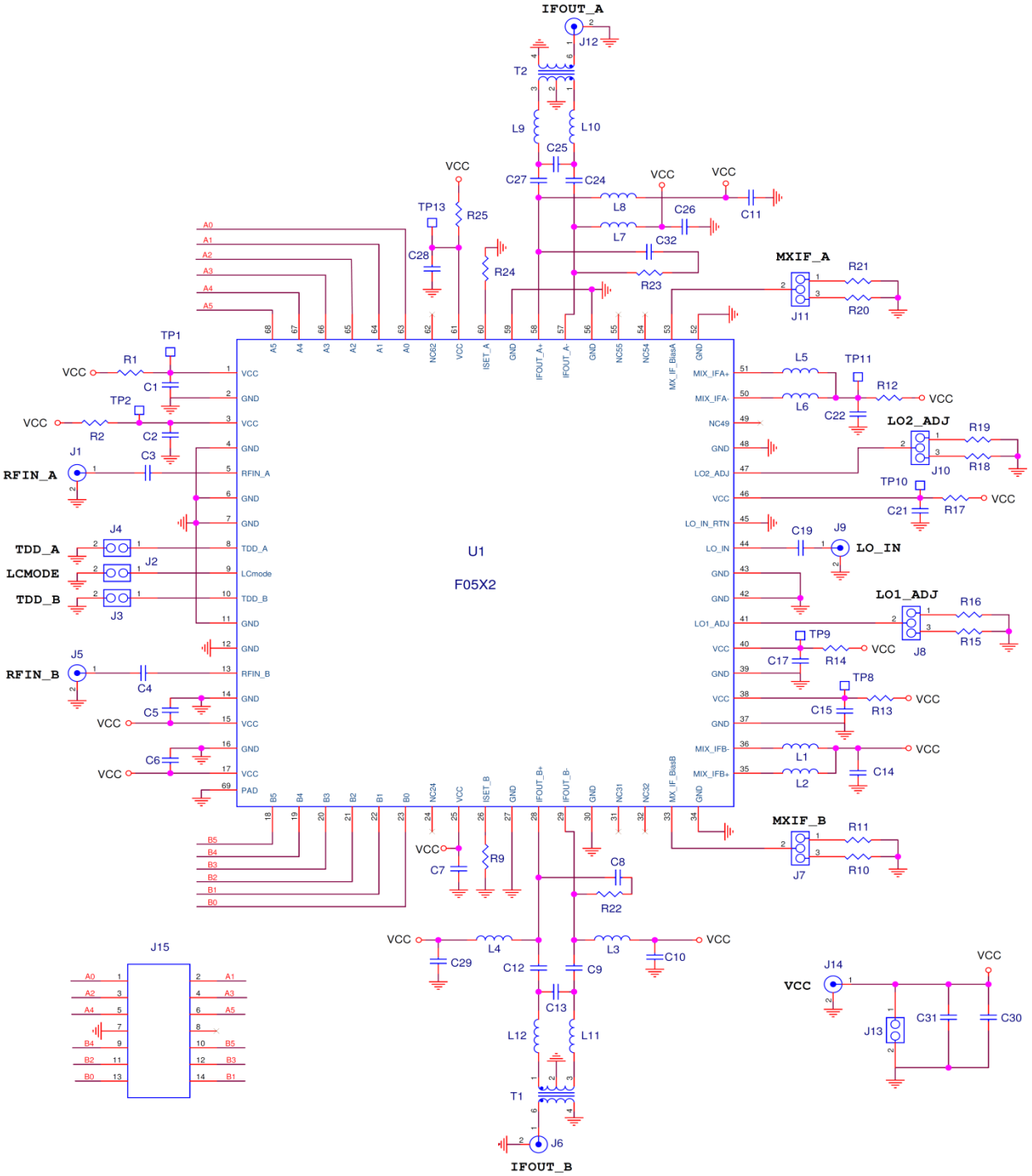
Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., provisions for an R-C circuit at the input of each control and data pin is recommended. This applies to pins 8, 9, 10, 18 - 23, and 63 - 68 as shown below.

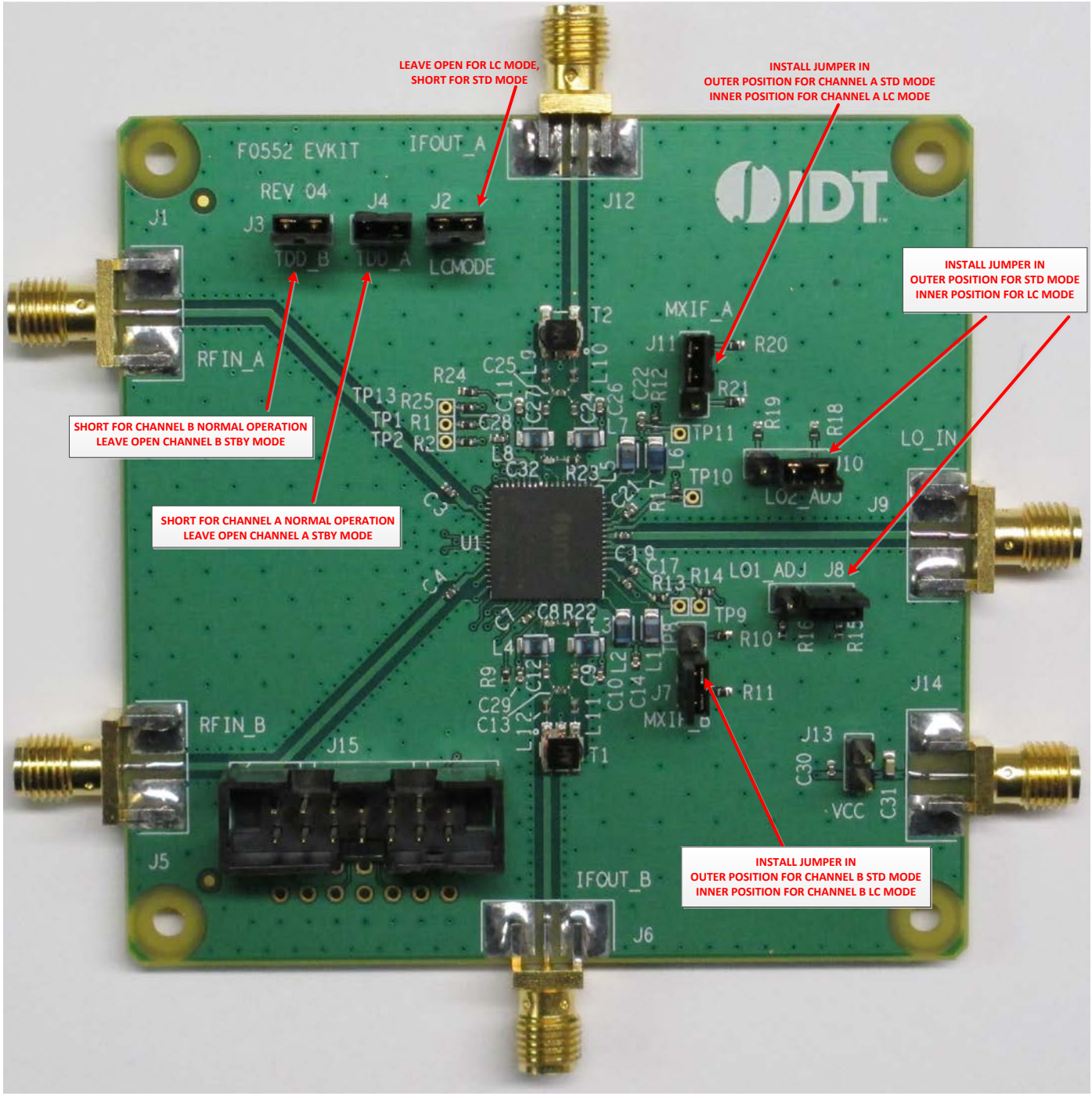


EVKIT AND TYPICAL APPLICATION SCHEMATIC

The following schematic describes the recommended EVkit and applications circuit.



EVKIT PICTURE



BOM 1 AND 2

Two BOMs are included: BOM1 supports the 4:1 output transformation from 200Ω to 50Ω used for production test and BOM2 supports the 2:1 output transformation from 200Ω to 100Ω used to generate the typical operating curve graphs.

- For Standard (STD) Mode, use resistor values in **RED** and short J2 LCMODE jumper (short pin to GND).
- For Low Current (LC) Mode, use resistor values in **BLUE** and open J2 LCMODE jumper (open pin).

BOM1 includes components for 4:1 output transformation supporting production test (IF center frequency 184MHz)

4:1 Transformer, IF = 184MHz 8/13/14

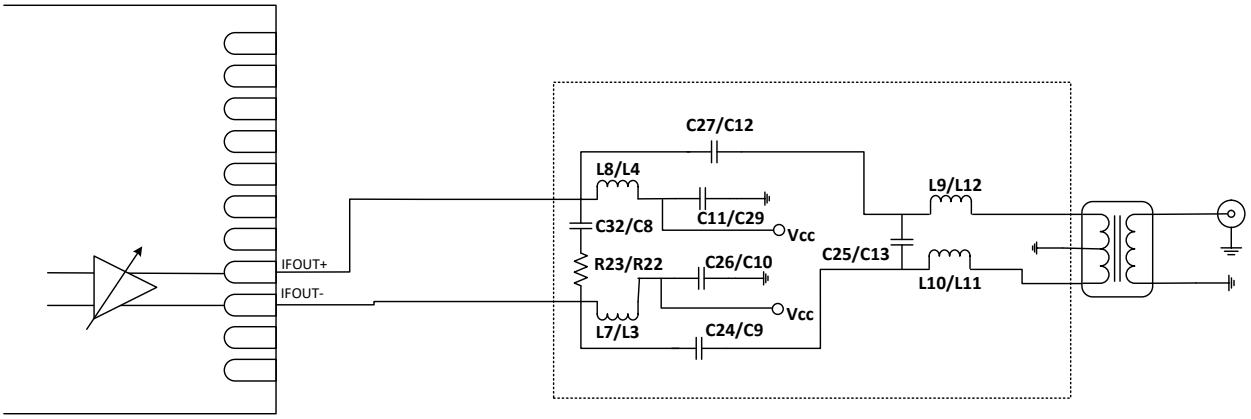
Part Reference	QTY	DESCRIPTION	Mfr. Part #	Mfr.
C3, 4, 19	3	CAP CER 39PF ±5% 50V C0G (0402)	GRM1555C1H390JZ010	Murata
C9, 12, 24, 27	4	CAP CER 1000PF ±5% 50V C0G (0402)	GRM1555C1H102JA01D	Murata
C1, 2, 5, 6, 7, 10, 11, 14, 15, 17, 21, 22, 26, 28, 29, 30	16	CAP CER 10NF ±10% 16V X7R (0402)	GRM155R71C103KA01D	Murata
C31	1	CAP CER 10UF ±20% 6.3V X5R (0603)	GRM188R60J106ME47D	Murata
C8, 32	2	CAP CER 0.6PF ±0.1PF 50V C0G (0402)	GRM1555C1HR60B	Murata
R15	1	RES 91.0 OHM ±1% 1/10W (0402)	ERJ-2RKF91R0X	Panasonic
R16	1	RES 180 OHM ±1% 1/10W (0402)	ERJ-2RKF1800X	Panasonic
R18	1	RES 1.21K OHM ±1% 1/10W (0402)	ERJ-2RKF1211X	Panasonic
R19	1	RES 1.91K OHM ±1% 1/10W (0402)	ERJ-2RKF1911X	Panasonic
R10, 21	2	RES 62.0 OHM ±1% 1/10W (0402)	ERJ-2RKF62R0X	Panasonic
R9, 24	2	RES 3.48K OHM ±1% 1/10W (0402)	ERJ-2RKF3481X	Panasonic
R11, 20	2	RES 40.2 OHM ±1% 1/10W (0402)	ERJ-2RKF40R2X	Panasonic
R22, 23	2	RES 100 OHM ±1% 1/10W (0402)	ERJ-2RKF1000X	Panasonic
R1, 2, 12, 13, 14, 17, 25, L9-L12	11	RES 0.0 OHM 1/10W (0402)	ERJ-2GE0R00X	Panasonic
L1-8	8	IND 390nH ±5% 0805CS (2012)	0805CS-391XJLB	Coilcraft
J6, 12, 14	3	SMA_END_LAUNCH (Big)	142-0701-851	Emerson Johnson
J1, 5, 9	3	SMA_END_LAUNCH (small)	142-0711-821	Emerson Johnson
J15	1	CONN HEADER VERT SGL 7 x 2 POS GOLD	N2514-6002-RB	3M
J2,3,4,13	4	CONN HEADER VERT SGL 2 x 1 POS GOLD	961102-6404-AR	3M
J7, 8, 10, 11	4	CONN HEADER VERT SGL 3 x 1 POS GOLD	961103-6404-AR	3M
T1, 2	2	4:1 Center Tap Balun (SM-22)	TC4-1WG2+	Mini Circuits
U1	1	Sampling IF receiver (TQFN-68)	F0502	IDT
C13, 25		Not Installed CER CAP (0402)		
	1	Printed Circuit Board	F0502 EVKit Rev 04	

BOM2 includes components for 2:1 output transformation used for TOCs (IF center frequency 184MHz +/ - 40MHz)

2:1 Transformer, IF = 184MHz 8/13/14

Part Reference	QTY	DESCRIPTION	Mfr. Part #	Mfr.
C3, 4, 19	3	CAP CER 150PF ±5% 50V C0G (0402)	GRM1555C1H151JA01D	Murata
C9,12, 24, 27	4	CAP CER 20PF ±5% 50V C0G (0402)	GRM1555C1H200JZ01D	Murata
C1, 2, 5, 6, 7, 10, 11, 14,15, 17, 21, 22, 26, 28, 29, 30	16	CAP CER 10NF ±10%16V X7R (0402)	GRM155R71C103KA01D	Murata
C31	1	CAP CER 10UF ±20% 6.3V X5R (0603)	GRM188R60J106ME47D	Murata
C13, 25	2	CAP CER 3PF ±0.25PF 50V C0G (0402)	GRM1555C1H3R0CZ01D	Murata
C8, 32	2	CAP CER 0.6PF ±0.1pF 50V C0G (0402)	GRM1555C1HR60BB01D	Murata
R15	1	RES 91.0 OHM ±1% 1/10W (0402)	ERJ-2RKF91R0X	Panasonic
R16	1	RES 180 OHM ±1% 1/10W (0402)	ERJ-2RKF1800X	Panasonic
R18	1	RES 1.21K OHM ±1% 1/10W (0402)	ERJ-2RKF1211X	Panasonic
R19	1	RES 1.91K OHM ±1% 1/10W (0402)	ERJ-2RKF1911X	Panasonic
R10, 21	2	RES 62.0 OHM ±1% 1/10W (0402)	ERJ-2RKF62R0X	Panasonic
R9, 24	2	RES 3.48K OHM ±1% 1/10W (0402)	ERJ-2RKF3481X	Panasonic
R11, 20	2	RES 40.2 OHM ±1% 1/10W (0402)	ERJ-2RKF40R2X	Panasonic
R22, 23	2	RES 100 OHM ±1% 1/10W (0402)	ERJ-2RKF1000X	Panasonic
R1, 2, 12, 13, 14, 17, 25	7	RES 0.0 OHM 1/10W (0402)	ERJ-2GE0R00X	Panasonic
L1, 2, 5, 6	4	IND 390nH ±5% 0805CS (2012)	0805CS-391XJLB	Coilcraft
L3, 4, 7, 8	4	IND 150nH ±5% 0805CS (2012)	0805CS-151XJLB	Coilcraft
L9-12	4	IND 30nH ±5% 0402CS	0402CS-30NXJLU	Coilcraft
J1, 5, 9	3	SMA_END_LAUNCH (Big)	142-0701-851	Emerson Johnson
J6,12,14	3	SMA_END_LAUNCH (small)	142-0711-821	Emerson Johnson
J15	1	CONN HEADER VERT SGL 7 x 2 POS GOLD	N2514-6002-RB	3M
J2, 3, 4, 13	4	CONN HEADER VERT SGL 2 x 1 POS GOLD	961102-6404-AR	3M
J7, 8, 10, 11	4	CONN HEADER VERT SGL 3 x 1 POS GOLD	961103-6404-AR	3M
T1, 2	2	2:1 Center Tap Balun (SM-22)	TC2-72T+	Mini Circuits
U1	1	Sampling IF receiver (TQFN -68)	F0502	IDT
	1	Printed Circuit Board	F0502EV Kit Rev 04	

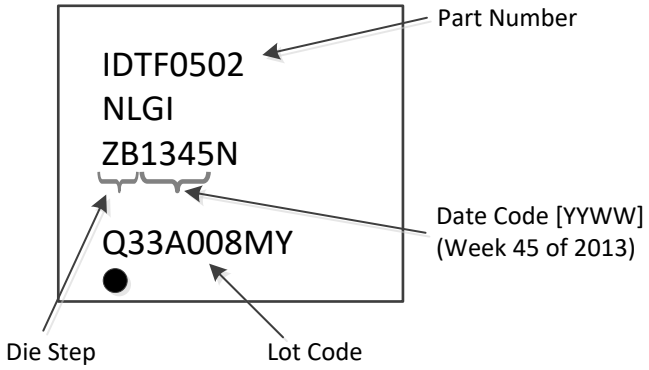
IF BIAS AND OUTPUT MATCHING CIRCUIT AND BOM FOR VARIOUS IFS



IF NETWORK BOM FOR DIFFERENT FREQUENCIES

Item #	Part Reference	Value				Unit
		IF frequency				
		80 (60-100)	138, 184 (98-240)	276 (190-316)	330 (250-410)	MHz
1	C9, 12, 24, 27	75	20	8	6	pF
2	C13,25	11	3	1.2	0.7	pF
3	C8, C32	0.6	0.6	0.6	0.6	pF
4	R22, R23	100	100	100	100	ohm
5	L3, 4, 7, 8	220	150	82	56	nH
6	L9-12	36	30	24	18	nH

TOP MARKING



ORDERING INFORMATION

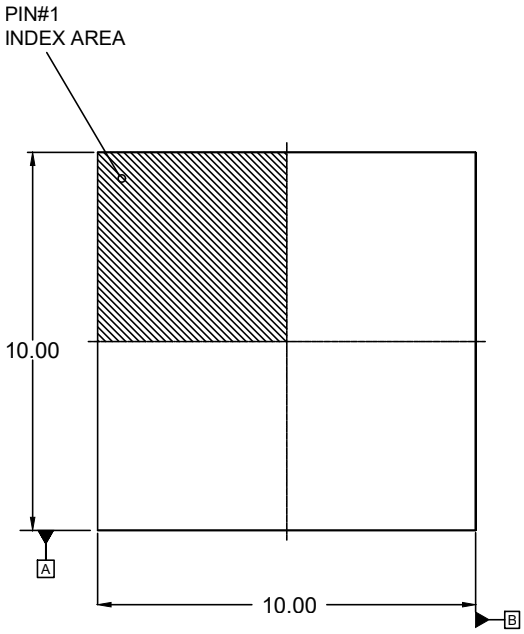
Part Number	Package Description	Carrier Type	Temperature Range
F0502NLGI	68-VFQFPN, 10 × 10 mm	Tape and Reel	-40°C to +85°C
F0502NLGI8		Tray	

REVISION HISTORY

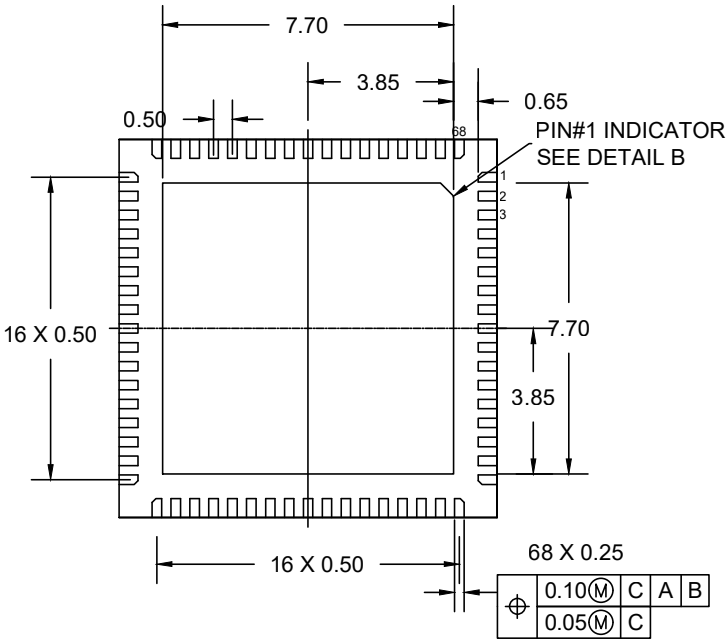
Revision Date	Description
February 8, 2022	Rebranded to Renesas.
July 20, 2016	Initial release.

Package Outline Drawing

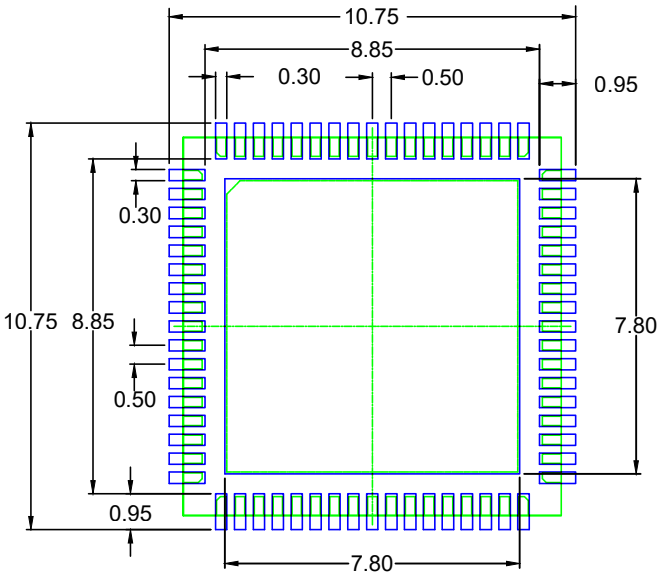
Package Code:NLG68P1
68-VFQFPN 10.0 x 10.0 x 0.90 mm Body, 0.5mm Pitch
PSC-4111-01, Revision: 01, Date Created: Feb 15, 2022



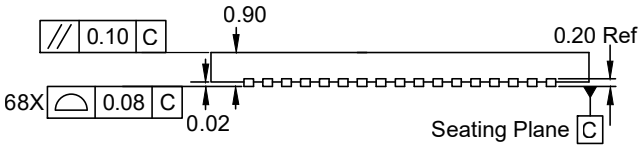
TOP VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN DIMENSION



SIDE VIEW

NOTES:

1. All dimension are in mm, angles in degrees.
2. Top down view, as viewed on PC.
3. Land pattern in blue. NSMD land pattern assumed.
4. Land pattern recommendation as per IPC-7351B generic requirement for surface mount design and land pattern.

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(Disclaimer Rev.1.01 Jan 2024)

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