Description

The 8V19N474 is a fully integrated FemtoClock NG Jitter Attenuator and Clock Synthesizer designed as a high-performance clock solution for conditioning and frequency/phase management of 10/40/100/400 Gigabit-Ethernet line cards. The device delivers excellent phase noise performance as required to drive physical layer devices, and provides the clean clock frequencies (e.g., 625MHz, 500MHz, 312.5MHz, 250MHz, 156.25MHz, and 125MHz).

A two-stage PLL architecture supports both jitter attenuation and frequency multiplication. The first stage PLL is the jitter attenuator and uses an external VCXO for best possible phase noise characteristics. The second stage PLL locks on the VCXO-PLL output signal and synthesizes the target frequency. This PLL has a VCO circuit at 2500MHz.

The 8V19N474 generates the output clock signals from the VCO by frequency division. Five independent frequency dividers are available: four support integer-divider ratios and one integer as well as fractional-divider ratios. Delay circuits can be used for achieving alignment and controlled phase delay between clock signals. The two redundant inputs are monitored for activity.

Four selectable clock switching modes are provided to handle clock input failure scenarios. Auto-lock, individually programmable output frequency dividers, and phase adjustment capabilities are added for additional flexibility. The 8V19N474 is configured through an SPI interface and reports lock and signal loss status in internal registers and via a lock detect (LOCK) output. Internal status bit changes can also be reported via the nINT output. The device is ideal for driving converter circuits in wireless infrastructure, radar/imaging, and instrumentation/medical applications. The device is a member of the high-performance clock family from IDT.

Typical Applications

- Low-phase noise clock generation
- 10/40/100 Gigabit-Ethernet line cards
- Wireless infrastructure
- Reference clock for ADC and DAC circuits
- Radar and imaging
- Instrumentation and medical

Features

- High-performance clock RF-PLL
  - Optimized for low phase noise: -153dBc/Hz (1MHz offset; 156.25MHz clock)
  - Integrated phase noise (12kHz–20MHz) of 75fs RMS typical
- Dual-PLL architecture
  - 1st-PLL stage with external VCXO for clock jitter attenuation
  - 2nd-PLL stage with internal FemtoClock NG PLL at 2500MHz
- 6 output banks with a total of 12 outputs, organized in:
  - Two clock banks with one integer frequency divider and three differential outputs
  - Two clock banks with one integer frequency divider and two differential outputs
  - One clock bank with one fractional output divider and one differential output
  - One VCXO-PLL output bank with one selectable LVDS/two LVCMOS outputs
- Four output banks contain a phase delay circuit with steps of the VCO clock period (400ps)
- Supported clock output frequencies include:
  - From the integer dividers: 2500MHz, 1250MHz, 625MHz, 500MHz, 312.5MHz, 250MHz, 156.25MHz, and 125MHz
  - From the fractional divider: 80–300MHz
- Low-power LVPECL/LVDS outputs support configurable signal amplitude, DC and AC coupling and LVPECL, LVDS line terminations techniques
- Redundant input clock architecture
  - Two inputs
  - Individual input signal monitor
  - Digital holdover
  - Manual and automatic clock selection
  - Hitless switching
- Status monitoring and fault reporting
  - Input signal status
  - Holdover and reference loss status
  - Lock status with one status pin
  - Maskable status interrupt pin
- Voltage supply:
  - Device core supply voltage: 3.3V
  - Output supply voltage: 3.3V, 2.5V, or 1.8V
  - SPI control I/O voltage: 1.8V or 3.3V (selectable), 3.3V tolerant inputs when set to 1.8V
- Package: 8 × 8 mm 81-FPBGA, RoHS 6/6
- Temperature range: -40°C to +85°C

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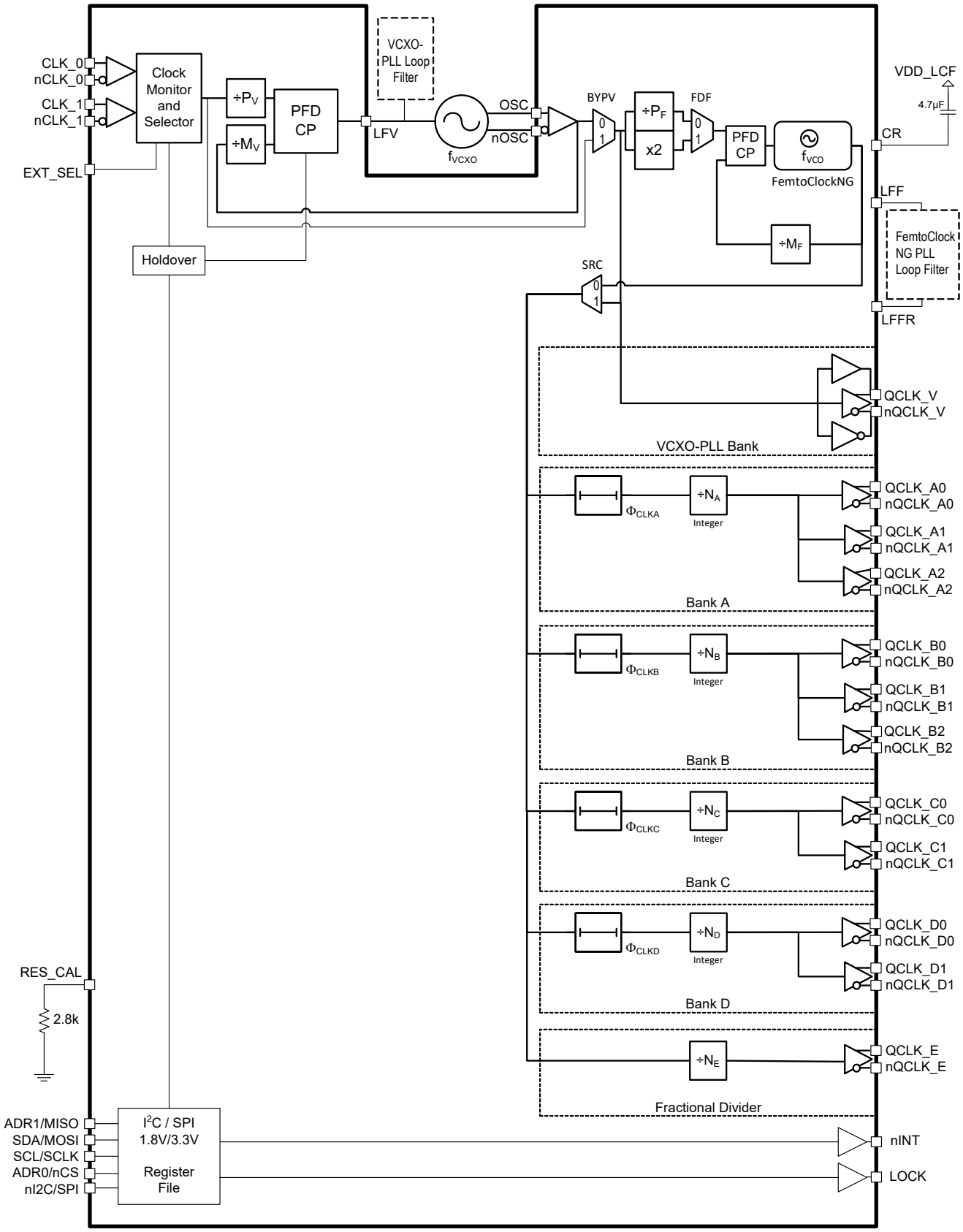
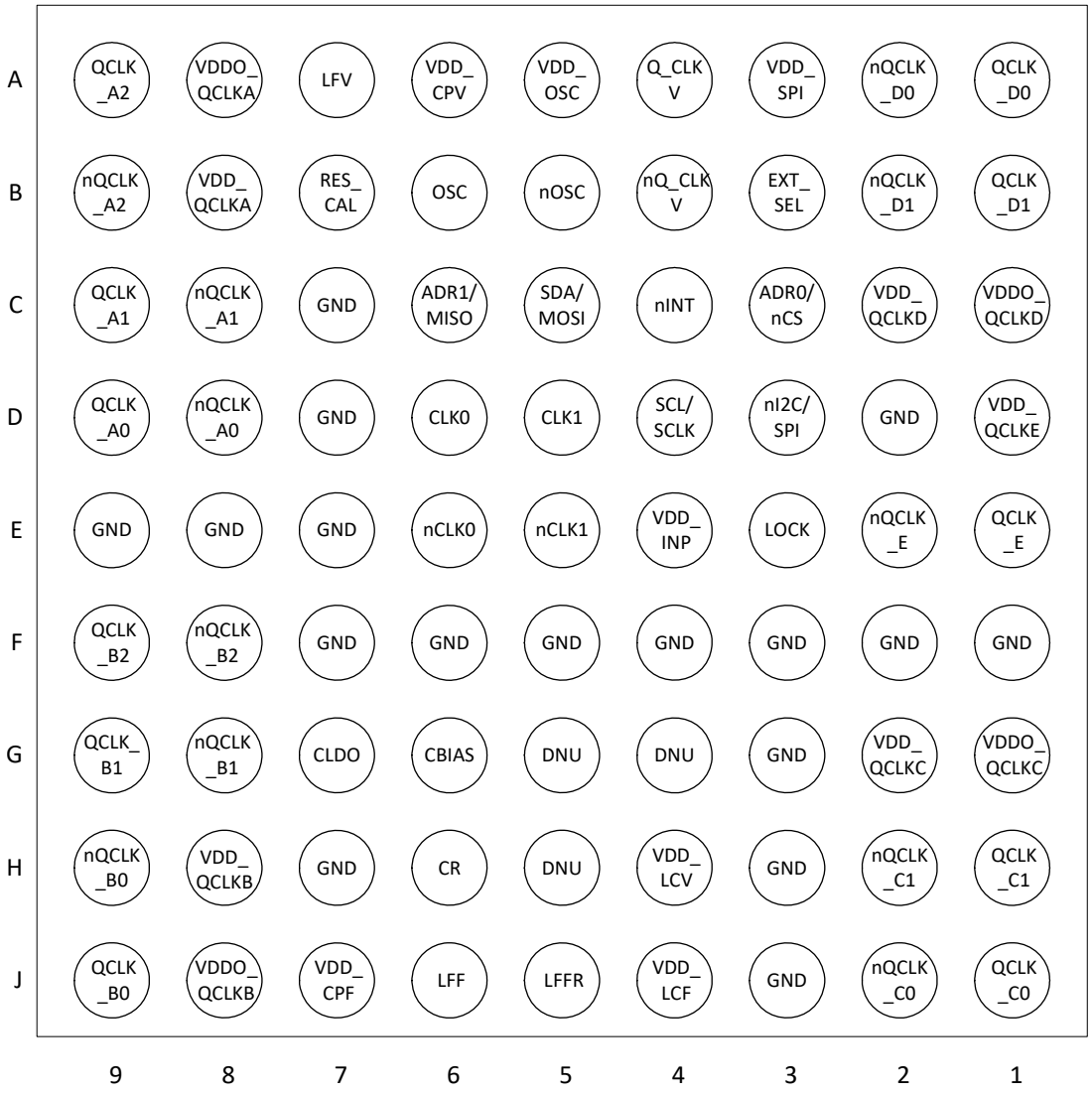
Block Diagram

Figure 1. Block Diagram



Pin Assignments

Figure 2. Ball Map for 8 × 8 mm 81-FPBGA Package Body (Bottom View)



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Pin Descriptions

Table 1. Pin Descriptions

Ball	Name	Type[a]		Description
D6	CLK_0	Input	PD	Device clock 0 inverting and non-inverting differential clock input. Inverting input is biased to V_{DD_V}/2 by default when left floating. Compatible with LVPECL, LVDS, and LVCMOS signals.
E6	nCLK_0		PD/PU	
D5	CLK_1	Input	PD	Device clock 1 inverting and non-inverting differential clock input. Inverting input is biased to V_{DD_V}/2 by default when left floating. Compatible with LVPECL, LVDS, and LVCMOS signals.
E5	nCLK_1		PD/PU	
B3	EXT_SEL	Input	PD	Clock reference select. 1.8V interface levels with hysteresis and 3.3V tolerance
D9, D8	QCLK_A0, nQCLK_A0	Output		Differential clock output A0 (Channel A). Configurable LVPECL/LVDS style and amplitude. Output levels are determined by the VDDO_QCLKA supply voltage.
C9, C8	QCLK_A1, nQCLK_A1	Output		Differential clock output A1 (Channel A). Configurable LVPECL/LVDS style and amplitude. Output levels are determined by the VDDO_QCLKA supply voltage.
A9, B9	QCLK_A2, nQCLK_A2	Output		Differential clock output A2 (Channel A). Configurable LVPECL/LVDS style and amplitude. Output levels are determined by the VDDO_QCLKA supply voltage.
J9, H9	QCLK_B0, nQCLK_B0	Output		Differential clock output B0 (Channel B). Configurable LVPECL/LVDS style and amplitude. Output levels are determined by the VDDO_QCLKB supply voltage.
G9, G8	QCLK_B1, nQCLK_B1	Output		Differential clock output B1 (Channel B). Configurable LVPECL/LVDS style and amplitude. Output levels are determined by the VDDO_QCLKB supply voltage.
F9, F8	QCLK_B2, nQCLK_B2	Output		Differential clock output B2 (Channel B). Configurable LVPECL/LVDS style and amplitude. Output levels are determined by the VDDO_QCLKB supply voltage.
J1, J2	QCLK_C0, nQCLK_C0	Output		Differential clock output C0 (Channel C). Configurable LVPECL/LVDS style and amplitude. Output levels are determined by the VDDO_QCLKC supply voltage.
H1, H2	QCLK_C1, nQCLK_C1	Output		Differential clock output C1 (Channel C). Configurable LVPECL/LVDS style and amplitude. Output levels are determined by the VDDO_QCLKC supply voltage.
A1, A2	QCLK_D0, nQCLK_D0	Output		Differential clock output D0 (Channel D). Configurable LVPECL/LVDS style and amplitude. Output levels are determined by the VDDO_QCLKD supply voltage.
B1, B2	QCLK_D1, nQCLK_D1	Output		Differential clock output D1 (Channel D). Configurable LVPECL/LVDS style and amplitude. Output levels are determined by the VDDO_QCLKD supply voltage.
E1, E2	QCLK_E, nQCLK_E	Output		Differential clock output E (Channel E). Configurable LVPECL/LVDS style and amplitude. Output is supplied by 3.3V (VDD_QCLKE).
A4, B4	QCLK_V, nQCLK_V	Output		Differential VCXO-PLL clock outputs. Selectable LVPECL/LVDS/(2x LVCMOS 1.8V) style.
C4	nINT	Output		Status output pin for signaling internal changed conditions. Selectable 1.8V/3.3V LVCMOS/LVTTL interface levels.
E3	LOCK	Output		PLL lock detect status output for both PLLs. Selectable 1.8V/3.3V LVCMOS/LVTTL interface levels.

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Table 1. Pin Descriptions (Cont.)

Ball	Name	Type[a]		Description
C5	SDA/MOSI	Input/ Output	—	Serial Control Port I^2C data I/O / SPI-4 wire Data Input / SPI-3 wire Data I/O. ▪ *When SPI input (MOSI)*: 1.8V interface levels with hysteresis and 3.3V tolerance. ▪ *When SPI-3-wire output (SDA):* Selectable 1.8V/3.3V output levels. ▪ *When I^2C output (SDA):* Open collector: Use an external pull-up resistor to the selected serial interface supply voltage.
C6	ADR1/MISO	Input/ Output	PD	Serial Control Port I^2C Address Bit 1/SPI Data Output. ▪ *When input (ADR1):* 1.8V interface levels with hysteresis and 3.3V tolerance. ▪ *When SPI output (MISO):* Selectable 1.8V/3.3V output levels.
D4	SCL/SCLK	Input	—	Serial Control Port I^2C Clock Input / SPI Clock Input. 1.8V interface levels with hysteresis and 3.3V tolerance. ▪ *When I^2C (SCL):* Use an external pull-up resistor to the selected serial interface supply voltage.
C3	ADR0/nCS	Input	—	Serial Control Port/I^2C Address Bit 0/SPI Chip Select Input. 1.8V interface levels with hysteresis and 3.3V tolerance.
D3	nI2C/SPI	Input	PD	Serial Interface I^2C/SPI Select. 1.8V interface levels with hysteresis and 3.3V tolerance.
H6	CR	Analog		Internal VCO regulator bypass capacitor. Use a 4.7µF capacitor between the CR and the VDD_LCF terminals.
H5	DNU			Do not use.
A7	LFV	Output		VCXO-PLL charge pump output. Connect to the loop filter for the external VCXO.
B6	OSC	Input	PD	VCXO non-inverting and inverting differential clock input. Compatible with LVPECL, LVDS and LVCMOS signals.
B5	nOSC		PD/PU	
J6	LFF	Output		Loop filter/charge pump output for the FemtoClock NG PLL. Connect to the external loop filter.
J5	LFFR	Analog		Ground return path pin for the VCO loop filter.
B7	RES_CAL	Analog		Connect a 2.8kΩ (1%) resistor to GND for output current calibration.
C7, D2, D7, E7, E8, E9, F1, F2, F3, F4, F5, F6, F7, G3, H3, H7, J3	GND	Power		Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
G4	DNU			Do not use.
G5	DNU			Do not use.
G6	CBIAS	Analog		Internal bias circuit for VCO. Connect a 4.7µF capacitor to GND.
G7	CLDO	Analog		Internal LDO bypass for VCO. Connect a 10µF capacitor to GND.
A8	VDDO_QCLKA	Power		Positive supply voltage (3.3V, 2.5V, or 1.8V) for the QCLK_A[2:0] outputs.

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Table 1. Pin Descriptions (Cont.)

Ball	Name	Type[a]		Description
B8	VDD_QCLKA	Power		Positive supply voltage (3.3V) for channel A.
J8	VDDO_QCLKB	Power		Positive supply voltage (3.3V, 2.5V or 1.8V) for the QCLK_B[2:0] outputs.
H8	VDD_QCLKB	Power		Positive supply voltage (3.3V) for channel B.
G1	VDDO_QCLKC	Power		Positive supply voltage (3.3V, 2.5V, or 1.8V) for the QCLK_C[1:0] outputs.
G2	VDD_QCLKC	Power		Positive supply voltage (3.3V) for channel C.
C1	VDDO_QCLKD	Power		Positive supply voltage (3.3V, 2.5V, or 1.8V) for the QCLK_D[1:0] outputs.
C2	VDD_QCLKD	Power		Positive supply voltage (3.3V) for channel D.
D1	VDD_QCLKE	Power		Positive supply voltage (3.3V) for the QCLK_E output and channel.
A3	VDD_SPI	Power		Positive supply voltage (3.3V) for the SPI interface.
E4	VDD_INP	Power		Positive supply voltage (3.3V) for the differential inputs (CLK[1:0]).
H4	VDD_LCV	Power		Positive supply voltage (3.3V) for the VCXO-PLL.
J4	VDD_LCF	Power		Positive supply voltage (3.3V) for the internal oscillator of the FemtoClock NG PLL.
A6	VDD_CPV	Power		Positive supply voltage (3.3V) for internal VCXO_PLL circuits.
J7	VDD_CPF	Power		Positive supply voltage (3.3V) for internal FemtoClock NG circuits.
A5	VDD_OSC	Power		Positive supply voltage (3.3V) for the VCXO input.

[a] PU (pull-up) and PD (pull-down) indicate internal input resistors (for values, see Figure 38).

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Principles of Operation

Overview

The 8V19N474 generates low-phase noise, synchronized clock output signals locked to an input reference frequency. The device contains two PLLs with configurable frequency dividers. The first PLL (VCXO-PLL, suffix V) uses an external VCXO as the oscillator and provides jitter attenuation. The external loop filter is used to set the VCXO-PLL bandwidth frequency in conjunction with internal parameters. The second, low-phase noise PLL (FemtoClock NG, suffix F) multiplies the VCXO-PLL frequency to the VCO frequency of 2500MHz. The FemtoClock NG PLL is completely internal and provides a central reference timing reference point for all output signals. From this point, fully synchronous dividers generate the output frequencies.

The device has five output channels (A to E): four channel with one integer output divider (A to D) and one channel with a fractional output divider (E). The clock outputs are configurable with support for LVPECL, LVDS formats, and a variable output amplitude. In channels A to D, the clock phase can be adjusted in phase. Individual outputs, channels and unused circuit blocks support powered-down states for operation at reduced power consumption. The register map, accessible through a selectable 3/4-wire SPI or I^2C interface with read-back capability controls the main device settings and delivers device status information. For redundancy purpose, there are two selectable reference frequency inputs and a configurable switch logic with manual, auto-selection, and holdover support.

Phase-Locked Loop Operation

Frequency Generation

The 8V19N474 supports four operation modes: Dual-PLL and VCXO-PLL with jitter attenuation, frequency synthesis, and the buffer/divider mode. Frequencies higher than the input frequency can be generated by the device by utilizing one or both PLLs. Using the PLL(s) require(s) the user to set the frequency dividers to match input, VCXO and VCO frequency and to achieve frequency and phase lock on the used PLLs. The frequency of the external VCXO is chosen by the user. The internal VCO frequency range is 2400–2500MHz. Table 2 displays the available frequency dividers for each of the four modes. Table 4 and Table 5 show example divider configurations.

The four operation modes are summarized as follows:

- Dual-PLL Jitter Attenuation Mode – Input clock jitter is attenuated by the VCXO-PLL (1st stage PLL). The 2nd stage PLL (FemtoClock NG) is locked to the 1st stage PLL and synthesizes a frequency in the range of 2400–2500MHz. Output dividers scale the frequency down to the target frequency. Dividers P_V, M_V, P_F, M_F, N_x and (optionally) N_E require a user configuration. This is the device's main operation mode with the highest flexibility in frequency generation. The best phase noise is achieved with internal frequency doubler turned on.
- VCXO-PLL Jitter Attenuation Mode – Input clock jitter is attenuated by the VCXO-PLL (1st stage PLL). The VCXO-output signal is divided by the output dividers to the target frequency. Dividers P_V, M_V, and N_X require a user configuration. The VCXO sets the highest frequency the device can achieve. The output phase noise is equivalent to the phase noise of the VCXO scaled by the output divider.
- Frequency Synthesis Mode – The 1st stage PLL is bypassed. The 2nd stage PLL (FemtoClock NG) is directly locked to the input source and synthesizes a frequency in the range of 2400–2500MHz. Output dividers scale the frequency down to the target frequency. Dividers P_V, P_F, M_F, N_x and (optionally) N_E require a user configuration. This mode is recommend for applications with a low-jitter input source.
- Divider/Buffer Mode – Both PLLs are bypassed. Output dividers scale the input frequency to the target frequency. Dividers P_V and N_x require a user configuration. In this mode, the PLL frequency specifications do not apply.

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Table 2. PLL Divider Values

Divider	Range	Operation			
		Jitter Attenuation		Frequency Synthesis	Divider/Buffer
		Dual-PLL (BYPV=0, SRC=0)	VCXO-PLL (BYPV =0, SRC=1)	VCXO-PLL Bypassed (BYPV = 1, SRC=0)	Both PLLs Bypassed (BYPV=1, SRC=1)
VCXO-PLL Pre-Divider P_V	÷1…÷32767: (15 bit)	Input clock frequency $f_{CLK} = \frac{f_{VCXO}}{M_V} \times P_V$		No external VCXO required	
VCXO-PLL Feedback Divider M_V	÷1…÷32767: (15 bit)				
FemtoClock NG Pre-Divider P_F	÷1…÷63: (6 bit)	VCXO frequency: $f_{VCXO} = f_{OVC} \times \frac{P_F}{M_F}$ f_{VCO} [a] P_F [b]	—	Input clock frequency: $f_{CLO} = f_{VCO} \times \frac{P_F}{M_F}$ f_{VCO} [a] P_F [b]	Output frequency $f_{OUT} = \frac{f_{CLK}}{N_X \times P_V}$
FemtoClock NG Feedback Dividers M_F	÷8 …÷511 (9 bit)				
Output Divider N*x* (*x* = A–D)	÷1…÷160 (Integer)[c]	Output frequency $f_{OUT} = \frac{f_{VCO}}{N_X}$	Output frequency $f_{OUT} = \frac{f_{VCXO}}{N_X}$	Output frequency $f_{OUT} = \frac{f_{VCO}}{N_X}$	
Output Divider N*E*	Fractional Divider[d]: N_{INT}: $4…2^4-1$ (Integer part) N_{FRAC}: $1…2^{24}-1$ (Fractional part)	Output frequency $f_{OUT} = \frac{f_{VCO}}{N_E}$ $N_E = 2 \times \left(N_{INT} + \frac{N_{FRAC}}{2^{24}} \right)$	—		

[a] f_{VCO} = 2400–2500MHz.

[b] Set P_F to 0.5 in the equation if the frequency doubler is engaged (FDF = 1).

[c] For a list of supported integer output dividers N*x* see Table 30

[d] Greatest N*E* fractional divider is $2 \times (14 + [2^{24}-1] / 2^{24}) \approx 29.99999988$

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VCXO-PLL

The prescaler P_V and the VCXO-PLLs feedback divider M_V require configuration to match the input frequency to the VCXO-frequency. With a divider value range of 15 bit the dividers M_V and P_V, the device support is very flexible and supports a wide range of input and VCXO-frequencies. In addition, the range of available input and feedback dividers allows to adjust the phase detector frequency independent of the used input and VCXO frequencies as shown in Table 4 and Table 5. The VCXO-PLL charge pump current is controllable via internal registers and can be set in 50µA steps from 50µA to 1.6mA. The VCXO-PLL can be bypassed (BYPV): when in bypass, the FemtoClock NG PLL locks to the pre-divided input frequency.

Table 3. Example Configurations for f_{VCXO} = 25MHz

Input Frequency (MHz)	VCXO-PLL Divider Settings		f_{PFD} (MHz)
	PV	MV	
25	1	1	25
	4	4	6.25
	16	16	1.5625
	64	64	0.390625
19.44	486	3125	0.04

Table 4. Example Configurations for f_{VCXO} = 125MHz

Input Frequency (MHz)	VCXO-PLL Divider Settings		f_{PFD} (MHz)
	PV	MV	
125	1	1	125
	5	5	25
	25	25	5
	125	125	1
156.25	5	4	31.25
	50	40	3.125
	500	400	0.3125

Table 5. Example Configurations for f_{VCXO} = 156.25MHz

Input Frequency (MHz)	VCXO- PLL Divider Settings		f_{PFD} (MHz)
	PV	MV	
19.44	1944	15625	0.01
25	4	25	6.25
	40	250	0.625
	400	2500	0.0625
125	4	5	31.25
	40	50	3.125
	400	500	0.3125

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Table 5. Example Configurations for f_{VCXO} = 156.25MHz (Cont.)

Input Frequency (MHz)	VCXO- PLL Divider Settings		f_{PFD} (MHz)
	PV	MV	
156.25	1	1	156.25
	10	10	15.625
	100	100	1.5625

Table 6. VCXO-PLL Bypass Settings

BYPV	Operation
0	VCXO-PLL operation.
1	VCXO-PLL bypassed and disabled. The reference clock for the FemtoClock NG PLL is the selected input clock. The input clock selection must be set to manual by the user. Clock switching and holdover are not defined. Device synthesizes an output frequency but will not attenuate input jitter. No external VCXO component and loop filter required.

FemtoClock NG PLL

The FemtoClock NG PLL is the second stage PLL and locks to the output signal of the VCXO-PLL (BYPV=0). It requires configuration of the frequency doubler FDF or the pre-divider PF and the feedback divider MF to match the VCXO-PLL frequency to the VCO frequency of 2500MHz. Best phase noise is typically achieved by engaging the internal frequency doubler (FDF= 1, x2). If engaged, the signal from the first PLL stage is doubled in frequency, increasing the phase detector frequency of the FemtoClock NG PLL. Enabling the frequency doubler disables the frequency pre-divider PF. If the frequency doubler is not used (FDF = 0), the PF pre-divider has to be configured. Typically PF is set to ÷1 to keep the phase detector frequency as high as possible. Set PF to other divider values to achieve specific frequency ratios between first and second PLL stage. This PLL is internally configured to high-bandwidth.

Table 7. Frequency Doubler

FDF	Operation
0	Frequency doubler off. PF divides clock signal from VCXO-PLL or input (in bypass)
1	Frequency doubler on (x2). Signal from VCXO-PLL or input (in bypass) is doubled in frequency. PF divider has no effect.

Table 8. Example PLL Configurations

VCXO-Frequency (MHz)	FemtoClock NG Divider Settings for VCO		
	2500MHz		
	FDF	PF	MF
25	x2	–	50
125	x2	–	10
	–	1	20
156.25	x2	–	8
	–	1	16

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Channel Frequency Divider

The 8V19N474 supports five independent output channels, A to E. The channels A to D have one configurable integer frequency divider N*x* (*x* = A to D) that divides the VCO frequency to the desired output frequency with very low phase noise. The integer divider values can be selected from the range of ÷1 to ÷160 as shown in Table 9. Channel E supports fractional divider ratios and is listed in Table 10).

Table 9. Integer Frequency Divider Settings

Channel Divider N*x*[a]	Output Clock Frequency (MHz) for VCO (MHz)
	2500
÷1	2500
÷2	1250
÷3	833.333
÷4	625
÷5	500
÷8	312.5
÷10	250
÷16	156.25
÷20	125
÷30	83.333
÷32	78.125
÷40	62.5
÷50	50
÷60	41.667
÷64	39.0625
÷80	31.25
÷100	25
÷120	20.833
÷128	19.53125
÷160	15.625

[a] *x* = A–D

Table 10. Typical Fractional Frequency Divider Settings

Channel Divider N*E* [a]	Output Clock Frequency (MHz) for VCO = 2500MHz
$15.\overline{51}$	161.1328125
18.75	133.333

[a] Greatest N*E* fractional divider is $2 \times (14 + [2^{24}-1] / 2^{24}) \approx 29.99999988$

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Table 11. PLL Feedback Path Settings

SRC	Operation
0	The output divider input signal is the FemtoClock NG PLL.
1	The output divider input signal is the VCXO-PLL output signal. FemtoClock NG PLL is bypassed.

Redundant Inputs

The two inputs are compatible with LVDS, LVPECL signal formats and also support single-ended signals (LVCMOS, see Applications Information for applicable input interface circuits).

Definitions

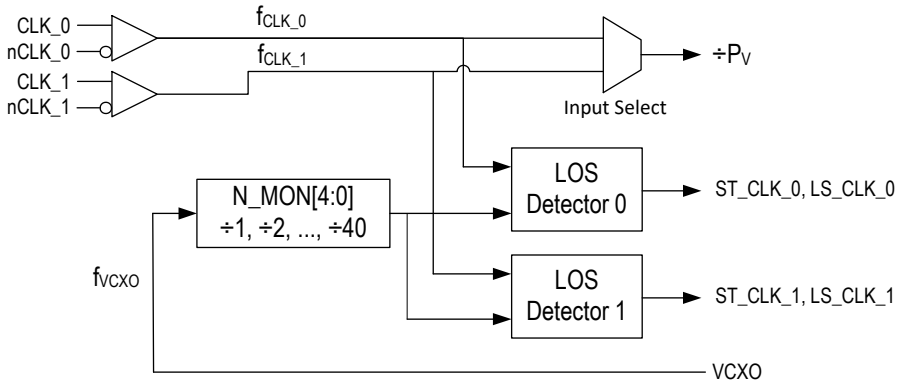
- Primary clock – The CLK_*n* input selected by the selection logic.
- Secondary clock – The CLK_*n* input not selected by the selection logic.
- PLL reference clock – The CLK_*n* input selected as the PLL reference signal by the selection logic. In automatic switching mode, the selection can be overwritten by a state machine.

Monitoring

Loss of Input Signal (LOS)

In operation, a clock input is declared invalid (LOS) with the corresponding ST_CLK_*n* and LS_CLK_*n* indicator bits set after a specified number of consecutive clock edges. If differential input signals are applied, the input will also detect an LOS condition in case of a zero differential input voltage. The device supports LOS detect circuits, one for each input. The signal detect circuits compare the signals at the CLK_0 and CLK_1 inputs to internally frequency-divided signals from the VCXO-PLL (for information, see Figure 3). The loss-of-signal fault condition is declared upon three or more missing clock input edges. LOS requires configuration of the N_MON[4:0] frequency divider setting to individually match the input frequencies CLK_*n* to the VCXO frequency: $f_{VCXO} \div N\_MON[4:0] = f_{CLK\_n}$. For example, if one of the input frequencies is 25MHz and a 125MHz VCXO is used, set N_MON[4:0] =÷5 (for configuration information, see Table 28). Then, LOS is declared after three consecutive missing clock edges. LOS is signaled through the ST_CLK_*n* (momentary) and LS_CLK_*n* (sticky, resettable) status bits and can reported as an interrupt signal on the nINT output. The LOS circuit requires the jitter attenuation mode of device (BYPV=0). LOS does not detect frequency errors.

Figure 3. LOS Detect Circuit



Input Re-Validation

A clock input is declared valid and the corresponding LOS bit is reset after the clock input signal returned for user-configurable number of consecutive input periods. This re-validation of the selected input clock is controlled by the CNTV setting (verification pulse counter).

Clock Selection

The 8V19N474 supports five input selection modes: manual with and without holdover, short-term holdover, and two automatic switch modes.

Table 12. Clock Selection Settings

Mode			Name	Description	Flags				Application
nHO_EN	nMA1	nMA0			ST_CLKn	nST_HOLD	ST_SEL	ST_REF	
0	X	X	Manual Holdover Control (default)	Input selection follows user-configuration of the EXT_SEL pin or INT_SEL register bit as set by nEXT_INT. Input selection is *never* changed by the internal state machine.					
				LOS on the primary reference clock: Active reference stays selected and the PLLs may stall. Device will not go into holdover.	LOS status	1	Selected input	0[a]	Startup and external selection control with holdover
				Manual change of the reference clock: The device *will go into holdover* and the hold-off down-counter (CNTH) starts. The device initiates a clock switch *after* expiration of the hold-off counter. Duration of holdover is set by CNTH × CNTR / f_{VCXO}. Holdover is terminated even if the secondary clock input is bad (LOS). See "Manual Holdover Control (nHO_EN = 0)"		0[b]	Selected input[c]	LOS status of *selected* input	
1	0	0	Manual Control	Input selection follows user-configuration of the EXT_SEL pin or INT_SEL register bit as set by nEXT_INT. Input selection is *never* changed by the internal state machine.					
				LOS on the primary reference clock: Active reference stays selected and the PLLs may stall. Device will not go into holdover.	LOS status	1	Selected input	0	External selection control
				Manual change of the reference clock: The device will not go into holdover and will attempt to lock to the newly selected reference.		1	Selected input	Actual LOS status of selected input	
1	0	1	Automatic	Input selection follows LOS status. A failing input clock will cause an LOS event for that clock input. If the selected clock has an LOS event, the device will immediately initiate a clock failover switch.					
				LOS on the primary reference clock: The device will switch to the secondary clock without holdover. Input selection is determined by a state machine and may differ from the user's clock selection No valid clock scenario: If no valid input clocks exist, the device will not attempt to switch and will not enter the holdover state. The PLL is not locked. Re-validation of all input clocks will result in the PLL to attempt to lock on that input clock. See "Revertive Switching".	LOS status	1	Selected input determined by state machine	Actual LOS status of selected input determined by state machine	Multiple inputs with qualified clock signals
				Manual change of the reference clock: The device will switch to the newly selected clock without holdover. If the newly selected clock is not valid, the PLL may stall.		1	Selected Input	Actual LOS status of selected input	

Table 12. Clock Selection Settings (Cont.)

Mode			Name	Description	Flags				Application
nHO_EN	nMA1	nMA0			ST_CLKn	nST_HOLD	ST_SEL	ST_REF	
1	1	0	Short-term Holdover	Input selection follows user-configuration of EXT_SEL pin or INT_SEL register bit as set by nEXT_INT. Selection is never changed by the internal state machine.					
				LOS on the primary reference clock: A failing reference clock will cause an LOS event. If the selected reference fails, the device will enter holdover *immediately*. Re-validation of the selected input clock is controlled by the CNTV setting. A successful re-validation will result in the PLL to re-lock on that input clock.	LOS status	0 For holdover duration	Selected Input	LOS status for duration of LOS until revalidation	Use if a single reference is occasionally interrupted
				Manual change of the reference clock: The device will switch to the newly selected clock without holdover. If the newly selected clock is not valid, the PLL may stall.		1	Selected Input	Actual LOS status of selected input	
1	1	1	Automatic with Holdover	Input selection follows LOS status. A failing input clock will cause an LOS event for that clock input. If the *selected* clock has an LOS event, the device will go into holdover and switches input clocks after the hold-off counter expires.					
				LOS on the primary reference clock or Manual change of the reference clock: The device will go into holdover and the hold-off down-counter (CNTH) starts. The device initiates a clock failover switch to a valid secondary clock input *after* expiration of the hold-off counter. Duration of holdover is set by CNTH*CNTR / f_{VCXO}. The holdover is terminated prior to the hold-off count-down if the primary clock revalidates or is terminated by a manual change of the reference clock. See "Automatic with Holdover (nHO_EN = 1, nM/A[1:0] = 11)" and See "Revertive Switching" No valid clock scenario: The device remains in holdover if the secondary input clock is invalid.	LOS status	0 For holdover duration	Selected input determined by state machine	Actual LOS status of selected input	Multiple inputs

[a] For the duration of an invalid input signal (LOS)

[b] For the duration of holdover.

[c] Delayed by holdover period.

Holdover

In holdover state, the output frequency and phase is derived from an internal, digital value based on previous frequency and phase information. Holdover characteristics are defined in Table 45.

Manual Holdover Control (nHO_EN = 0)

This is the default switching mode of the device. The switch control is manual: the EXT_SEL pin or the INT_SEL bit as set by nEXT_INT determines the selected reference clock input. If the selection is changed by the user, the device will enter holdover until the CNTH[7:0] counter expires. Then, the new reference is selected (input switch). Application for this mode is startup and external selection control.

- ST_REF: status of selected reference clock
- ST_CLK_n will both reflect the status of the corresponding input
- ST_SEL: the new selection
- nST_HOLD = 0 for the duration of holdover

Automatic with Holdover (nHO_EN = 1, nM/A[1:0] = 11)

If an LOS event is detected on the active reference clock:

- Holdover begins immediately
- Corresponding ST_REF and LS_REF go low immediately
- Hold-off countdown begins immediately.

During this time, both input clocks continue to be monitored and their respective ST_CLK and LS_CLK flags are active. LOS events will be indicated on ST_CLK and LS_CLK when they occur.

If the active reference clock resumes and is validated during the hold-off countdown:

- Its ST_CLK status flag will return high and the LS_CLK is available to be cleared by an SPI write of 1 to that register bit
- No transitions will occur of the active REF clock; ST_SEL does not change
- Revertive bit has no effect during this time (whether 0 or 1)

When the hold-off countdown reaches zero:

- If the active reference has resumed and has been validated during the countdown, it will maintain being the active reference clock
  - ST_SEL does not change
  - ST_REF returns to 1
  - LS_REF can be cleared by an SPI write of 1 to that register
  - Holdover turns off and the VCXO-PLL attempts to lock to the active reference clock
- If the active reference has not resumed but the other clock input CLK_*n* is validated, then
  - ST_SEL changes to the new active reference
  - ST_REF returns to 1
  - LS_REF can be cleared by an SPI write of 1 to that register
  - Holdover turns off
- If there is no validated CLK:
  - ST_SEL does not change
  - ST_REF remains low
  - LS_REF cannot be cleared by an SPI write of 1 to that register
  - Holdover remains active

Revertive capability returns if REVS = 1.

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Hold-off Counter

A configurable down-counter applicable to the “Automatic with holdover” and “manual with holdover” selection modes. The purpose of this counter is a deferred, user-configurable input switch. The counter expires when a zero-transition occurs; this triggers a new reference clock selection. The counter is clocked by the frequency-divided VCXO-PLL signal. The CNTR setting determines the hold-off counter frequency divider and the CNTH setting the start value of the hold-off counter. For example, set CNTR to a value of ÷131072 to achieve 953.67Hz (or a period of 1.048ms at f_{VCXO}=125.0MHz): the 8-bit CNTH counter is clocked by 953.67Hz and the user-configurable hold-off period range is 0ms (CNTR = 0x00) to 267ms (CNTR = 0xFF). After the counter expires, it reloads automatically from the CNTH SPI register. After the LOS latched status bit (LS_CLK_*n*) for the corresponding input CLK_*n* has been cleared by the user, the input is enabled for generating a new LOS event.

The CNTR counter is only clocked if the device is configured in the clock selection mode, “Automatic with holdover,” *AND* the *selected* reference clock experiences an LOS event or in the “manual with holdover” mode with manual switching. Otherwise, the counter is automatically disabled (not clocked).

Revertive Switching

Revertive switching is only applicable to the two automatic switch modes discussed in Table 12:

- Revertive switching enabled – Re-validation of any non-selected input clock(s) will cause a new input selection according to the user-preset input priorities (revertive switch). An input switch is only done if the re-validated input has a higher priority than the currently selected reference clock.
- Revertive switching disabled – Re-validation of a non-selected input clock has no impact on the clock selection. Default setting is revertive switching disabled.

VCXO-PLL Lock Detect (LOLV)

The VCXO-PLL lock detect circuit uses the signal phase difference at the phase detector as loss-of-lock criteria. Loss-of-lock is reported if the actual phase difference is larger than a configurable phase detector window set by the LOCK_TH[14:0] configuration bits. A loss-of-lock state is reported through the nST_LOLV and nLS_LOLV status bits (see Table 16); it can also be reported as a hardware signal on the LOCK output as well as an interrupt signal on the nINT output. The VCXO-PLL lock detect function requires to set FVCV = 0.

FemtoClock NG Loss-of-Lock (LOLF)

FemtoClock NG PLL loss of lock is signaled through the nST_LOLF (momentary) and nLS_LOLF (sticky, resettable) status bits, and can reported as a hardware signal on the LOCK output as well as an interrupt signal on the nINT output.

Differential Outputs

Table 13. Output Features

Output	Style	Amplitude[a]	Disable	Power Down	Termination
QCLK_*y*	LVPECL	350–850mV 4 steps	Yes	Yes	50Ω to V_{TT}[b]
	LVDS				100Ω differential
QCLK_V	LVPECL	350–850mV 4 steps	Yes	Yes	50Ω to V_{TT}
	LVDS				100Ω differential
	LVCMOS[c]	1.8V	Yes	Yes	

[a] Amplitudes are measured single-ended.

[b] See Table 49 for V_{TT} (Termination voltage) values.

[c] LVCMOS style: nQCLK_V and QCLK_V are complementary.

Table 14. Individual Clock Output Settings

PD[a]	Output Power	STYLE	Termination	Enable	State	A[1:0]	Amplitude (mV)[b]
1	Off	X	100Ω differential or no termination	X	Off	X	X
0	On	0	100Ω differential (LVDS)	0	Disable[c]	XX	X
				1	Enable	00	350
						01	500
						10	700
						11	850
		1	50Ω to V_{TT}[d] (LVPECL)	0	Disable	XX	X
				1	Enable	00	350
						01	500
						10	700
						11	850

[a] Power-down modes are available for the individual channels A-D and the outputs QCLK_y (A0–D1). QCLK_*E* is defined: nPD_E=0: power-down and nPE=0.

[b] Output amplitudes of 700mV and 850mV require a 3.3V output supply (V_{DDO_V}). 350mV and 500mV output amplitudes support V_{DDO_V} = 2.5V and 1.8V.

[c] Differential output is disabled in static low/high state

[d] See Table 49 for V_{TT} (Termination voltage) values.

Output Phase-Delay

Output phase delay is supported in each channel. The selected VCO frequency sets the delay unit to $1/f_{VCO}$.

Table 15. Delay Circuit Settings

Delay Circuit	Unit	Steps	Range
Clock phase Φ_{CLK_x}	$\frac{1}{f_{VCO}}$ f_{VCO} = 2500MHz: 400ps	256	0–102ns

Status Conditions and Interrupts

The 8V19N474 has an interrupt output to signal changes in status conditions. Settings for status conditions can be accessed in the Status registers. The device has several conditions that can indicate faults and status changes in the operation of the device. These are shown in Table 16 and can be monitored directly in the status registers. Status bits (named: ST_*condition*) are read-only and reflect the momentary device status at the time of read-access. Several status bits are also copied into latched bit positions (named: LS_*condition*).

The latched version is controlled by the corresponding fault and status conditions and remains set (sticky) until reset by the user by writing 1 to the status register bit. The reset of the status condition only has an effect if the corresponding fault condition is removed; otherwise, the status bit will set again. Setting a status bit on several latched registers can be programmed to generate an interrupt signal (nINT) via settings in the Interrupt Enable bits (named: IE_*condition*). A setting of 0 in any of these bits will mask the corresponding latched status bits from affecting the interrupt status pin. Setting all IE bits to 0 has the effect of disabling interrupts from the device.

Table 16. Status Bit Functions

Status Bit		Function			Interrupt Enable Bit
Momentary	Latched	Description	Status if Bit is: 1	Status if Bit is: 0	
ST_CLK_0	LS_CLK_0	CLK 0 input status	Active	LOS	IE_CLK_0
ST_CLK_1	LS_CLK_1	CLK 1 input status	Active	LOS	IE_CLK_1
nST_LOLV	nLS_LOLV	VCXO-PLL loss of lock	Locked	Loss of lock	IE_LOLV
nST_LOLF	nLS_LOLF	FemtoClock NG-PLL loss of lock	Locked	Loss of lock	IE_LOLF
nST_HOLD	nLS_HOLD	Holdover	Not in holdover	Device in holdover	IE_HOLD
ST_VCOF	—	FemtoClock NG VCO calibration	Not completed	Completed	—
ST_SEL	—	Clock input selection	0 = CLK_0 1 = CLK_1		—
ST_REF	LS_REF	PLL reference status	Valid reference[a]	Reference lost	IE_REF

[a] Manual and short-term holdover mode: 0 indicates if the selected reference is lost, 1 if not lost.
Automatic mode: will transition to 0 while the input clock is lost and during input selection by priority.
Manual holdover mode: 0 indicates that a manual change of the reference clock has occurred and is still in holdover.
Automatic with holdover mode: 0 indicates the reference is lost and still in holdover.

Interrupts are cleared by resetting the appropriate bit(s) in the latched register after the underlying fault condition has been resolved. When all valid interrupt sources have been cleared in this manner, this will release the nINT output until the next unmasked fault.

Table 17. LOCK Function

Status Bit (PLL)		Status Reported on LOCK[a] Output[b]
nLS_LOLV (VCXO-PLL)	nLS_LOLF (FemtoClock NG)	
Locked	Locked	1
Locked	Not locked	0
Not locked	Locked	0
Not locked	Not locked	0

[a] Hardware interrupts on nINT require setting the IE_LOLV and IE_LOLF bits to “enable interrupt”.

[b] SELSV1 controls the logic level 1.8V/3.3V of LOCK and nINT outputs.

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Device Startup, Reset, and Synchronization

At startup, an internal POR (power-on reset) resets the device and sets all register bits to their default value. The 8V19N474 forces the VCXO control voltage at the LFV pin to half of the power supply voltage to center the VCXO-frequency. In the default configuration the QCLK_*y* outputs are disabled at startup.

Recommended configuration sequence (in order):

1. (Optional) Set the value of the CPOL register bit to define the SPI read mode supported by the SPI controller. Set the SDO_ACT bit in register 0x00 as appropriate for SPI access to the device.
2. Configure all PLL and output divider and delay circuits as well as other device configurations, such as the charge pump currents.
3. Set the initialization bit, INIT_CLK.

   This will initiate all divider and delay circuits and synchronize them to each other. The INIT_CLK bit will self-clear.
4. Set the RELOCK and PB_CAL bits.

   This step should not be combined with the previous step (setting INIT_CLK) in a multi SPI-byte register access. Both bits will self-clear.
5. Clear the FVCV bit to release the VCXO control voltage and VCXO-PLL will attempt to lock to the input clock signal starting from its center frequency.
6. Clear the status flags.
7. Enable the outputs by accessing the output-enable registers in a separate SPI write access.

Serial Interface

The 8V19N474 supports both I^2C and SPI configuration interfaces. The nI2C/SPI control input selects between the interfaces. The serial interface selection has to be applied at power-up and should not be changed during operation of the device. Changing the state of the nI2C/SPI pin during operation may put the serial interface in an undetermined state.

Table 18. Serial Interface Configuration

nI2C/SPI	SDO_ACT	Operation	Pins[a]	Recommended External Resistor[b]	
Pin D3	Reg. 0x00, D1			SELSV0 = 0 (1.8V)	SELSV0 = 1 (3.3V)
0 (default)	X	I^2C	I/O: SDA (I/O)	PU to 1.8V	PU to 3.3V
			I: SCL	PU to 1.8V	PU to 3.3V
			I: ADR[1:0]	PD to GND or PU to 1.8V	PD to GND or PU to 3.3V
1	1	SPI (4 wire)	O: MISO	—	
			I: MOSI, SCLK, nCS	Weak PD to GND	
	0	SPI (3 wire)	I/O: MOSI	Weak PD to GND	
			I: SCLK, nCS	Weak PD to GND	

[a] I/O: Pin is Input/Output, I: pin is input-only, O: pin is output only.

[b] PD = Pull-down resistor, PU = Pull-up resistor.

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SPI Interface (nI2C/SPI = 1)

If the serial interface is configured to SPI, the serial control port will respond as a slave in an 3/4-wire SPI configuration to allow read and write access to any of the internal registers for device programming or read back. The SPI interface consists of the SCLK (clock), MOSI (serial data input and output in 3-wire mode, input in 4-wire mode), MISO (output in 4-wire mode), and nCS (chip select) pins. The MISO output is of push/pull type. A data transfer consists any integer multiple of 8 bits and is always initiated by the SPI master on the bus. Internal register data is organized in SPI bytes of 8 bits each.

3/4-Wire Mode. In 3-wire mode, the MOSI pin acts as bidirectional input/output and the MISO pin is in high-impedance state. In 4-wire mode, the MOSI pin is the SPI input and the MISO pin is the SPI output. The SPI interface mode is defined by the SDO_ACT bit in the SPI device configuration register.

Active Clock Edge. In a write operation, the data on MOSI will be clocked in on the rising edge of SCLK. In a read operation, data on the MISO (4-wire) / MOSI (3-wire) will be clocked out on the falling or rising edge of SCLK depending on the CPOL setting (CPOL = 0: output data changes on the falling edge, CPOL = 1: output data changes on the rising edge).

Reset. The SRESET bit in the device SPI configuration register resets the registers 0x02 to 0x63 to their default values. The 0x00 and 0x01 registers are not reset by asserting SRESET.

Logic levels. The SPI outputs MISO (4-wire) and MOSI (3-wire, when output) have selectable 1.8V/3.3V logic output levels. The SELSV0 register bit controls the logic level. SELSV0 = 0: 1.8V logic and SELSV0 = 1: 3.3V logic.

Starting a data transfer requires nCS to set and hold at logic low level during the entire transfer. Setting nCS = 0 will enable the SPI interface. The master must initiate the first 8-bit transfer. The first bit presented by the SPI master in each transfer is the LSB (least significant bit). The first bit presented to the slave is the direction bit R/nW (1=Read, 0=Write), and the following seven bits are the address bits A[0:6] pointing to an internal register in the address space 0x00 to 0x63.

Read operation from an internal register: a read operation starts with an 8-bit transfer from the master to the slave: MOSI is clocked on the *rising* edge of SCLK. The first bit is the direction bit R/nW which must be to 1 to indicate a read transfer, followed by 7 address bits A[0:6]. After the first 8 bits are clocked into MOSI, data is available at the MISO (4-wire) / MOSI (3-wire) output: the register content addressed by A[0:6] is loaded into the shift register and the next 8 SCLK *falling* clock cycles (CPOL=0) will then present the loaded register data on the MISO output and transfer these to the master. Transfers must be completed by de-asserting nCS after any multiple of 8 SCLK cycles. If nCS is de-asserted at any other number of SCLKs, the SPI behavior is undefined. SPI byte (8 bit) and back-to-back read transfers of multiple registers are supported with an address auto-increment. During multiple transfers, nCS must stay at logic low level and MISO (4-wire) / MOSI (3-wire) will present multiple registers (A), (A+1), (A+2), etc. with each 8 SCLK cycles. During SPI Read operations, the user may continue to hold nCS low and provide further bytes of data for up to a total of 100 (0x64) bytes in a single block read.

Write operation to a 8V19N474 register: During a write transfer, an SPI master transfers one or more bytes of data into the internal registers of the device. A write transfer starts by asserting nCS to low logic level. The first bit presented by the master must set the direction bit R/nW to 0 (Write) and the 7 address bits A[0:6] must contain the 7-bit register address. Bits D0 to D7 contain 8 bits of payload data, which is written into the register addressed by A[0:6] at the end of a 8-bit write transfer. Multiple, subsequent register transfers from the master to the slave are supported by holding nCS asserted at logic low level during write transfers. The 7-bit register address will auto-increment. Transfers must be completed with de-asserting nCS after any multiple of 8 SCLK cycles. If nCS is de-asserted at any other number of SCLKs, the SPI behavior is undefined.

End of transfer: After nCS de-asserts to logic 1, the SPI bus is available to transfers to other slaves on the SPI bus. See also the READ diagram (Figure 4) and WRITE (Figure 5) displaying the transfer of two bytes of data from and into registers.

Registers 0x5C to 0x63. Reserved registers and registers in the address range 0x5C to 0x63 should not be used. Do not write into any registers in the 0x5C to 0x63 range.

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Figure 4. Logic Diagram: SPI 4-Wire READ Data from 8V19N474 Registers for CPOL = 0 and CPOL = 1

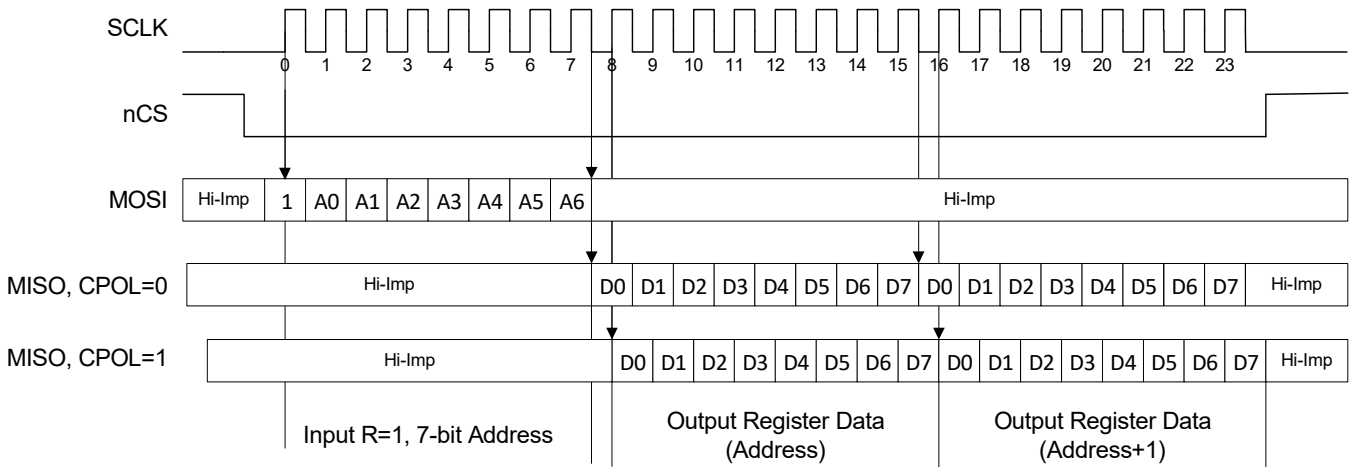


Figure 5. Logic Diagram: SPI 4-Wire WRITE Data into 8V19N474 Registers

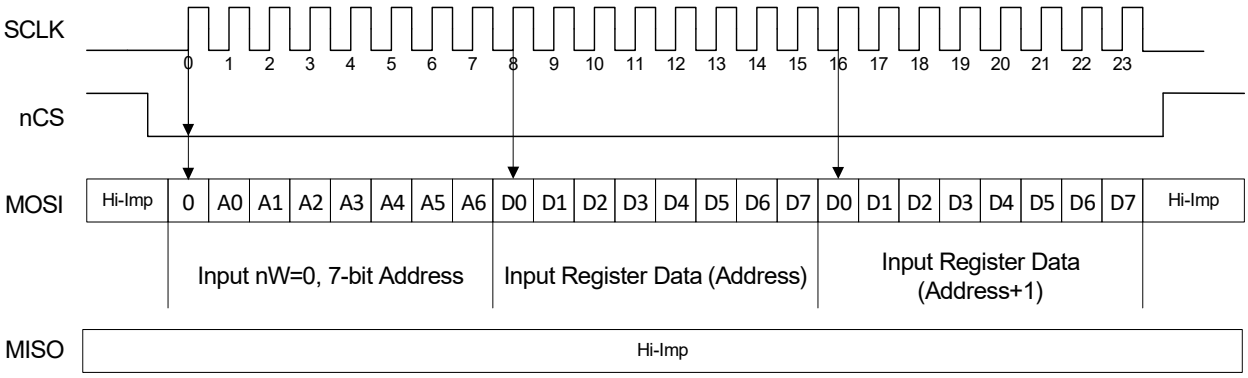
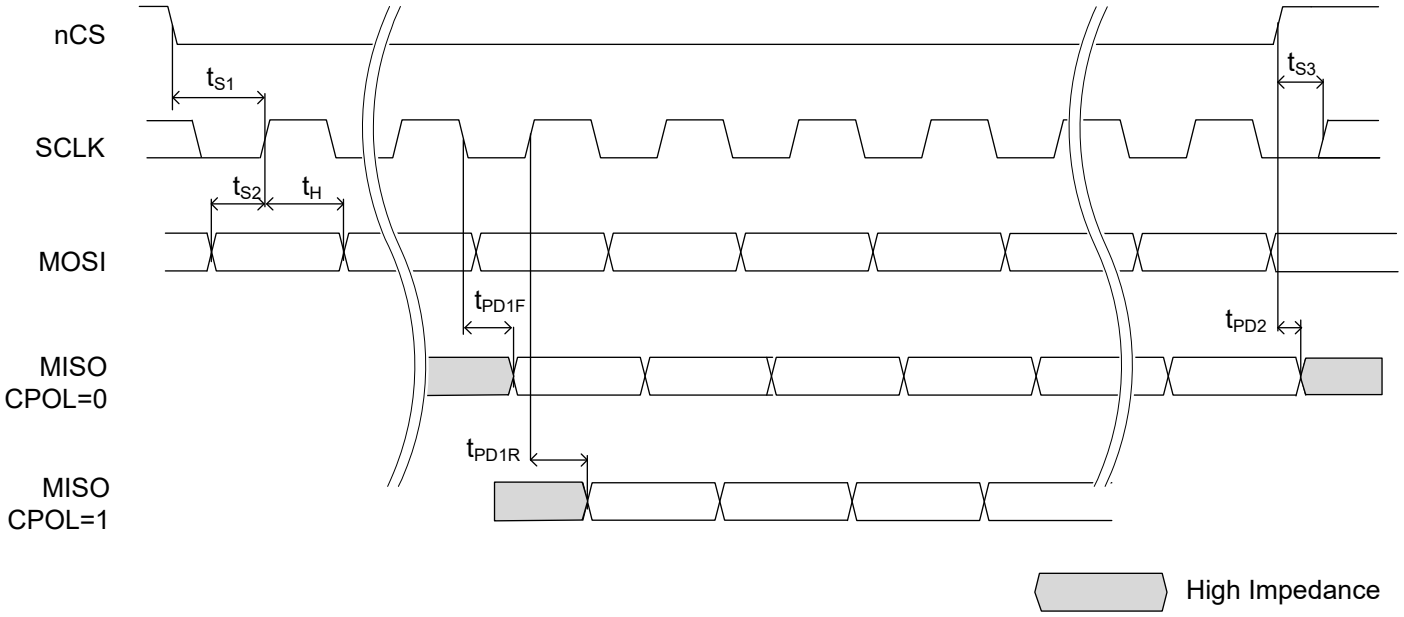


Table 19. SPI Read / Write Cycle Timing Parameters[a]

Symbol	Parameter	Test Condition	Minimum	Maximum	Unit
f_{SCLK}	SCLK frequency			20	MHz
t_{S1}	Setup time, nCS (falling) to SCLK (rising)		5		ns
t_{S2}	Setup time, MOSI to SCLK (rising)		5		ns
t_{S3}	Setup time, nCS (rising) to SCLK (rising)		5		ns
t_H	Hold time, SCLK (rising) to MOSI		5		ns
t_{PD1F}	Propagation delay, SCLK (falling) to MISO	CPOL=0		12	ns
t_{PD1R}	Propagation delay, SCLK (rising) to MISO	CPOL=1		12	ns
t_{PD2}	Propagation delay, nCS to MISO disable			5	ns

[a] nI2C/SPI = 1 (SPI interface)

Figure 6. SPI Timing Diagram



I²C Interface (nI2C/SPI = 0)

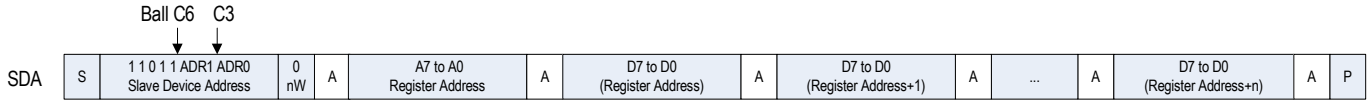
When the serial interface is configured to I²C, the 8V19N474 will respond as a slave in an I²C compatible configuration at a base address of 11011[ADR1, ADR0]b, to allow access to any of the internal registers for device programming or examination of internal status. The ADR[1:0] bits of the I²C interface address are set by the logic state of the ADR1 (C6) and ADR0 (C3) balls. If more than one 8V19N474 is connected to the same I²C bus, set ADR1 and ADR0 to different states on each device to avoid address conflicts.

I²C Mode Operation

The I²C interface fully supports v1.2 of the *I²C Specification* for Normal and Fast mode operation. The device acts as a slave device on the I²C bus at 100kHz, or 400kHz using a fixed base address of 11011[ADR1, ADR0]b. The interface accepts byte-oriented block write and block read operations. One address byte specifies the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data is moved into the registers byte by byte and before a STOP bit is received.

For full electrical I²C compliance, it is recommended to use external pull-up resistors for SDA and SCL. The internal pull-up resistors have a size of 51kΩ typical.

Figure 7. I²C Write Data (Master Transmit, Slave Receive) From Any Register Address



Write to slave to the specified register address A[7:0]. The slave auto-increments the register address and data is written sequentially.

S Start (Master)

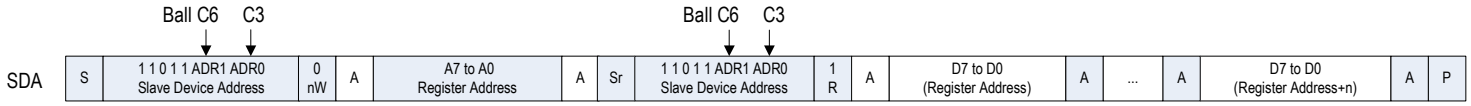
P Stop (Master)

A Acknowledge (Slave to Master)

Master transmit, Slave Receive

Slave transmit, Master Receive

Figure 8. I²C Read Data (Slave Transmit, Master Receive) From Any Register Address



Read from slave from the specified register address A[7:0]. Data is transmitted to the master after a change of the transfer direction with a repeated start The slave auto-increments the register address and transmits register data to the master sequentially.

S Start (Master)

Sr Repeated start (Master)

P Stop (Master)

A Acknowledge (Slave to Master)

A Acknowledge (Master to Slave)

Master transmit, Slave Receive

Slave transmit, Master Receive

Register Descriptions

This section contains all addressable registers, sorted by function, followed by a detailed description of each bit field. Several functional blocks with multiple instances in this 8V19N474 have individual registers controlling their settings, but since the registers have an identical format and bit meaning, they are described only once, with an additional table to indicate their addresses and default values. All writable fields come up with default values as indicated in the Factory Defaults column unless altered by values loaded from non-volatile storage during the initialization sequence.

Fixed read-only bits will have defaults as indicated in their specific register descriptions. Read-only status bits will reflect valid status of the conditions they are designed to monitor once the internal power-up reset has been released. Unused registers and bit positions are Reserved. Reserved bit fields may be used for internal debug test and debug functions.

List of Registers

Table 20. Configuration Registers

Register Address	Register Description
0x00	Device Configuration
0x01	I^2C Address (I^2C only)
0x02–0x0F	Reserved
0x10–0x11	PLL Frequency Divider: PV
0x12–0x13	PLL Frequency Divider: MV
0x14	Reserved
0x15–0x16	LOCK_TH
0x17	PLL Control: BYPV
0x18	PLL Control: SRC, VCO_SEL
0x19	PLL Frequency Divider: PF, FDF
0x1A–0x1B	PLL Frequency Divider: MF
0x1C–0x1E	PLL Control
0x1F	I/O Voltage Select
0x20–0x23	Input Selection
0x24–0x26	Channel A
0x27	Reserved
0x28–0x2A	Output States QCLK_A0–A2
0x2B	Reserved
0x2C–0x2E	Channel B
0x2F	Reserved
0x30–0x32	Output States QCLK_B0–B2
0x33	Reserved
0x34–0x36	Channel C
0x37	Reserved
0x38–0x39	Output States QCLK_C0–C1
0x3A–0x3B	Reserved

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Table 20. Configuration Registers (Cont.)

Register Address	Register Description
0x3C–0x3E	Channel D
0x3F	Reserved
0x40–0x41	Output States QCLK_D0–D1
0x42–0x43	Reserved
0x44–0x47	Channel E
0x48	Output States QCLK_E
0x49–0x4A	Reserved
0x4B	Output States QCLK_V
0x4C	Interrupt Enable
0x4D	Reserved
0x4E–0x4F	Reserved
0x50	Status (Latched)
0x51	Status (Momentary)
0x52	Reserved
0x53	Status (Momentary)
0x54	Reserved
0x55–0x57	General Control
0x58	Channel Enable A–E and QCLK_V
0x59–0x5B	Reserved
0x5C–0x5E	Reserved
0x5F–0x60	Reserved
0x61–0x62	Reserved
0x63	Reserved

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Device Configuration Registers

Table 21. Device Configuration Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x00	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SDO_ACT	SRESET
0x01	Reserved	I2C_ADR[6:0]						
0x1F	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SELSV1	SELSV0

Table 22. Device Configuration Register Descriptions

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
SRESET	R/W Auto-Clear	0 Value = not reset	Soft Reset 0 = Normal Operation 1 = Register reset. The device loads the default values into the register 0x02–0xFF. The content of the register addresses, 0x00 and 0x01, and the serial interface engine, are not reset.
I2C_ADR[6:0]	R	11011[ADR1][ADR0]	I^2C Device Address (I^2C only) This read-only register stores the binary I^2C device address: 11011[ADR1][ADR0]. Bit D1 is equal to the logic state of the ADR1 pin, and bit D0 is equal to the logic state of the ADR0 pin. In SPI mode (nI2C/SPI = 1), ADR1 and ADR0 read logic 0.
SDO_ACT	R/W	0 Value: SPI-3-wire mode	SPI 3/4 Wire Mode (SPI only) Selects the unidirectional or bidirectional data transfer mode for the SDIO pin. 0 = SPI 3-wire mode: – MOSI is the SPI bidirectional data I/O pin. – MISO pin is not used and is in high-impedance. 1 = SPI 4-wire mode – MOSI is the SPI data input pin. – MISO is the SPI data output pin.
SELSV1	R/W	1 Value: 3.3V	Selects the voltage level of the LOCK and nINT outputs 0 = LOCK, nINT interface pins are 1.8V. 1 = LOCK, nINT interface pins are 3.3V (default).
SELSV0	R/W	0 Value: 1.8V	Selects the voltage level of the I^2C/SPI interface. Applicable to pins configured to output. 0 = I^2C/SPI interface pins are 1.8V (default). 1 = I^2C/SPI interface pins are 3.3V.

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PLL Frequency Divider Registers

Table 23. PLL Frequency Divider Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x10	PV[7:0]							
0x11	Reserved	PV[14:8]						
0x12	MV[7:0]							
0x13	Reserved	MV[14:8]						
0x15	LOCK_TH[7:0]							
0x16	Reserved	LOCK_TH[14:8]						
0x19	FDF	Reserved	PF[5:0]					
0x1A	MF[7:0]							
0x1B	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MF8

Table 24. PLL Frequency Divider Register Descriptions

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
PV[14:0]	R/W	000 0100 0000 0000 Value=÷1024	VCXO-PLL Input Frequency Pre-Divider The value of the frequency divider (binary coding). Range: ÷1 to ÷32767
MV[14:0]	R/W	000 0100 0000 0000 Value=÷1024	VCXO-PLL Feedback-Divider The value of the frequency divider (binary coding). Range: ÷1 to ÷32767
LOCK_TH[14:0]	R/W	000 0000 1000 0000 Value = 128	PLL lock detect phase window threshold The device reports VCXO-PLL lock when the phase difference between the internal signals f_{REF} and f_{VCXO_REF} are lower than or equal to the phase difference set by LOCK_TH[14:0] for more than 1000 f_{VCXO_DIV} clock cycles. Requires $M_V \geq 4$. Set LOCK_TH[14:0] < M_V. ($f_{REF} = f_{CLK} \div P_V$ is the internal output of the PV divider, $f_{VCXO\_DIV} = f_{VCXO} \div M_V$ is the internal output of the MV divider).

Table 24. PLL Frequency Divider Register Descriptions (Cont.)

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
PF[5:0]	R/W	00 0001 Value = ÷1	FemtoClock NG Pre-Divider The value of the frequency divider (binary coding). Range: ÷1 to ÷63 00 0000: PF is bypassed
FDF	R/W	0 Value = f_{VCXO} ÷ PF	Frequency Doubler The input frequency of the FemtoClock NG PLL (2nd stage) is: 0 = The output signal of the BYPV multiplexer, divided by the PF divider. 1 = The output signal of the BYPV multiplexer, doubled in frequency. Use this setting to improve phase noise. The PF divider has no effect if FDF = 1.
MF[8:0]	R/W	0 0001 1000 Value = ÷24	FemtoClock NG Feedback-Divider The value of the frequency divider (binary coding). Range: ÷8 to ÷511

PLL Control Registers

Table 25. PLL Control Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x17	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BYPV
0x18	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SRC	VCO_SEL
0x1C	POLV	FVCV	Reserved	CPV[4:0]				
0x1D	Reserved	Reserved	OSVEN	OFFSET[4:0]				
0x1E	Reserved	Reserved	Reserved	CPF[4:0]				

Table 26. PLL Control Register Descriptions

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
BYPV	R/W	0 VCXO-PLL enabled	VCXO-PLL Bypass 0 = VCXO-PLL is enabled. 1 = VCXO-PLL is disabled and bypassed.
SRC	R/W	0 PLL enabled	FemtoClock NG PLL Bypass 0 = FemtoClock NG PLL is enabled. 1 = FemtoClock NG PLL is disabled and bypassed. The VCXO-PLL output signal is frequency divided by the channel dividers.
VCO_SEL	R/W	0 Value = f_{VCO}=2500 MHz	VCO Select 0 = Selects VCO at f_{VCO} = 2400–2500MHz. 1 = Do not use.
POLV	R/W	0 Value = Positive Polarity	VCXO Polarity 0 = Positive polarity. Use for an external VCXO with a positive f(V_C) characteristics. 1 = Negative polarity. Use for an external VCXO with a negative f(V_C) characteristics.
FVCV	R/W	1 Value: Value: LFV = V_{DD_V}/2	VCXO-PLL Force VC Control Voltage 0 = Normal operation. 1 = Forces the voltage at the LFV control pin (VCXO input) to V_{DD_V}/2. VCXO-PLL unlocks and the VCXO is forced to its mid-point frequency. FVCV = 1 is the default setting at startup to center the VCXO frequency. FVCV should be cleared after startup to enable the PLL to lock to the reference frequency.

Table 26. PLL Control Register Descriptions (Cont.)

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
CPV[4:0]	R/W	0 1111 Value: 0.8mA	VCXO-PLL Charge-Pump Current Controls the charge pump current I_{CPV} of the VCXO-PLL. Charge pump current is the binary value of this register plus one multiplied by 50µA. I_{CPV} = 50µA × (CPV[4:0] + 1). CPV[4:0] = 00000 sets ICPV to the minimum current of 50µA. Maximum charge pump current is 1.6mA. Default setting is 0.8mA: ((15 + 1) × 50µA).
OSVEN	R/W	0	VCXO-PLL Offset Enable 0 = No offset. 1 = Offset enabled. A static phase offset of OFFSET[4:0] is applied to the PFD of the VCXO-PLL.
OFFSETV[4:0]	R/W	0 0000 Value: 0°	VCXO-PLL Static Phase Offset Controls the static phase detector offset of the VCXO-PLL. Phase offset is the binary value of this register multiplied by 0.9° of the PFD input signal (OFFSET [4:0] × f_{PFD} ÷ 400). Maximum offset is 31 × 0.9° = 27.9°. Setting OFFSET to 0.0° eliminates the thermal noise of an offset current. If the VCXO-PLL input jitter period T_{JIT} exceeds the average input period, set OFFSET to a value larger than f_{PFD} × T_{JIT} × 400 to achieve a better charge pump linearity and lower in-band noise of the PLL.
CPF[4:0]	R/W	0 0110 Value: 1.4mA	FemtoClock NG-PLL Charge-Pump Current Controls the charge pump current I_{CPF} of the FemtoClock NG PLL. Charge pump current is the binary value of this register plus one multiplied by 200µA. I_{CPF} = 200µA × (CPF[4:0] + 1). CPV[4:0] = 00000 sets I_{CPF} to the minimum current of 200µA. The maximum charge pump current is 6.4mA. Default setting is 1.4mA: ((6+1) × 200µA).

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Input Selection Mode Registers

Table 27. Input Selection Mode Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x20	N_MON[4:0]					IN_BLOCK	nHO_EN	nEXT_INT
0x21	Reserved	Reserved	Reserved	REVS	nM/A[1:0]		Reserved	INT_SEL
0x22	CNTH[7:0]							
0x23	CNTR[1:0]		Reserved	Reserved	Reserved	Reserved	CNTV[1:0]	

Table 28. Input Selection Mode Register Descriptions

Register Description							
Bit Field Name	Field Type	Default (Binary)	Description				
N_MON[4:0]	R/W	00000 Value: ÷1	Clock frequency divider for the input activity monitor The clock activity monitor compares the device input frequency (f_{IN}) to the frequency of the VCXO divided by N_MON. For optimal operation of the activity monitor, the frequency f_{VCXO} ÷ N_MON should match the input frequency. For example, for f_{IN}=61.44MHz and f_{VCXO}=61.44MHz, set N_MON=÷1; for f_{IN}=25MHz and f_{VCXO}=125MHz, set N_MON = ÷5.				
			0XX 00 = ÷1	100 00 = ÷2	101 00 = ÷3	110 00 = ÷4	111 00 = ÷5
			0XX 01 = ÷2	100 01 = ÷4	101 01 = ÷6	110 01 = ÷8	111 01 = ÷10
			0XX 10 = ÷4	100 10 = ÷8	101 10 = ÷12	110 10 = ÷16	111 10 = ÷20
			0XX 11 = ÷8	100 11 = ÷16	101 11 = ÷24	110 11 = ÷32	111 11 = ÷40
IN_BLOCK	R/W	0 Value: Not blocked	Inactive input clock block 0 = Both input clock signals CLK0 and CLK1 are routed to the input clock multiplexer. 1 = The input clock that is currently not active is gated off (blocked).				
nHO_EN	R/W	0 Value: Enter Holdover	Manual Holdover Control 0 = Enter holdover on a manual input reference switch. Using the EXT_SEL control pin or the INT_SEL control bit, as defined by nEXT_INT for manual reference switching. nMA[1:0] has no meaning. 1 = The device switching and holdover modes are controlled by nMA[1:0].				
nEXT_INT	R/W	0 Value: External selection	Input clock selection 0 = The EXT_SEL pin (B3) controls the input clock selection. 1 = The INT_SEL bit (register 0x21, D0) controls the input clock selection.				

Table 28. Input Selection Mode Register Descriptions (Cont.)

<table>
<tr><th colspan="4">Register Description</th></tr>
<tr><th>Bit Field Name</th><th>Field Type</th><th>Default (Binary)</th><th>Description</th></tr>
<tr><td>REVS</td><td>R/W</td><td>0

Value: off</td><td>Revertive Switching
The revertive input switching setting is only applicable to the two automatic selection modes shown in Table 12. If nM/A[1:0] = X0, the REVS setting has no meaning.
0 = Disabled: Re-validation of the non-selected input clock has no impact on the clock selection.
1 = Enabled: Re-validation of the non-selected input clock will cause a new input selection according to the pre-set input priorities (revertive switch).
The default setting is revertive switching turned off.</td></tr>
<tr><td>nM/A[1:0]</td><td>R/W</td><td>00

Value: Manual Selection</td><td>Reference Input Selection Mode
In any of the manual selection modes (nM/A[1:0] = 00 or 10), the VCXO-PLL reference input is selected by INT_SEL. In any of the automatic selection modes, the VCXO-PLL reference input is selected by an internal state machine according to the input LOS states and the priorities in the input priority registers.
00 = Manual selection (no holdover).
01 = Automatic selection (no holdover).
10 = Short-term holdover.
11 = Automatic selection with holdover.</td></tr>
<tr><td>INT_SEL</td><td>R/W</td><td>0

Value: CLK0 selected / primary clock</td><td>VCXO-PLL Input Reference Selection
When in internal selection mode (nEXT_INT = 1), INT_SEL controls the VCXO-PLL reference input for manual selection modes (nHO_EN = 1, nM/A[1:0] = X0, or VCXO-PLL primary clock for automatic selection modes (nM/A[1:0] = X1).
<table>
<tr><th>INT_SEL</th><th>Internal and Manual Clock Selection Modes</th><th>Automatic Modes</th></tr>
<tr><td>0</td><td>CLK_0 is reference input</td><td>CLK_0 is primary clock</td></tr>
<tr><td>1</td><td>CLK_1 is reference input</td><td>CLK_1 is primary clock</td></tr>
</table>
In external selection modes, INT_SEL has no meaning.</td></tr>
<tr><td>CNTH[7:0]</td><td>R/W</td><td>1000 0000 Value: 134ms)</td><td>Short-term holdover: Hold-off counter period.
The device initiates a clock failover switch upon counter expiration (zero transition). The counters start to count backward after an LOS event is detected. The hold-off counter period is determined by the binary number of VCXO-PLL output pulses divided by CNTR[1:0]. With a VCXO frequency of 125MHz and CNTR[1:0] = 10, the counter has a period of (1.048ms × binary setting). After each zero-transition, the counter automatically re-loads to the setting in this register. The default setting is 134ms (VCXO = 125MHz: 1/125MHz × 2^{17} × 128).</td></tr>
</table>

Table 28. Input Selection Mode Register Descriptions (Cont.)

<table>
<tr><th colspan="5">Register Description</th></tr>
<tr><th>Bit Field Name</th><th>Field Type</th><th>Default (Binary)</th><th colspan="2">Description</th></tr>
<tr><td rowspan="5">CNTR[1:0]</td><td rowspan="5">R/W</td><td rowspan="5">10

Value: 2^{17}</td><td colspan="2">Short-term holdover reference divider</td></tr>
<tr><td rowspan="2">CNTR[1:0]</td><td colspan="2">CNTH frequency (period; range)</td></tr>
<tr><td>125MHz VCXO</td><td>156.25MHz VCXO</td></tr>
<tr><td>00 = $f_{VCXO} \div 2^{15}$</td><td>3814Hz (0.262ms; 0–66.8ms)</td><td>4768Hz (0.209ms; 0–53.4ms)</td></tr>
<tr><td>01 = $f_{VCXO} \div 2^{16}$</td><td>1907Hz (0.524ms; 0–133ms)</td><td>2384Hz (0.419ms; 0–106.9ms)</td></tr>
<tr><td>10 = $f_{VCXO} \div 2^{17}$</td><td>953Hz (1.048ms; 0–267ms)</td><td>1192Hz (0.838ms; 0–213.9ms)</td></tr>
<tr><td>CNTV[1:0]</td><td>R/W</td><td>10

Value: 32)</td><td colspan="2">Revalidation Counter
Controls the number of required consecutive, valid input reference pulses for clock re-validation on CLK_n in number of input periods. At an LOS event, the re-validation counter loads this setting from the register and counts down by one with every valid, consecutive input signal period. Missing input edges (for one input period) will cause this counter to re-load its setting. An input is re-validated when the counter transitions to zero and the corresponding LOS flag is reset.
00 = 2 (shortest possible)
01 = 16
10 = 32
11 = 64</td></tr>
</table>

Channel Registers

The content of the channel registers sets the channel state, the clock divider the clock phase delay, and the power-down state.

Table 29. Channel Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x24: Channel A 0x2C: Channel B 0x34: Channel C 0x3C: Channel D	N_*A*[7:0] N_*B*[7:0] N_*C*[7:0] N_*D*[7:0]							
0x25: Channel A 0x2D: Channel B 0x35: Channel C 0x3D: Channel D	ΦCLK_*A*[7:0] ΦCLK_*B*[7:0] ΦCLK_*C*[7:0] ΦCLK_*D*[7:0]							
0x26: Channel A 0x2E: Channel B 0x36: Channel C 0x3E: Channel D	PD_*A* PD_*B* PD_*C* PD_*D*	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x44: Channel E 0x45: Channel E 0x46: Channel E	N_*E*_FRAC[7:0] N_*E*_FRAC[15:8] N_*E*_FRAC[23:16]							
0x47: Channel E	Reserved	Reserved	Reserved	Reserved	N_*E*_INT[3:0]			
0x58	Reserved	Reserved	EN_QCLK_V	EN_QCLK_A	EN_QCLK_B	EN_QCLK_C	EN_QCLK_D	EN_QCLK_E

Table 30. Channel Register Descriptions[a]

Register Description				
Bit Field Name	Field Type	Default (Binary)	Description	
N_*x*[7:0]	R/W	N_*A*, N_*B*: 0000 0001 Value= ÷3 N_*C*, N_*D*: 0000 0100 Value= ÷6	Output Frequency Divider N N_*x*[7:0]Divider Value	
			1000 0000 0000 0000 0000 0001 0000 0010 0000 0011 0000 0100 0000 0110	÷1 ÷2 ÷3 ÷4 ÷5 ÷6 ÷8
			0100 0011 0100 0100 0100 0110	÷10 ÷12 ÷16
			0100 1011 0100 1100	÷20 ÷24
			0101 0011 0100 1110 0101 0100	÷30 ÷32 ÷36
			0101 1011 0101 0110	÷40 ÷48
			0110 0011	÷50
			0110 0100 0101 1110	÷60 ÷64
			0101 1111	÷72
			0110 0110	÷80
			0110 1110	÷96
			0111 1011	÷100
			0111 1100 0111 0110	÷120 ÷128
			0111 1110	÷160

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Table 30. Channel Register Descriptions[a] (Cont.)

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
N_*E*_FRAC[23:0]	R/W	0110 1111 111 0 1011 0100 1 010 Value: 7,334,730	Fractional output divider, fractional part Together with N_E_INT, forms the fractional output divider N*E* value. $N_E = 2 \times \left(N_{INT} + \frac{N_{FRAC}}{2^{24}} \right)$ The default value is N*E* = 2 × (9 + 0.4371839761732) = 18.8743679523. Greatest N*E* fractional divider is 2 × (14 + [2^{24} - 1] / 2^{24}) ≈ 29.99999988
N_*E*_INT[3:0]	R/W	1001 Value: 9	Fractional output divider, integer part See N_*E*_FRAC[23:0] Greatest N*E* fractional divider is 2 × (14 + [2^{24} - 1] / 2^{24}) ≈ 29.99999988
ΦCLK_*x*[7:0] f_{VCO}=2500MHz	R/W	0000 0000	CLK_*x* phase delay ΦCLK_*x*[7:0] f_{VCO}=2500MHz: Delay in ps = ΦCLK_*x* × 400ps (256 steps) ΦCLK_*x*[7:0] Delay (f_{VCO} = 2500MHz) 0000 0000 — 0ps 0000 0001 — 400ps … — … 1111 1111 — 102ns
PD_*x*	R/W	0 Value: power up	0 = Channel *x* is powered up 1 = Channel *x* is powered down
EN_*x*	R/W	0 Value: disabled	QCLK_*x* channel output enable 0 = All outputs of channel *x* are disabled at the logic low state 1 = All outputs of channel *x* are enabled
EN_QCLK_*V*	R/W	0 Value: disabled	QCLK_*V* output enable 0 = QCLK_*V* is disabled at the logic low state 1 = QCLK_*V* is enabled

[a] *x* = A, B, C, D.

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Output Registers

The content of the output registers set the power-down state, the output style and amplitude.

Table 31. Output Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x28: QCLK_A0 0x29: QCLK_A1 0x2A: QCLK_A2	PD_*A0* PD_*A1* PD_*A2*	Reserved	Reserved	STYLE_*A0* STYLE_*A1* STYLE_*A2*	A_*A0*[1:0] A_*A1*[1:0] A_*A2*[1:0]		Reserved	Reserved
0x30: QCLK_B0 0x31: QCLK_B1 0x32: QCLK_B2	PD_*B0* PD_*B1* PD_*B2*	Reserved	Reserved	STYLE_*B0* STYLE_*B1* STYLE_*B2*	A_*B0*[1:0] A_*B1*[1:0] A_*B2*[1:0]		Reserved	Reserved
0x38: QCLK_C0 0x39: QCLK_C1	PD_*C0* PD_*C1*	Reserved	Reserved	STYLE_*C0* STYLE_*C1*	A_*C0*[1:0] A_*C1*[1:0]		Reserved	Reserved
0x40: QCLK_D0 0x41: QCLK_D1	PD_*D0* PD_*D1*	Reserved	Reserved	STYLE_*D0* STYLE_*D1*	A_*D*0[1:0] A_*D*1[1:0]		Reserved	Reserved
0x48: QCLK_E	nPD_*E*	Reserved	Reserved	STYLE_*E*	A_*E*[1:0]		Reserved	Reserved
0x4B: QCLK_V	PD_*V*	Reserved	STYLE_*V*[1:0]		A_*V*[1:0]		Reserved	Reserved

Table 32. Output Register Descriptions[a]

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
PD_*y*	R/W	0 Value: power up	0 = Output QCLK_*y* is powered up 1 = Output QCLK_*y* is powered down
PD_*V*	R/W	0: Value: power up	0 = Output QCLK_*V* is powered up 1 = Output QCLK_*V* is powered down
nPD_*E*	R/W	0 Value: Power down	0 = Output QCLK_*E* and channel *E* including the fractional divider N_*E* are powered down 1 = Output QCLK_*E* is powered up

Table 32. Output Register Descriptions[a] (Cont.)

Register Description				
Bit Field Name	Field Type	Default (Binary)	Description	
A_*y*[1:0] A_E[1:0]	R/W	01 Value: 500mV	QCLK_*y*, QCLK_E, QCLK_V Output amplitude	
			Setting for STYLE = 0 (LVDS)	Setting for STYLE = 1 (LVPECL)
A_*V*[1:0]	R/W	00 Value: 350mV	A[1:0] = 00: 350mV A[1:0] = 01: 500mV A[1:0] = 10: 700mV A[1:0] = 11: 850mV Termination: 100Ω across	A[1:0] = 00: 350mV A[1:0] = 01: 500mV A[1:0] = 10: 700mV A[1:0] = 11: 850mV Termination: 50Ω to V_{TT}[b]
STYLE_*y* STYLE_*E*	R/W	0 Value: LVDS	QCLK_*y*, QCLK_*E* Output format 0 = Output is LVDS (Requires LVDS 100Ω output termination) 1 = Output is LVPECL (Requires LVPECL 50Ω output termination to the specified recommended termination voltage).	
STYLE_*V*[1:0]	R/W	10 Value: LVCMOS	QCLK_*V* Output format 00 = Output is LVDS (Requires LVDS 100Ω output termination) 01 = Output is LVPECL (Requires LVPECL 50Ω termination to V_{TT}[b]) 1x = Both QCLK_*V* and nQCLK_*V* are single-ended LVCMOS 1.8V outputs. QCLK_V and nQCLK_V are complementary (180° phase difference).	

[a] *y* = A0, A1, A2, B0, B1, B2, C0, C1, D0, D1.

[b] See Table 49 for V_{TT} (Termination voltage) values.

Status Registers

Table 33. Status Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x4C	Reserved	Reserved	IE_LOLF	IE_LOLV	IE_REF	IE_HOLD	IE_CLK_1	IE_CLK_0
0x50	Reserved	Reserved	nLS_LOLF	nLS_LOLV	LS_REF	nLS_HOLD	LS_CLK_1	LS_CLK_0
0x51	Reserved	ST_SEL	nST_LOLF	nST_LOLV	ST_REF	nST_HOLD	ST_CLK_1	ST_CLK_0
0x53	Reserved	Reserved	Reserved	Reserved	Reserved	ST_VCOF	Reserved	Reserved

Table 34. Status Register Descriptions[a]

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
IE_LOLF	R/W	0	Interrupt Enable for FemtoClock NG-PLL loss of lock 0 = Disabled: Setting nLS_LOLF will not cause an interrupt on nINT 1 = Enabled: Setting nLS_LOLF will assert the nINT output (nINT=0, interrupt)
IE_LOLV	R/W	0	Interrupt Enable for VCXO-PLL loss of lock 0 = Disabled: Setting nLS_LOLV will not cause an interrupt on nINT 1 = Enabled: Setting nLS_LOLV will assert the nINT output (nINT=0, interrupt)
IE_CLK_*n*	R/W	0	Interrupt Enable for CLK*n* input loss-of-signal. 0 = Disabled: Setting LS_CLK_*n* will not cause an interrupt on nINT 1 = Enabled: Setting LS_CLK_*n* will assert the nINT output (nINT=0, interrupt)
IE_REF	R/W	0	Interrupt Enable for Input Reference Loss. 0 = Disabled: Setting LS_REF will not cause an interrupt on nINT 1 = Enabled: Setting LS_REF will assert the nINT output (nINT=0, interrupt)
IE_HOLD	R/W	0	Interrupt Enable for holdover 0 = Disabled: Setting nLS_HOLD will not cause an interrupt on nINT 1 = Enabled: Setting nLS_HOLD will assert the nINT output (nINT=0, interrupt)
nLS_LOLF	R/W	-	FemtoClock NG-PLL loss of lock (latched status of nST_LOLF) Read 0 = ≥1 loss-of-lock events detected since the last nLS_LOLV clear Read 1 = No loss-of-lock detected since the last nLS_LOLV clear Write 1 = Clear status latch (clears pending nLS_LOLF interrupt)
nLS_LOLV	R/W	-	VCXO-PLL loss of lock (latched status of nST_LOLV) Read 0 = ≥1 loss-of-lock events detected since the last nLS_LOLV clear. Read 1 = No loss-of-lock detected since the last nLS_LOLV clear Write 1 = Clear status latch (clears pending nLS_LOLV interrupt)

Table 34. Status Register Descriptions[a] (Cont.)

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
LS_CLK_*n*	R/W	-	Input CLK_*n* status (latched status of ST_CLK_*n*). Read 0 = ≥1 LOS events detected on CLK_*n* since the last LS_CLK_*n* clear Read 1 = No loss-of-signal detected on CLK_*n* since the last LS_CLK_*n* clear Write 1 = Clear LS_CLK_*n* status latch (clears pending LS_CLK_*n* interrupts on nINT)
ST_SEL	R	-	Input selection (momentary) Reference Input Selection Status of the state machine. In any input selection mode, reflects the input selected by the state machine. 0 = CLK_0 1 = CLK_1
nST_LOLF	R	-	FemtoClock NG-PLL loss of lock (momentary) Read 0 = Loss-of-lock event detected Read 1 = No loss-of-lock detected A latched version of this status bit is available (nLS_LOLF).
nST_LOLV	R	-	VCXO-PLL loss of lock (momentary) Read 0 = Loss-of-lock event detected Read 1 = No loss-of-lock detected A latched version of this status bit is available (nLS_LOLV).
ST_CLK_*n*	R	-	Input CLK_*n* status (momentary). 0 = LOS detected on CLK_*n* 1 = No LOS detected; CLK_*n* input is active A latched version of this status bit is available (LS_CLK_*n*).
LS_REF	R/W	-	PLL reference status (latched status of ST_REF). Read 0 = Reference lost since the last LS_REF clear Read 1 = Reference valid since the last LS_REF clear Write 1 = Clear LS_REF status latch (clears pending LS_REF interrupts on nINT)
nLS_HOLD	R/W		Holdover status indicator (latched status of nST_HOLD) Read 0 = VCXO-PLL has entered holdover state ≥1 times after last nLS_HOLD clear Read 1 = VCXO-PLL is (or attempts to) lock(ed) to an input clock Write 1 = Clear status latch (clears pending nLS_HOLD interrupt)
ST_VCOF	R	-	FemtoClock NG-PLL calibration status (momentary) Read 0 = FemtoClock NG PLL auto-calibration is completed Read 1 = FemtoClock NG PLL calibration is active (not completed)

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Table 34. Status Register Descriptions[a] (Cont.)

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
ST_REF	R	-	Input reference status (momentary). 0 = No input reference present 1 = Input reference is present at the clock selected input clock
nST_HOLD	R	-	Holdover status indicator (momentary) 0 = VCXO-PLL in holdover state, not locked to any input clock 1 = VCXO-PLL is (or attempts to) lock(ed) to input clock A latched version of this status bit is available (nLS_HOLD).

[a] CLK*n* = CLK*0*, CLK*1*

General Control Registers

Table 35. General Control Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x55	INIT_CLK	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x56	RELOCK	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x57	PB_CAL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CPOL

Table 36. General Control Register Descriptions

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
INIT_CLK	W only Auto-Clear	X	1 = Initialize divider functions. Required as part of the startup procedure.
RELOCK	W only Auto-Clear	X	1 = Force the FemtoClock NG PLL to re-lock.
PB_CAL	W only Auto-Clear	X	Precision Bias Calibration Setting this bit to 1 will start the calibration of an internal precision bias current source. The bias current is used as a reference for outputs configured as LVDS, and as a reference for the charge pump currents. This bit will auto-clear after the calibration is completed. Set as part of the startup procedure.
CPOL	R/W	0	SPI Read Operation SCLK Polarity 0 = Data bits on SDIO/SDO are output at the falling edge of SCLK edge 1 = Data bits on SDIO/SDO are output at the rising edge of SCLK edge

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Electrical Characteristics

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the 8V19N474. Functional operation of the device at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 37. Absolute Maximum Ratings

Item	Rating
Supply voltage, V_{DD_V} and V_{DDO_V}	3.6V
Inputs	-0.5V to V_{DD_V} + 0.5V
Outputs, V_O (LVCMOS)	-0.5V to V_{DDO_V} + 0.5V
Outputs, I_O (LVPECL) Continuous current Surge current	 50mA 100mA
Outputs, I_O (LVDS) Continuous current Surge current	 50mA 100mA
Operating junction temperature, T_J	125°C
Storage temperature, T_{STG}	-65°C to 150°C
ESD - Human Body Model[a]	2000V
ESD - Charged Device Model[a]	500V

[a] According to JEDEC JS-001-2012/JESD22-C101

Pin Characteristics

Table 38. Pin Characteristics, V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}[a]	Input capacitance	OSC, nOSC		2	4	pF
		other inputs		2	4	pF
R_{PU}	Input pull-up resistor	nCLK_0, nCLK_1		51		kΩ
R_{PD}	Input pull-down resistor	CLK_0, nCLK_0, CLK_1, nCLK_1, EXT_SEL, ADR1/MISO, nI2C/SPI		51		kΩ
R_{OUT}	LVCMOS output impedance	nINT, LOCK		25		Ω

[a] Guaranteed by design

DC Characteristics

Table 39. Power Supply DC Characteristics, V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C[a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD_V}	Core supply voltage		3.135	3.3	3.465	V
V_{DDO_V}	Output supply voltage		1.71	1.8, 2.5, 3.3	3.465	V
I_{DD_V}	Power supply current			580	797	mA

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

Table 40. Typical Power Supply DC Current Characteristics, V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C[a]

Symbol	Supply Pin Current		Test Case 1[b]	2[b]	3[c]	4[c]	5[c]	6[c]	Units
	QCLK_A[2:0], QCLK_B[2:0]	VDDO_QCLKA, B	3.3	3.3	3.3	3.3	1.8	1.8	V
		Style	LVDS	LVDS	LVPECL	LVPECL	LVPECL	LVPECL	
		State	On	On	On	On	On	On	
		Amplitude	700	850	850	700	500	350	mV
	QCLK_C[1:0], QCLK_D[1:0]	VDDO_QCLKC, D	3.3	3.3	3.3	3.3	1.8	1.8	V
		Style	LVDS	LVDS	LVPECL	LVPECL	LVDS	LVDS	
		State	On	On	On	On	On	On	
		Amplitude	700	850	850	700	500	350	mV
	QCLK_E	VDD_QCLKE	3.3	3.3	3.3	3.3	3.3	3.3	V
		Style	LVDS	LVDS	LVPECL	LVPECL	LVDS	LVDS	
		State	Off	Off	On	On	On	On	
		Amplitude	—	—	850	700	500	350	mV
I_{DD_COA}	Current through VDDO_QCLKA pin		62	77	65	59	52	46	mA
I_{DD_CA}	Current through VDD_QCLKA pin		30	30	29	29	29	29	mA
I_{DD_COB}	Current through VDDO_QCLKB pin		62	77	70	64	55	49	mA
I_{DD_CB}	Current through VDD_QCLKB pin		25	25	29	29	29	29	mA
I_{DD_COC}	Current through VDDO_QCLKC pin		41	51	52	48	33	23	mA
I_{DD_CC}	Current through VDD_QCLKC pin		29	29	28	28	28	28	mA
I_{DD_COD}	Current through VDDO_QCLKD pin		42	52	53	48	33	23	mA
I_{DD_CD}	Current through VDD_QCLKD pin		26	26	28	28	28	28	mA
I_{DD_CE}	Current through VDD_QCLKE pin		2	2	54	51	45	40	mA
I_{DD_SPI}	Current through VDD_SPI pin		9	9	8	8	7	7	mA
I_{DD_INP}	Current through VDD_INP pin		15	15	15	15	14	14	mA

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Table 40. Typical Power Supply DC Current Characteristics, V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C[a] (Cont.)

Symbol	Supply Pin Current	Test Case						Units
		1[b]	2[b]	3[c]	4[c]	5[c]	6[c]	
I_{DD_LCV}	Current through VDD_LCV pin	70	70	69	69	68	68	mA
I_{DD_LCF}	Current through VDD_LCF pin	63	63	62	62	62	62	mA
I_{DD_CPV}	Current through VDD_CPV pin	12	12	12	12	12	12	mA
I_{DD_CPF}	Current through VDD_CPF pin	52	52	50	50	48	48	mA
I_{DD_OSC}	Current through VDD_OSC pin	32	37	36	34	35	34	mA
I_{DD_TOT}	Total Device Current Consumption	572	627	660	634	578	540	mA
P_{TOT}	Total Device Power Consumption	1.88	2.06	1.83	1.76	1.66	1.64	mW
$P_{TOT, SYS}$	Total System Power Consumption[d]	1.89	2.07	2.18	2.09	1.91	1.78	mW

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] f_{CLK} (input) = 10MHz, f_{VCXO} = 40MHz, f_{VCO} = 2400MHz, PV=80, MV=320, MF=30, FDF=1. Supply current is independent of the output frequency configuration used for this table: QA[2:0]=40MHz, QB[1:0]=480MHz, QC[1:0]=30MHz, QD=480MHz, QE = not used. QCLK_y outputs terminated according to amplitude settings: LVPECL outputs terminated to V_{TT}.

[c] f_{CLK} (input) = 125MHz, f_{VCXO} = 125MHz, f_{VCO} = 2500MHz, PV=1024, MV=1024, MF=10, FDF=1. Supply current is independent of the output frequency configuration used for this table: QA[2:0]=QB[1:0]=QC[1:0]=QD=156.25MHz, QE = 100MHz. QCLK_y outputs terminated according to amplitude settings: LVPECL outputs terminated to V_{TT}.

[d] Includes total device power consumption and the power dissipated in external output termination components.

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Table 41. LVCMOS DC Characteristics, V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C[a]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
Control inputs SCL/SCLK, SDA/MOSI, ADR1/MISO, nI2C/SPI and ADR0/nCS and EXT_SEL (1.8V/JESD7A-8 logic, input hysteresis and 3.3V tolerance)							
V_I	Input voltage			-0.3		V_{DD_V}	V
V_{T+}	Positive-going input threshold voltage			0.660		1.365	V
V_{T-}	Negative-going input threshold voltage			0.495		1.170	V
V_H	Hysteresis voltage		V_{T+} - V_{T-}	0.165		0.780	V
I_{IH}	Input high current	Inputs with pull-down resistor[b]	V_{DD_V} = 3.3V, V_{IN} = 3.3V			150	µA
		Other inputs[c]				5	
I_{IL}	Input low current	Inputs with pull-down resistor[b]	V_{DD_V} = 3.465V, V_{IN} = 0V	-5			µA
		Other inputs[c]		-150			
Control outputs ADR1/MISO (when output), nINT, LOCK configured to 3.3V (SELSV0 = 0, SELSV1=0)							
V_{OH}	Output high voltage	ADR1/MISO (when output), nINT, LOCK	I_{OH} = -4mA	2.0			V
V_{OL}	Output low voltage		I_{OL} = 4mA			0.55	V
Control outputs ADR1/MISO (when output), nINT, LOCK configured to 1.8V (SELSV0 = 1, SELSV1=1)							
V_{OH}	Output high voltage		I_{OH} = -4mA	1.35		1.8	V
V_{OL}	Output low voltage		I_{OL} = 4mA			0.45	V
Clock outputs QCLK_V, nQCLK_V configured to LVCMOS (STYLE_V[1:0] = 1x)							
V_{OH}	Output high voltage		I_{OH} = -8mA	1.35		1.8	V
V_{OL}	Output low voltage		I_{OL} = 8mA			0.45	V

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] nI2C/SPI, ADR1/MISO, EXT_SEL

[c] ADR0/nCS, SCL/SCLK, SDA/MOSI

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Table 42. Differential Input DC Characteristics, V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C[a]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input high current	Pull-down inputs[b]	V_{DD_V} = V_{IN} = 3.465V			150	µA
		Pull-down/pull-up inputs[c]				150	µA
I_{IL}	Input low current	Pull-down inputs[b]	V_{DD_V} = 3.465V, V_{IN} = 0V	-150			µA
		Pull-down/pull-up inputs[c]		-150			µA

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] Non-Inverting inputs: CLK_0, CLK_1, OSC

[c] Inverting inputs: nCLK_0, nCLK_1, nOSC

Table 43. LVPECL DC Characteristics (QCLK_y, STYLE=1), V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C[a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output high voltage[b] [c]	350mV amplitude setting	V_{DDO_V} - 1.034	V_{DDO_V} - 0.892	V_{DDO_V} - 0.750	V
		500mV amplitude setting	V_{DDO_V} - 1.057	V_{DDO_V} - 0.912	V_{DDO_V} - 0.768	V
		700mV amplitude setting	V_{DDO_V} - 1.092	V_{DDO_V} - 0.950	V_{DDO_V} - 0.808	V
		850mV amplitude setting	V_{DDO_V} - 1.087	V_{DDO_V} - 0.960	V_{DDO_V} - 0.833	V
V_{OL}	Output low voltage[b c]	350mV amplitude setting	V_{DDO_V} - 1.413	V_{DDO_V} - 1.265	V_{DDO_V} - 1.117	V
		500mV amplitude setting	V_{DDO_V} - 1.574	V_{DDO_V} - 1.420	V_{DDO_V} - 1.266	V
		700mV amplitude setting	V_{DDO_V} - 1.782	V_{DDO_V} - 1.633	V_{DDO_V} - 1.485	V
		850mV amplitude setting	V_{DDO_V} - 1.918	V_{DDO_V} - 1.778	V_{DDO_V} - 1.638	V

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] Outputs terminated with 50Ω to V_{TT}. See Table 49 for termination voltage V_{TT} values.

[c] 700mV and 850mV amplitude settings are only available at V_{DDO_V} ≥ 2.5V.

Table 44. LVDS DC Characteristics (QCLK_y, STYLE=0), V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C[a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OS}	Offset voltage[b] [c]	350mV amplitude setting	V_{DDO_V} - 1.034	V_{DDO_V} - 0.947	V_{DDO_V} - 0.862	V
		500mV amplitude setting	V_{DDO_V} - 1.133	V_{DDO_V} - 1.045	V_{DDO_V} - 0.961	V
		700mV amplitude setting	V_{DDO_V} - 1.229	V_{DDO_V} - 1.142	V_{DDO_V} - 1.056	V
		850mV amplitude setting	V_{DDO_V} - 1.316	V_{DDO_V} - 1.226	V_{DDO_V} - 1.138	V
ΔV_{OS}	V_{OS} magnitude change			25	50	mV

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] V_{OS} changes with V_{DD}

[c] 700mV and 850mV amplitude settings are only available at $V_{DDO\_V} \geq 2.5V$

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AC Characteristics

Table 45. AC Characteristics, V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C[a] [b]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input frequency		CLK_*n*	0.008		250	MHz
f_{VCXO}	VCXO frequency			10	125	250	MHz
$f_{PFD, F}$	Phase-frequency detector frequency		FemtoClock NG			250	MHz
f_{VCO}	VCO frequency range			2400		2500	MHz
f_{OUT}	Output frequency	Integer divider	QCLK_*y*, N=÷1	2400		2500	MHz
			QCLK_*y*, N=÷2	1200		1250	MHz
			QCLK_*y*, N=÷4	600		625	MHz
			QCLK_*y*, N=÷8	300		312.5	MHz
			QCLK_*y*, N=÷10	240		250	MHz
			QCLK_*y*, N=÷16	150		156.25	MHz
			QCLK_*y*, N=÷20	120		125	MHz
		Fractional divider	QCLK_E, NE range: 29.$\overline{99}$ to 8.$\overline{33}$	80		300	MHz
Δf_{OUT}	Output frequency accuracy		Integer output divider NA-D			0	ppb
			Fractional output divider NE, f_{OUT} = 156.25MHz			10	ppb
V_{IN}	Input voltage amplitude[c]	CLK_*n*		0.15		1.2	V
V_{DIFF_IN}	Differential input voltage amplitude[c, d]	CLK_*n*		0.3		2.4	V
V_{CMR}	Common mode input voltage			1.0		V_{DD_V} – (V_{IN} / 2)	V
odc	Output duty cycle		QCLK_*y*	45	50	55	%
t_R / t_F	Output rise/fall time, differential		QCLK_*y* (LVPECL), 20–80%			200	ps
			QCLK_*y* (LVDS), 20–80%			250	ps
	Output rise/fall time LVCMOS		QCLK_V, nINT, LOCK, SDA/MOSI, 20–80%			1.2	ns

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Table 45. AC Characteristics, V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C[a] [b]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{O(PP)}$[e]	LVPECL output voltage swing, peak-to-peak, 156.25MHz	350mV amplitude setting	355	380	406	mV
		500mV amplitude setting	479	515	551	mV
		700mV amplitude setting	649	692	734	mV
		850mV amplitude setting	769	826	884	mV
	LVPECL differential output voltage swing, peak-to-peak, 156.25MHz	350mV amplitude setting	710	760	812	mV
		500mV amplitude setting	958	1030	1102	mV
		700mV amplitude setting	1298	1384	1468	mV
		850mV amplitude setting	1538	1642	1768	mV
V_{OD}[f]	LVDS output voltage swing, peak-to-peak, 156.25MHz	350mV amplitude setting	313	346	378	mV
		500mV amplitude setting	425	479	533	mV
		700mV amplitude setting	595	656	717	mV
		850mV amplitude setting	732	798	864	mV
	LVDS differential output voltage swing, peak-to-peak, 156.25MHz	350mV amplitude setting	626	692	756	mV
		500mV amplitude setting	850	958	1066	mV
		700mV amplitude setting	1190	1312	1434	mV
		850mV amplitude setting	1464	1596	1728	mV
*t*sk(o)	Output skew[g] [h]	QCLK_*y* (same N divider)			70	ps
	All delays set to 0	QCLK_*y* (any N divider, incident rising edge)			70	ps
$t_{D, LOS}$	LOS state detected (measured in input reference periods)	f_{IN} = 125MHz			2	T_{IN}
$t_{D, LOCK}$	PLL lock detect	PLL re-lock time after a short-term holdover scenario. Measured from LOS to both PLLs lock-detect asserted; hold-off timer = TBD, VCXO-PLL bandwidth = 100Hz, initial frequency error <200ppm.			300	ms
$t_{D, RES}$	PLL lock residual time error	Refer to PLL lock detect $t_{D,LOCK}$. Reference point: final value of clock output phase after all phase transitions settled.			20	ns
Δf_{HOLD}	Holdover accuracy	Maximum frequency deviation during a holdover duration of 200ms and after the clock re-validate event			±5	ppm

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] VCXO-PLL bandwidth = 100Hz.

[c] V_{IL} should not be less than -0.3V and V_{IH} should not be greater than VDD_*v*

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[d] Common Mode Input Voltage is defined as the cross-point voltage.

[e] LVPECL outputs terminated with 50Ω to V_{DDO_V} – 1.5V (350mV amplitude setting), V_{DDO_V} – 1.75V (500mV amplitude setting), V_{DDO_V} – 2.0V (700mV amplitude setting), V_{DDO_V} – 2.25V (850mV amplitude setting).

[f] LVDS outputs terminated 100Ω across terminals.

[g] This parameter is defined in accordance with JEDEC standard 65.

[h] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

Clock Phase Noise Characteristics

Table 46. Clock Phase Noise Characteristics (f_{VCXO}=125MHz), V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C[a] [b] [c]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
tjit(Ø)	Clock RMS phase jitter (Random)	156.25MHz	Integration range: 12kHz–20MHz		92	113	fs
		250MHz	Integration range: 12kHz–20MHz		75	85	fs
Φ_N(10)	Clock single-side band phase noise (Integer divider)	500MHz	10Hz offset (determined by VCXO)		-73		dBc/Hz
Φ_N(100)			100Hz offset (determined by VCXO)		-92		dBc/Hz
Φ_N(1k)			1kHz offset from carrier		-116	-110	dBc/Hz
Φ_N(10k)			10kHz offset from carrier		-131	-125	dBc/Hz
Φ_N(100k)			100kHz offset from carrier		-135	-134	dBc/Hz
Φ_N(1M)			1MHz offset from carrier		-146	-142	dBc/Hz
Φ_N(≥10M)			≥10MHz offset from carrier and noise floor		-157	-153	dBc/Hz
Φ_N(10)	Clock single-side band phase noise (Integer divider)	250MHz	10Hz offset (determined by VCXO)		-78		dBc/Hz
Φ_N(100)			100Hz offset (determined by VCXO)		-98		dBc/Hz
Φ_N(1k)			1kHz offset from carrier		-122	-119	dBc/Hz
Φ_N(10k)			10kHz offset from carrier		-137	-133	dBc/Hz
Φ_N(100k)			100kHz offset from carrier		-141	-140	dBc/Hz
Φ_N(1M)			1MHz offset from carrier		-152	-150	dBc/Hz
Φ_N(≥10M)			≥10MHz offset from carrier and noise floor		-160	-155	dBc/Hz
Φ_N(10)	Clock single-side band phase noise (Integer divider)	156.25MHz	10Hz offset (determined by VCXO)		-83		dBc/Hz
Φ_N(100)			100Hz offset (determined by VCXO)		-102		dBc/Hz
Φ_N(1k)			1kHz offset from carrier		-126	-122	dBc/Hz
Φ_N(10k)			10kHz offset from carrier		-140	-136	dBc/Hz
Φ_N(100k)			100kHz offset from carrier		-145	-144	dBc/Hz
Φ_N(1M)			1MHz offset from carrier		-155	-152	dBc/Hz
Φ_N(≥10M)			≥10MHz offset from carrier and noise floor		-161	-157	dBc/Hz

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Table 46. Clock Phase Noise Characteristics (f_{VCXO}=125MHz), V_{DD_V} = 3.3V ±5%, V_{DDO_V} = (3.3V, 2.5V, or 1.8V) ±5%, T_A = -40°C to +85°C[a] [b] [c]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$\Phi_N(10)$	Clock single-side band phase noise (Integer divider)	125MHz	10Hz offset (determined by VCXO)		-84		dBc/Hz
$\Phi_N(100)$			100Hz offset (determined by VCXO)		-104		dBc/Hz
$\Phi_N(1k)$			1kHz offset from carrier		-128	-125	dBc/Hz
$\Phi_N(10k)$			10kHz offset from carrier		-143	-138	dBc/Hz
$\Phi_N(100k)$			100kHz offset from carrier		-147	-146	dBc/Hz
$\Phi_N(1M)$			1MHz offset from carrier		-156	-152	dBc/Hz
$\Phi_N(\geq 10M)$			≥10MHz offset from carrier and noise floor		-161	-155	dBc/Hz

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] Phase noise specifications are applicable for all outputs active, Nx not equal.

[c] VCXO characteristics: Epson VG-4513 at 125MHz and phase noise: -129dBc/Hz at 1kHz, -147dBc/Hz at 10kHz offset, -151dBc/Hz at 100kHz offset

Conditions for Phase Noise Characteristics

VCXO characteristics: Epson VG-4513 at f = 125MHz and phase noise: -129dBc/Hz at 1kHz, -147dBc/Hz at 10kHz offset, -151dBc/Hz at 100kHz offset.

- Input reference frequency: 125MHz
- VCXO-PLL bandwidth: 25Hz
- VCXO-PLL charge pump current: 0.45mA
- FemtoClock-NG PLL bandwidth: 182kHz
- V_{DD_V} = V_{DD_V} = 3.3V, T_A = 25°C

Figure 9. 500MHz Output Phase Noise

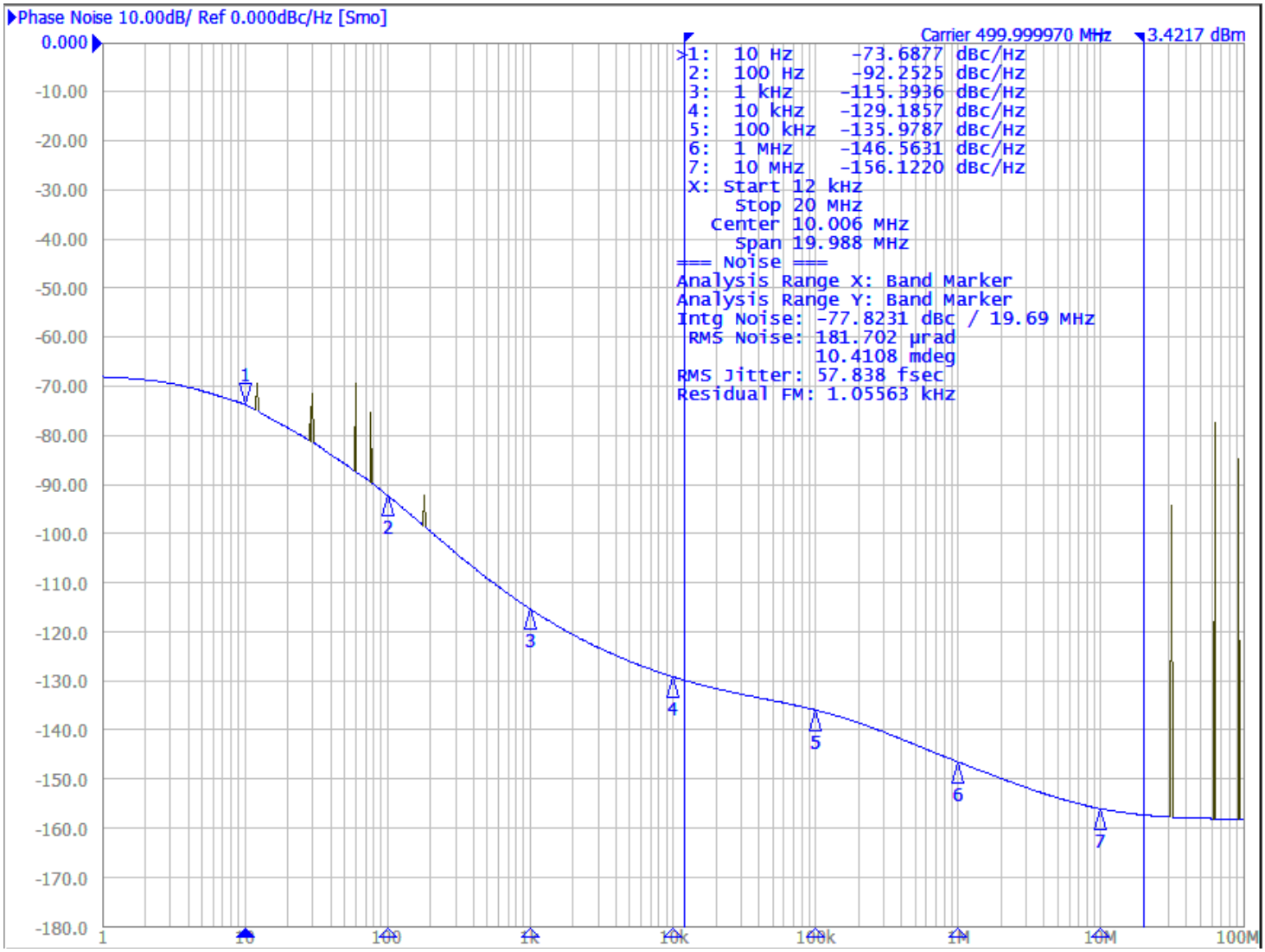


Figure 10. 312.5MHz Output Phase Noise

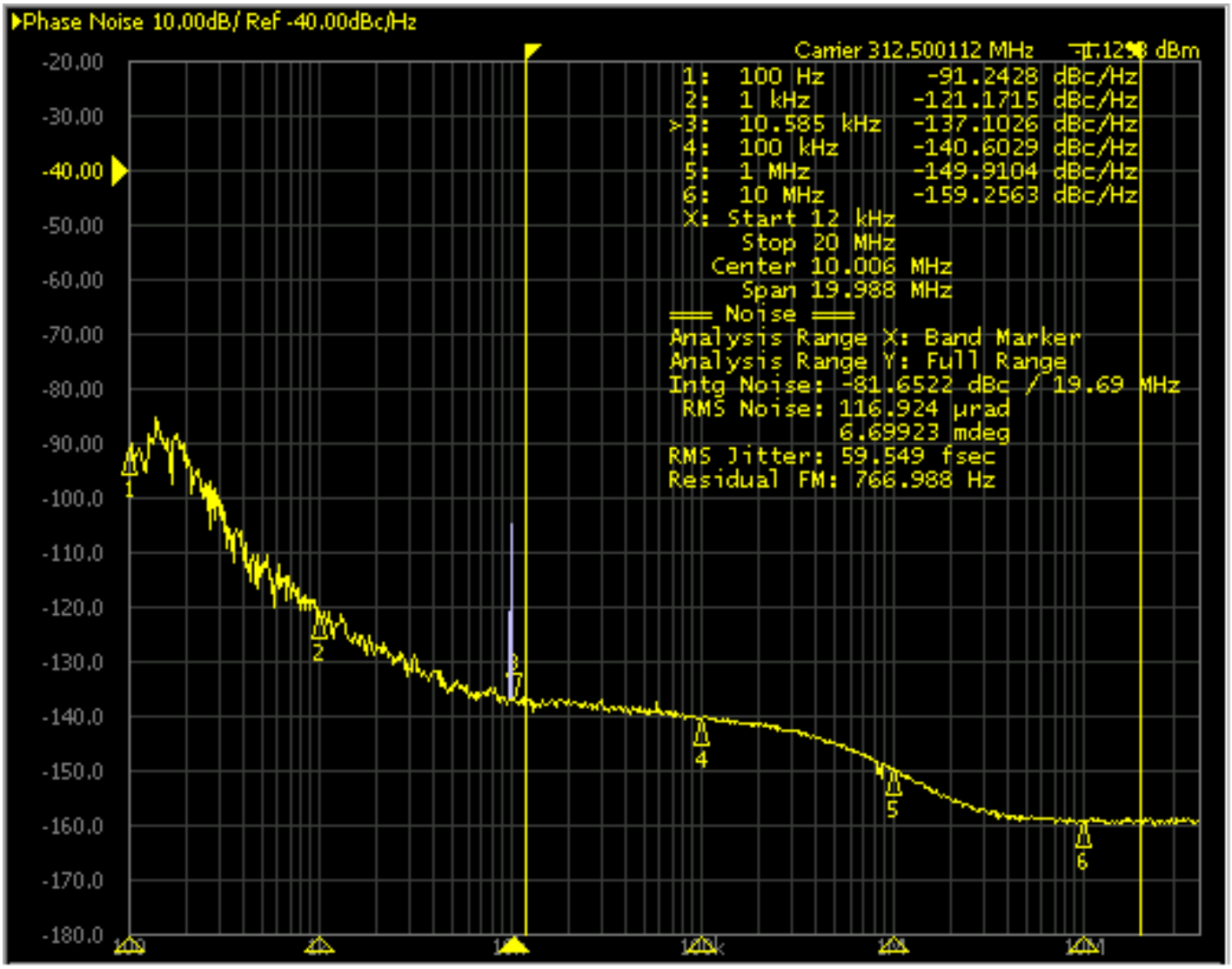


Figure 11. 250MHz Output Phase Noise

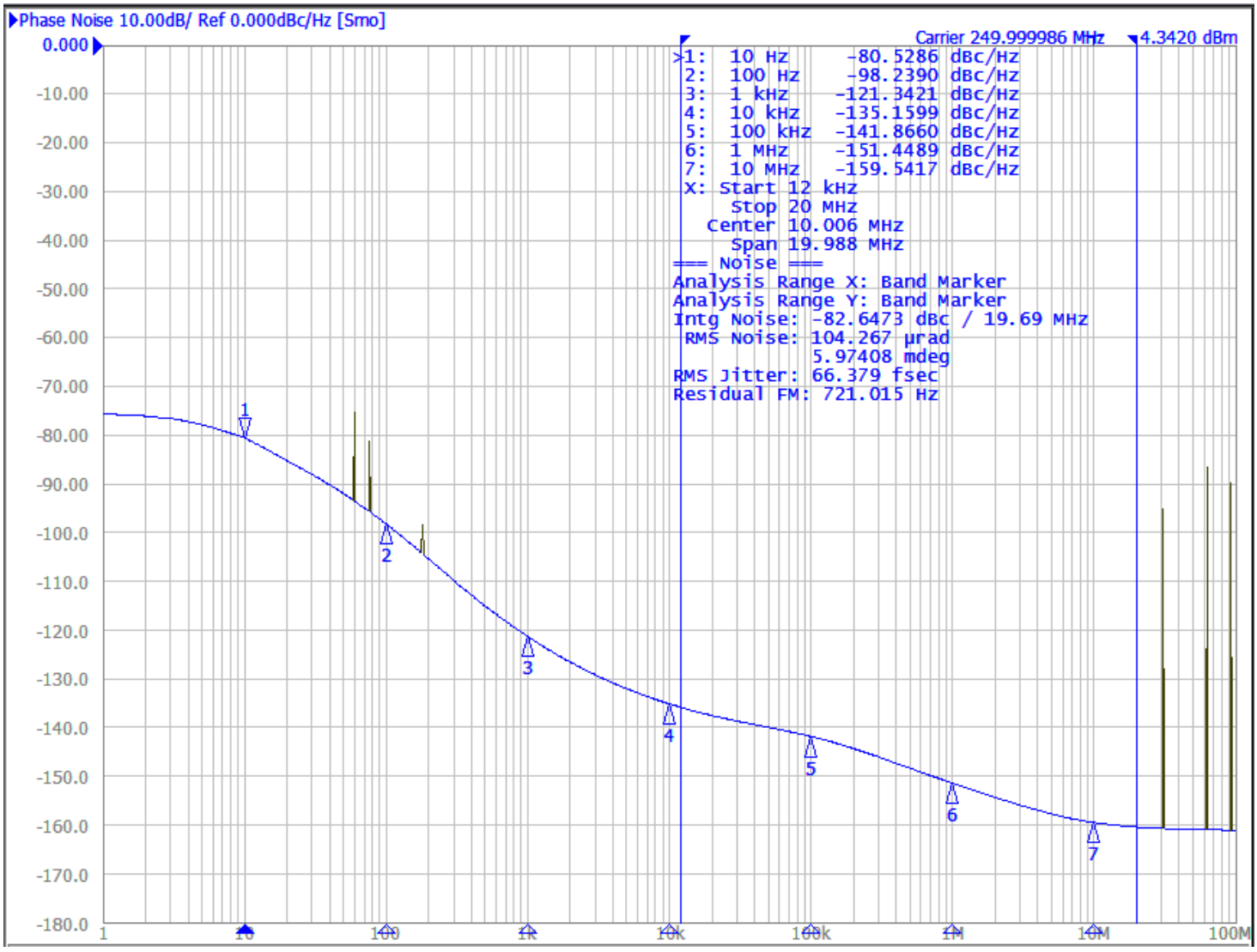


Figure 12. 156.25MHz Output Phase Noise

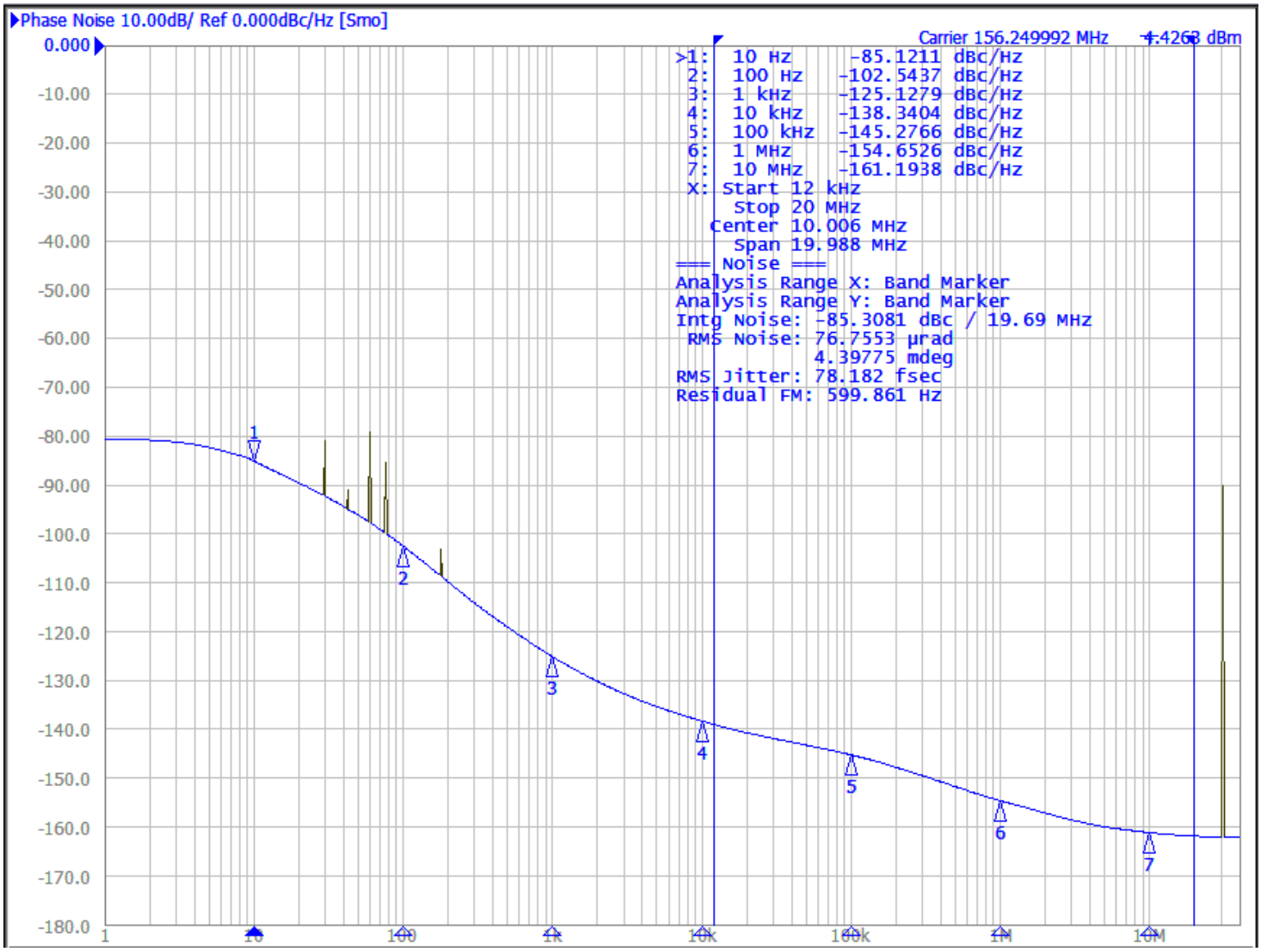
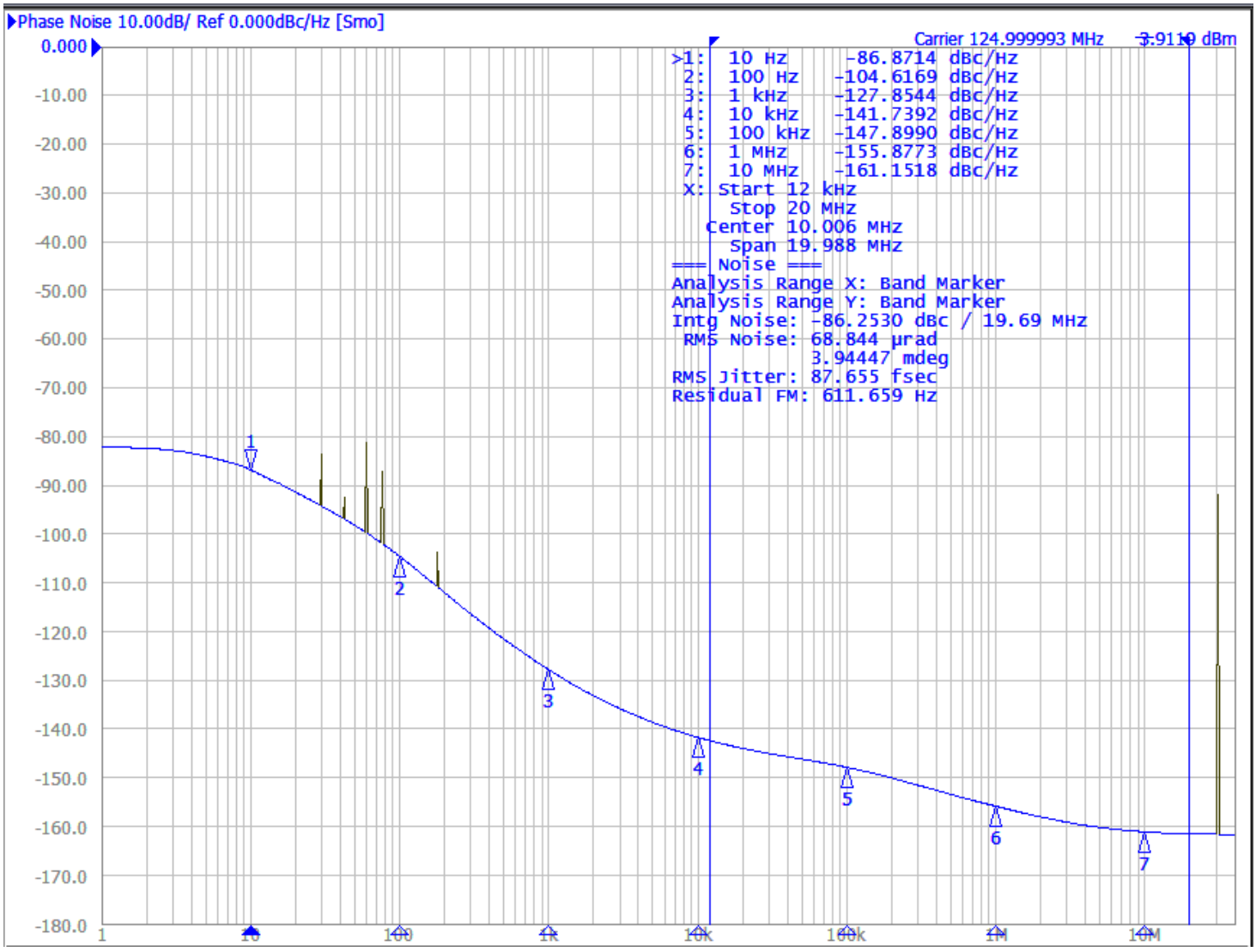


Figure 13. 125MHz Output Phase Noise



Thermal Characteristics

Table 47. Thermal Resistance for 81-FPBGA Package[a]

Multi-Layer PCB, JEDEC Standard Test Board				
Symbol	Thermal Parameter	Condition	Value	Unit
Θ_{JA}	Junction to ambient	0 m/s air flow	45.1	°C/W
		2 m/s air flow	39.1	°C/W
Θ_{JC}	Junction to case		17.8	°C/W
Θ_{JB}	Junction to board[b]		13.2	°C/W

[a] Standard JEDEC 2S2P multilayer PCB.

[b] Thermal model where the heat dissipated in the component is conducted through the board. T_B is measured on or near the component lead.

Temperature Considerations

The 8V19N474 supports applications in a natural convection environment as long as the junction temperature does not exceed the specified junction temperature, T_J. In applications where the heat dissipates through the PCB, Θ_{JB} is the correct metric to calculate the junction temperature. The following calculation uses the junction-to-board thermal characterization parameter, Θ_{JB}, to calculate the junction temperature, T_J. Care must be taken to not exceed the maximum allowed junction temperature T_J of 125 °C.

The junction temperature, T_J, is calculated using the following equation:

$$T_J = T_B + P_{TOT} \times \theta_{JB}$$

where:

- T_J is the junction temperature at steady state conditions in °C
- T_B is the board temperature at steady state condition in °C, measured on or near the component lead
- Θ_{JB} is the thermal characterization parameter to report the difference between T_J and T_B
- P_{TOT} is the total device power dissipation

Application power dissipation scenarios: Applications may use device settings that result in a lower power dissipation than the maximum power scenario. The 8V19N474 is a multi-functional, high-speed device that targets a variety of applications. Since this device is highly programmable with a broad range of settings and configurations, the power consumption will vary as settings and configurations are changed. Table 48 shows the typical current consumption and total device power consumption along with the junction temperature for the test cases shown in Table 40. The table also displays the maximum board temperature for the Θ_{JB} model.

Reducing power consumption: The output state (on/off) and the output amplitude have the largest impact on the device power consumption and the junction temperature: setting the output amplitude to lower voltages and supplying the outputs by 1.8V reduces power consumption. Unused and periodically unused outputs and inputs should be turned off in phases of inactivity to reduce power. For any given divider setting, the clock frequency has no impact on the device power consumption of the device.

Table 48. Typical Device Power Dissipation and Junction Temperature

Test Case[a]	Output Configuration	Device		Θ_{JB} Thermal Model	
		I_{DD_TOT}	P_{TOT}	T_J[b]	$T_{B, MAX}$[c]
		mA	W	°C	°C
1	QCLK_A-D: LVDS, 700mV, VDDO=3.3V	572	1.88	109.8	100.2
2	QCLK_A-D: LVDS, 850mV, VDDO=3.3V	627	2.06	112.2	97.8
3	QCLK_A-E: LVPECL, 850mV, VDDO=3.3V	660	1.83	109.2	100.8
4	QCLK_A-E: LVPECL, 700mV, VDDO=3.3V	634	1.76	108.2	101.8
5	QCLK_A-E: LVPECL/LVDS, 500mV, VDDO=1.8V/3.3V	578	1.66	106.9	103.1
6	QCLK_A-E: LVPECL/LVDS, 350mV, VDDO=1.8V/3.3V	540	1.64	106.6	103.4

[a] See Table 40 for device settings.

[b] Junction temperature at board temperature T_B=85°C

[c] Maximum board temperature for junction temperature <125°C: $T_{B, MAX} = T_{J, MAX} - \Theta_{JB} \times P_{TOT}$

Applications Information

Output Termination

LVPECL-Style Outputs

Differential outputs configured to LVPECL-style are of open-emitter type and require a termination with a DC current path to GND. This section displays parallel and thevenin termination, Y-termination, and source termination for various output supply (V_{DDO_V}) and amplitude settings. V_{TT} is the termination voltage.

Figure 14. LVPECL Parallel Termination 1

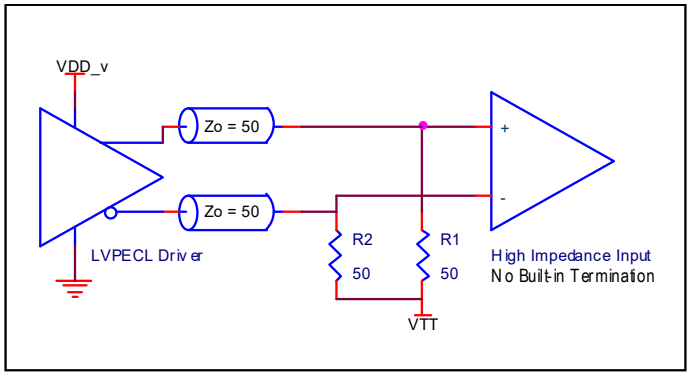


Table 49. Termination Voltage V_{TT} for Figure 14[a]

LVPECL Amplitude (mV)	V_{TT} (V)
350	V_{DDO_V} - 1.60
500	V_{DDO_V} - 1.75
700	V_{DDO_V} - 1.95
850	V_{DDO_V} - 2.10

[a] Output power supplies supporting 3.3V, 2.5V and 1.8V are VDDO_QCLKA, VDDO_QCLKB, VDDO_QCLKC and VDDO_QCLKD.

Figure 15. LVPECL Parallel Termination 2

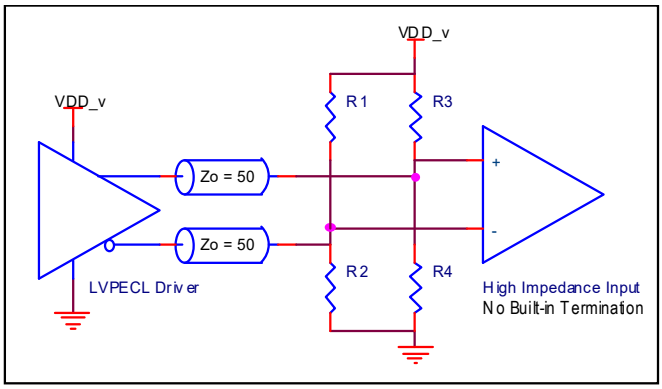


Table 50. Termination Resistor Values for Figure 15

V_{DDO_V} (V)[a]	LVPECL Amplitude (mV)	R1, R3 (Ω)	R2, R4 (Ω)
3.3	350	97.1	103.1
	500	106.5	94.3
	700	122	84.6
	850	137.5	78.6
2.5	350	138.8	78.1
	500	166.7	71.4
	700	227.3	64.1
	850	312.5	59.5
1.8	350	450	56.3
	500	–	50

[a] Output power supplies supporting 3.3V, 2.5V and 1.8V are VDDO_QCLKA, VDDO_QCLKB, VDDO_QCLKC, and VDDO_QCLKD.

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Figure 16. LVPECL Y-Termination

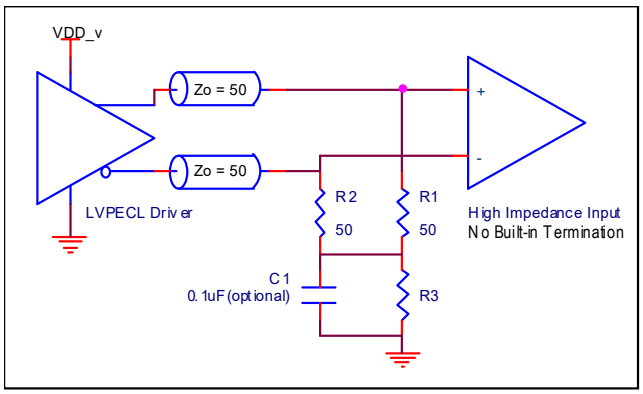

Table 51. Termination Resistor Values for Figure 16

V_{DDO_V} (V)[a]	LVPECL Amplitude (mV)	R3 (Ω)
3.3	350, 500, 700, 850	50
2.5	350, 500, 700, 850	18
1.8	350, 500	0

[a] Output power supplies supporting 3.3V, 2.5V and 1.8V are VDDO_QCLKA, VDDO_QCLKB, VDDO_QCLKC, and VDDO_QCLKD.

Figure 17. LVPECL Source Termination

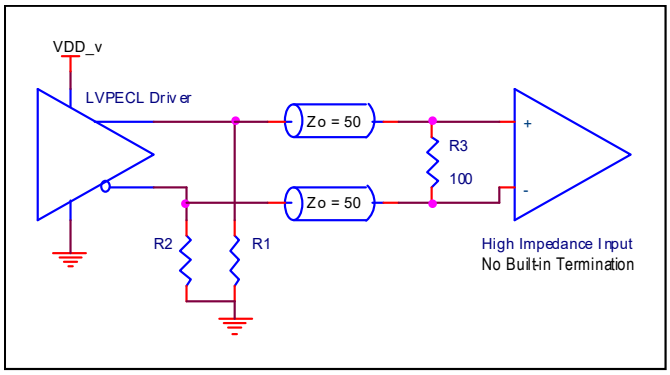

Table 52. Termination Resistor Values for Figure 17

V_{DDO_V} (V)[a]	LVPECL Amplitude (mV)	R1, R2 (Ω)
3.3	350, 500, 700, 850	100–200
2.5	350, 500, 700, 850	80–150
1.8	350	50–100

[a] Output power supplies supporting 3.3V, 2.5V and 1.8V are VDDO_QCLKA, VDDO_QCLKB, VDDO_QCLKC, and VDDO_QCLKD.

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LVDS-Style Outputs

LVDS-style outputs support fully differential terminations. LVDS does not require board-level, pull-down resistors for DC termination. Figure 18 and Figure 19 show typical termination examples with DC coupling for the LVDS style driver. In these examples, the receiver is high-input impedance without built-in termination. LVDS-style with a differential termination is preferred for best common-mode rejection and lowest device power consumption.

Figure 18. LVDS Termination

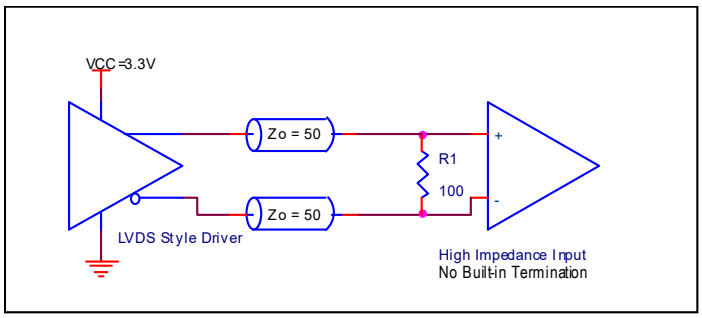
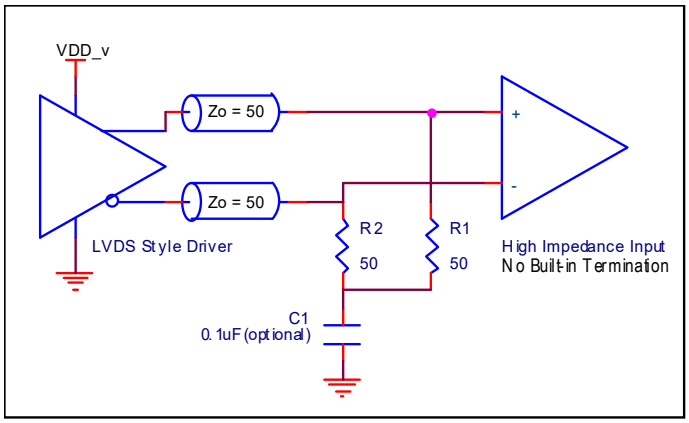


Figure 19. LVDS Termination (Alternative)



Power Supply Design and Recommended Application Schematics

Please refer to the 8V19N474 Hardware Design Guide for comprehensive information about power supply and isolation, loop filter design for VCXO and VCO, schematics, input and output interfaces/terminations and an example schematics. This guide shows a recommended power supply filter schematic in which the 8V19N474 is operated at V_{DD_V} = 3.3V (the output supply voltages of V_{DDO_V} = 3.3V, 2.5V, and 1.8V are supported). This example focuses on power supply connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set for the application.

As with any high-speed analog circuitry, the power supply pins are vulnerable to board supply or device generated noise. The 8V19N474 requires an external voltage regulator for the V_{DD_V} pins for isolation of board supply noise. This regulator (example component: PS7A8300RGT) is indicated in the schematic by the power supply, VREG_3.3V. Consult the voltage regulator specification for details of the required performance. To achieve optimum jitter performance, power supply isolation is required to minimize device generated noise. The VDD_LCF terminal requires the cleanest power supply. The device provides separate power supplies to isolate any high switching noise from coupling into the internal PLLs and into other outputs as shown. In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF and 0.01µF capacitors in each power pin filter should be placed on the device side.

The other components can be on the opposite side of the PCB. Pull-up and pull-down resistors to set configuration pins can all be placed on the PCB side opposite the device side to free up device side area if necessary. Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

Package Outline Drawings

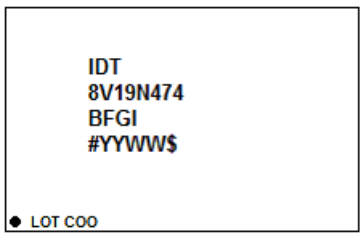
The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/81-fpbga-package-outline-drawing-80-x-80-x-135-mm-body-08mm-pitch-bfbfg81d1

Ordering Information

Orderable Part Number	Package	Shipping Packaging	Temperature
8V19N474BFGI	8 × 8 mm 81-FPBGA	Tray	-40°C to +85°C
8V19N474BFGI8		Tape and Reel	

Marking Diagram



1. Line 1 indicates the prefix.
2. Line 2 indicates the part number.
3. Line 3 indicates the package part number code.
4. Line 4:
   – “YYWW” is the last digit of the year and week that the part was assembled.
   – #: denotes sequential lot number.
   – $: denotes mark code.

Glossary

Abbreviation	Description
Index *n*	Denominates an clock input. Range: 0 to 1
Index *x*	Denominates a channel, channel frequency divider and the associated configuration bits. Range: A, B, C, D
Index *y*	Denominates a QCLK output and associated configuration bits. Range: A0, A1, A2, B0, B1, B2, C0, C1, D0, D1
VDD_v	Denominates core voltage supply pins. Range: VDD_QCLKA, VDD_QCLKB, VDD_QCLKC, VDD_QCLKD, VDD_QCLKE, VDD_SPI, VDD_INP, VDD_LCV, VDD_LCF, VDD_CPV, VDD_CPF, and VDD_OSC
VDDO_v	Denominates output voltage supply pins. Range: VDDO_QCLKA, VDDO_QCLKB, VDDO_QCLKC and VDDO_QCLKD
status_condition	Status conditions are: LOLV (Loss of VCXO-PLL lock), LOLF (Loss of FemtoClock NG-PLL lock) and LOS (Loss of Input Signal)
[...]	Index brackets describe a group associated with a logical function or a bank of outputs
{…}	List of discrete values
Suffix V	Denominates a function associated with the VCXO-PLL
Suffix F	Denominates a function associated with the 2nd stage PLL (FemtoClock NG)

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Revision History

Revision Date	Description of Change
May 15, 2018	▪ Added Figure 10 (312.5MHz Output Phase Noise) ▪ Updated the Package Outline Drawings; however, no technical changes
November 12, 2017	Removed “QCLK_*y*, N=÷25” from Table 45
April 9, 2017	▪ Removed footnote [a] from Table 2 ▪ Updated Table 3 ▪ Updated footnote [a] in Table 15 ▪ Updated the default information for SELSV1 and SELSV0 in Table 22 ▪ Updated the description of INT_SEL in Table 28 ▪ Updated various descriptions in Table 34
March 29, 2017	Initial release.

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