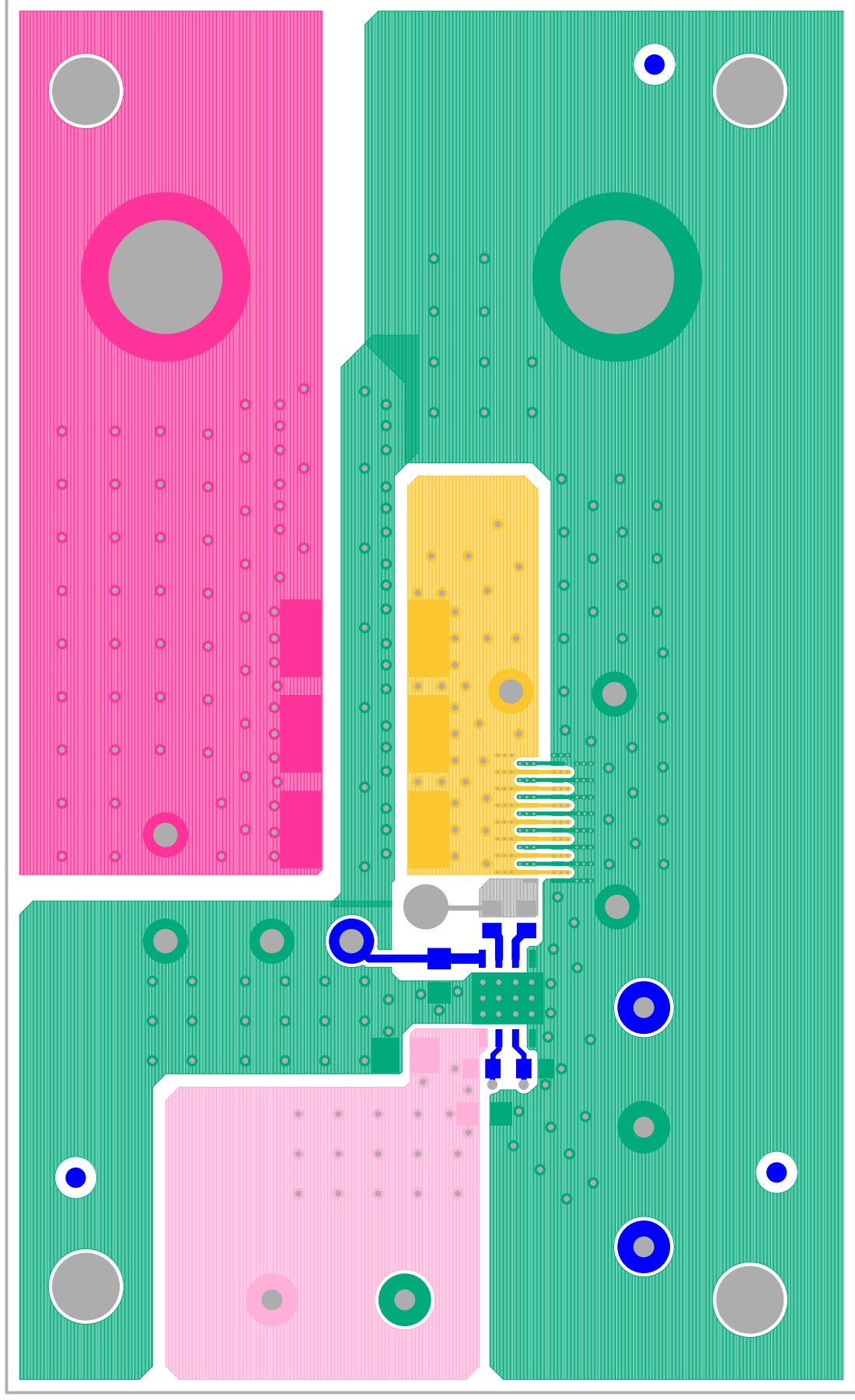


ASSEMBLY TOP
INTERSIL CORPORATION
02-26-2019

02-26-2019

ISL71040MEV1Z REV.B

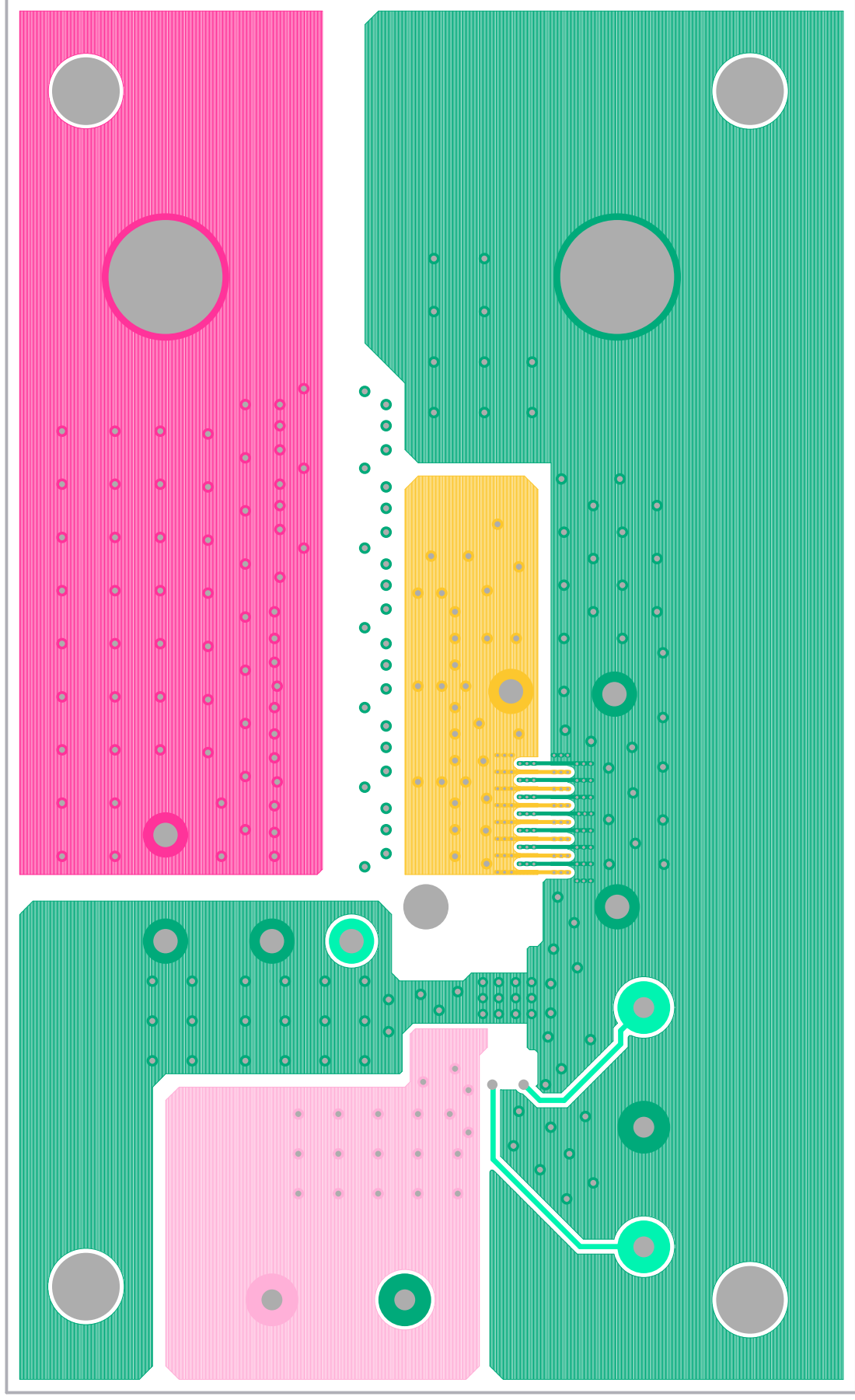


TOP LAYER COMPONENT SIDE

INTERSIL CORPORATION

02-26-2019

ISL71040MEV1Z REV.B

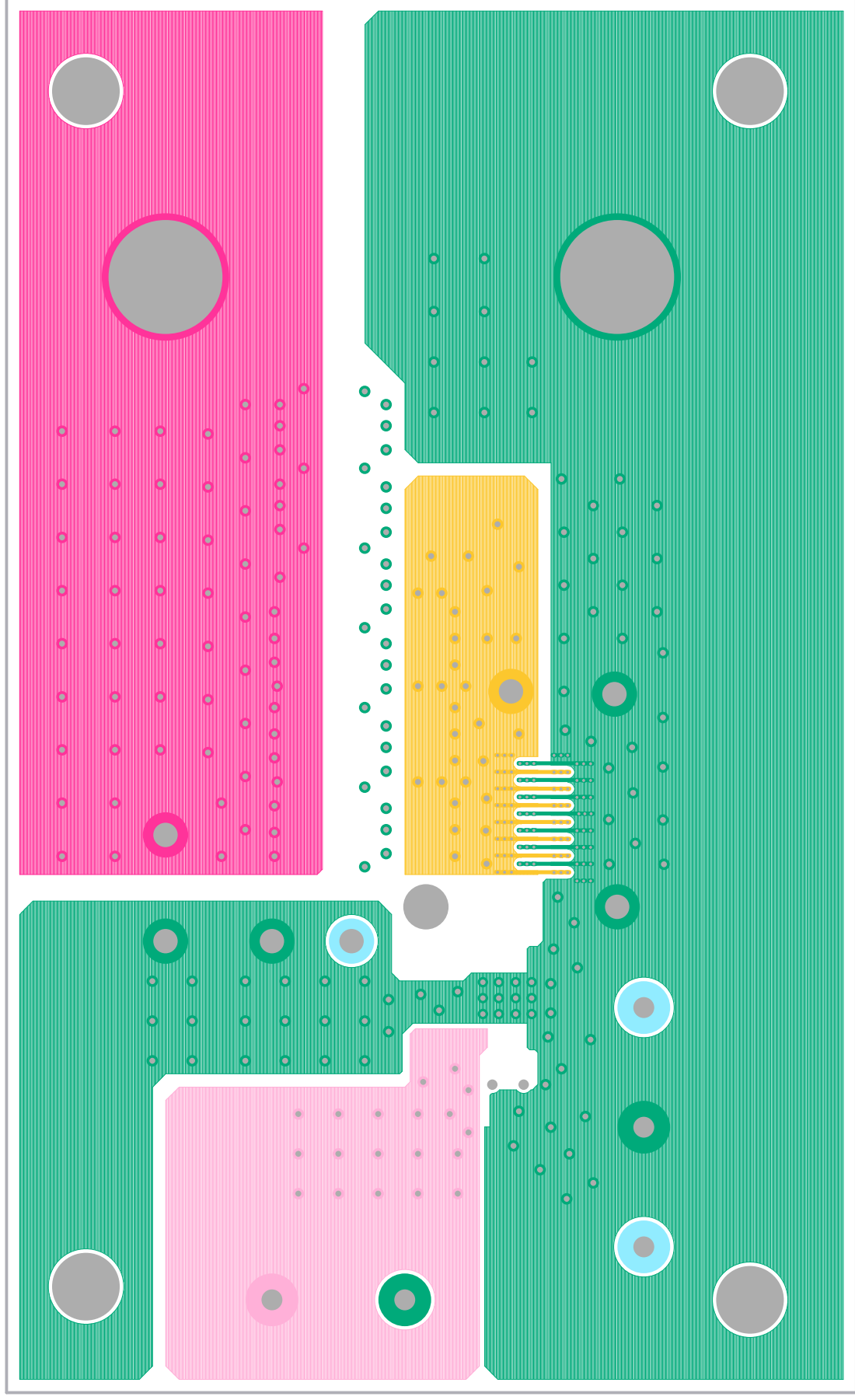


LAYER 2

INTERSIL CORPORATION

02-26-2019

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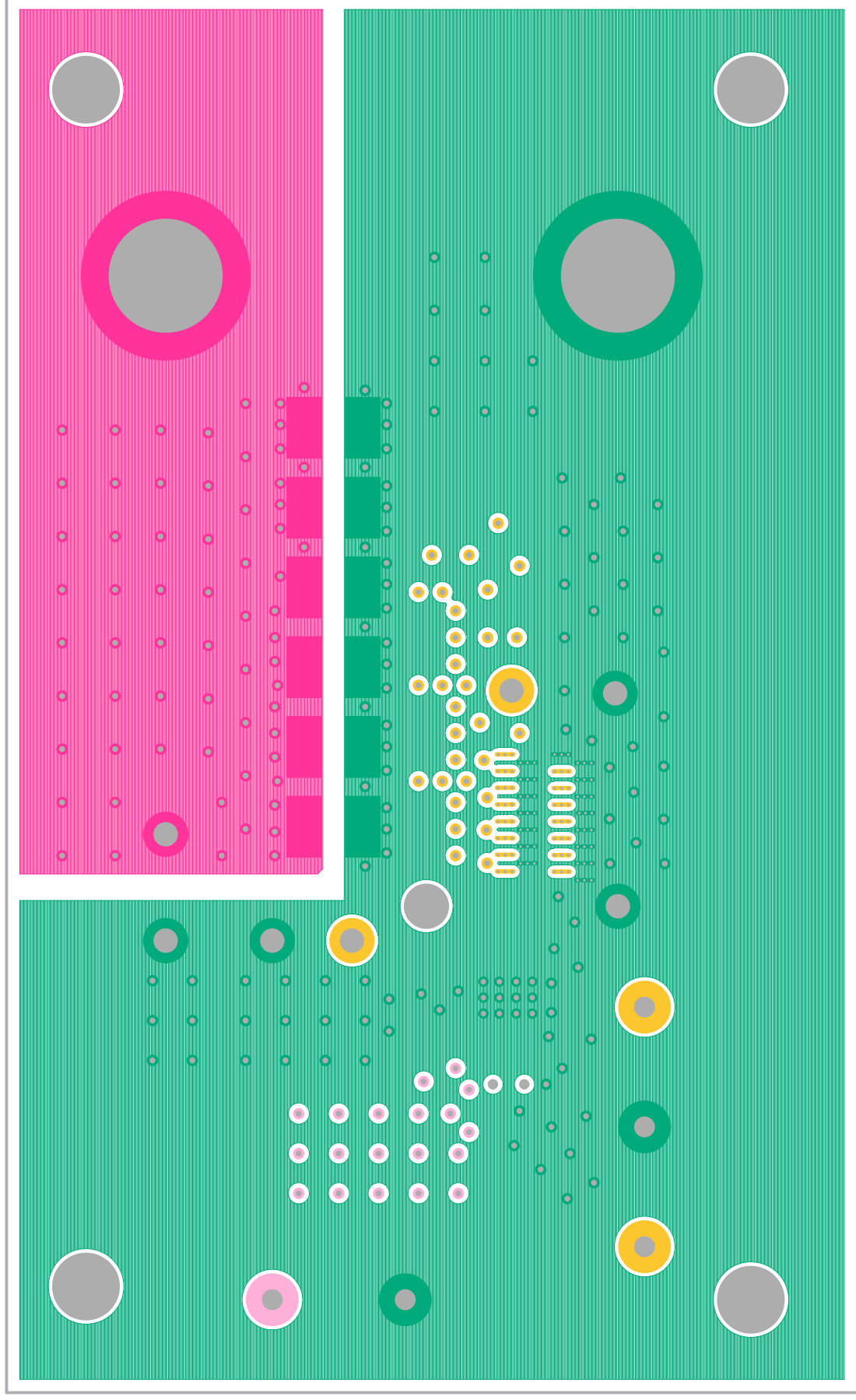


LAYER 3

INTERSIL CORPORATION

02-26-2019

ISL71040MEV1Z REV.B

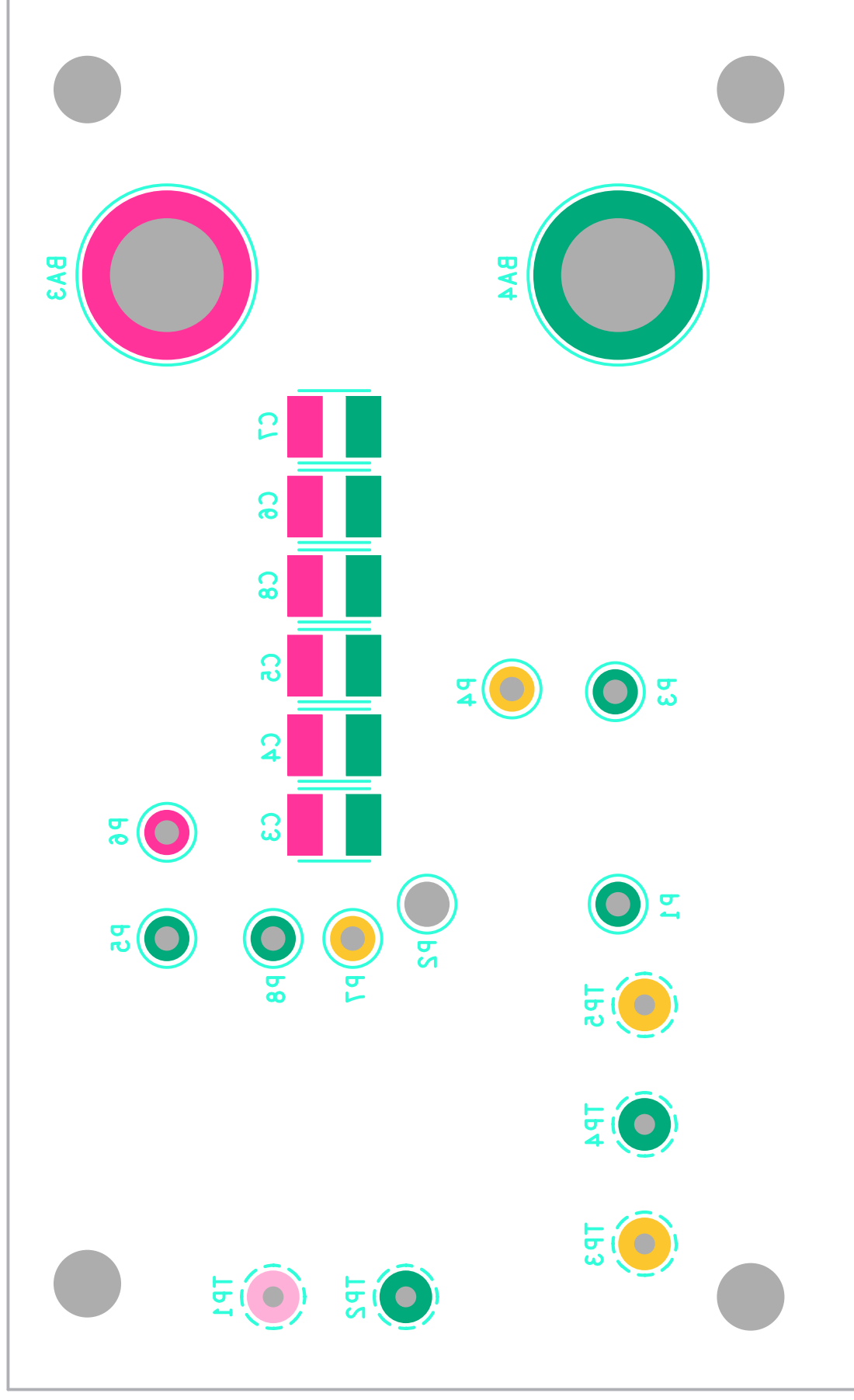


BOTTOM LAYER SOLDER SIDE

INTERSIL CORPORATION

02-26-2019

ISL71040MEV1Z REV. B



SILK SCREEN BOTTOM

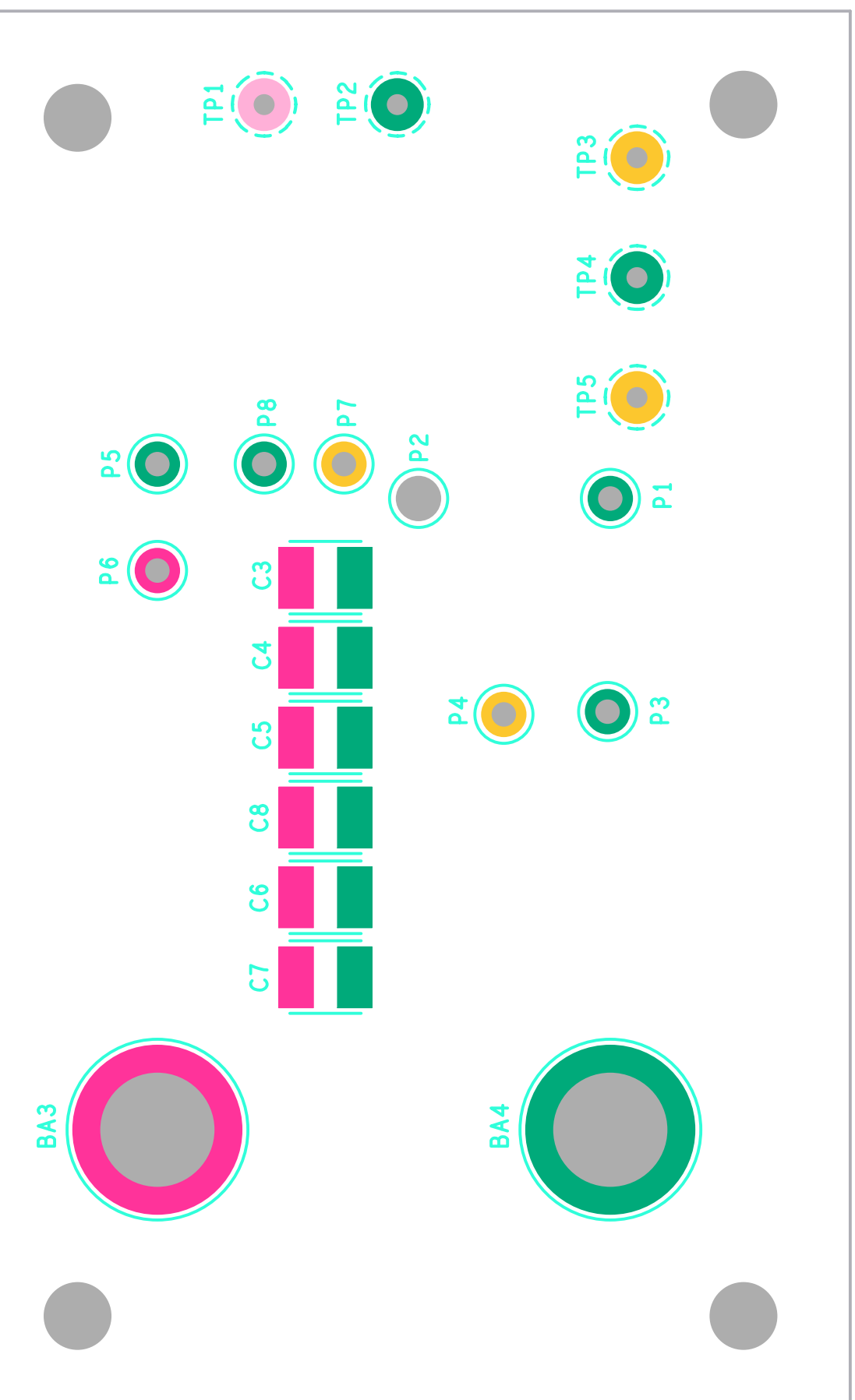
INTERSIL CORPORATION

02-26-2019

05-56-5019

INTERSTIL COOPERATION

SITK SCREEN BOTTOM



ISFL1040MEV15 REV.B

05-5e-501a

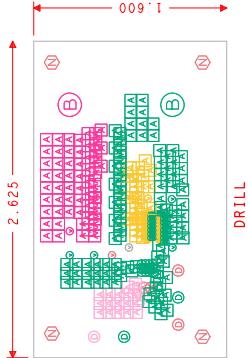
INSERT COBORIZATION ASSEMBLY BOTTOM

	C3
	C4
	C5
	C8
	C6
	C7

PHYSICAL BOARD DIMENSIONS
& LAYER STRUCTURE

	SILK TOP	silk1.art
	MASK TOP	smask1.art
	(TOP)COMPONENT	layer1.art
	LAYER 2	layer2.art
	LAYER 3	layer3.art
	(BOTTOM) SOLDER	layer4.art
	MASK BOTTOM	smaskb.art
	SILK BOTTOM	silkb.art

.062" +/- 10%



DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILS			
FIGURE	SIZE	PLATED	QTY
⊙	6.0	PLATED	93
⊙	10.0	PLATED	2
⊙	11.0	PLATED	12
⊠	12.0	PLATED	217
⊙	40.0	PLATED	5
⊙	46.0	PLATED	8
⊕	215.0	PLATED	2
⊞	128.0	NON-PLATED	4

NOTES:

1. THIS BOARD IS RoHS COMPLIANT.
2. PRINTED WIRING BOARD DESIGN AND ACCEPTANCE CRITERIA SHALL BE IAW WITH THE REQUIREMENTS OF IPC-D-275 AND IPC-A-600.
3. MATERIAL: FR4 (RoHS COMPLIANT), 2 OZ COPPER.
4. APPLY SOLDER MASK, BOTH SIDES OVER BARE COPPER IAW IPC-SM-840. CLASS 2 (LPI) (BLUE MASK).
5. ALL PATTERNS ARE VIEWED FROM THE PRIMARY SIDE LOOKING THROUGH THE BOARD.
6. UNLESS OTHERWISE SPECIFIED ALL HOLE DIAMETERS ARE AFTER PLATING.
7. APPLY SILKSCREEN USING WHITE NON-CONDUCTIVE EPOXY BASED INK.
8. PWB MUST BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY. USE NETLIST PROVIDED ISL71040MEV1ZB_IPC356_IPC IAW IPC-D-356.
9. MARK DATE CODE AND MANUFACTURES IDENTIFICATION ON SOLDER SIDE PER IPC-6011 AND IPC-6012.
10. TOLERANCE ON ALL DRILL HOLES SHALL BE IAW IPC-D-2221 & 2222 UNLESS OTHERWISE SPECIFIED.
11. ALL 11 MIL VIAS ARE TO BE THERMAL NON-CONDUCTIVE EPOXY FILLED AND CAPPED.
12. ALL 6 MIL VIAS ARE TO BE CONDUCTIVE EPOXY FILLED (COPPER FILLED) AND CAPPED.

Drawn By: Tim Klemann	Date Drawn: 02/26/2019	Engineer: Kiran Bernard
Released By:	Date Released:	ISL71040M EVALUATION BOARD LAYOUT
Updated By:	Date Updated:	
		MASK# ISL71040MEV1Z
		REV. B
intersil		FILENAME: ~/ISL71040M/ISL71040MEV1ZB
		SHEET 1 of 1