

## VersaClock 7 RC21/RC31 Series – Measurement of Hitless Switching

This document provides the steps needed to setup Hitless Switching on VersaClock 7 (VC7) RC21/RC31 Series using Renesas IC Toolbox (RICBox).

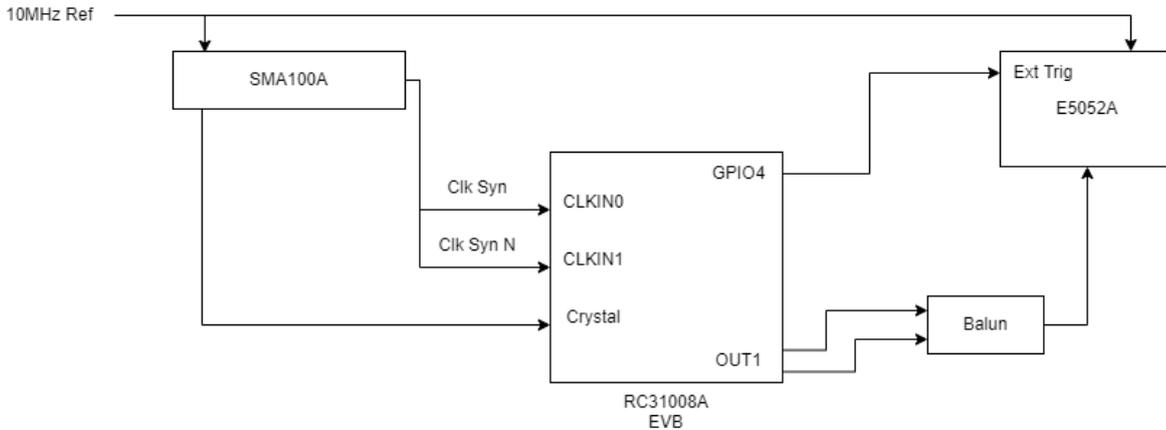
For more information about RICBox, see the [Renesas IC Toolbox User Guide](#). The measurement of hitless switching will be done using the E5052A Signal Source Analyzer.

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## 1. Bench Setup

Equipment used for this measurement are the RC21008A/RC31008A Evaluation Kit (EVK), Rohde & Schwarz SMA100A with the SMA-B29 module, and Agilent E5052A. The 10MHz Ref signal is needed to synchronize the SMA100A and the E5052A in order for the phase plot to be as flat as possible. Similar equipment and differential clock sources can be used as well.



### 1.1 RC21008A/RC31008A EVB Setup

Connect the USB-C cable to the host PC. Communications will be I<sup>2</sup>C. Ensure there is a method to connect a GPIO to the E5052A External Trigger.

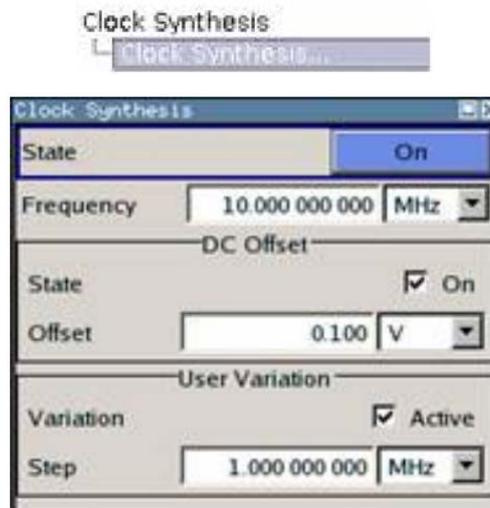
### 1.2 SMA100A Setup

There are three elements to be setup:

- RF out
- clk syn
- External reference enable

To setup the RF out, first push the **Frequency** button and enter the desired value. Second, push the **Level** button and enter **600mV**. Turn on the output.

To setup the clk syn, push the **Menu** button on the front panel. Navigate down to **Clock Synthesis**. Navigate down to Clock Synthesis and push the main knob to display the configuration menu.

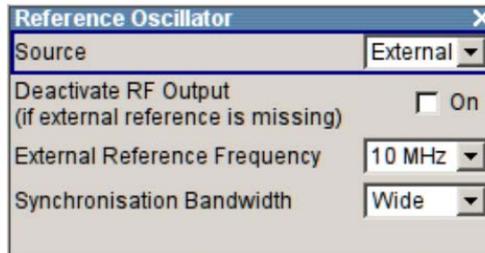


Enter the desired **Frequency** and set the **DC Offset** to 1.2V. For this example, we will be using 100MHz. The true signal is connected to CLKIN0 and the complimentary signal is connected to CLKIN1. The 180 degree phase offset is the worst case scenario. Enable the outputs by setting the state to **On**.

To setup the external reference, do one of the following:

- In the block diagram, select "RF > config... > RF Frequency > Reference Oscillator"
- Press the MENU key and select "RF > RF Frequency > Reference Oscillator"
- Press the SETUP key and select "Setup > System > Reference Oscillator"

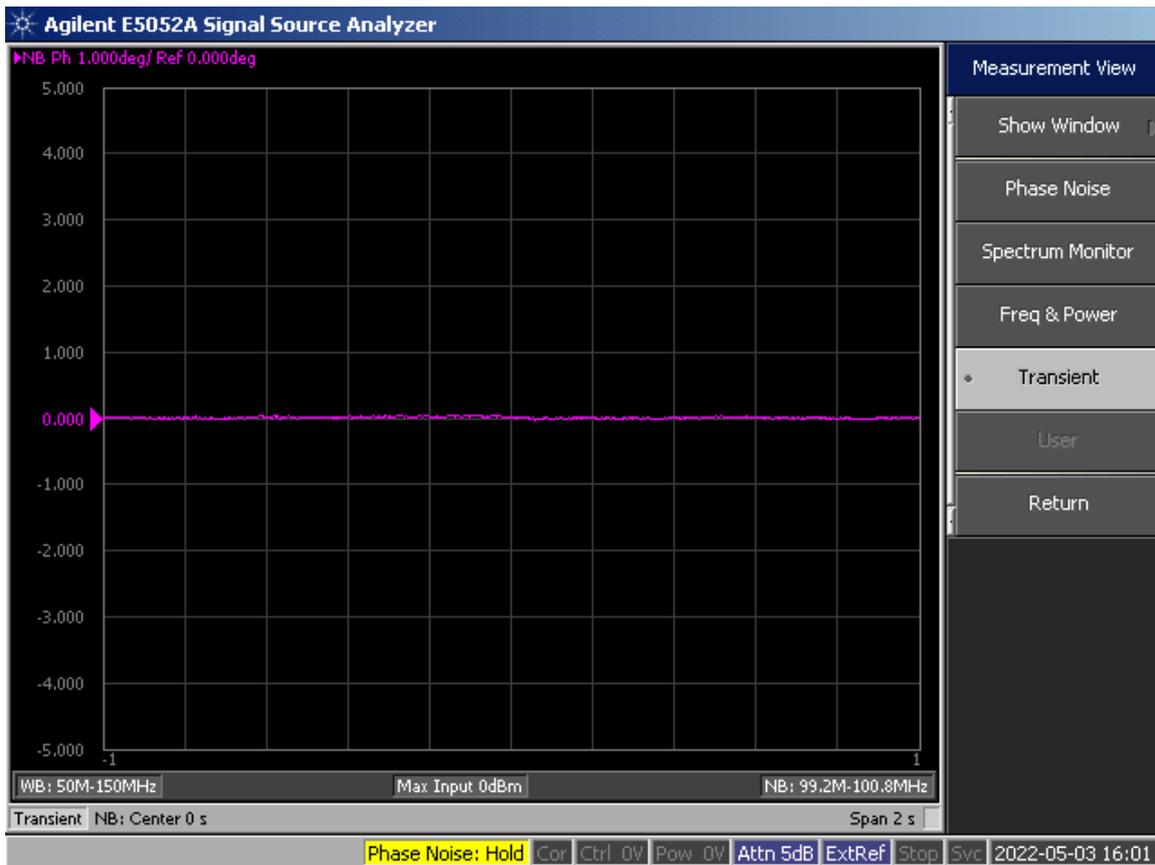
Select **External** for the "Source".



### 1.3 E5052A Setup

In order to measure hitless switching, the Transient feature of the E5052A will be used.

1. From the root menu, click on **Measurement View**.
2. Next, click **Transient**. By double-clicking the lower right of the screen, NB Ph, the plot will become full screen.
3. The full screen view of the Transient plot is now visible. Click **Return**.



The span for capturing data needs to be set.

1. Click the **Span** button.
2. For the Narrow Span setting, a value of 2 seconds will be used. Click on **Return** when done.

The scale of the y axis needs to be set.

1. Click the **Scale** button.
  - a. The typical specification for hitless switching is 100ps. To convert into degrees, use the following formula:
$$100 \text{ ps} \times 360^\circ \times (\text{output frequency})$$
  - b. The output frequency will be set to 100MHz which makes the datasheet specification limit 3.6 degrees. As a result, the deg/div will be set to '1'.

The X axis will need to be adjusted.

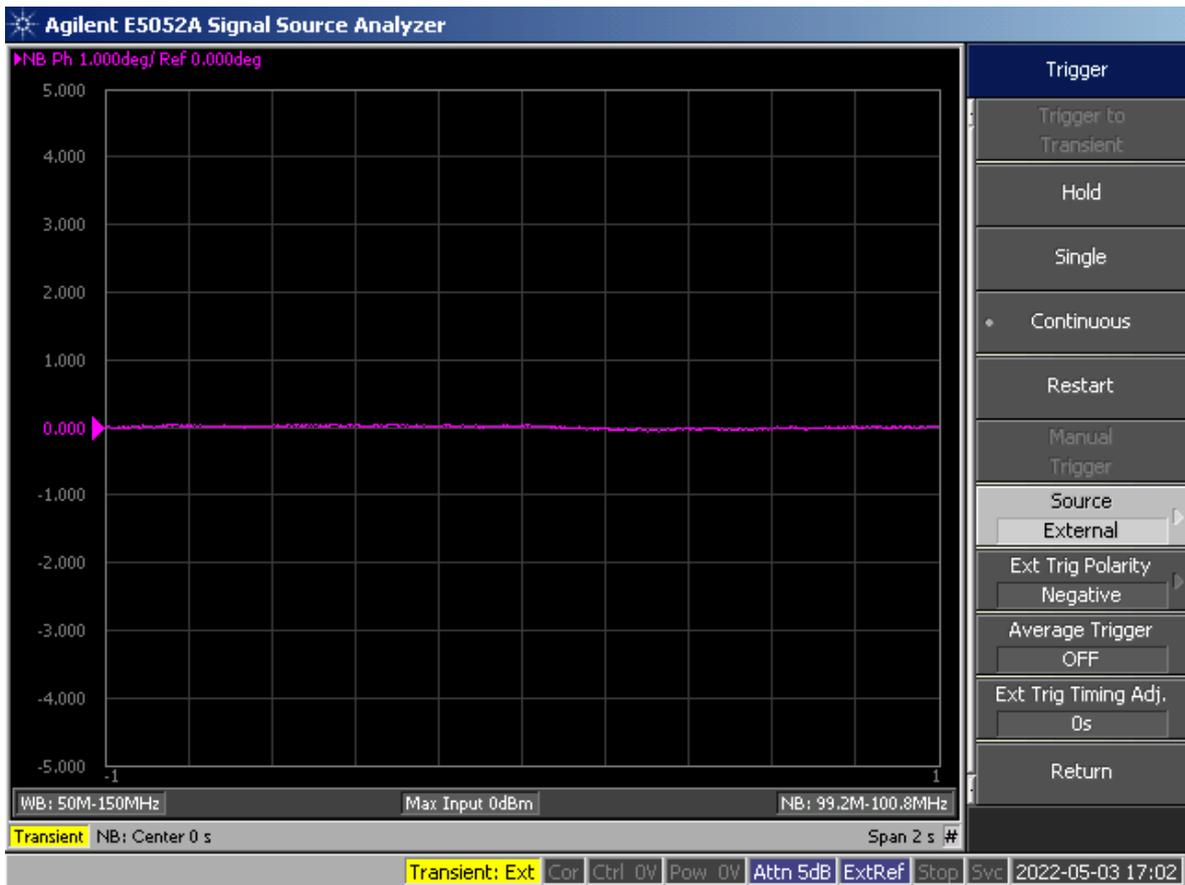
1. Click the X Axis button.
2. The Auto setting needs to be set to OFF, Left set to '-1', and Right set to '1'.

The next step is to setup the Transient measurement for the expected frequency of 100MHz.

1. Click **Setup**.
2. For this sub-menu, the WB Frequency will be set to 50MHz – 150MHz.
3. Target Frequency will be set to 100MHz.
4. Frequency Range will be set to 1.6MHz.
5. Phase Reference will be set to 100MHz.
6. Click **Return** when done.

The final step is to setup the Trigger to use Ext Trig.

1. Click the **Trigger** button.
2. Click Trigger to Transient.
3. Click **Continuous**. The phase plot should be very flat around 0 degrees.
4. Click **Source** and select **External**.
5. Select **Negative** for Ext Trig Polarity.



The last step is to connect GPIO4 of the EVB to the Ext Trig of E5052A. As the clock switch is occurring, the DPLL Lock Status will momentarily go Low.

## 2. RICBox Installation

For more information on installing RICBox software for VC7, see the [Renesas IC Toolbox User Guide](#).

## 3. Creating the Settings File

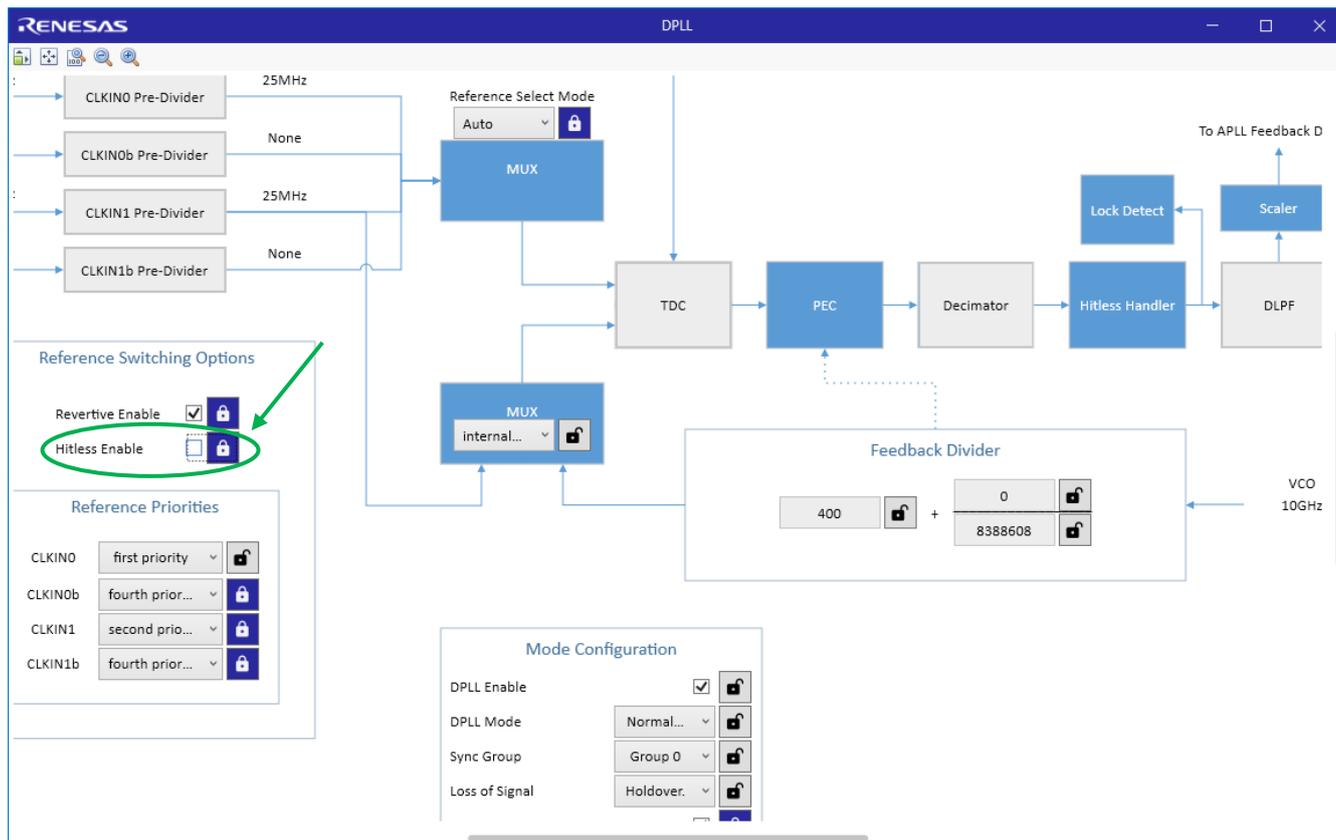
RICBox settings files or '.rbs' files are used to save and distribute custom device configurations. Each settings file contains all of the register settings for a given device. For more information, see Appendix A, Appendix B, and Appendix C.

## 4. CLKIN Switching

In order to cause a switch, the clock signal connected to CLKIN0 must be removed. One way to accomplish this is to remove the cable connected to CLKIN0. Another way is to disable the clock generator connected to CLKIN0. The method used in this example will be to disable/enable the input buffer using RICBox. For more information, see Appendix D.

### 4.1 Non-Hitless Switching vs Hitless Switching

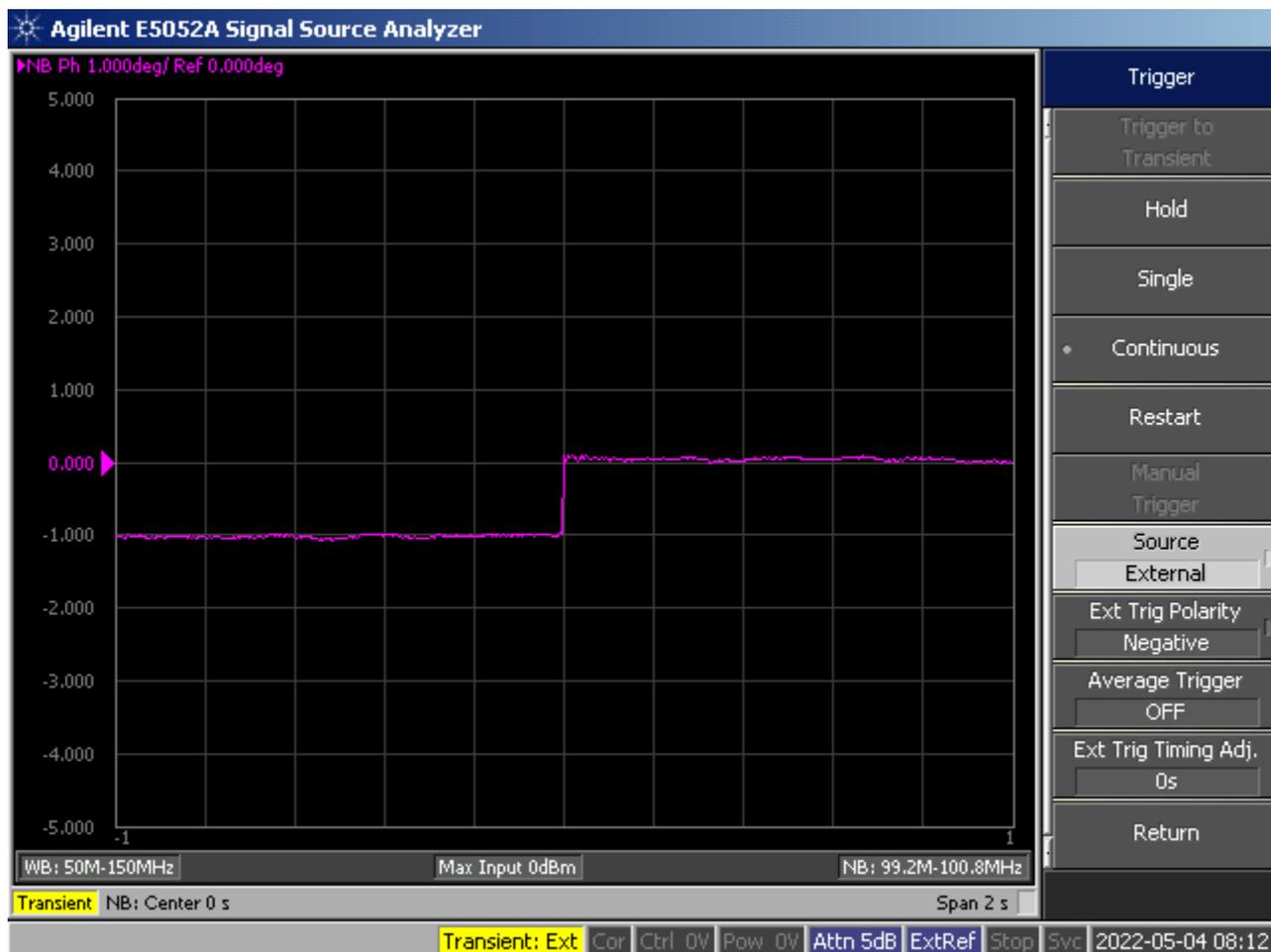
Hitless Switching can be disabled by un-checking Hitless Enable in the DPLL sub diagram.



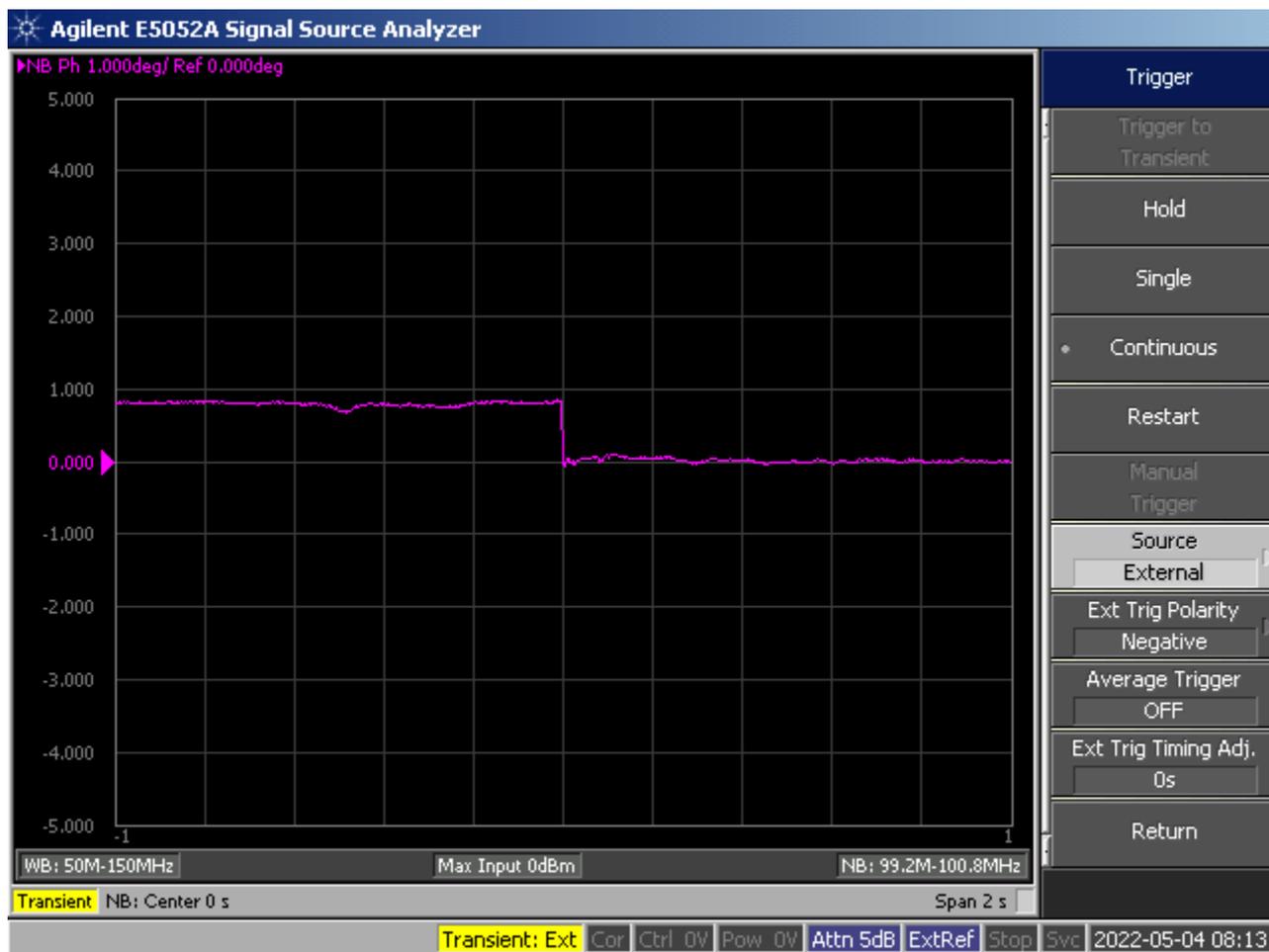
## 4.2 Hitless Switching

Force a switch using one of the methods mentioned in [CLKIN Switching](#).

- CLKIN0 to CLKIN1



- CLKIN1 to CLKIN0

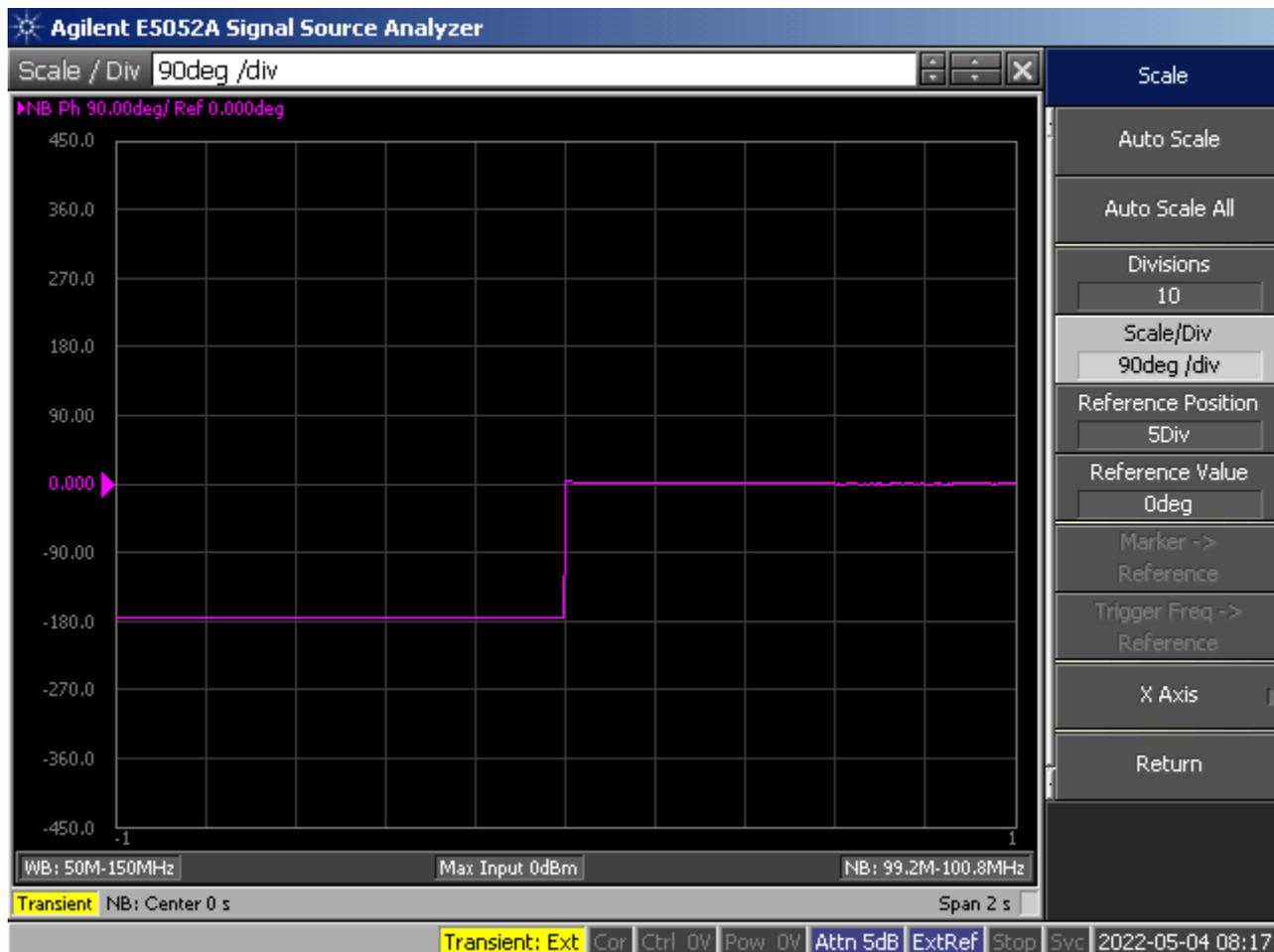


With Hitless enabled, the delta in degrees will be around or less than the datasheet typical specification of 3.6 degrees.

### 4.3 Non-Hitless Switching

To view this transition, the E5052A Scale/Div setting was set to 90 deg/div. As mentioned earlier, a single LVDS clock source was used to supply CLKIN0 and CLKIN1. The true side of the LVDS signal is connected to CLKIN0 while the complementary side is connected to CLKIN1. This creates a worst case scenario as the input clocks are 180 degrees out of phase. Next, force a switch to CLKIN1 and then back to CLKIN0.

- CLKIN0 to CLKIN1



- CLKIN1 to CLKIN0

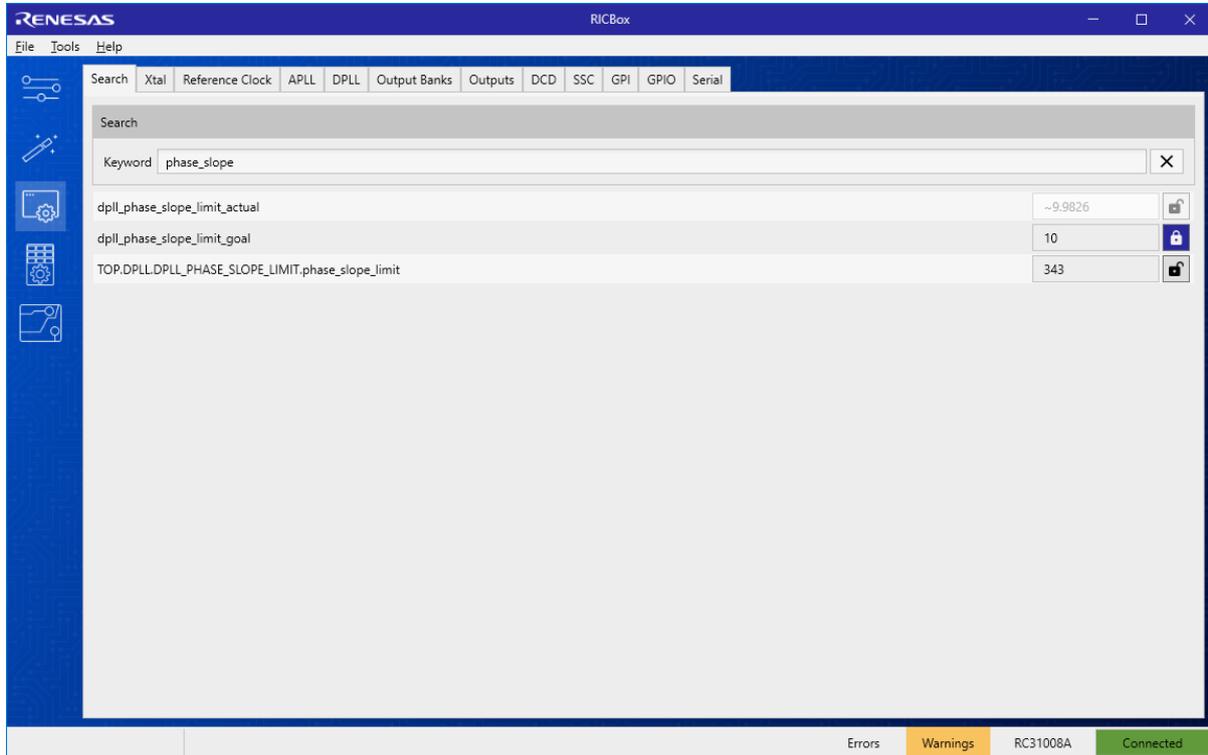


## 4.4 Phase Slope Limit

During a hitless switch from one input clock to another, the transition is “abrupt”. The phase slope limiter can be used to limit how fast a transition is allowed.

To set the phase slope limit:

1. Click on **Configuration** view in RICBox.
2. Enter ‘phase\_slope’ in the **Keyword** field and click enter.
3. In the field called ‘dpll\_phase\_slope\_limit\_goal’, enter ‘10’.



4. Move to the E5052A and set the Span to 5ms and adjust the X axis to display -2.5ms to 2.5ms.
5. Cause a hitless switch.
6. Add two markers to measure the phase.
7. Use the following formula to convert to ns/s:

$$\frac{(y_2 - y_1)}{(x_2 - x_1)} \times \frac{10^9}{(360^\circ \times output\_frequency)}$$

where the y values are phase measurement in degrees and the x values are time in seconds.

For this measurement, we have the following data.

| X              | Y                 |
|----------------|-------------------|
| 200e-6 seconds | -0.552106 degrees |
| 500e-6 seconds | -0.443733 degrees |



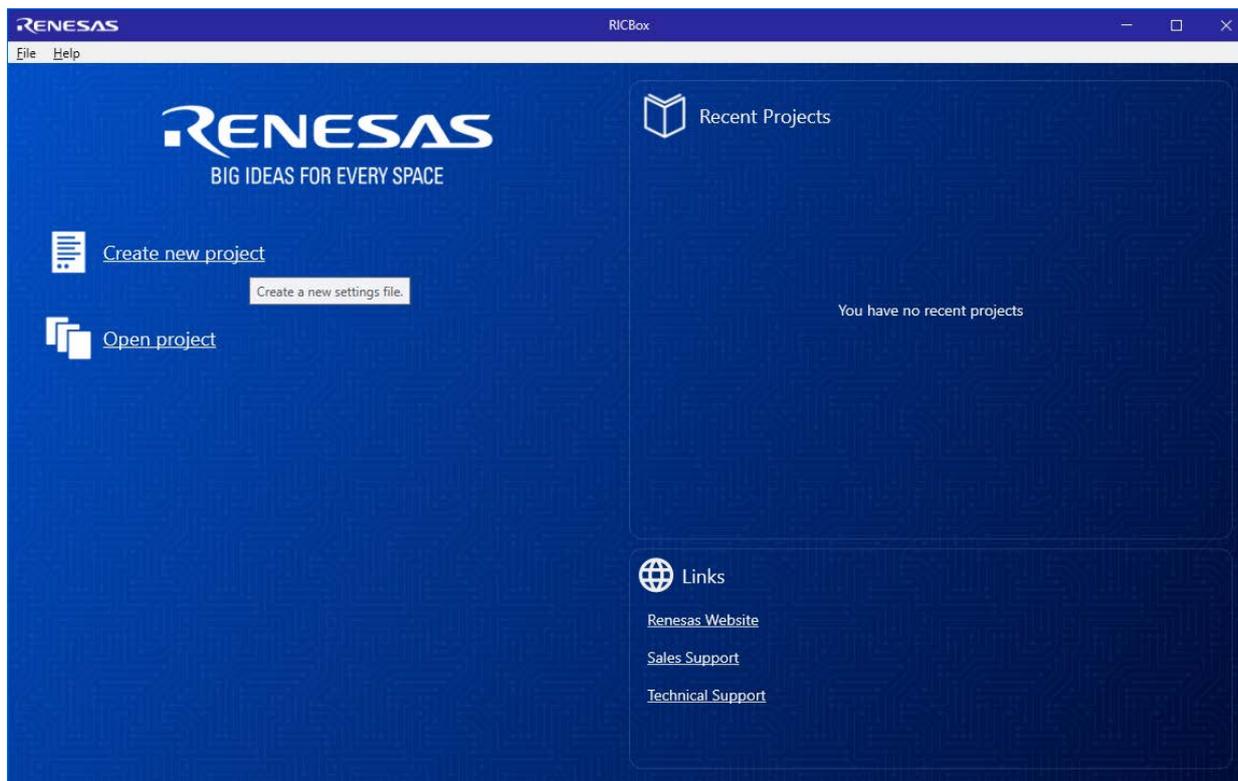
$$\frac{(-0.443733 - -0.552106)}{(500 - 200) \times 10^{-6}} \times \frac{10^9}{(360^\circ \times 100 \times 10^6 \text{Hz})} = 10.035 \text{ ns/s}$$

## 5. Revision History

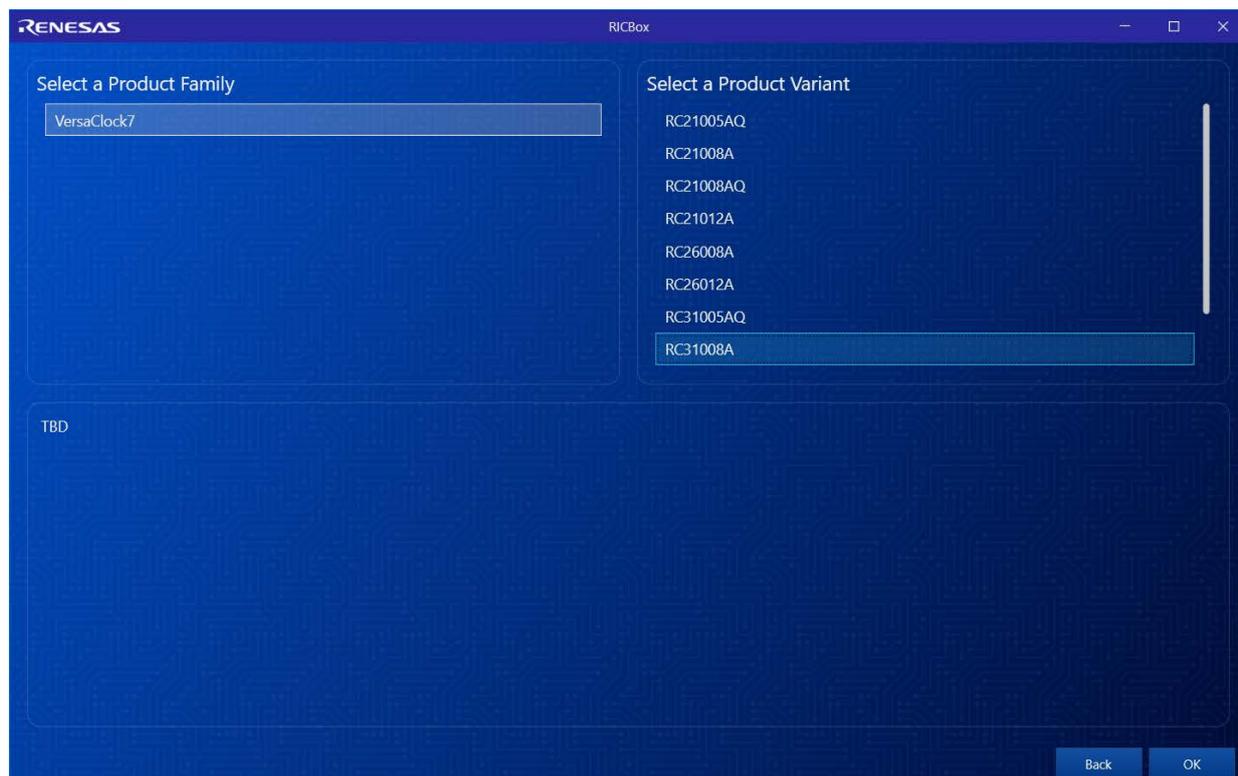
| Revision | Date        | Description      |
|----------|-------------|------------------|
| 1.00     | Aug 5, 2022 | Initial release. |

## Appendix A – Creating a New Configuration

To create a new configuration, open RICBox and click on **Create new project**.

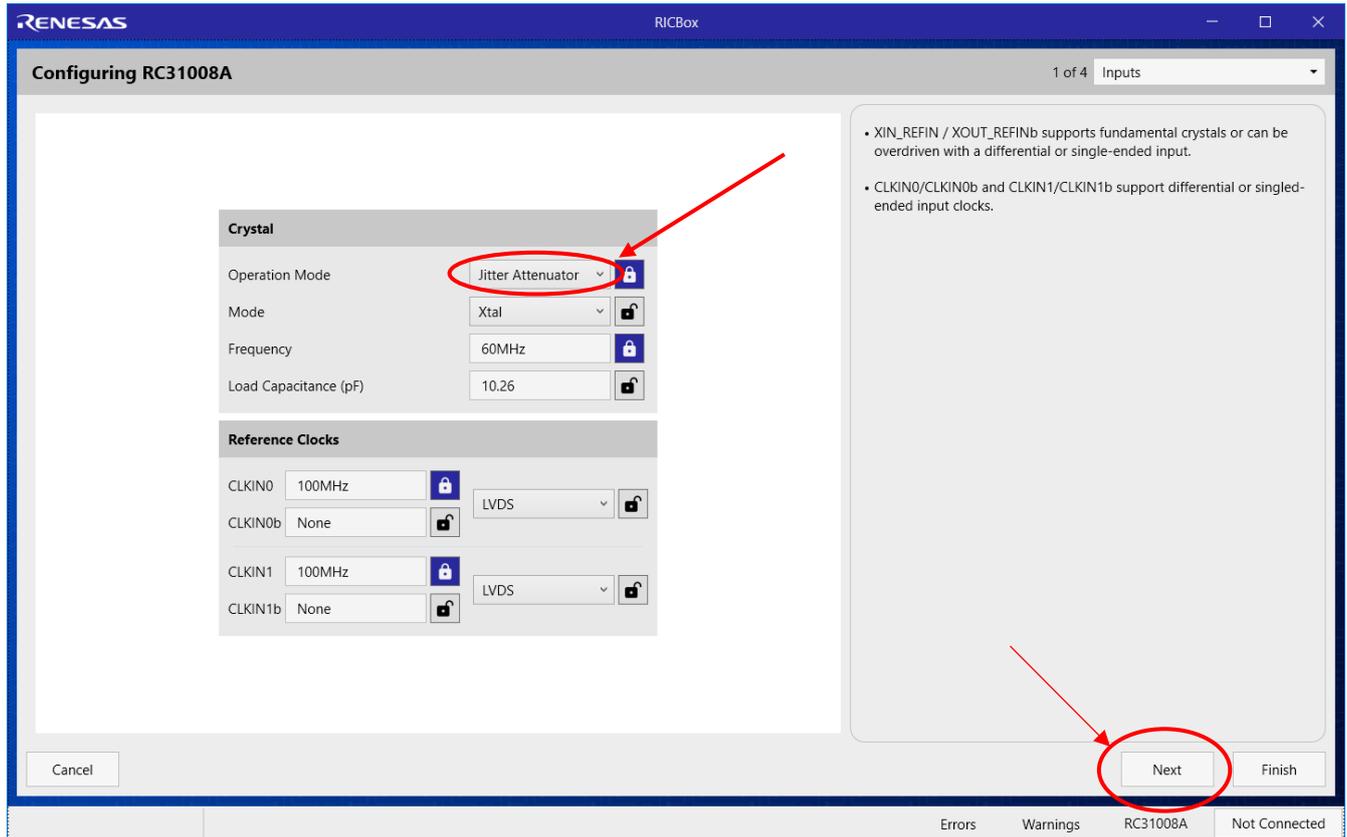


Choose RC31 device to be configured and push OK.



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Configure the RC31 for **Jitter Attenuator** mode and enter the information to match your setup. For this example, the input clock will be 100MHz LVDS. The True signal will be connected to CLKIN0 and the Complimentary signal will be connected to CLKIN1. Click **Next** to go to the DPLL page.





# VersaClock 7 RC21/RC31 Series – Measurement of Hitless Switching

Window showing a summary of the settings.

The screenshot displays the Renesas software interface for configuring the RC31008A. The window title is 'Untitled - RICBox'. The main settings area is organized into several sections:

- Settings**
  - Mode**: Operational Mode is set to JA.
- Input**
  - XTAL: 60MHz
  - XTAL load capacitance: 10.26 (0.0002ppt from goal of 10.26)
  - CLKIN0: 100MHz
  - CLKIN0b: None
  - CLKIN1: 100MHz
  - CLKIN1b: None
- SysClock**
  - Quad sys clock: ~227.2727MHz
- APLL**
  - APLL Frequency: 10GHz (29.8023ppt from goal of 10GHz)
  - Divider: ~83.3333 (83+44739243/2^27)
  - Loop Bandwidth: ~942.2456kHz
  - Phase Margin (degrees): ~59.2687
  - Third Pole Frequency: ~28.4205MHz
- DPPLL**
  - Enabled: yes
  - DPPLL Frequency: 10GHz
  - Divider: 400 (400+0/8388608)
  - Normal Bandwidth: ~23.8203Hz
  - Acquire Bandwidth: ~222.3227Hz
  - Decimator Bandwidth: ~1.9428kHz
- Outputs**
  - OUT1: 100MHz [LPHCSL]
  - OUT2: powered down (Hi-Z)
  - OUT3: powered down (Hi-Z)
  - OUT6: powered down (Hi-Z)
  - OUT7: powered down (Hi-Z)
  - OUT8: powered down (Hi-Z)
  - OUT10: powered down (Hi-Z)
  - OUT11: powered down (Hi-Z)
- Output Banks**: (Section header, no specific values listed)

The status bar at the bottom of the window shows 'Errors', 'Warnings', 'RC31008A', and 'Not Connected'.

## Appendix B – Setting Up Hitless Switching

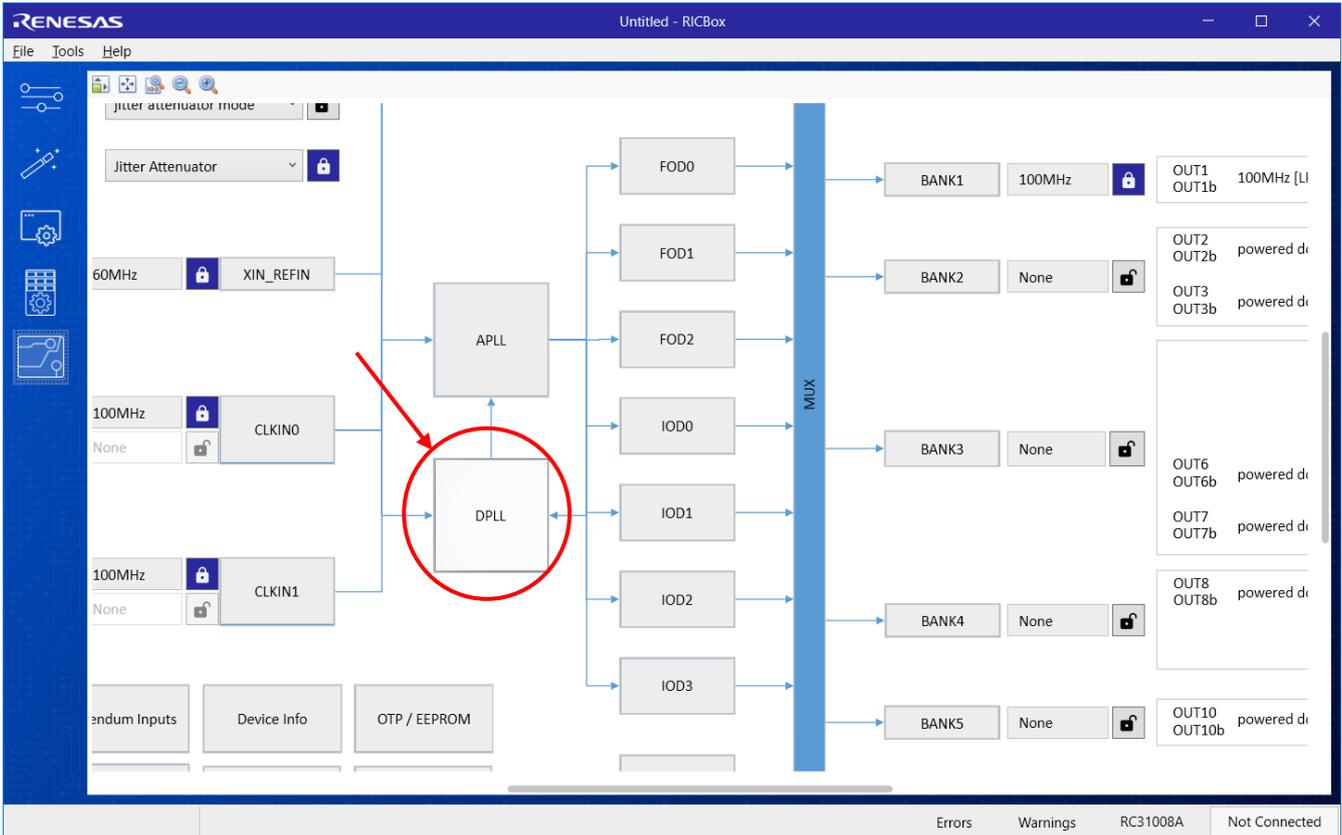
Click the **Block Diagram** icon to view block diagram.

The screenshot shows the RENESAS RICBox software interface for device RC31008A. The 'SysClock' section is highlighted with a red circle and arrow, indicating the 'Quad sys clock' setting.

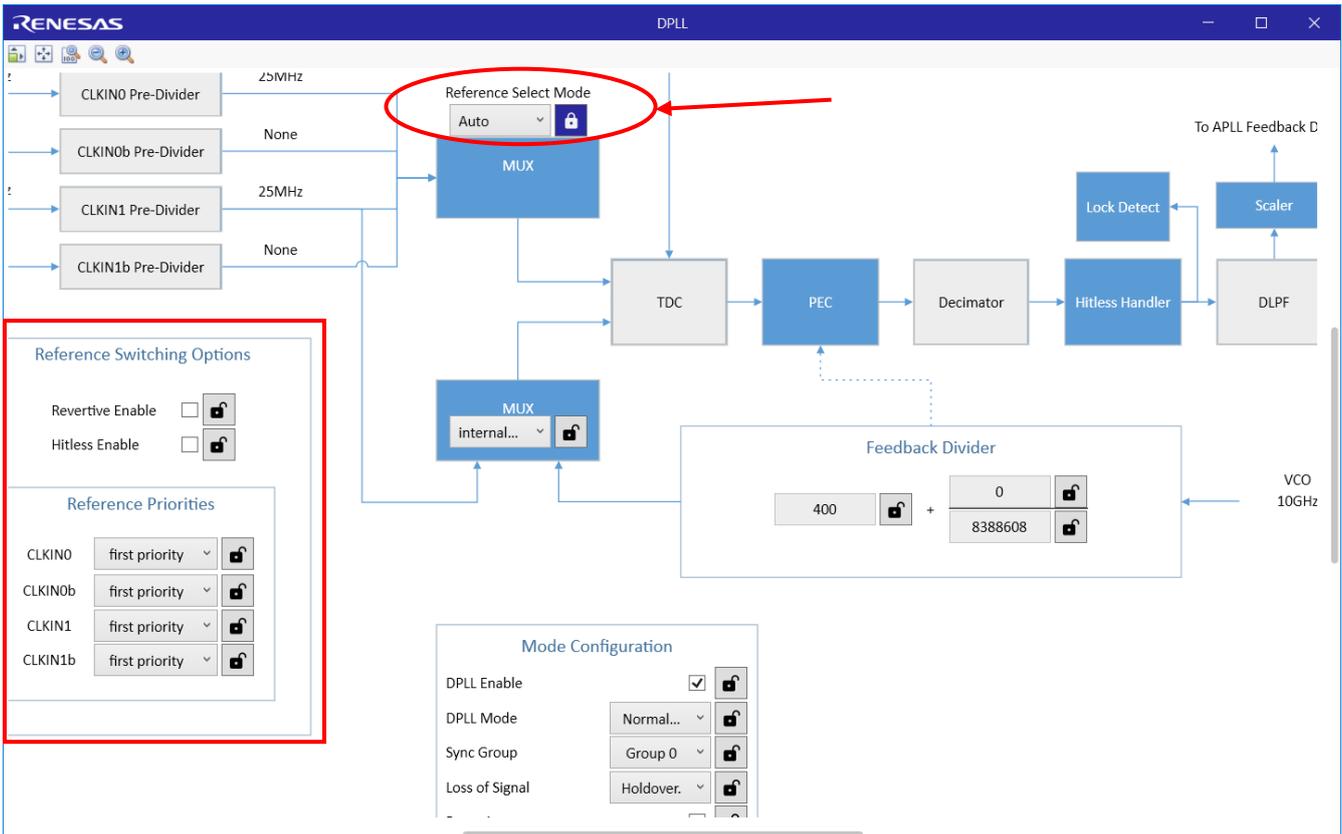
| Section      | Parameter              | Value                                 |  |
|--------------|------------------------|---------------------------------------|--|
| Settings     | Mode                   | Operational Mode: JA                  |  |
|              | Input                  | XTAL: 60MHz                           |  |
| Input        | XTAL load capacitance  | 10.26 (0.0002ppt from goal of 10.26)  |  |
|              | CLKIN0                 | 100MHz                                |  |
|              | CLKIN0b                | None                                  |  |
|              | CLKIN1                 | 100MHz                                |  |
| SysClock     | CLKIN1b                | None                                  |  |
|              | Quad sys clock         | ~227.2727MHz                          |  |
| APLL         | APLL Frequency         | 10GHz (29.8023ppt from goal of 10GHz) |  |
|              | Divider                | ~83.3333 (83+44739243/2^27)           |  |
|              | Loop Bandwidth         | ~942.2456kHz                          |  |
|              | Phase Margin (degrees) | ~59.2687                              |  |
| DPLL         | Third Pole Frequency   | ~28.4205MHz                           |  |
|              | Enabled                | yes                                   |  |
|              | DPLL Frequency         | 10GHz                                 |  |
|              | Divider                | 400 (400+0/8388608)                   |  |
| Outputs      | Normal Bandwidth       | ~23.8203Hz                            |  |
|              | Acquire Bandwidth      | ~222.3227Hz                           |  |
|              | Decimator Bandwidth    | ~1.9428kHz                            |  |
|              | OUT1                   | 100MHz [LPHCSL]                       |  |
| Output Banks | OUT2                   | powered down (Hi-Z)                   |  |
|              | OUT3                   | powered down (Hi-Z)                   |  |
|              | OUT6                   | powered down (Hi-Z)                   |  |
|              | OUT7                   | powered down (Hi-Z)                   |  |
|              | OUT8                   | powered down (Hi-Z)                   |  |
|              | OUT10                  | powered down (Hi-Z)                   |  |
|              | OUT11                  | powered down (Hi-Z)                   |  |
|              | Status                 |                                       | Errors: Warnings: RC31008A Not Connected |

# VersaClock 7 RC21/RC31 Series – Measurement of Hitless Switching

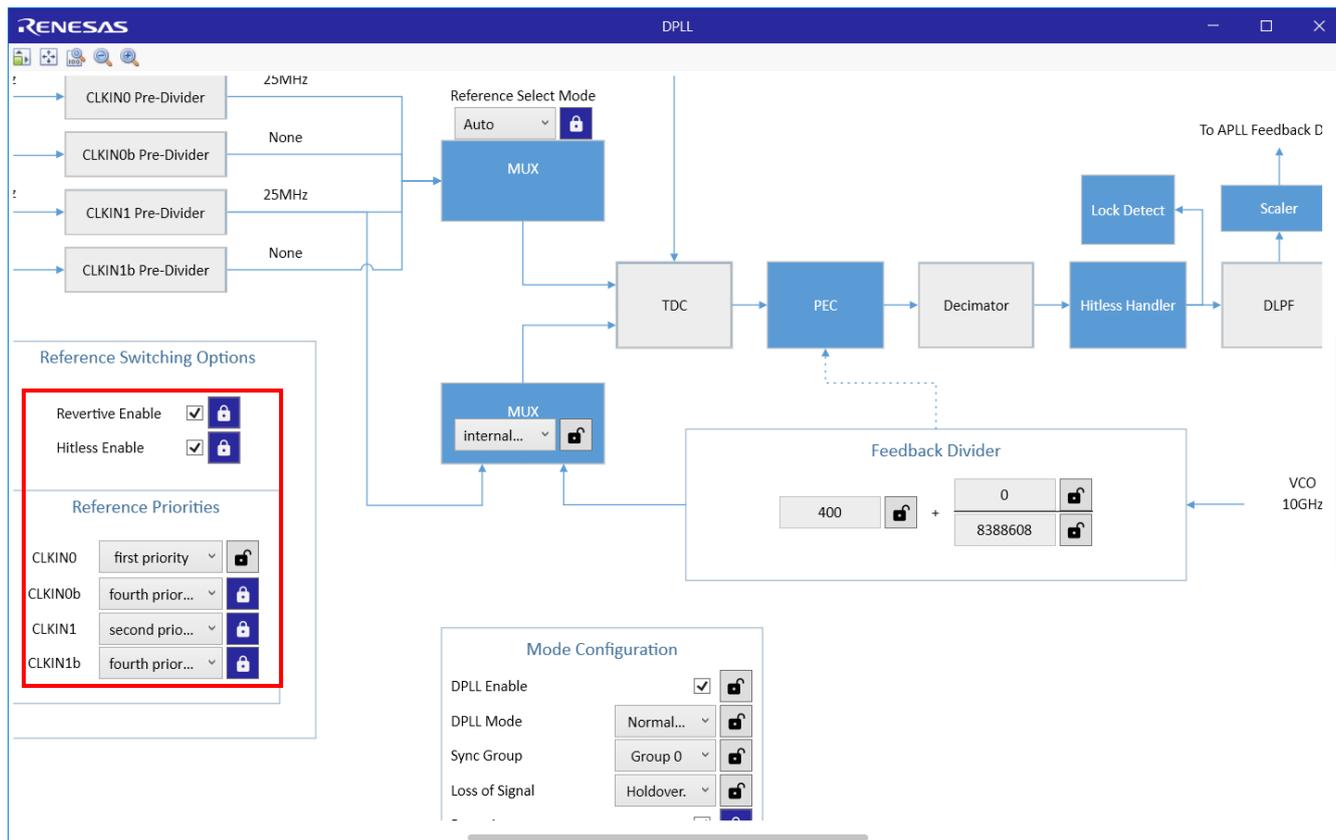
Click on the **DPLL** block to bring up the DPLL sub diagram.



For the **Reference Select Mode**, select **Auto**. This will display the **Reference Switching Options**.

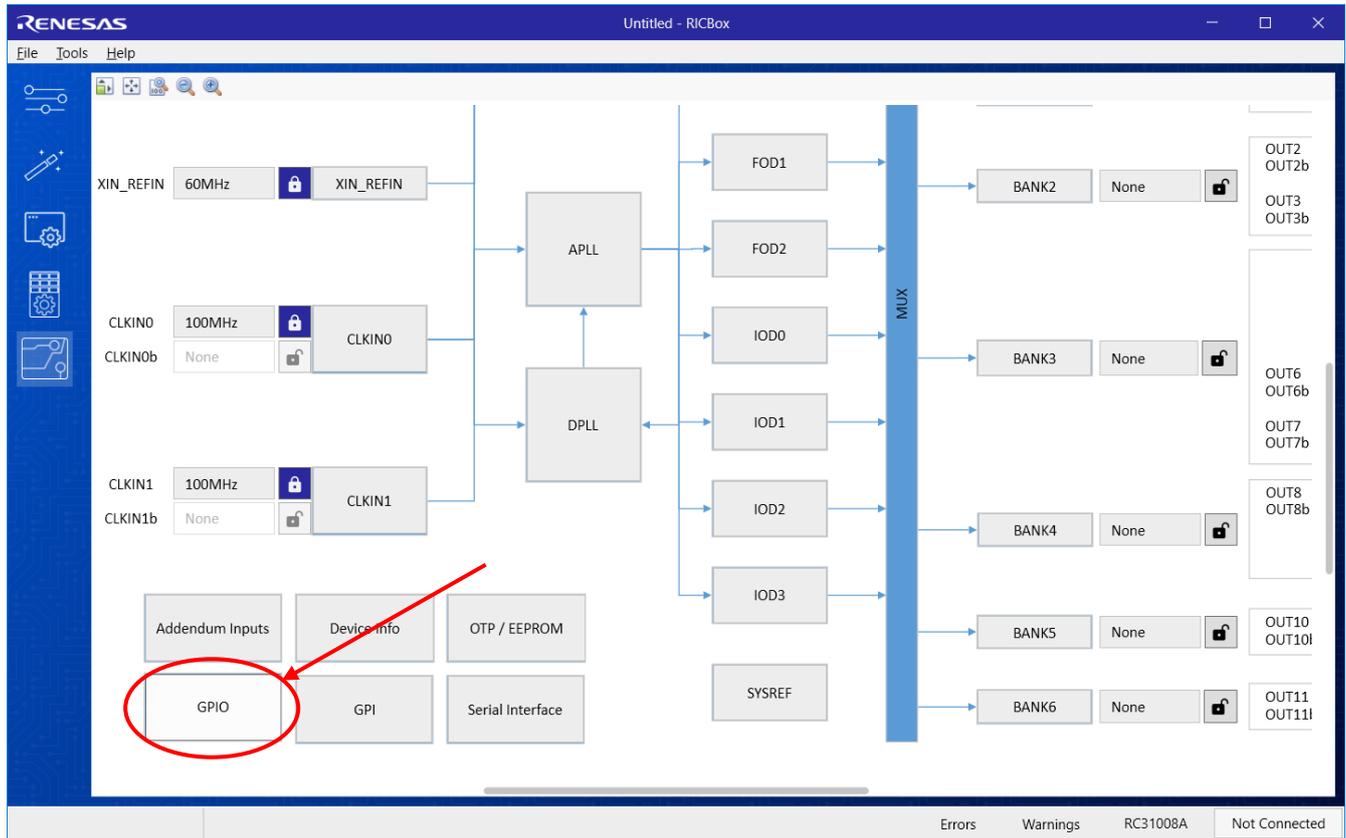


Next, click the boxes for **Revertive Enable** and **Hitless Enable**. Change CLKIN0b and CLKIN1b to **fourth priority**, and CLKIN1 to **second priority**.

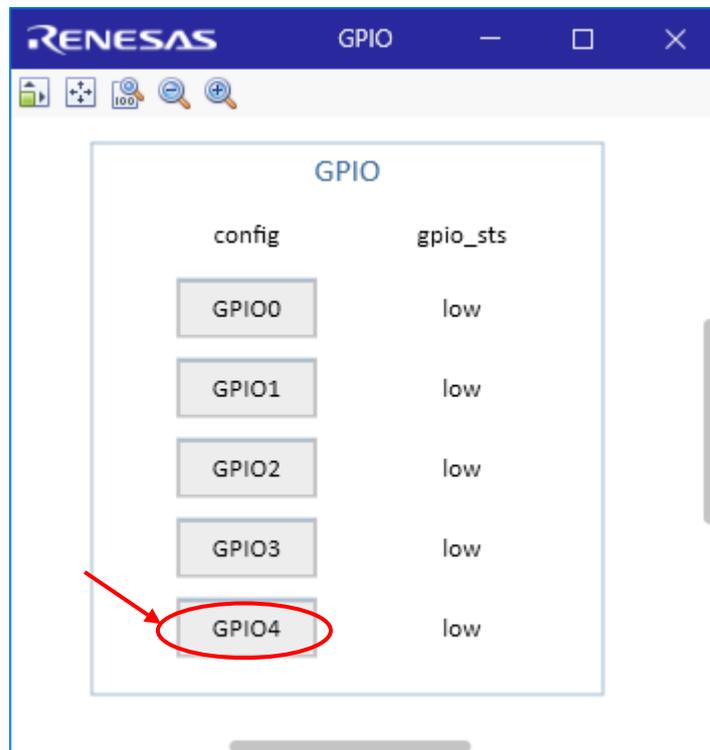


## Appendix C – Setting up GPIO for E5052A External Trigger

For this example, GPIO4 is used as the External Trigger for the E5052A. To configure GPIO4, click the **GPIO** button.

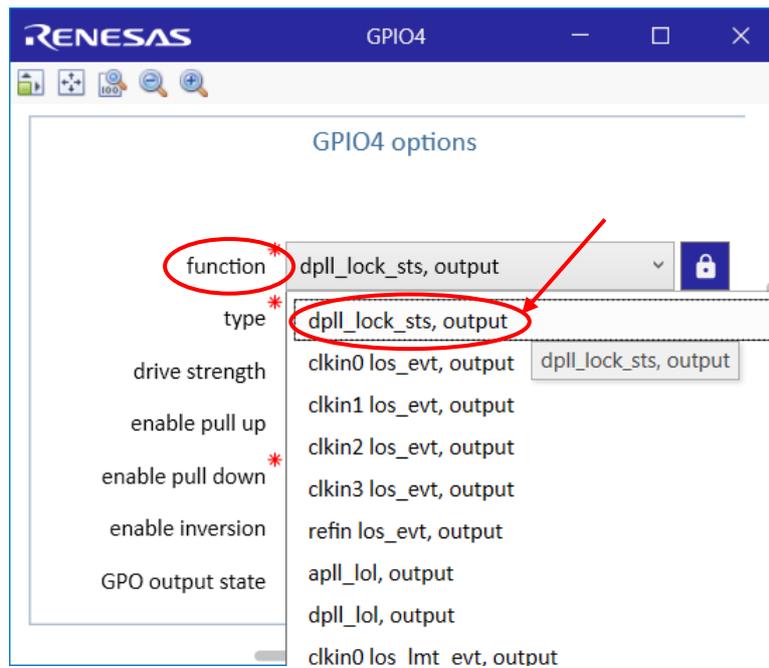


Click the **GPIO4** button.



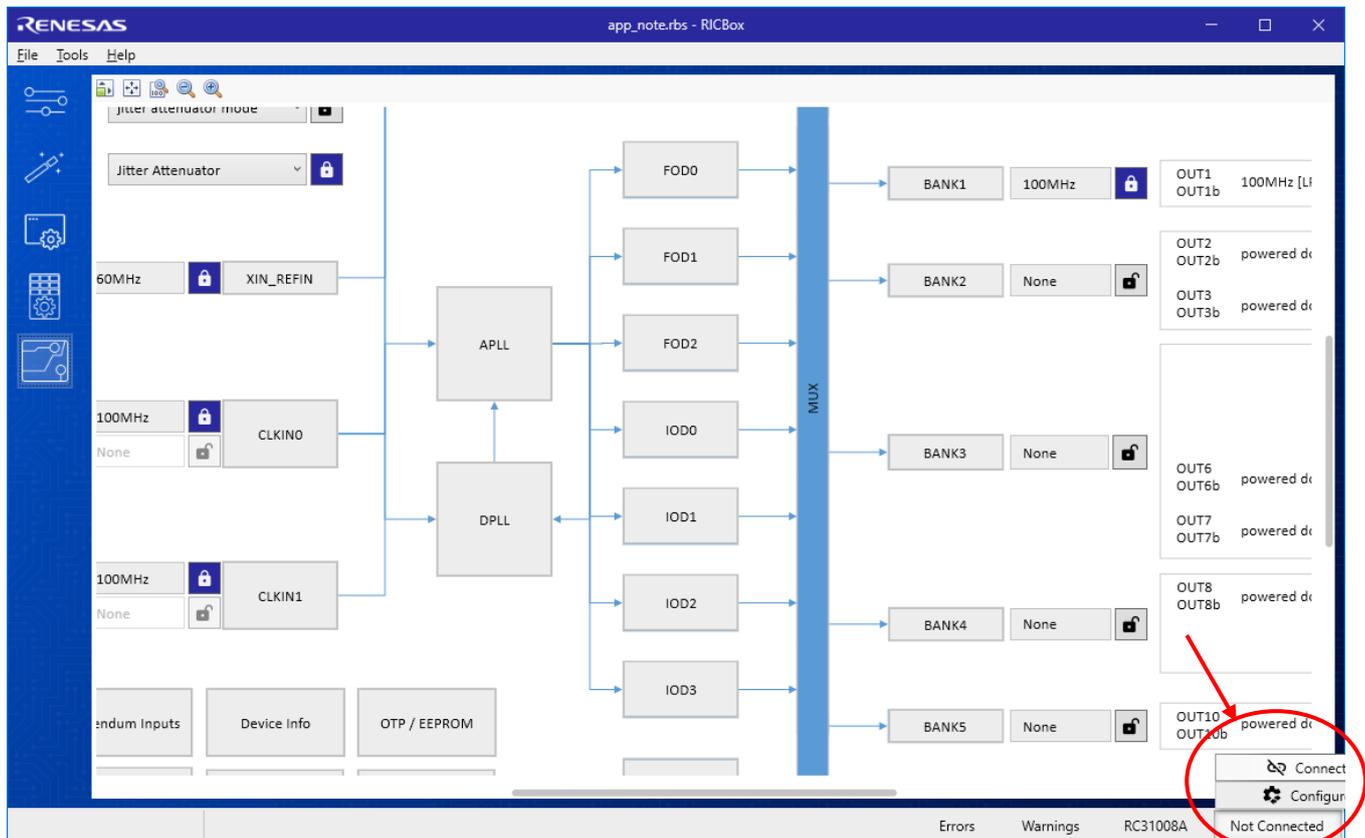
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Find the **function** pull-down list and select 'dpll\_lock\_sts'. Close the GPIO4 window and close the GPIO window.

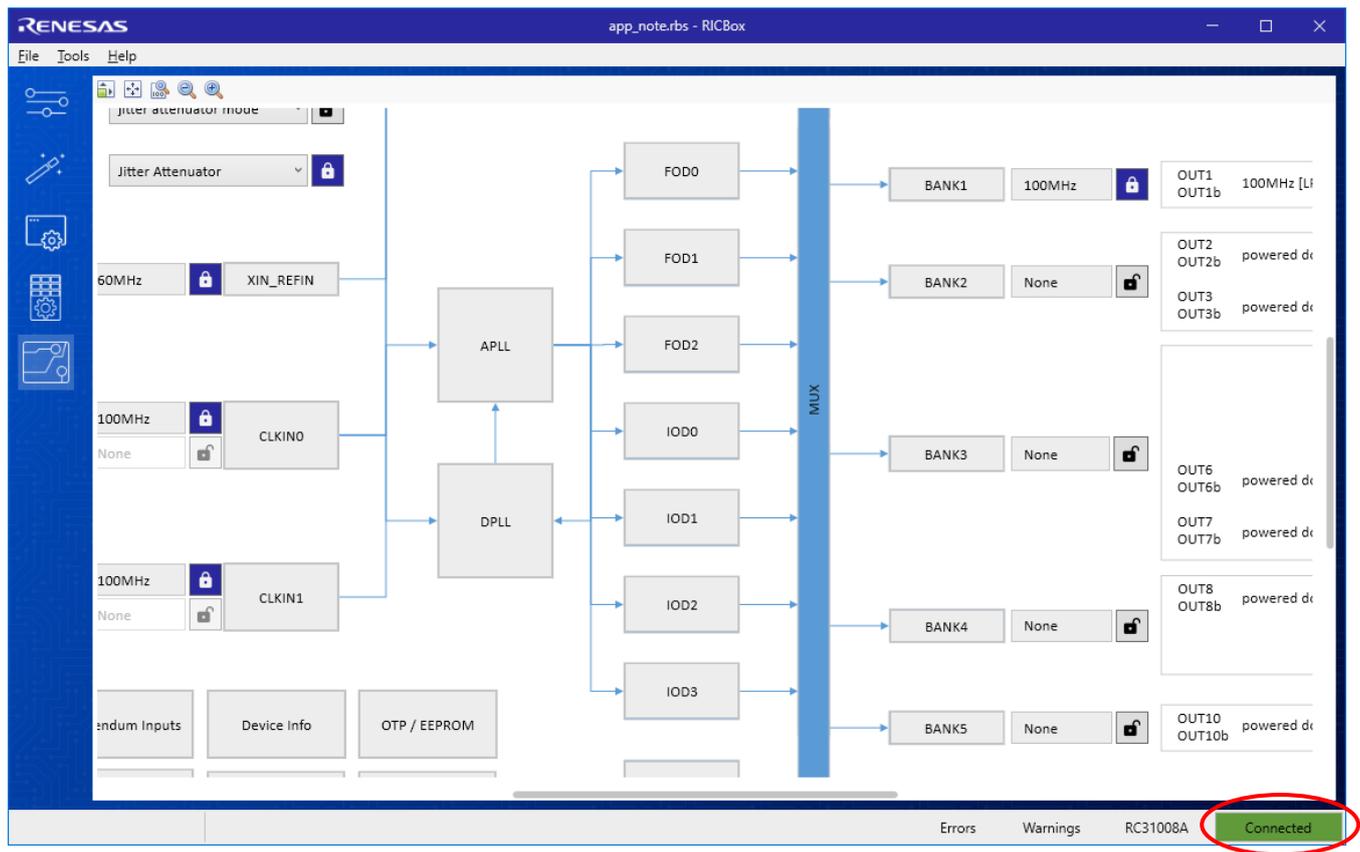


The 'dpll\_lock\_sts' will momentarily go from high to low as the clkln are switching. This transition will be used to trigger the E5052A.

After all settings are entered, click the **Not Connected** button in the lower right of the window and click **Connect**.

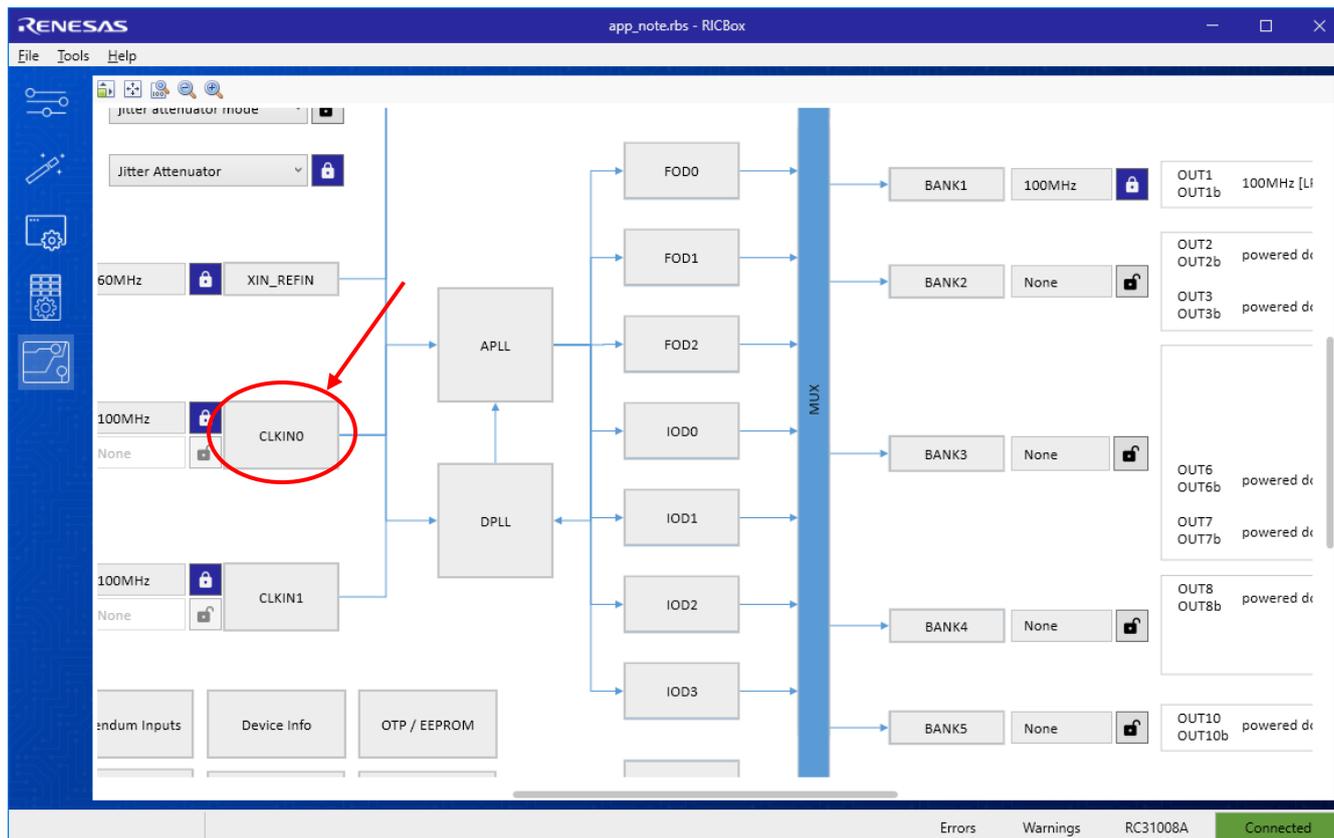


The button will turn **GREEN** and display **Connected**.

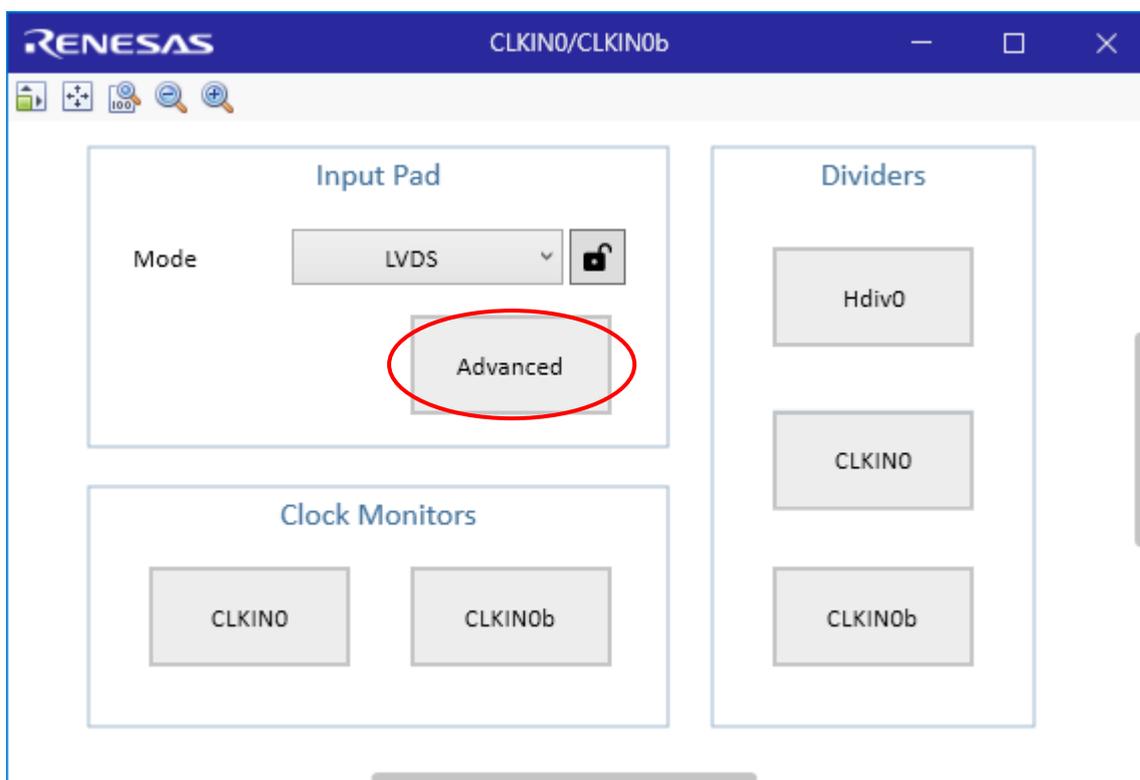


## Appendix D – Confirming Revertive Switching

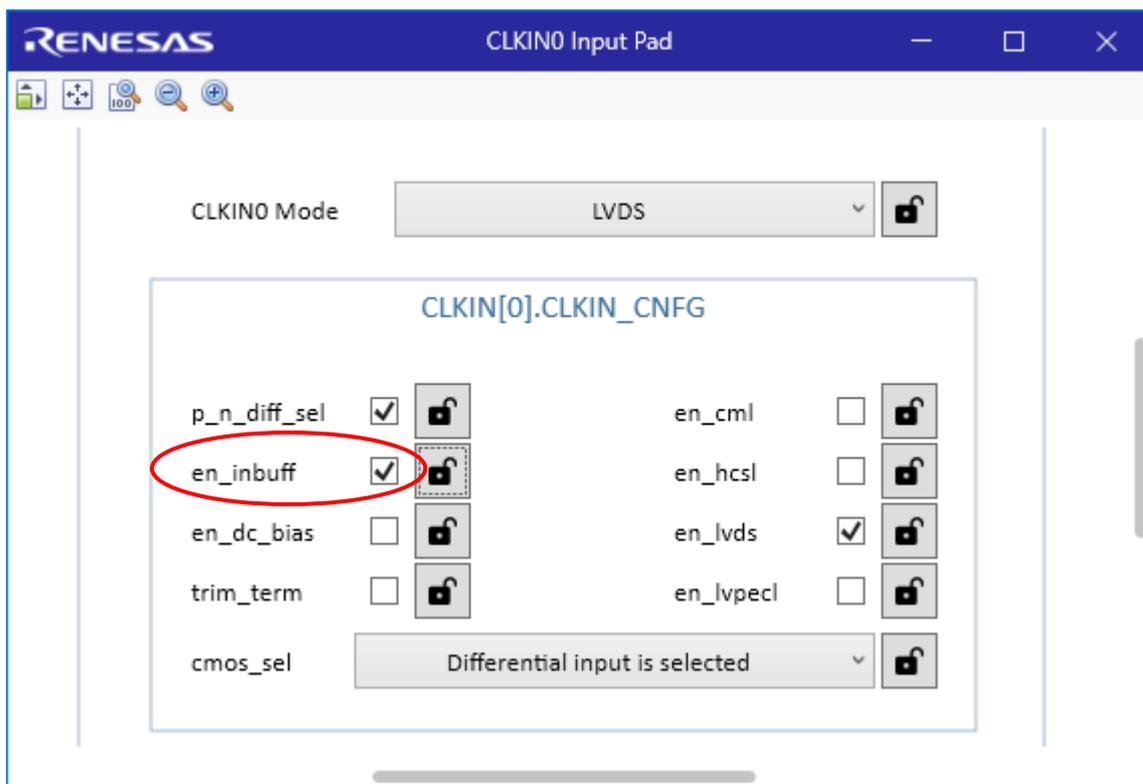
First, click on the **CLKIN0** block.



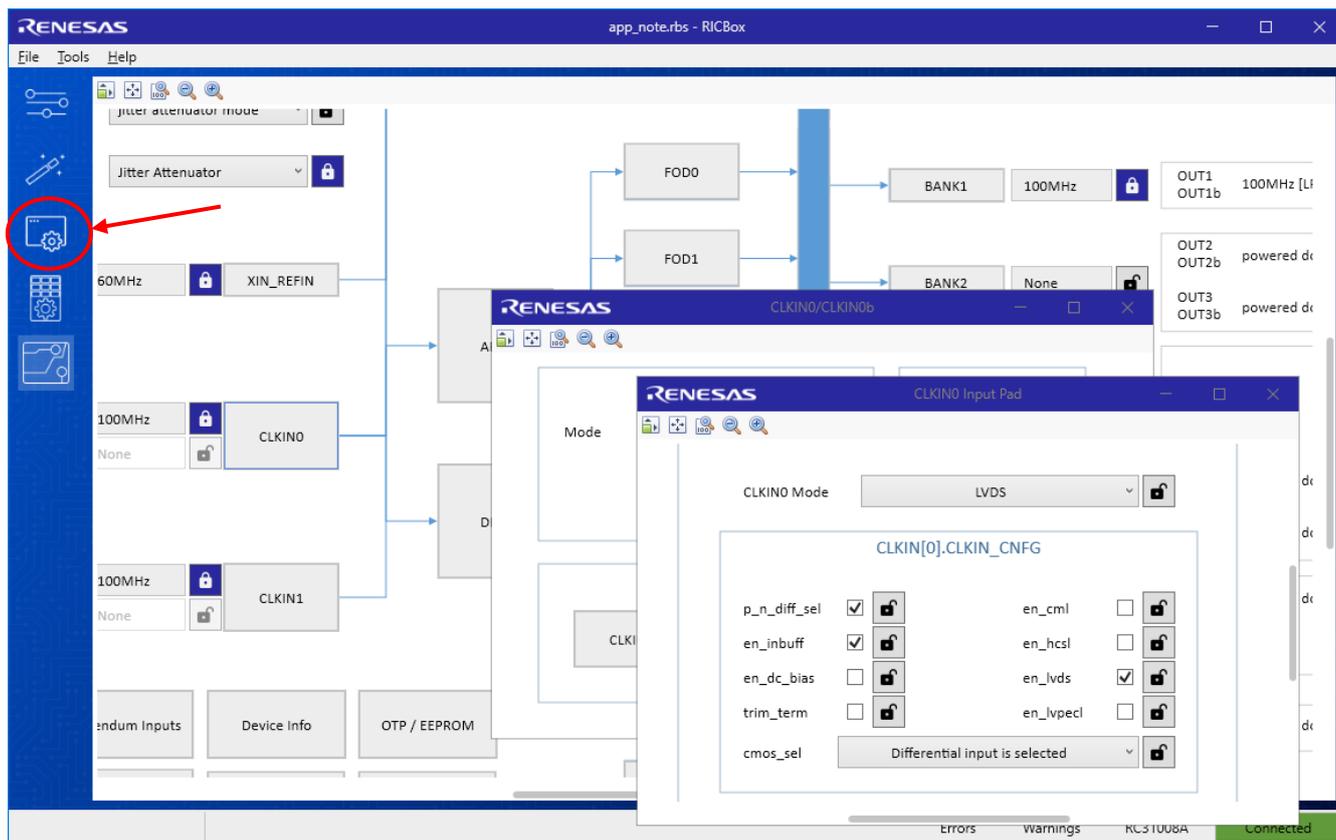
Next, click the **Advanced** button.



The control of interest is called 'en\_inbuff'.

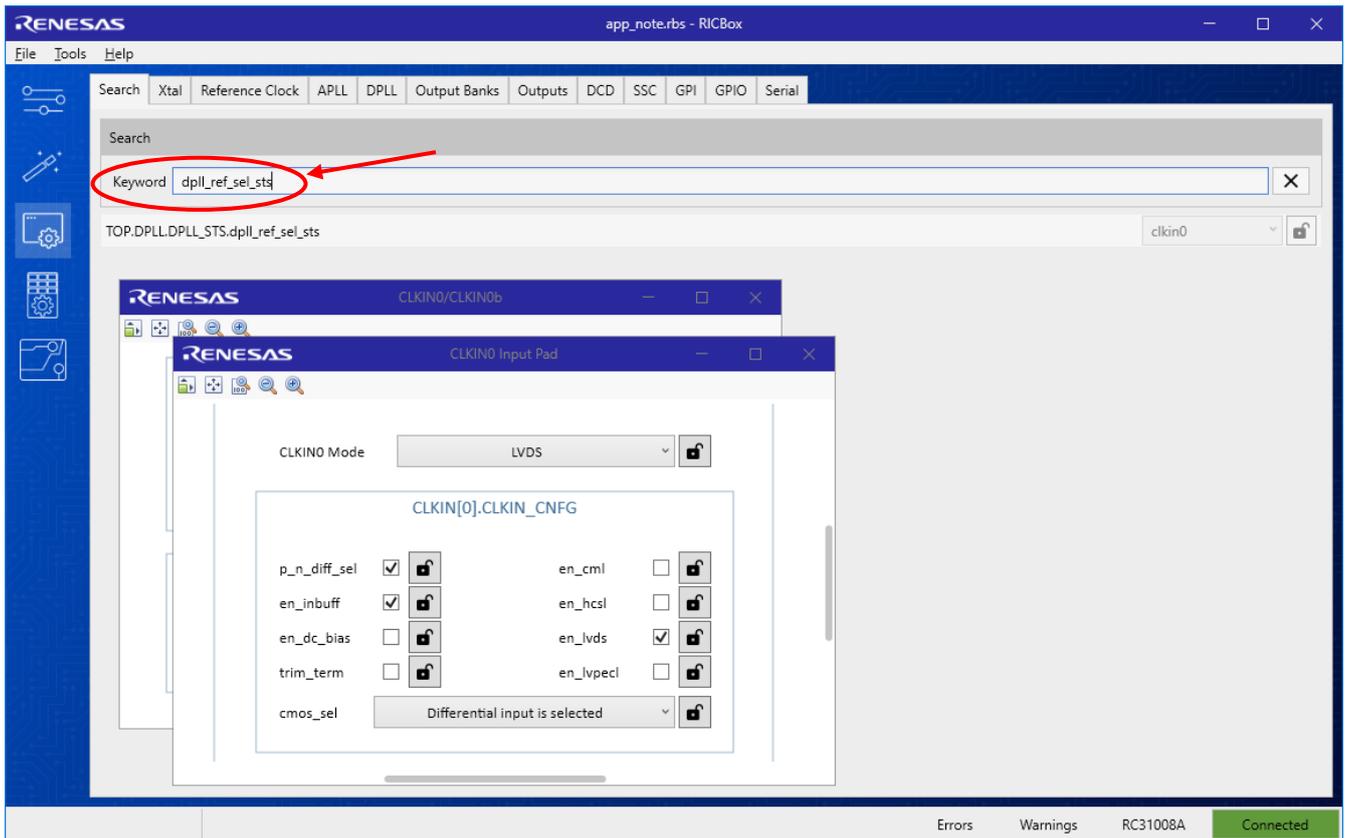


Click the icon shown below to switch over to Configuration view.

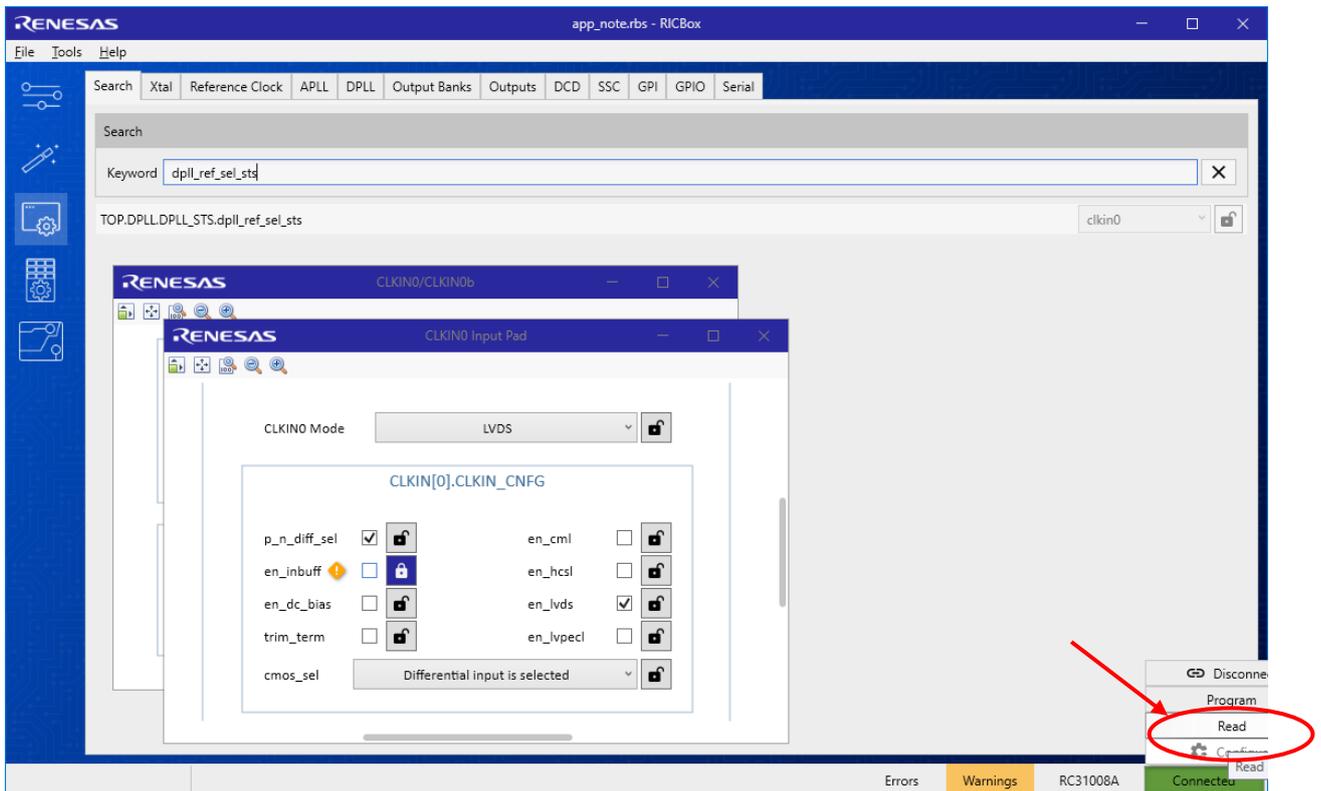


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In the **Keyword** field, enter 'dpll\_ref\_sel\_sts' and click enter. This register field will reflect the current selected reference that the DPLL is using.

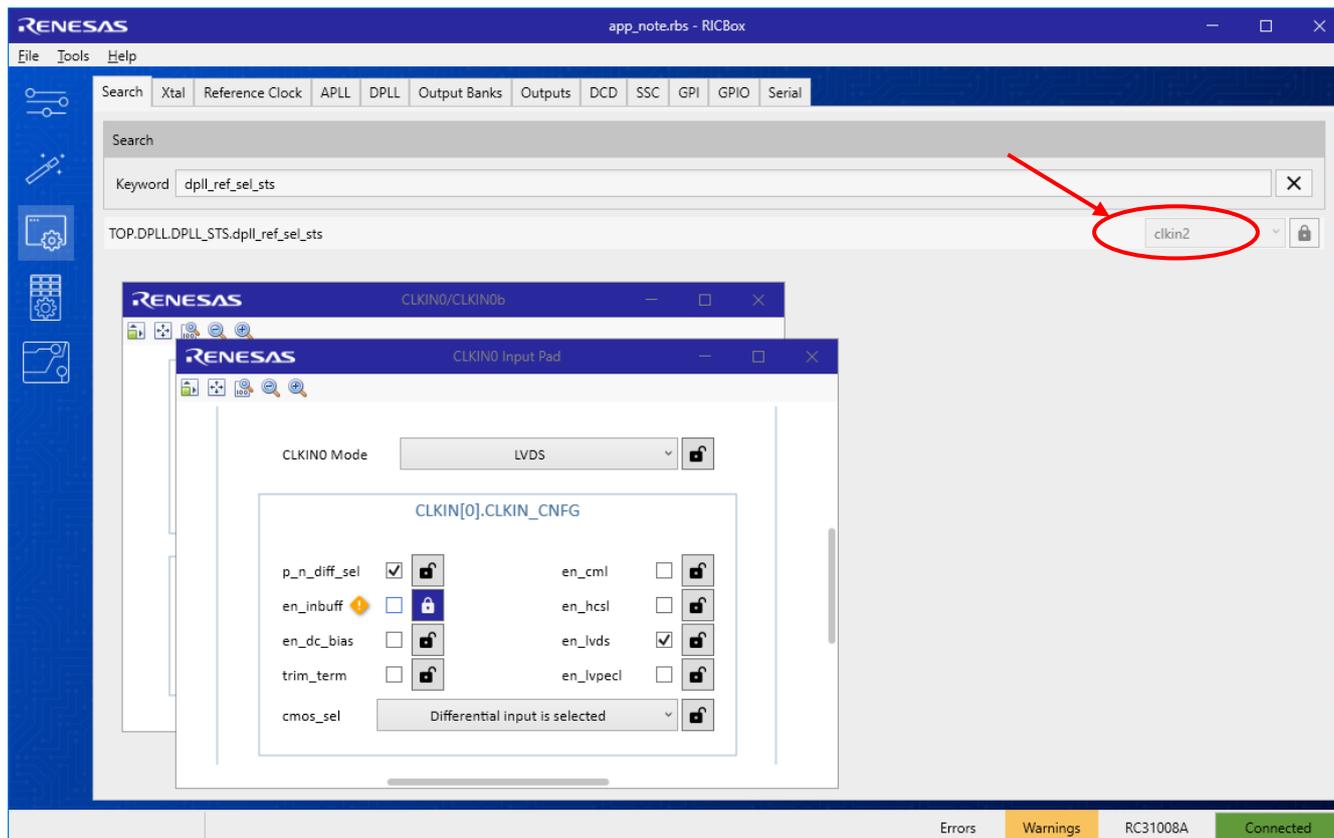


To force a switch, simply un-check 'en\_inbuff' control. An updated transient plot on the E5052A will appear. Now click the green **Connected** button then click **Read**.

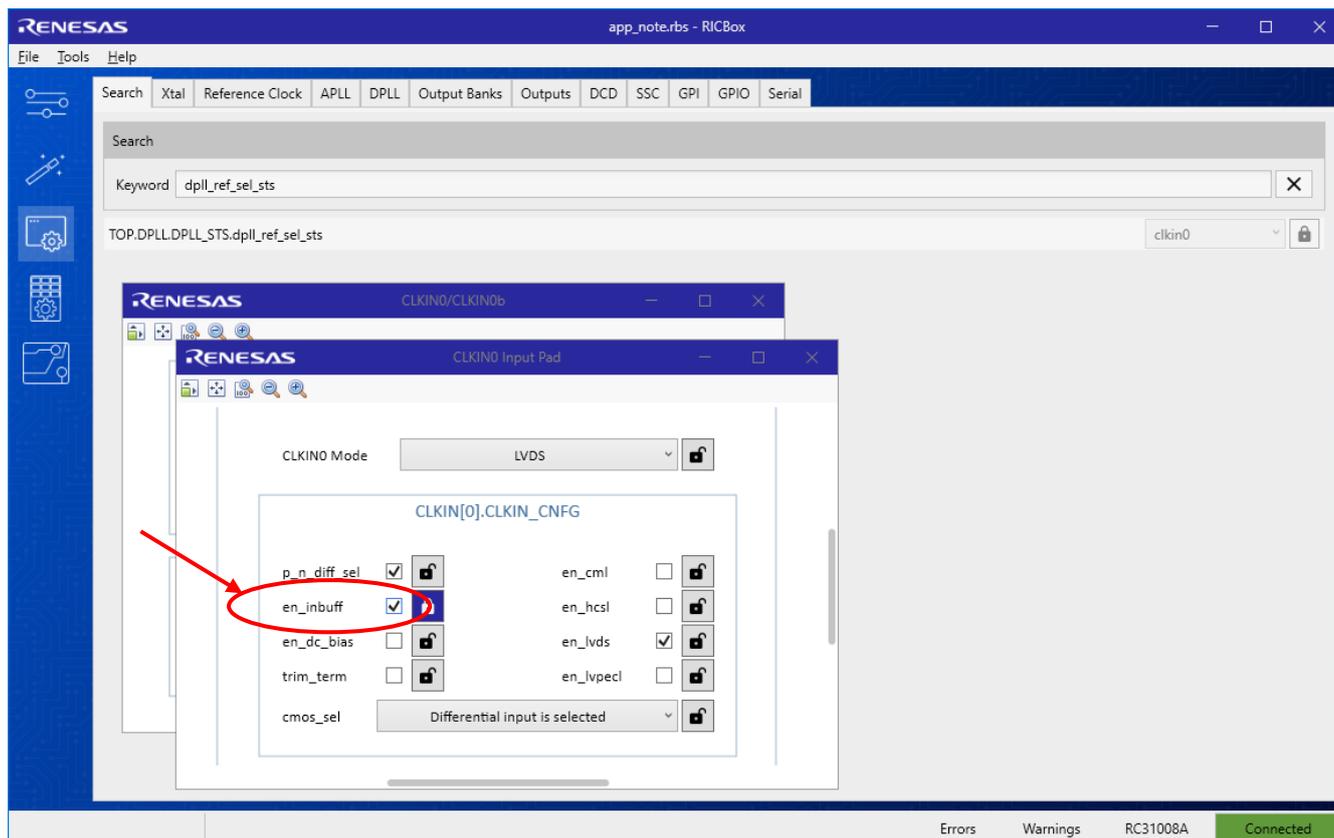


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After clicking **Read**, the status field will be updated.



To cause a revertive switch back, simply check the 'en\_inbuff' control and click **Read**.



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