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H8/300H Tiny Series

Using Timer B1 Interval Timing Function to Increment 8-Bit Counter

Introduction

The interval timer function of timer B1 is used to increment an 8-bit counter in RAM.

Target Device

H8/3687

Contents

1. Specifications

1. The interval timer function of timer B1 is used to increment an 8-bit counter in RAM.
2. A timer B1 interrupt is generated when timer counter B1 (TCB1) overflows, and the counter in RAM is incremented or initialized during the timer B1 interrupt handling.
3. The 8-bit counter in RAM starts from the initial value of H'0x00. When the counter's value becomes H'0xFF, it is initialized to H'0x00 and incrementation resumes.
4. A timer B1 interrupt is set to be generated every 133.072 ms.

2. Description of Functions Used

1. In this sample task, the 8-bit counter is incremented by the interval timer function of timer B1. Figure 2.1 is a block diagram of the interval timer function of timer B1. The elements of the block diagram are described below.

- The system clock (ϕ) is a 16-MHz clock that is used as a reference clock for operating the CPU and peripheral functions.
- Prescaler S (PSS) is a 13-bit counter with clock input of ϕ and is incremented every cycle.
- Timer mode register B1 (TMB1) selects the prescaler and input clock. In this sample task, PSS is selected as the prescaler and division by 8192 is selected as the prescaler division ratio.
- Timer counter B1 (TCB1) is an 8-bit read-only up-counter that is incremented by internal clock input. When TCB1 overflows, the timer B1 overflow interrupt request flag (IRRTB1) in interrupt request register 2 (IRR2) is set to 1.
- Timer counter 0 (TCNT0) is a 16-bit readable/writable up-counter that is incremented by internal or external clock input. In this sample task, TCNT0 is incremented at the rising edge of ϕ/2.
- Timer load register B1 (TLB1) is an 8-bit write-only register. When TLB1 is set during interval timer operation (TMB17 = 0), the TLB1 value is reflected in the TCB1.
- Timer B1 overflow interrupt request flag (IRRTB1) is set to 1 when the TCB1 overflows. A timer B1 interrupt is accepted and timer B1 interrupt handling starts when IRRTB1 is set to 1, the timer B1 interrupt enable (IENTA) of interrupt enable register 1 (IENR1) is set to 1, and the I bit of condition code register (CCR) is cleared to 0.

The TCB1's overflow cycle in this sample task is calculated by the following equation:

$$\text{TCB1 overflow cycle} = \frac{1}{\text{System clock} / 8192} \times 256 = 133.072 \text{ ms}$$

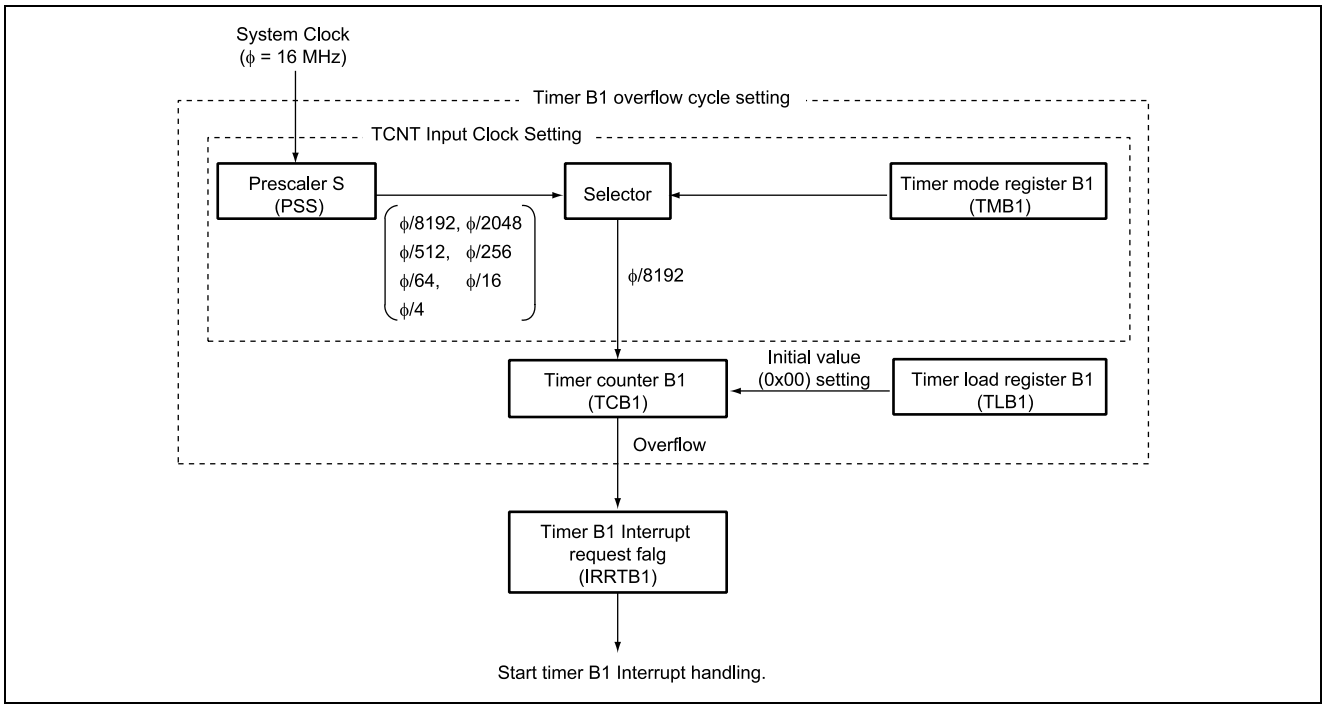


Figure 2.1 Timer B1's Interval Timer Function

2. Table 2.1 lists the function allocation for this sample task. The functions listed in table 2.1 are allocated so that the 8-bit counter is incremented by the interval timer function of timer B1.

Table 2.1 Function Allocation

Function	Description
PSS	13-bit counter with system clock input
TMB1	Selects prescaler (PSS) and sets the prescaler division ratio.
TCB1	8-bit up-counter with clock input of ϕ/8192
TLB1	Sets the initial value of TCB1.
IENTB1	Enables timer B1 interrupt requests
IRRTB1	Indicates whether or not a timer B1 interrupt request is issued

3. Description of Operations

Figure 3.1 shows this sample task's principle of operation. The hardware and software processing shown in figure 3.1 applies the interval timer function of timer B1 to increment the 8-bit counter.

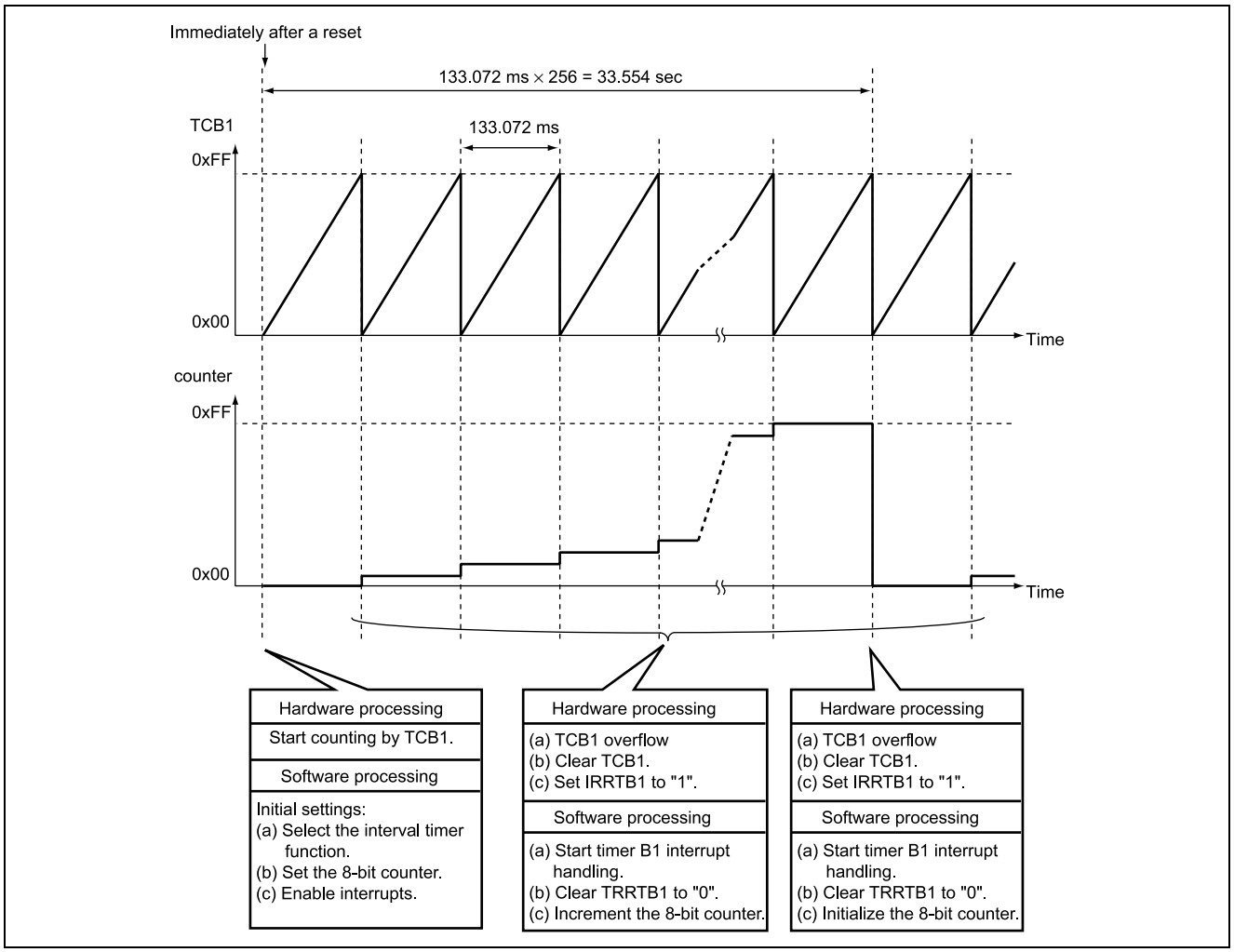


Figure 3.1 Operation Principle

4. Description of Software

4.1 Description of Modules

Table 4.1 describes the modules used in this sample task.

Table 4.1 Description of Modules

Module Name	Label Name	Function
Main routine	main	Selects the interval timer function, sets the 8-bit counter, and enables interrupts.
Count up	tb1int	During the timer B1 interrupt handling routine, increments or initializes the 8-bit counter.

4.2 Description of Arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers

The internal registers used in this sample task are described below.

- TMB1 imer mode register B Address: 0xF760

Bit	Bit Name	Setting	Function
7	TMB17	1	Auto-reload function select TMB17 = 0: Selects the interval timer function TMB17 = 1: Selects the auto-reload function
2	TMB12	TMB12 = 0	Clock select
1	TMB11	TMB11 = 0	TMB12 = 0, TMB11 = 0, TMB10 = 0:
0	TMB10	TMB10 = 0	TCB1 is incremented with internal clock ϕ/8192

- TCB1 Timer counter B1 Address: 0xF761
  Function: 8-bit up-counter which is incremented by internal clock input.
  Setting: —

- TLB1 Timer load register B1 Address: 0xF761
  Function: An 8-bit write-only register. If a value is set in TLB1 during interval timer operation (TMB17 = 0), this value is reflected on TCB1.
  Setting: 0x00

- IENR2 Interrupt enable register 2 Address: 0xFFF5

Bit	Bit Name	Setting	Function
5	IENTB1	1	Timer B1 interrupt request enable: IENTB1 = 0: Disables timer B1 interrupt requests IENTB1 = 1: Enables timer B1 interrupt requests

- IRR2 Interrupt flag register 2 Address: 0xF721

Bit	Bit Name	Setting	Function
5	IRRTB1	0	Timer B1 interrupt request flag: IRRTB1 = 0: Indicates that no timer B1 interrupt is requested. IRRTB1 = 1: Indicates that a timer B1 interrupt is requested.

4.4 Description of RAM

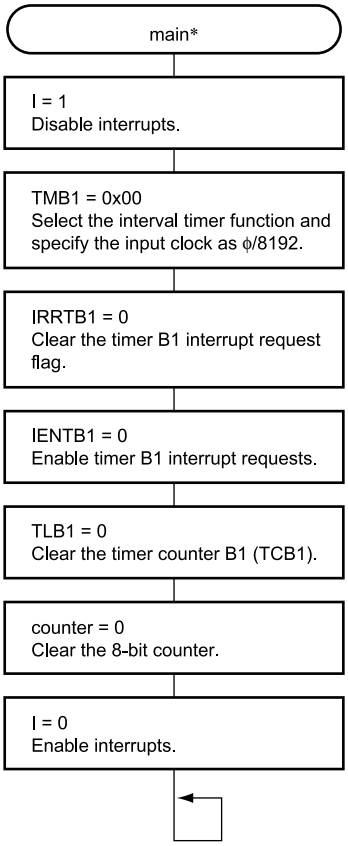
Table 4.2 describes the RAM used in this sample task.

Table 4.2 Description of RAM

Label Name	Function	Size	Used in
counter	8-bit counter	1 byte	Main routine Count up

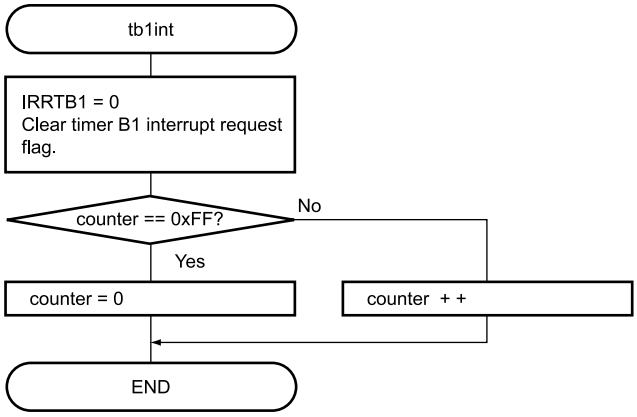
5. Flowchart

1. Main routine



Note: * The stack pointer is specified by INIT.SRC (assembly language).

2. Count up



6. Program List

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*   H8/300HN Series -H8/3687-                                                                                          */
/*   Application Note                                                                                                   */
/*                                                                                                                      */
/*   '8-bit Counter Count-Up by Interval Function'                                                                      */
/*                                                                                                                      */
/*   Function                                                                                                           */
/*   : Timer B1 Interval Timer                                                                                          */
/*                                                                                                                      */
/*   External Clock :         16MHz                                                                                     */
/*   Internal Clock :         16MHz                                                                                     */
/*   Sub Clock :              32.768kHz                                                                                 */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*   Symbol Definition                                                                                                  */
/************************************************************************************************************************/
struct BIT {
     unsigned char   b7:1;                  /* bit7 */
     unsigned char   b6:1;                  /* bit6 */
     unsigned char   b5:1;                  /* bit5 */
     unsigned char   b4:1;                  /* bit4 */
     unsigned char   b3:1;                  /* bit3 */
     unsigned char   b2:1;                  /* bit2 */
     unsigned char   b1:1;                  /* bit1 */
     unsigned char   b0:1;                  /* bit0 */
};

#define        TMB1               *(volatile unsigned char *)0xF760                  /* Timer Mode Register B1            */
#define        TCB1               *(volatile unsigned char *)0xF761                  /* Timer Counter B1                  */
#define        TLB1               *(volatile unsigned char *)0xF761                  /* Timer Load Register B1            */
#define        IENR2_BIT          (*(struct BIT *)0xFFF5)                            /* Interrupt Enable Register 2       */
#define        IENTB1             IENR2_BIT.b5                                       /* Timer B1 Interrupt Enable         */
#define        IRR2_BIT           (*(struct BIT *)0xFFF7)                            /* Interrupt Request Register 2      */
#define        IRRTB1             IRR2_BIT.b5                                        /* Timer B1 Interrupt Request Flag   */

#pragma interrupt   (tb1int)
/************************************************************************************************************************/
/*   Function define                                                                                                    */
/************************************************************************************************************************/
extern void INIT ( void );                                                          /* SP Set                            */
void main ( void );
void tb1int ( void );

/************************************************************************************************************************/
/*   RAM define                                                                                                         */
/************************************************************************************************************************/
volatile unsigned char  counter;                                                    /* 8bit Counter                      */
```

```
/************************************************************************************************************************/
/*   Vector Address                                                                                                     */
/************************************************************************************************************************/
#pragma section     V1                                                          /* VECTOR SECTOIN SET                   */
void (*const VEC_TBL1[])(void) = {                                              /* 0x00 - 0x0f                          */
     INIT                                                                       /* 00 Reset                             */
};
#pragma section     V2                                                          /* VECTOR SECTOIN SET                   */
void (*const VEC_TBL2[])(void) = {
          tb1int                                                                /* 3A Timer B1 Interrupt                */
};

#pragma section                                                                 /* P                                    */
/************************************************************************************************************************/
/*   Main Program                                                                                                       */
/************************************************************************************************************************/
void main ( void )
{
          set_imask_ccr(1);                                                     /* Interrupt Disable                    */

          TMB1 = 0x00;                                                          /* Set Interval Timer                   */
                                                                                /* TCB1 input clock : phi/8192          */
          IRRTB1 = 0;                                                           /* Clear IRRTB1                         */
          IENTB1 = 1;                                                           /* Timer B1 Interrupt Enable            */

          TLB1 = 0x00;                                                          /* Clear TCB1                           */
          counter = 0;                                                          /* Initialize 8bit Counter              */
          set_imask_ccr(0);                                                     /* Interrupt Enable                     */

          while(1);
}

/************************************************************************************************************************/
/*   Timer B1 Interrupt                                                                                                 */
/************************************************************************************************************************/
void tb1int ( void )
{
     IRRTB1 = 0;                                                                /* Clear IRRTB1                         */

          if(counter == 0xFF)                                                   /* 8bit Counter = 0xFF?                 */
               counter = 0;                                                     /* Clear 8bit Counter                   */
          else
               counter++;                                                       /* Increment 8bit Counter               */
}
```

Link Address Setting:

Section Name	Address
CV1	0x0000
CV2	0x003A
P	0x0100
B	0xFB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.29.03	—	First edition issued

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