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H8/300H Super Low Power Series

Using the Auto-reload Timer Function of Timer C to Set an Interrupt Period

Introduction

Using the Timer C auto-reload timer function, this function sets the interval of Timer C interrupts (in this example, the interval is 1.024 ms). This function inverts the output on a pin on every cycle of 250 interrupts generated by Timer C.

Target Device

H8/38099

Contents

1. Specifications

1. Using the Timer C auto-reload timer function, this function generates a Timer C interrupt every 1.024 ms.
2. The number of Timer C interrupts is counted as part of Timer C interrupt handling, and the P92 output is inverted every time 250 have been counted.
3. The interval for the inversion of P92 is 256 ms.
4. Timer counter C (TCC) is set to down-counter.

2. Description of Functions Used

2.1 Block Diagram of Timer C

Figure 1 shows the block diagram of the Timer C auto-reload function.

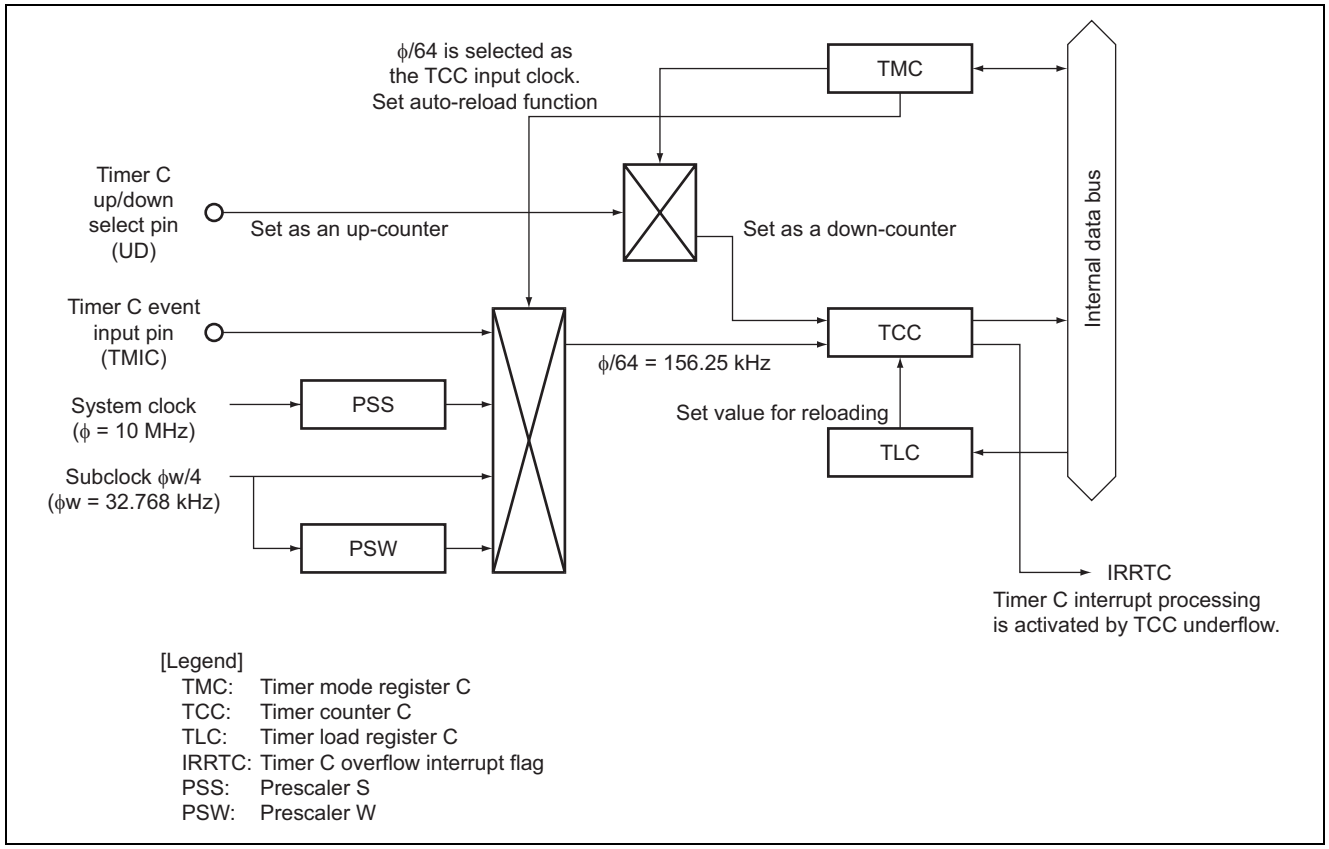


Figure 1 Timer C Function Block Diagram

2.2 Functions Used

2.2.1 Description of Functions

In this sample task, a Timer C interrupt is generated every 1.024 ms using the Timer C auto-reload function. Details of the bits of the individual registers will be explained in section 4.3, “Internal Registers”.

- The system clock (ϕ)
  The system clock (ϕ) is a 10-MHz system clock and is the reference clock for operation of the CPU and its peripheral functions.
- The prescaler S (PSS)
  The prescaler S (PSS) is a 17-bit counter using ϕ as input and counts up every cycle.
- Timer Mode Register C (TMC)
  Timer Mode Register C (TMC) is an 8-bit read/write register used to select the auto-reload function, control selection of counting up or down of Timer Counter C (TCC), and select input clock. That is, it determines whether selection of counting up or down by TCC is controlled by hardware (through the signal level on the UD pin), or if not, whether TCC functions as an up-counter or a down-counter. On a reset, TMC is initialized to H'10.
- Timer Counter C (TCC)
  Timer Counter C (TCC) is an 8-bit read-only up/down counter, which is incremented or decremented by internal clock/external event input. The input clock can be selected from a total of ten clocks, six of which are derived from the system clock divided by 8192, 2048, 512, 64, 16 and 4, three of which are derived from the subclock divided by 1024, 256 and 4, and one of which is the external clock. In this sample task, TCC is set to down-counter, and the system clock/64 is selected as the input clock of TCC.
- Timer Load Register C (TLC)
  Timer Load Register C (TLC) is an 8-bit write-only register and sets reload value for TCC. When a reload value is set in TLC, the same value is loaded into timer counter C as well, and TCC starts counting up/down from that value. When TCC overflows or underflows during operation in auto-reload mode, the TLC value is loaded into TCC. Accordingly, overflow/underflow period can be set within the range of 1 to 256 input clocks. The same address is allocated to TLC as to TCC. Upon reset, TCC is initialized to H'00. In this sample task, TLC is set at H'A0 so that TCC underflows every 1.024 ms.
- Timer C Interrupt Request Flag (IRRTC)
  Timer C Interrupt Request Flag (IRRTC) is set to 1 when TCC underflows. If, on the provision that IRRTC has been set to 1, Timer C Interrupt Enable (IENTC) of the Interrupt Enable Register 2 (IENR2) is set to 1, and the I bit of the Condition Code register (CCR) is cleared to 0, the Timer C interrupt sequence will start on reception of the Timer C interrupt.

2.2.2 Description of the Method of an Interrupt Period Setting by the Timer C Auto-Reload Function

The method for setting an interrupt period by the Timer C auto-reload function is described below. The interrupt period for the Timer C auto-reload function is set by the following formula.

$$\text{Timer C interrupt period (s)} = (\text{TCC input clock period (s)}) \times \text{reload value}$$

The Timer C interrupt period is set by setting the TCC input clock period to TMC and placing the setting for reloading in TLC.

2.2.3 Inversion of the P92 Output Pin

The method of inversion of the P92 output pin is described below.

- In the user RAM area, set up cnt to count the number of Timer C interrupts and CTEDF as a flag to indicate when the number of Timer C interrupts has reached 250.
- Increment cnt in the Timer C interrupt handler; when the value of cnt reaches 250, set CTEDF to 1.
- In the main routine, when CTEDF is 1, set CTEDF to 0, clear cnt, and invert the P92 output.
- Repeat the above process every time the number of Timer C interrupts reaches 250.

2.2.4 Watchdog Timer Function

H8/38099 incorporates a watchdog timer (WDT) that is turned on by default after a reset. The WDT is an 8-bit timer that can generate an internal reset signal when the timer counter overflows because a system crash has prevented the CPU from writing to it. In this sample task, the WDT function is not used, so it is turned off.

- Timer Control/Status Register WD1 (TCSRWD1)
  Timer Control/Status Register WD1 (TCSRWD1) performs TCSRWD1 and TCWD write control. TCSRWD1 also controls the watchdog timer operation and indicates the operating state. TCSRWD1 must be rewritten by using the MOV instruction. Bit-manipulation instructions cannot be used to change the setting.

2.3 Assignment of Functions

Table 1 lists the assignment of functions applicable to this sample task. The functions are assigned as indicated in table 1, and the interrupt period is set by the Timer C auto-reload function.

Table 1 Assignment of Functions

Function	Assignment of Functions
PSS	This is a 17-bit up-counter using the system clock as input
TCC	This is an 8-bit counter using a clock obtained by dividing the system clock by 64 as input
TMC	This is a register for selecting the auto-reload function and input clock, and performing up/down-counter control.
TLC	This sets TCC reload value.
IRRTC	This reflects the presence/absence of a Timer C interrupt request.
IENTC	This enables a Timer C interrupt request.
PCR9	This sets P92 as an output pin.
PDR9	This holds the data for output on pin P92.
P92	Output pin
TCRWD1	This stops the watchdog timer.

3. Principle of Operation

Figure 2 illustrates the principle of operation. As shown in figure 2, setting of the interrupt period by the Timer C auto-reload function is facilitated by both hardware and software operations.

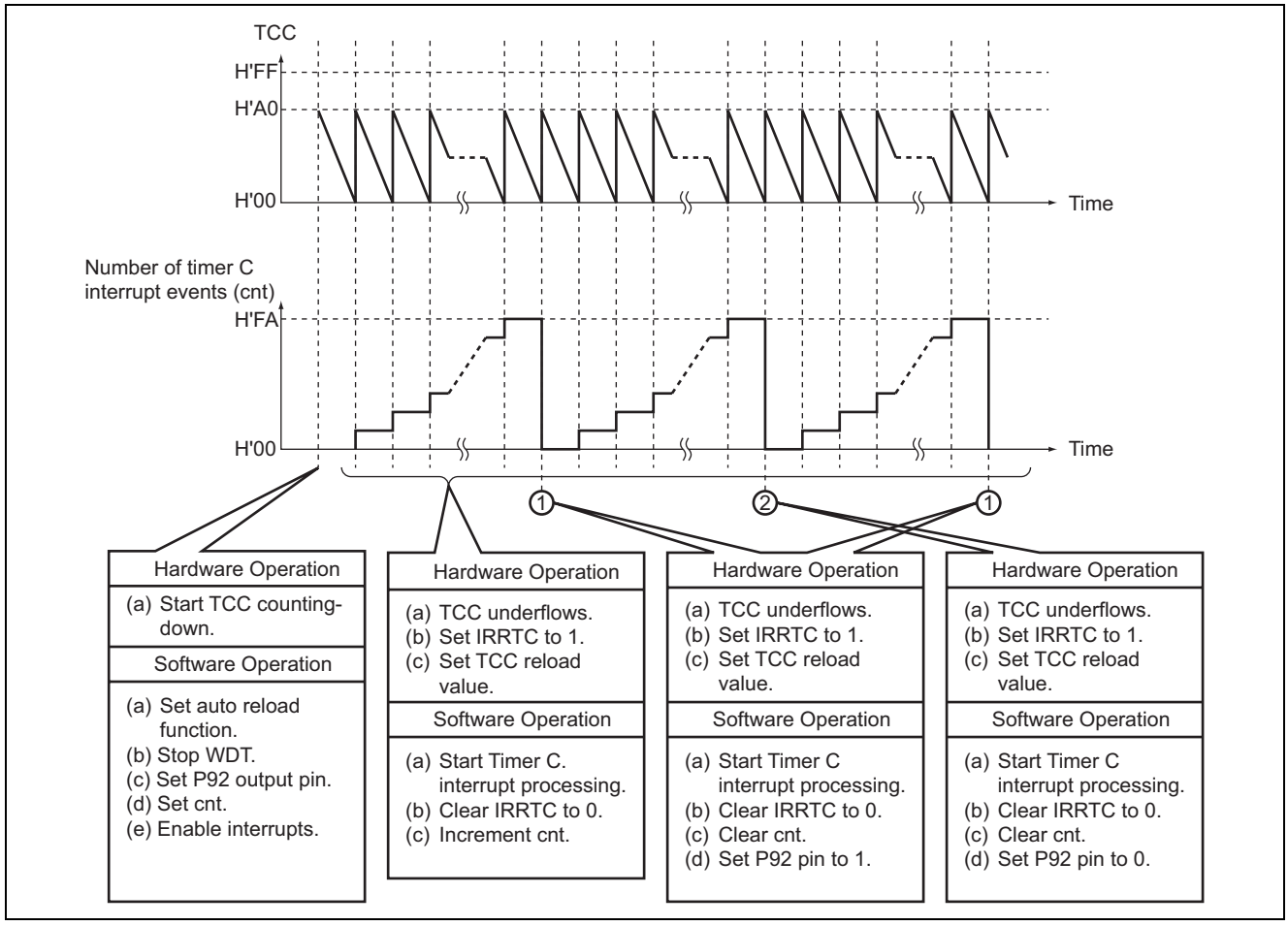


Figure 2 Principle of Operation for Interrupt Period Setting by the Timer C Auto-reload Function

4. Description of Software

4.1 Modules

The modules applicable to this sample task are listed in table 2.

Table 2 Description of Modules

Module Name	Label Name	Function
Main Routine	main	The main routine sets the auto-reload function, P92 pin, and user RAM locations, enables interrupts, and turns LEDs on and off.
Count up	tcint	The Timer C interrupt handler increments cnt. When the value of cnt is H'FA, CTEDF is set to 1.

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers

The following tables list the internal registers used in this sample task.

- Timer Mode Register C (TMC) Address: H'FFFFB4

Bit	Bit Name	Setting Value	R/W	Description
7	TMC7	1	R/W	Auto-Reload Function Select Selects whether timer C is used as an interval timer or auto-reload timer. 0: Interval timer function. 1: Auto-reload function.
6	TMC6	0	R/W	Counter Up/Down Control Selects whether selection of counting up or down by TCC is controlled by hardware (through the signal level on the UD pin) or, if not, whether TCC functions as an up-counter or down-counter. 00: TCC is an up-counter. 01: TCC is a down-counter. 1x: Hardware control through the signal level on the UD pin. UD pin input high: Down-counter. UD pin input low: Up-counter.
5	TMC5	1	R/W	
4	—	1	—	Reserved This bit is always read as 1 and cannot be modified.
3	TMC3	1	R/W	Clock Select TMC3 to TMC0 select the clock input for TCC. For the counting of external events, either the rising or falling edge can be selected. x000: Internal clock counting on ϕ/8192 x001: Internal clock counting on ϕ/2048 x010: Internal clock counting on ϕ/512 x011: Internal clock counting on ϕ/64 x100: Internal clock counting on ϕ/16 0101: Internal clock counting on ϕ/4 0110: Internal clock counting on ϕ_W/1024 1101: Internal clock counting on ϕ_W/256 1110: Internal clock counting on ϕ_W/4 0111: Counting falling edges of external events (TMIC)* 1111: Counting rising edges of external events (TMIC)*
2	TMC2	0	R/W	
1	TMC1	1	R/W	
0	TMC0	1	R/W	

Legend:
x: Don't care

Note: * The TMIC bit in the port mode register E (PMRE) must be set to 1 before the TMC3 to TMC0 bits are set to B'x111.

- Timer Counter C (TCC) Address: H'FFFFB5

Bit	Bit Name	Setting Value	R/W	Description
7	TCC7	—	R	TCC is an 8-bit read-only up/down-counter, which is incremented or decremented by internal clock or external event input. The clock source for input to this counter is selected by bits TMC3 to TMC0 in the timer mode register C (TMC). TCC values can be read by the CPU at any time. When TCC overflows from H'FF to H'00 or to the value set in TLC, or underflows from H'00 to H'FF or to the value set in TLC, the IRRTC bit in IRR2 is set to 1. TCC is allocated to the same address as TLC. Upon reset, TCC is initialized to H'00.
6	TCC6	—	R	
5	TCC5	—	R	
4	TCC4	—	R	
3	TCC3	—	R	
2	TCC2	—	R	
1	TCC1	—	R	
0	TCC0	—	R	

- Timer Load Register C (TLC) Address: H'FFFFB5

Bit	Bit Name	Setting Value	R/W	Description
7	TLC7	1	W	TLC is an 8-bit write-only register for setting the reload value of timer counter C (TCC). When a reload value is set in TLC, the same value is loaded into timer counter C as well, and TCC starts counting up/down from that value. When TCC overflows or underflows during operation in auto-reload mode, the TLC value is loaded into TCC. Accordingly, overflow/underflow period can be set within the range of 1 to 256 input clocks. The same address is allocated to TLC as to TCC. Upon reset, TLC is initialized to H'00.
6	TLC6	0	W	
5	TLC5	1	W	
4	TLC4	0	W	
3	TLC3	0	W	
2	TLC2	0	W	
1	TLC1	0	W	
0	TLC0	0	W	

- Interrupt Enable Register 2 (IENR2) Address: H'FFFFF4

Bit	Bit Name	Set Value	R/W	Description
1	IENTC	1	R/W	Timer C Interrupt Request Enable The timer C interrupt request is enabled when this bit is set to 1.

- Interrupt Request Register 2 (IRR2) Address: H'FFFFF7

Bit	Bit Name	Setting Value	R/W	Description
1	IRRTC	1	R/W	Timer C Interrupt Request Flag [Setting condition] • The timer C overflow or underflow occurs. [Clearing condition] • Writing of 0 to this bit

- Port Control Register 9 (PCR9) Address: H'FFFFEC

Bit	Bit Name	Setting Value	R/W	Description
2	PCR92	1	W	Setting PCR9 to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCR9 and PDR9 are valid when the corresponding pin is designated as a general I/O pin. PCR9 is a write-only register. PCR92 is always read as 1.

- Port Data Register 9 (PDR9) Address: H'FFFFDC

Bit	Bit Name	Setting Value	R/W	Description
2	P92	0/1*	R/W	When port 9 is read while PCR9 is set to 1, the value stored in PDR9 is read, regardless of the actual pin state. When port 9 is read while PCR9 is cleared to 0, the pin state is read.

Note: * This bit is toggled every second by the timer C interrupt handling routine.

- Timer Control/Status Register WD1 (TCSRWD1) Address: H'FFF03B

Bit	Bit Name	Setting Value	R/W	Description
7	B6WI	1	R/W	Bit 6 Write Inhibit The TCWE bit can be written only when the write value of the B6WI bit is 0. This bit is always read as 1.
6	TCWE	0	R/W	Timer Counter WD Write Enable TCWD can be written when the TCWE bit is set to 1. When writing data to this bit, the write value for bit 7 must be 0.
5	B4WI	*	R/W	Bit 4 Write Inhibit The TCSRWE bit can be written only when the write value of the B4WI bit is 0. This bit is always read as 1.
4	TCSRWE	*	R/W	Timer Control/Status Register WD Write Enable The WDON and WRST bits can be written when the TCSRWE bit is set to 1. When writing data to this bit, the write value for bit 5 must be 0.
3	B2WI	*	R/W	Bit 2 Write Inhibit The WDON bit can be written only when the write value of the B2WI bit is 0. This bit is always read as 1.
2	WDON	*	R/W	Watchdog Timer On TCWD starts counting up when this bit is set to 1 and halts when the WDON bit is cleared to 0. [Setting condition] • A reset is made • When 1 is written to the WDON bit and 0 to the B2WI bit while the TCSRWE bit is 1. [Clearing condition] • When 0 is written to the WDON bit and 0 to the B2WI bit while the TCSRWE bit is 1.
1	B0WI	1	R/W	Bit 0 Write Inhibit The WRST bit can be written only when the write value of the B0WI bit is 0. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Setting condition] • When TCWD overflows and an internal reset signal is generated [Clearing conditions] • Reset by $\overline{\text{RES}}$ pin • When 0 is written to the WRST bit and 0 to the B0WI bit while the TCSRWE bit is 1

Note: * These bits are manipulated so as to stop the watchdog timer. See the flowchart for the main routine.

4.4 RAM Usage

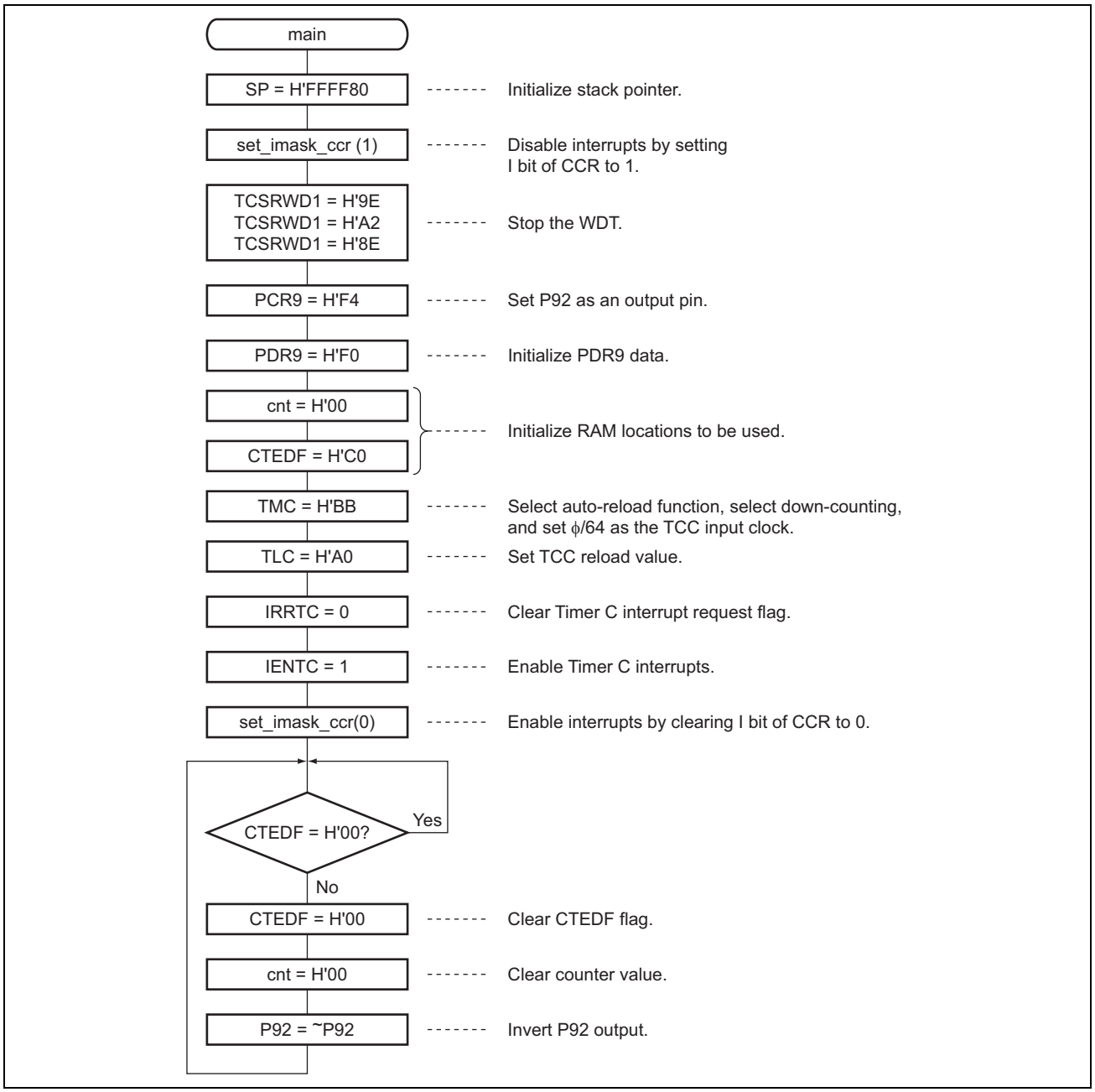
Table 3 lists and describes the RAM usage in this sample task.

Table 3 RAM Usage

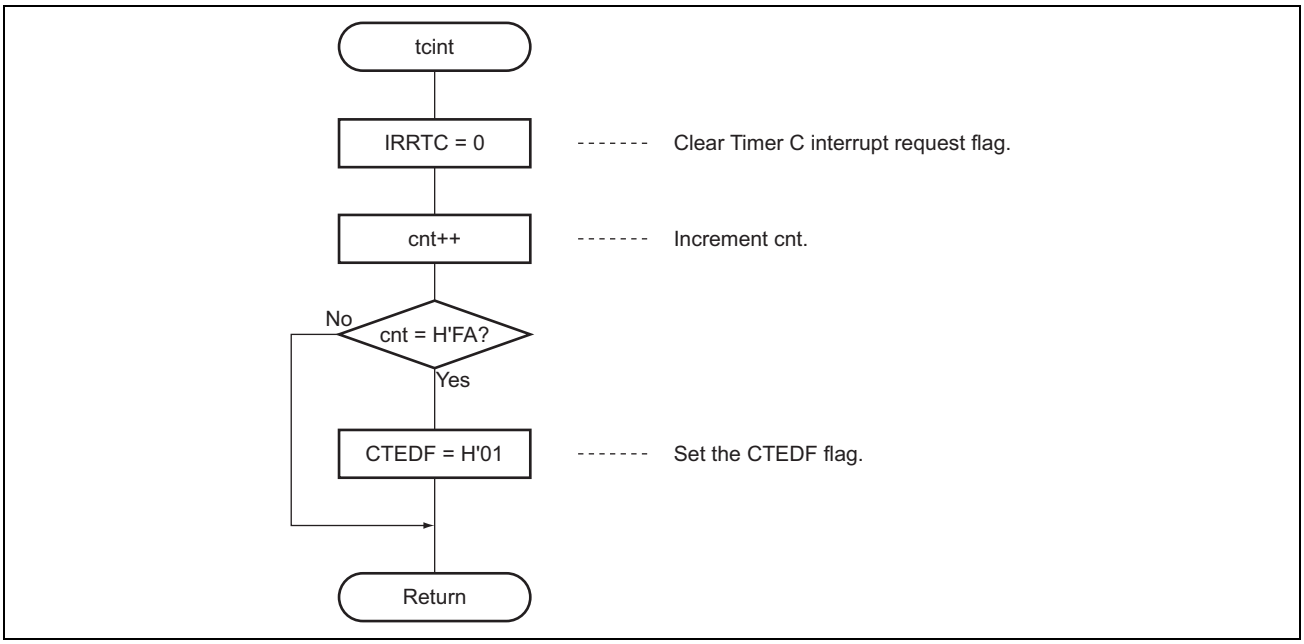
Type	Label Name	Description	Used in
unsigned char	cnt	Counts how many times Timer C interrupts are processed.	main
unsigned char	CTEDF	Flag used to indicate whether or not the value of cnt has reached H'FA When cnt < H'FA: CTEDF = H'00. When cnt = H'FA: CTEDF = H'01.	main, tcint

5. Flowcharts

5.1 Function main



5.2 Function tcint



6. Link Address Specifications

Section Name	Address
CV1	H'000000
CV2	H'0000D4
P	H'000800
B	H'FFF380

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