

IGBT

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Usage Notes for Paralleled IGBT

Introduction

This application note explains important information related to the use of multiple IGBTs in parallel connection.

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1. Outline

Multiple IGBTs are often used in parallel connection in order to increase the power of a system and reduce IGBT loss. When doing so, it is important to equalize the current flowing through in each device and give consideration to issues such as variations in device characteristics, symmetry of board layout, and gate drive circuits. If the current is in an unbalanced state and concentrated in only some of the devices, those devices may incur an excessive loss and eventually break down. Problems occurring with use of paralleled IGBTs can be categorized into two types: problems while the IGBTs are conducting (steady state) and problems while the IGBTs are switching (transient state). The causes of these problems differ and therefore require individual solutions. Table 1 lists precautions for use of paralleled IGBT.

Table 1. Precautions for Using Paralleled IGBTs

	Steady State (during IGBT conduction)	Transient State (during IGBT switching)
Circuit attributes	<ul style="list-style-type: none"> • Board layout symmetry (resistance component) • Thermal coupling of parallel devices 	<ul style="list-style-type: none"> • Board layout symmetry (inductance component) • Gate oscillation
IGBT attributes	<ul style="list-style-type: none"> • $V_{CE(sat)}$ variation • $V_{CE(sat)}$ temperature dependency 	<ul style="list-style-type: none"> • $V_{GE(th)}$ variation

2. Usage Notes for Operations in Steady State

When the IGBT is conducting, the difference in $V_{CE(sat)}$ of the devices connected in parallel and the difference in resistance between the board and the wiring causes unbalance in the collector current. Figure 1 shows the circuit diagram of two IGBTs connected in parallel and the waveform when the collector current is unbalanced in the steady state. This current unbalance causes a difference in device loss in the steady state, and also affects transient loss as it causes the current value during switching to fluctuate as well. Therefore, it is important to select devices of the same production lot, minimize the difference in $V_{CE(sat)}$, and design a symmetrical layout of parallel circuit connections. In addition, the current unbalance is $V_{CE(sat)}$ temperature dependent.

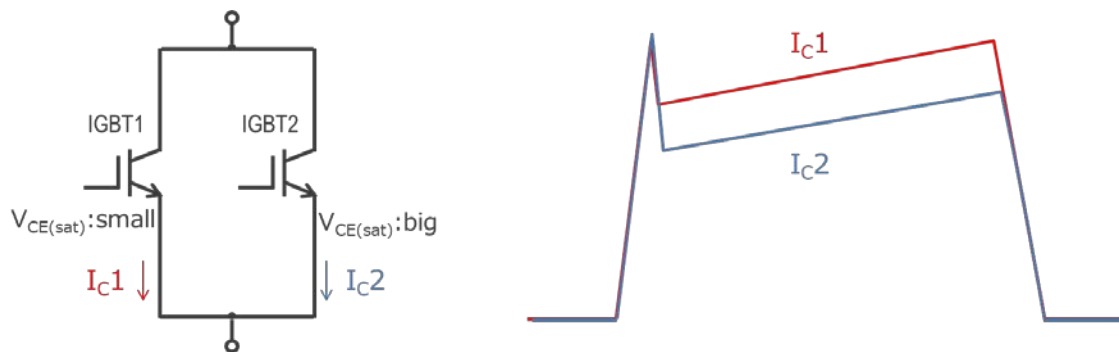


Figure 1. Circuit Diagram of 2 Paralleled IGBTs and Current Unbalance Waveform in Steady State

2.1 Current Unbalance in Steady State Caused by $V_{CE(sat)}$ Variation

IGBTs with different $V_{CE(sat)}$ will also have different output characteristics. As an example, Figure 2 shows a circuit diagram of two IGBTs with differing $V_{CE(sat)}$ connected in parallel, and output characteristics of each IGBT. For the $V_{CE(sat)}$ voltage of each device in the parallel circuit to be equivalent, the operating voltage must be the same value (V_x). Since the collector current value of IGBT1 is I_{C1} and IGBT2 is I_{C2} , the difference in values causes a current unbalance. In this case, IGBT1, which has the lower $V_{CE(sat)}$, has a larger current, and IGBT2, with the higher $V_{CE(sat)}$, has a smaller current.

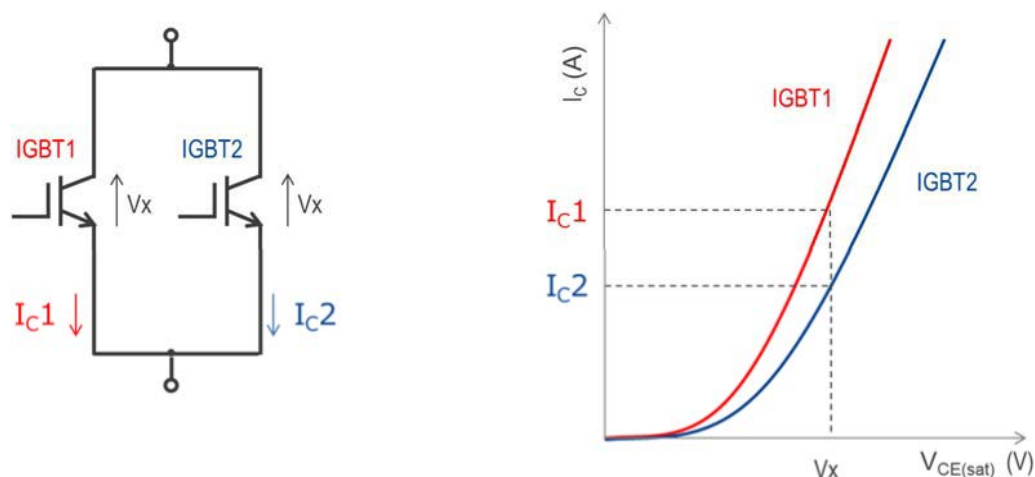


Figure 2. Circuit Diagram of 2 Paralleled IGBTs of Differing $V_{CE(sat)}$ and Output Characteristic Curve

As a countermeasure for current unbalance triggered by $V_{CE(sat)}$ variation, it is important to suppress the $V_{CE(sat)}$ difference to a minimum. Figure 3 shows $V_{CE(sat)}$ dispersion data for the 8th generation RBN50H65T1FPQ. When production lots differ, variation of lot is shown within the SPEC value range, but variation can be minimized by using devices of the same lot. Therefore, when using IGBTs in a parallel operation, it is essential that you use devices of the same production lot to keep the $V_{CE(sat)}$ difference at a minimum.

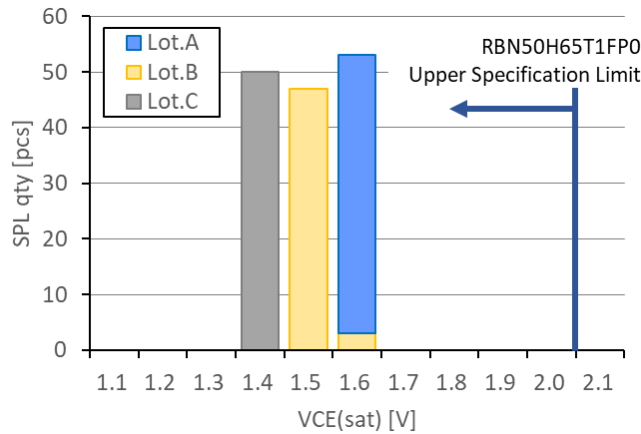


Figure 3. $V_{CE(sat)}$ distribution of RBN50H65T1FPQ (Measurement conditions: $V_{GE}=15V$, $I_C=50A$, $T_C=25^{\circ}C$)

2.2 Current Unbalance in Steady State Caused by Asymmetry of Substrate and Wiring

Parasitic resistance exists in the board and wiring paths. For example, consider a case in which two IGBT of the same $V_{CE(sat)}$ are connected in parallel, and parasitic resistances R_{c1} , R_{e1} , R_{c21} , R_{c22} , R_{e21} , and R_{e22} exist in each wiring. The circuit diagram and output characteristics of each device in this case are shown in Figure 4. The voltage-current characteristic for each device is a combination of the characteristics of the IGBT and the influence of the parasitic resistance, so a difference appears in the voltage-current characteristics in each device. In this circuit, the sum of the voltage drop in IGBT1 and the sum of the voltage drop in IGBT2 are equivalent and operate with V_x . Therefore, the current value that flows through IGBT1 is I_{c1} , and the current value that flows through IGBT2 is I_{c2} . The values differ between the two IGBTs, which causes a current unbalance. In this case, IGBT1 side with the lower resistance, has the larger current(I_{c1}), IGBT2 has the larger resistance so the smaller current(I_{c2}).

To prevent this from occurring, it is essential to design the board layout symmetrically so that paths operate in parallel and to ensure that parasitic resistance is equal.

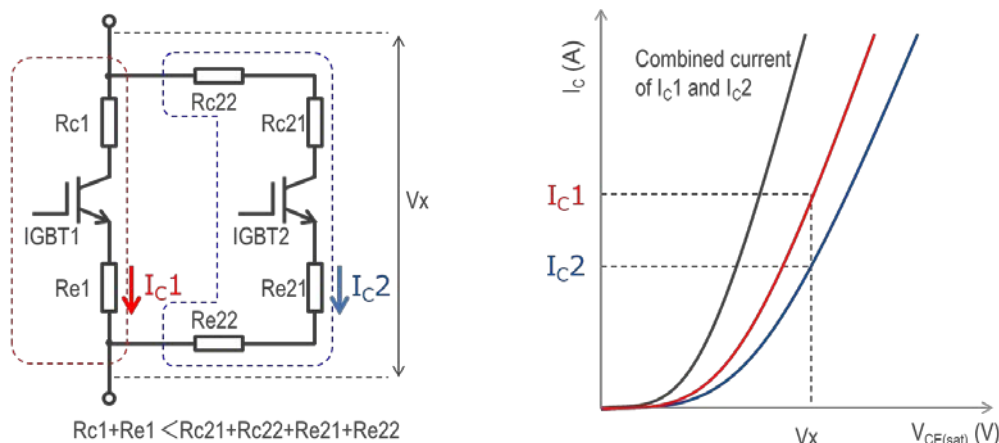


Figure 4. Circuit Diagram and Output Characteristics Curves when Parasitic Resistance Exists

Current unbalance can also be caused due to the position of the emitter-sense of the gate driver when driving IGBTs in parallel. Figure 5 shows a circuit diagram for when two devices of the same $V_{CE(sat)}$ are connected in parallel and the gate driver emitter-sense is connected at point A. However, we must consider IGBT2 when the resistance on the emitter side is larger than IGBT1. In this circuit, the voltage applied directly between the IGBT gate emitters is the value of the gate driver output voltage less the voltage drop from the IGBT emitters and point A. Gate-emitter voltages V_{GE1} and V_{GE2} , which are applied to IGBT1 and IGBT2, can be expressed in the following equations.

$$V_{GE1} = V_{dr} - I_{C1} \times (R_{e1})$$

$$V_{GE2} = V_{dr} - I_{C2} \times (R_{e21} + R_{e22})$$

When the gate-emitter voltage applied to an IGBT decreases, the output characteristic changes in the direction in which the IGBT $V_{CE(sat)}$ increases. Accordingly, the IGBT gate-emitter voltage becomes $V_{GE1} > V_{GE2}$, causing a current unbalance of $I_{C1} > I_{C2}$.

As a countermeasure, connect each IGBT emitter wiring and corresponding emitter-sense symmetrically, making sure that the same gate voltage is applied to each IGBT. It is also important to reduce the parasitic resistance between the emitter and the driver connection point by shortening the wiring on the emitter side so that the desired gate voltage is applied to the IGBT.

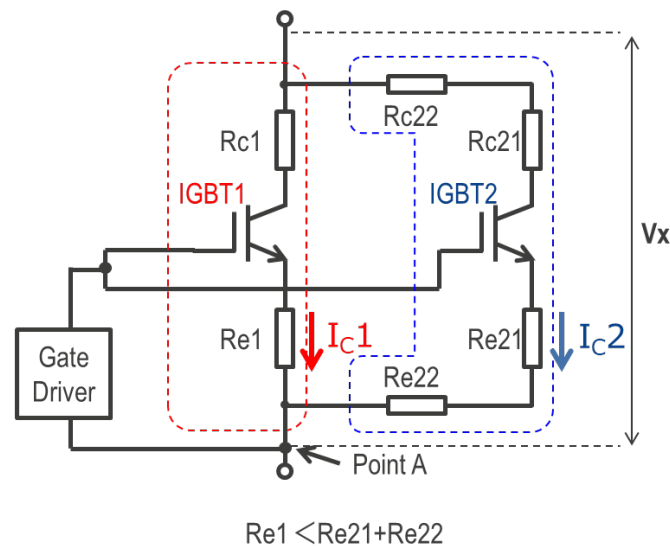


Figure 5. Effect of Circuit Symmetry from Gate Driver Perspective

2.3 $V_{CE(sat)}$ Temperature Dependency and Thermal Coupling of Devices

The behavior of the current unbalance will fluctuate according to the temperature dependency of output characteristics. Based on definitions, positive temperature dependence refers to the characteristic that $V_{CE(sat)}$ increases when junction temperature rises, and conversely, the negative temperature dependence means that $V_{CE(sat)}$ decreases when junction temperature rises. When used in parallel, positive temperature dependence improves current unbalance and serves as a stabilizer for the circuit. IGBTs have a cross point at which the temperature dependency changes. For safe circuit operations, we recommend that it be used in the positive temperature range. IGBTs have a cross point at which the temperature dependency changes. Figure 6 shows output characteristics of products with positive and negative temperature dependence, respectively. Product A behaves with positive temperature dependence in actual operation area because cross point is low, but product B behaves with negative temperature dependence since cross point is high.

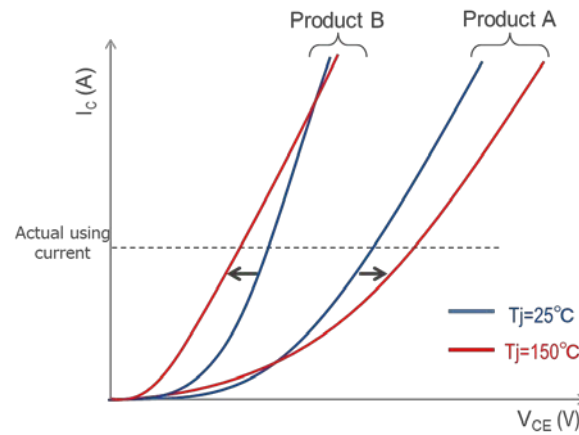


Figure 6. Temperature Dependency of Output Characteristics

In Figure 2, when both IGBT1 and IGBT2 have positive temperature dependency, the rise in junction temperature of IGBT2 (which has higher the $V_{CE(sat)}$) lessens, as does the transition of the output characteristic curve; as a result, operations maintain equilibrium. Conversely, the junction temperature rise of IGBT1 increases and the transition of the output characteristic curve also increases. Therefore, the difference between the output characteristic curves of IGBT1 and IGBT2 gradually shrink, and the current unbalance is gradually cancelled. On the other hand, if both IGBT1 and IGBT2 have negative temperature dependence, the difference mechanism of the output characteristic curves of the IGBT1 and IGBT2 will operate under the same mechanism as described above, and the current imbalance will become worse.

For the above reasons, you can see it is relatively easy to design with devices featuring positive temperature dependency in the current range to be used. On the other hand, devices with negative temperature dependency require sharing the heat sink (which strengthens the thermal coupling between the devices and reduces the temperature difference) and reducing the distance between the parallel devices, as shown in Figure 7. Renesas IGBTs boast characteristics that reduce the area of negative temperature dependency, making parallel connection easier.

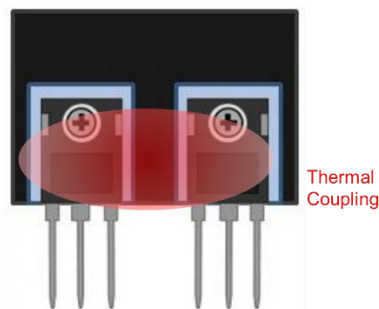


Figure 7. Example of Strong Thermal Coupling through Shared Heat Sink

3. Notes on Transient Conditions

When an IGBT is in a transient state (turn-on, turn-off), current unbalance can be caused by factors such as characteristic variations of parallel devices and differences in board and wiring inductance components.

3.1 Current Unbalance in Transient Condition Caused by Device Characteristic Variations

Current unbalance occurs in the transient state when IGBTs with different characteristics due to manufacturing variations or other factors are connected in parallel. Variations in $V_{GE(th)}$ are critical when it comes to current unbalance in the transient state. In this section, we will explain the mechanism of current unbalance based on experimental results using samples purposely created with differing $V_{GE(th)}$ values. Table 2 shows the samples used in the experiment. Figure 8 shows the measurement circuit and conditions. The board layout of the parallel circuit is symmetrical and is not the cause of current unbalance.

Table 2. Samples of Differing $V_{GE(th)}$ Used for Experiment (P/N: RBN50H65T1PFQ)

	IGBT1	IGBT2	Measurement Conditions
$V_{GE(th)}$	4.06V	6.06V	$V_{CE}=10V, I_C=1.0mA$
$V_{CE(sat)}$	1.42V	1.43V	$V_{GE}=15V, I_C=50A$

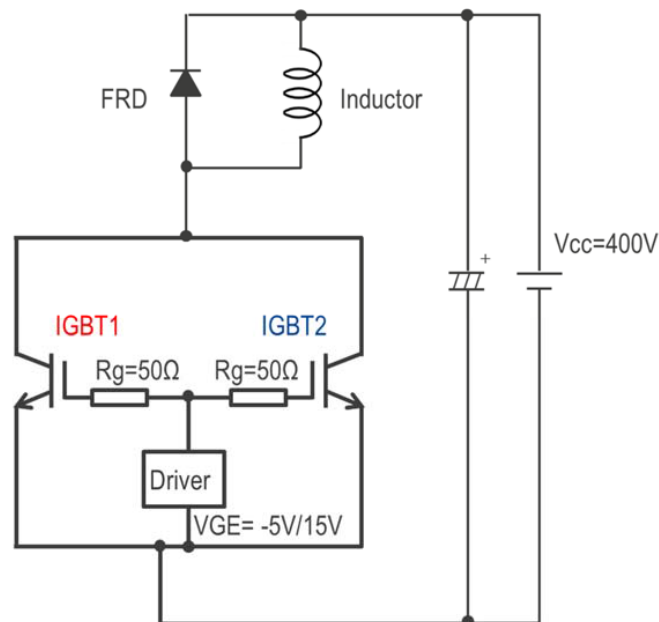


Figure 8. Switching Evaluation Circuit Diagram Used for Experiment

Current unbalance in the IGBT transient state shows different behaviors during turn-on and turn-off. Figure 9 shows the waveform during turn-on. You can see that when the IGBT1 current is high, the IGBT2 current is low. This is because IGBT1 with low $V_{GE(th)}$ turns on first at t_1 , and IGBT2 lags behind, turning on at t_2 . This current unbalance increases as the $V_{GE(th)}$ difference is big or as the rise in gate voltage is slow. As a result the current flows only toward the lower $V_{GE(th)}$ is long and then the difference between t_1 and t_2 will be widened which current began to flow.

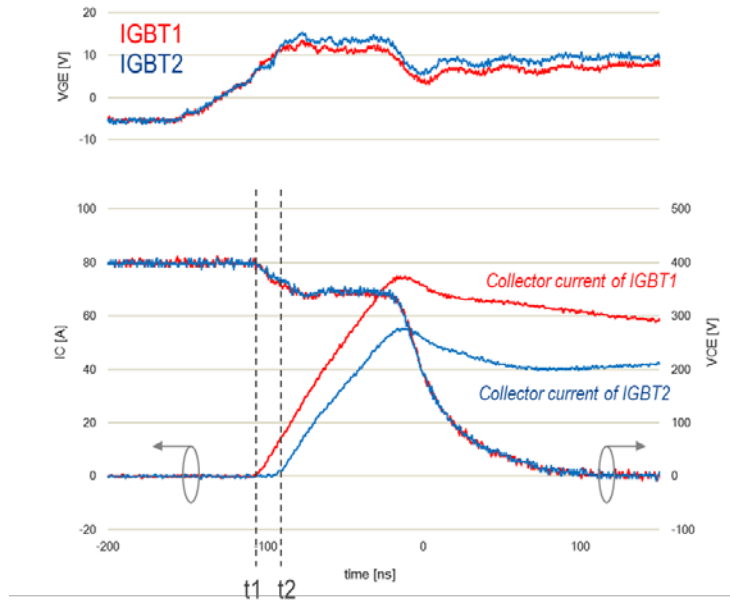


Figure 9. Current Unbalance Waveform during Turn-on

Figure 10 shows the waveform during turn-off. In t3 to t4 timing, IGBT1 current increases and IGBT2 current decrease in those time. This is because IGBT2, the device with the higher $V_{GE(th)}$, starts turning off first.

Again, the countermeasure against current unbalance caused by the $V_{GE(th)}$ difference is to always use device from the same production lot. This significantly minimizes the $V_{GE(th)}$ difference between IGBTs connected in parallel.

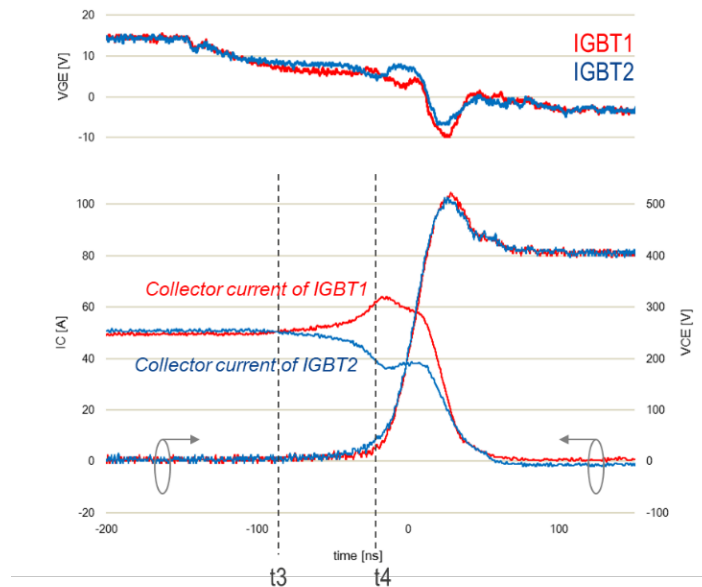


Figure 10. Current Unbalance Waveform during Turn-off

3.2 Current Unbalance in Transient Condition Caused by Circuit Layout Factors

If the parasitic inductance of the main circuit wiring is not uniform between the parallel circuit, for example if the inductance between the gate driver's emitter sense position and the IGBT emitter is different, current unbalance will occur. An example of this is shown in Figure 11. Key countermeasures are minimizing the parasitic inductance by shortening the wiring on the emitter side or designing an even layout.

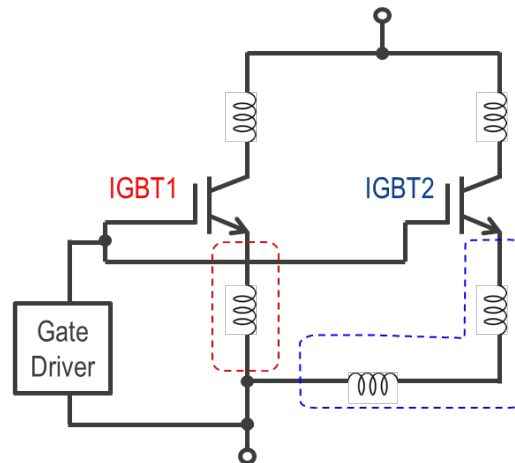


Figure 11. Example of Undesirable Emitter Sense Position in Pattern Layout

3.3 Gate Oscillation

When IGBTs are directly connected in parallel without gate resistance, a parasitic vibration waveform may be seen at the gate. This parasitic oscillation is caused when the collector-emitter voltage is turned off/on at high-speed. Especially the voltage is turned off timing, the oscillation voltage due to the wiring inductance passes through gate-collector capacitance C_{gd} and forms a resonance circuit with the gate lead inductance (Figure 12 (left)). For this reason, with no gate resistance, the Q factor (sharpness) of the resonance circuit increases, and when the resonance condition occurs, a large oscillating voltage is generated both between GC and GE, causing parasitic oscillation.

As a countermeasure, individual gate resistors are connected to IGBT1 and IGBT2 as shown in Figure 12 (right) to suppress parasitic inductance (L_{gst}) on the gate wiring and parasitic oscillation due to IGBT input capacity.

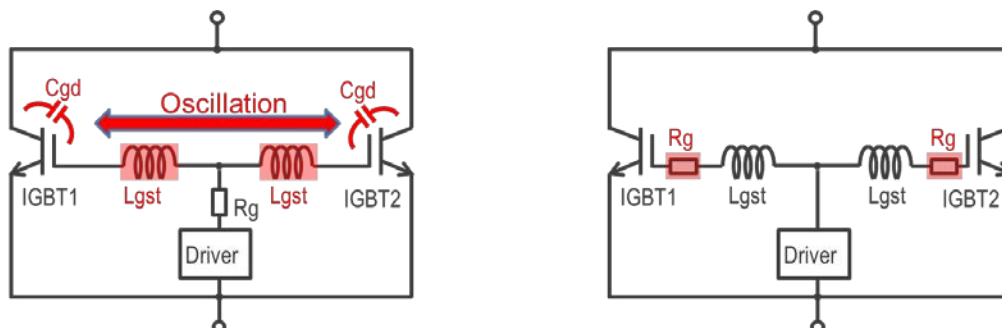


Figure 12. Circuit Susceptible to Gate Oscillation (left) and Protected Against Gate Oscillation (right)

4. Influence of Current Unbalance on Application Operations

We will now discuss the effect of current unbalance based on the explanations provided up to this point. In this section, we use a full bridge inverter as an example to explain the level of influence on operations of devices of differing characteristics in parallel. Figure 13 shows the circuit diagram and measurement conditions.

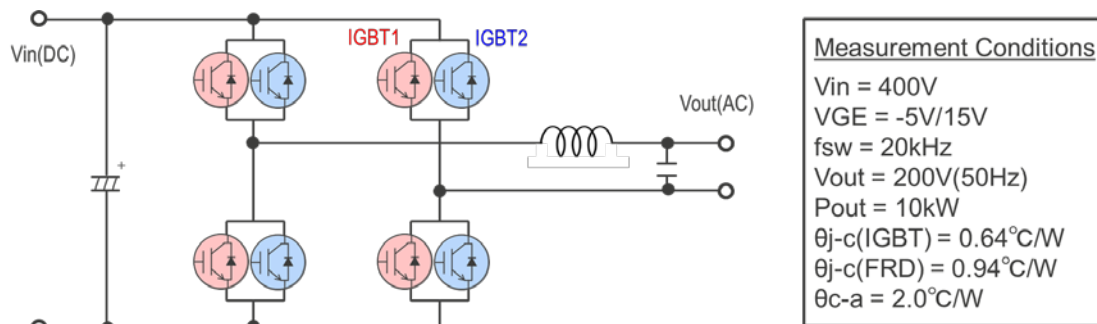


Figure 13. Full Bridge Inverter Circuit Diagram and Measurement Conditions

Table 3 lists the $V_{GE(th)}$ と $V_{CE(sat)}$ values for the devices used when connecting IGBT1 and IGBT2 in parallel. However, the built-in diodes have equivalent characteristics and are not thermally coupled. In addition, the board layout of the parallel circuit is symmetrical and is not the cause of current unbalance.

Table 3. Samples of Differing Characteristics Used for Verification (P/N: RBN50H65T1PFQ)

	IGBT1	IGBT2	Measurement Conditions
$V_{GE(th)}$	3.71V	5.69V	$V_{CE}=10V, I_C=1mA$
$V_{CE(sat)}$	1.33V	1.52V	$V_{GE}=15V, I_C=50A$

In order to calculate the losses and calorific values of IGBT1 and IGBT2 in full bridge inverter operations, IGBT1 and IGBT2 were operated in parallel in the experimental environment described in section 3.1 to measure the loss. The loss and junction temperature of the full bridge inverter circuit were estimated from this loss.

Figure 14 shows the loss generated in each device during full bridge inverter operations based on gate resistance of 47Ω. As you can see, the loss for IGBT1 is larger than that of IGBT2. In particular, IGBT conduction loss and turn-on loss differ significantly. The difference in loss is due to the current unbalance in steady state and transient state, as explained in sections 2 and 3.

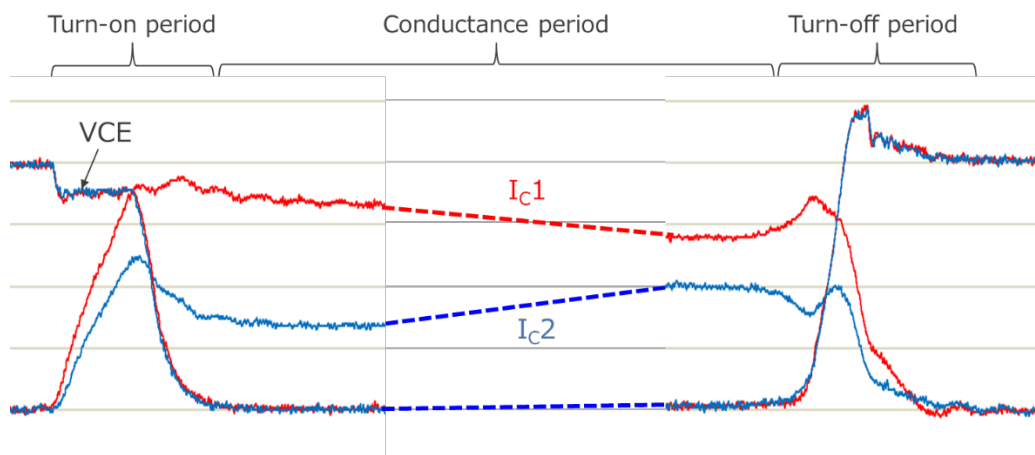
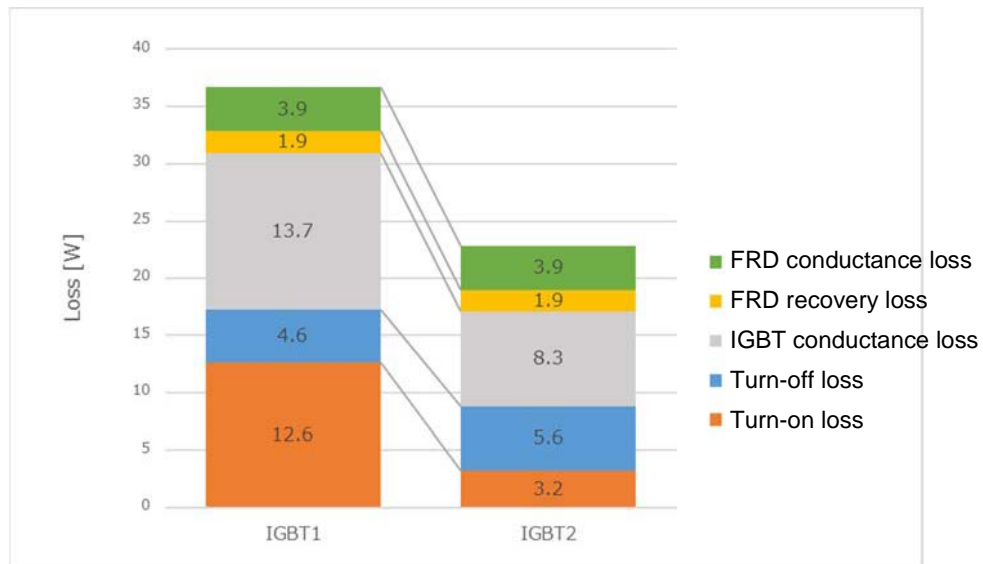


Figure 14. Device Loss Analysis and Waveform for Full Bridge Inverter Operations

In addition, the junction temperature of the devices at this time is 122°C for IGBT1 and 78°C for IGBT2. In other words, a temperature bias of 44°C exists between the parallel devices.

Further, as explained in section 3, current unbalance in the transient state fluctuates based on gate resistance. Figure 15 shows gate resistance dependency on temperature differences between parallel devices. When gate resistance is 100Ω, the temperature difference between devices is 68°C, 1.6 times the difference when gate resistance is 47Ω.

When there is a large temperature difference between devices on the actual board, the junction temperature of some IGBTs will increase, possibly exceeding the guaranteed value and resulting in damage. Therefore, it is important to check the current monitor how much deferent happened current unbalance at verification stage.

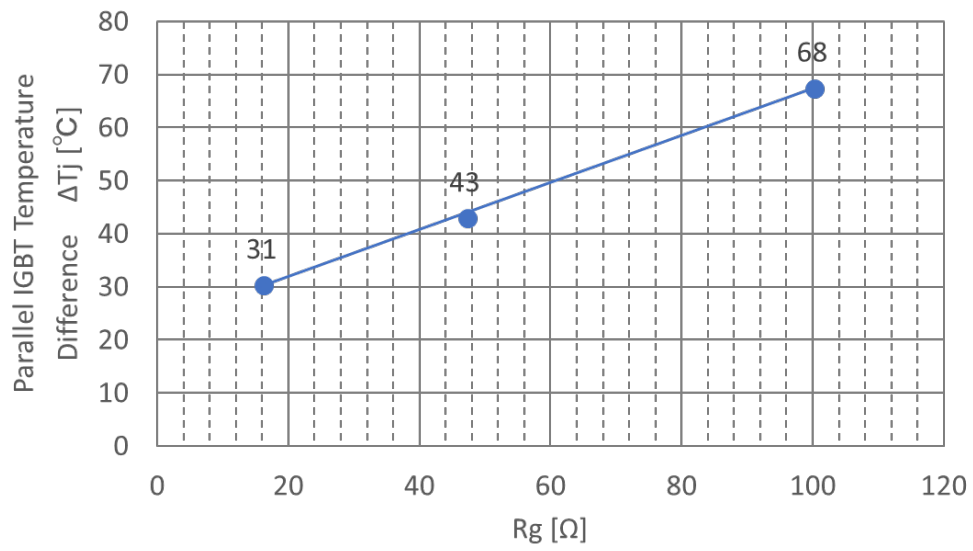
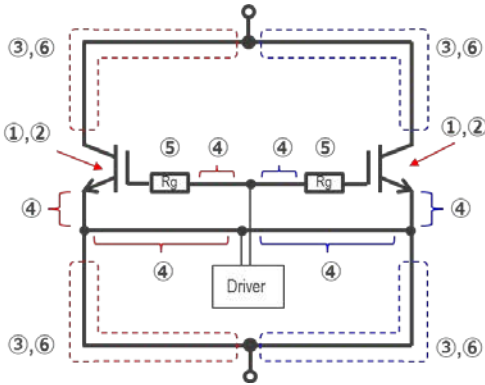


Figure 15. Gate Resistance Dependency on Temperature Differences Between Devices

5. Notes for Using IGBTs in Parallel and Recommended Layouts

Finally, Figure 16 shows an optimal circuit layout for using IGBTs in parallel connection as well as several notes to be aware of during such usage.



<Usage Notes for IGBT device>

- ① Always use device from the same production lot to minimize differences in device characteristics.
- ② Always use in the area in which $V_{CE(sat)}$ has a positive temperature characteristic.

<Usage Notes for Circuit Layout>

- ③ Make sure the board layout between arms is symmetrical.
- ④ Make sure the emitter connection point for the gate driver is equally distant to both sides and as close to the emitter port as possible. Also make sure the gate wiring distance is as short and equal as possible.
- ⑤ Gate resistance put on each device.
- ⑥ Design the pattern to be thick and wide in order to minimize wiring impedance.

Figure 16. Optimal Circuit Layout

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