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R32C/100 Series

Serial Interface Operation (Receiving in Asynchronous Serial Interface Mode)

1. Abstract

This document describes an example of the setting procedure for transmitting in the asynchronous serial interface mode (UART mode) using an arbitrary bit rate and data format.

2. Introduction

The application example described in this document applies to the following MCU:

•MCU: R32C/111 Group

This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the R32C/111 Group. Check the manual for any additions or modifications to functions. Careful evaluation is recommended before using this application note.

3. Application Example

This section describes how to transmit data at a bit rate of 9600bps (Xin = 16 MHz, PLL clock = 100 MHz and actual bit rate = 9586bps) using asynchronous serial interface mode.
Table 3.1 lists specifications of asynchronous serial interface mode.

Table 3.1 Setting Conditions for Receiving Data Using Asynchronous Serial Interface Mode

Item	Setting
Bit rate	9600bps
Character length	8 bit-length
Parity	Odd
Stop bit length	1 bit-length
Transmit/receive clock	Internal clock
Receive control	RTS
Bit order	LSB first

The following is the formula for calculating the actual bit rate.

$$\text{Actual bit rate} = \frac{\text{UiBRG register (i = 0 to 6) count source}}{16 \times (\text{UiBRG register value} + 1)}$$

Table 3.2 lists examples of bit rate settings.

Table 3.2 Bit Rate Setting Examples

Target Bit Rate (bps)	Count Source of UiBRG	PLL Clock: 96 MHz		PLL Clock: 100 MHz		PLL Clock: 120 MHz		PLL Clock: 128 MHz	
		Peripheral Clock: 24 MHz		Peripheral Clock: 25 MHz		Peripheral Clock: 30 MHz		Peripheral Clock: 32 MHz	
		Setting value of UiBRG	Actual bit rate (bps)	Setting value of UiBRG	Actual bit rate (bps)	Setting value of UiBRG	Actual bit rate (bps)	Setting value of UiBRG	Actual bit rate (bps)
1200	f8	155(9Bh)	1202	162(A2h)	1198	194(C2h)	1202	207(CFh)	1202
2400	f8	77(4Dh)	2404	80(50h)	2411	97(61h)	2392	103(67h)	2404
4800	f8	38(26h)	4808	40(28h)	4764	48(30h)	4783	51(33h)	4808
9600	f1	155(9Bh)	9615	162(A2h)	9586	194(C2h)	9615	207(CFh)	9615
14400	f1	103(67h)	14423	108(6Ch)	14335	129(81h)	14423	138(8Ah)	14388
19200	f1	77(4Dh)	19231	80(50h)	19290	97(61h)	19133	103(67h)	19231
28800	f1	51(33h)	28846	53(35h)	28935	64(40h)	28846	68(44h)	28986
31250	f1	47(2Fh)	31250	49(31h)	31250	59(3Bh)	31250	63(3Fh)	31250
38400	f1	38(26h)	38462	40(28h)	38109	48(30h)	38265	51(33h)	38462
51200	f1	28(1Ch)	51724	30(1Eh)	50403	36(24h)	50676	38(26h)	51282

In this application note, the RTS output is used for receive control. To output the RTS in the R32C/111 Group, set the direction bits and the function select registers for the $\overline{\text{RTS}}$ pin.
Table 3.3 lists the RTS Pin, Port Direction Bit and Function Select Register Settings.

Table 3.3 $\overline{\text{RTS}}$ Pin, Port Direction Bit and Function Select Register Settings

Channel	Port	Port Direction Bit	Setting Value	Function Select Register	Setting Value
$\overline{\text{RTS0}}$	P6_0	PD6_0	1	P6_0S	03h
$\overline{\text{RTS1}}$	P6_4	PD6_4	1	P6_4S	03h
$\overline{\text{RTS2}}$	P7_3	PD7_3	1	P7_3S	03h
$\overline{\text{RTS3}}$	P4_0	PD4_0	1	P4_0S	03h
$\overline{\text{RTS4}}$	P9_4 (1)	PD9_4 (1)	1	P9_4S (1)	03h
$\overline{\text{RTS5}}$	P8_1	PD8_1	1	P8_1S	03h
$\overline{\text{RTS6}}$	P4_4	PD4_4	1	P4_4S	03h

Notes:
1. N-channel open drain output.
2. Set the PRC2 bit in the PRCR register to 1 (write enabled) just before rewriting this register. Do not generate any interrupts or DMA transfers between setting the PRC2 bit to 1 and rewriting this register.

3.1 Data Reception in Asynchronous Serial Interface Mode

1)When setting the RE bit in the UiC1 register to 1 (write enabled), the MCU waits for data reception (i = 0 to 6). At the same time, the output level of the $\overline{\text{RTSi}}$ pin becomes low, notifying the transmitting side that reception is enabled.

2)When the first bit of received data (start bit) is input to the RXDi pin, the output level of the $\overline{\text{RTSi}}$ pin becomes high. Then the remaining data is received bit by bit in the following order: data bit (LSB) through data bit (MSB), parity bit, and stop bit.

3)When the stop bit is received, the value in UARTi receive register is transferred to the UiRB register. At the same time, the RI bit in the UiC1 register becomes 1 (data held in the UiRB register), indicating the reception is completed. The IR bit in the SiRIC register becomes 1 (interrupt requested).

4) When reading the lower byte in the UiRB register, RI bit becomes 0 (no data held in the UiRB register). At the same time, the output level of the $\overline{\text{RTSi}}$ pin becomes low.

Figure 3.1 shows a Connection Example for Transmission, and Figure 3.2 shows the Transmit Operation Timing.

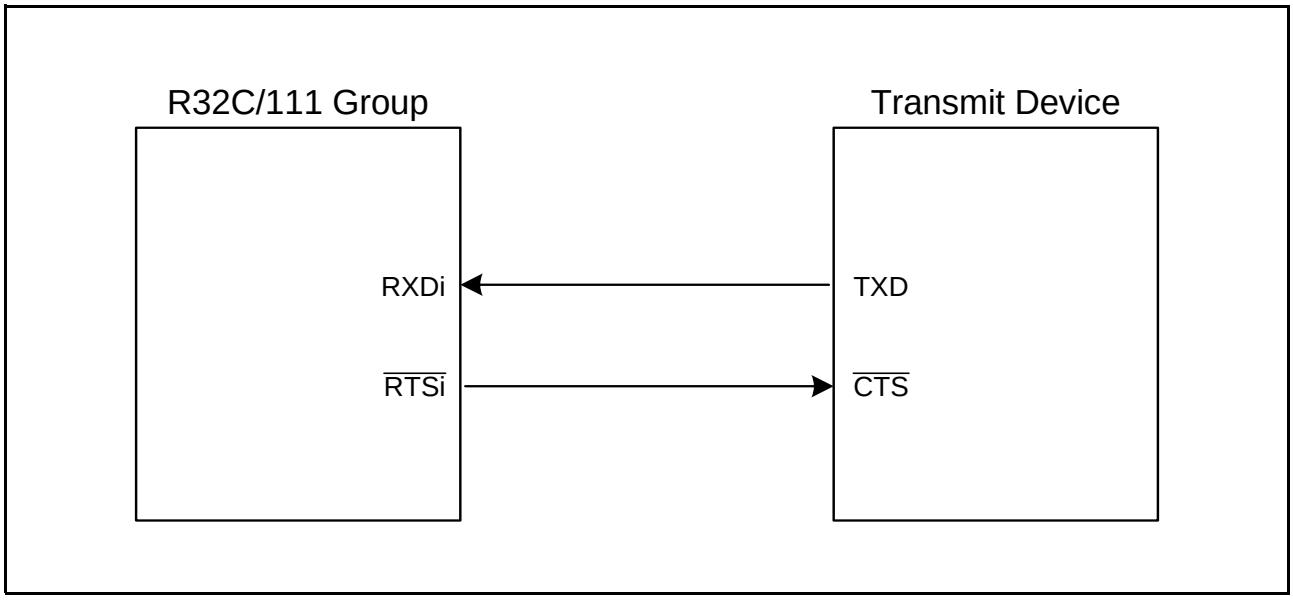

Figure 3.1 Connection Example for Transmission

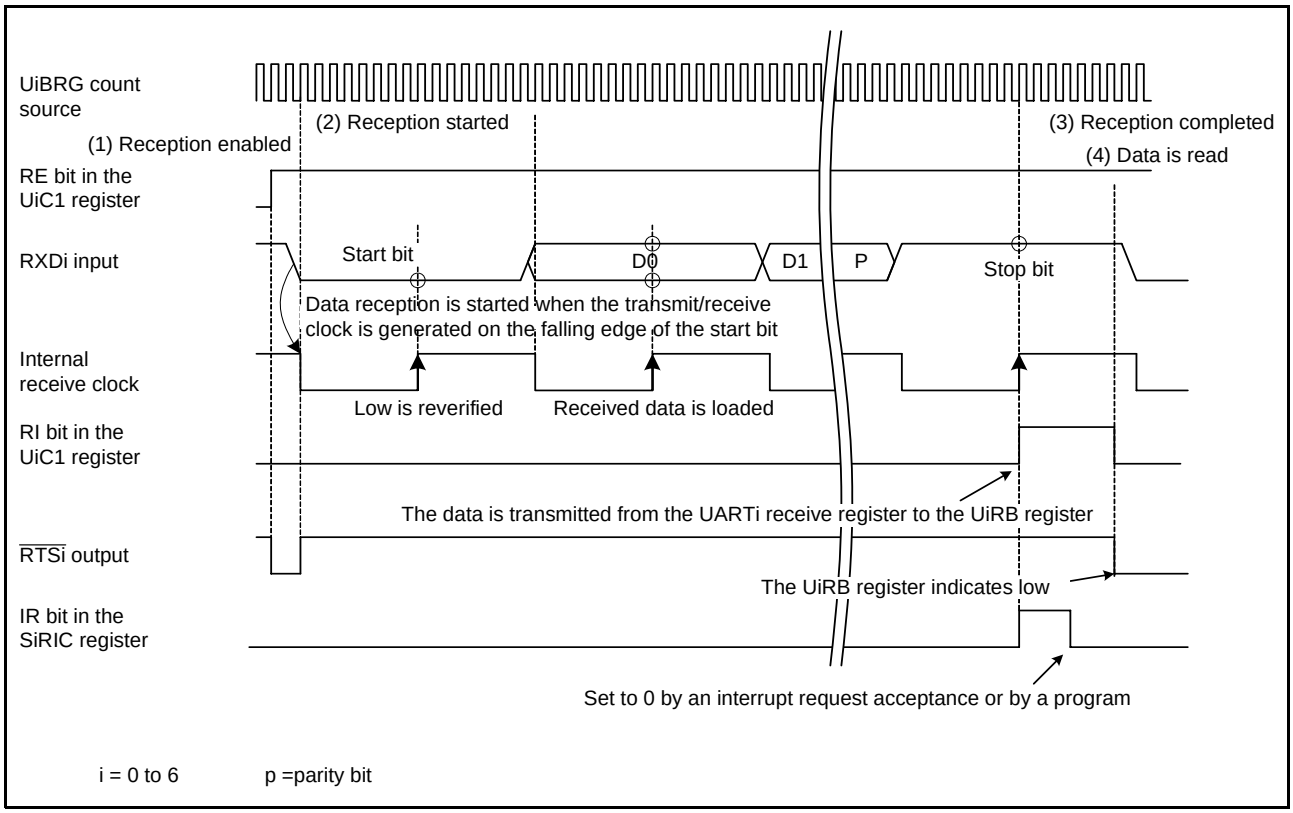

Figure 3.2 Transmit Operation Timing

3.2 Settings

This section describes the procedure and values to execute the examples shown in section 3.1 “Data Reception in Asynchronous Serial Interface Mode”. For details on each register, refer to hardware manual. The MCU enters reception standby mode by initializing UARTi (i = 0 to 6).
The sample program detects that the interrupt request bit in the UARTi receive interrupt becomes 1 (interrupt requested) and stores the received data.
Figure 3.3 shows the main Processing Flowchart (i = 0 to 6) and Figure 3.4 shows the UARTi Initialization Process Flowchart (i = 0 to 6).

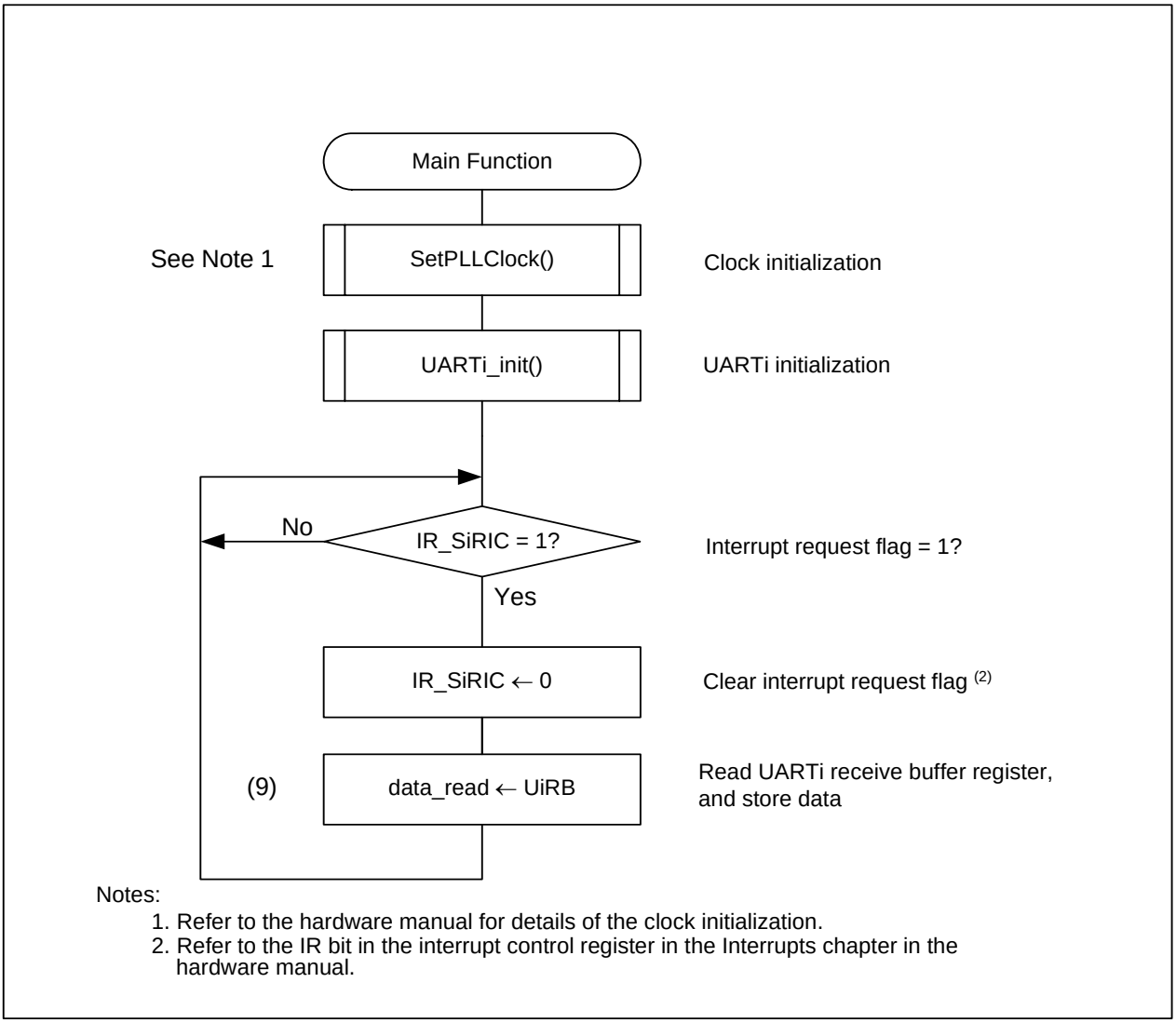

Figure 3.3 main Processing Flowchart (i = 0 to 6)

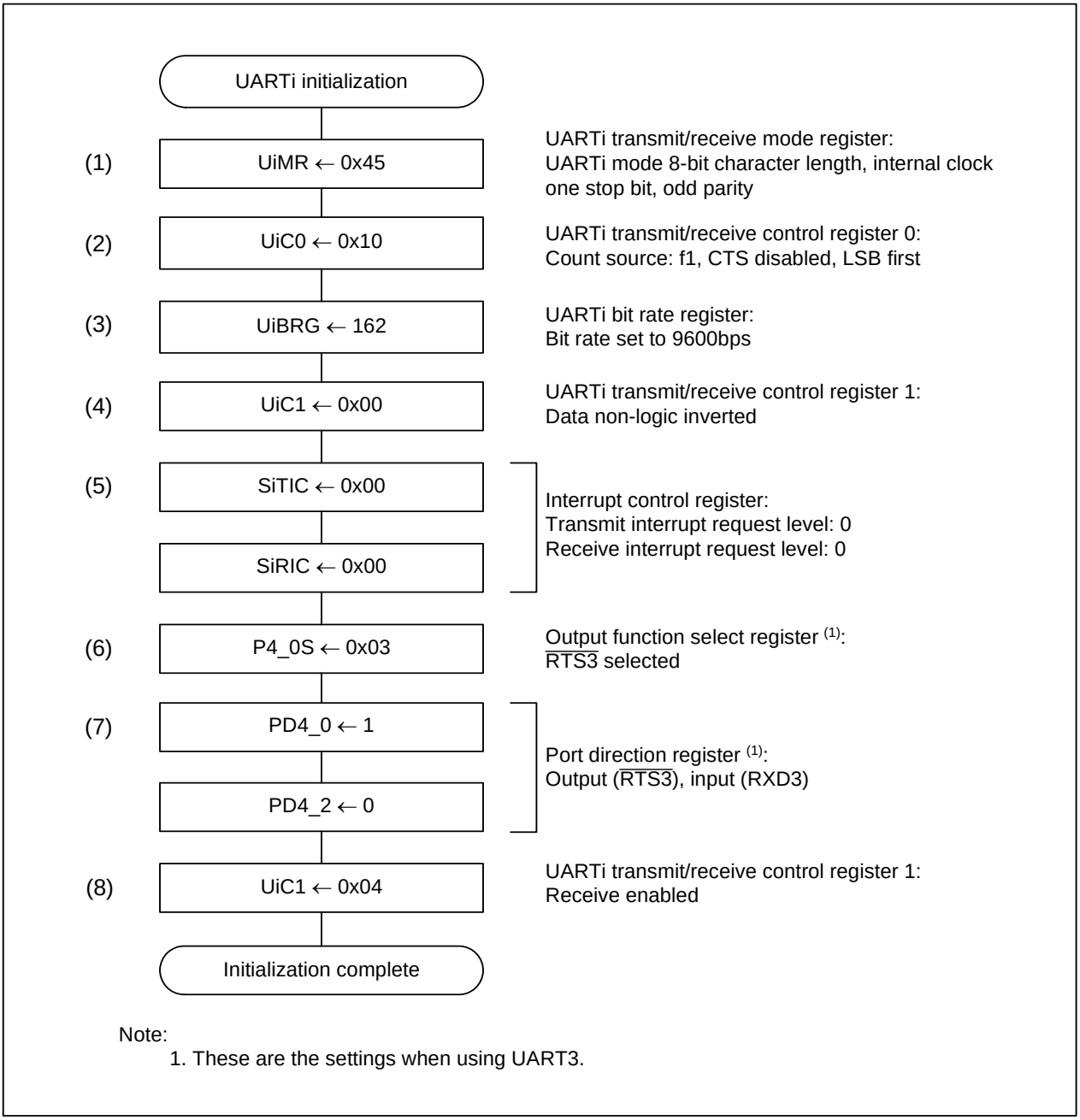

Figure 3.4 UARTi Initialization Process Flowchart (i = 0 to 6)

3.3 Detailed Settings

Set UARTi Transmit/Receive Mode Register (i = 0 to 6)

UARTi Transmit/Receive Mode Register (UiMR)

b7							b0
0	1	0	0	0	1	0	1

- SMOD2 to SMOD0: Serial Interface Mode Select Bit
  - 101b: UART Mode, 8–bit Character Length
- CKDIR: Internal/External Clock Select Bit
  - 0: Internal clock
- STPS: Stop Bit Length Selection Bit
  - 0: 1 stop bit
- PRY: Odd/Even Parity Select Bit
  - 0: Odd parity
- PRYE: Parity Enable Bit
  - 1: Parity enabled
- IOPOL: TXD, RXD Input/Output Polarity Switch Bit
  - 0: Non inverted

Set UARTi Transmit/Receive Control Register 0

UARTi Transmit/Receive Control Register 0 (UiC0)

b7							b0
0	0	0	1	0	0	0	0

- CLK1,CLK0: UiBRG Count Source Select Bit
  - 00b: f1

  Do not set bits CLK1 and CLK0 to 11b.
- Set to 0
- TXEPT: Transmit Shift Register Empty Flag
  - 0: Data held in the transmit shift register (transmission in progress)
  - 1: No data held in the transmit shift register (transmission completed)
- CRD: CTS Disable Bit
  - 1: CTS disabled
- NCH: Data Output Select Bit
  - 0: PinsTXDi/SDA and SCLi are push-pull output

  The TXD2 pin is an N channel open drain output; it will not switch to push-pull output even if set to 0.
- CKPOL: CLK Polarity Select Bit
  - 0: Output transmit data on the falling edge of the transmit/receive clock and input receive data on the rising edge
- UFORM: Bit Order Select Bit
  - 0: LSB first

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Set UARTi Bit Rate Register (i = 0 to 6)

b7							b0
162							

UARTi Bit Rate Register (UiBRG)

The UiBRG register divides the count source by n+1 (n = setting value)

162: Divided by 163

Set UARTi Transmit/Receive Control Register 1

b7							b0
0	0	0	0	0	0	0	0

UARTi Transmit/Receive Control Register 1 (UiC1)

TE	Transmit Enable Bit	0: Transmission disabled
TI	Transmit Buffer Empty Flag	0: Data held in UiTB register 1: No data held in UiTB register
RE	Receive Enable Bit	0: Reception disabled
RI	Receive Complete Flag	0: No data held in UiRB register 1: Data held in UiRB register
UiIRS	UARTi Transmit Interrupt Source Selection Bit	0: UiTB register is empty (TI = 1)
UiRRM	UARTi Continuous Receive Mode Enable Bit	0: Continuous receive mode disabled
UiLCH	Logical Inversion Select Bit	0: Data non logic-inverted
Set to 0		

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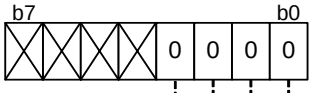
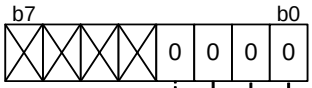
Set the interrupt control register (i = 0 to 6).



UARTi Transmit Interrupt Control Register (SiTIC)

ILVL2 to ILVL0	Interrupt Request Level Select Bits 000b: Level 0 (Interrupt disabled)
IR	Interrupt Request Flag 0: No interrupt requested

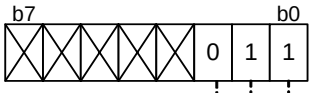


UARTi Receive Interrupt Control Register (SiRIC)

ILVL2 to ILVL0	Interrupt Request Level Select Bits 000b: Level 0 (Interrupt disabled)
IR	Interrupt Request Flag 0: No interrupt requested

Set the function select register.

Setting when UART3 is used.

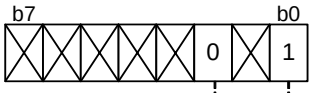


Port P4_0 Function Select Register (P4_0S)

PSEL2 to PSEL0	Port P4_0 Output Function Select Bits 011b: $\overline{\text{RTS3}}$ output

Set the port direction register.

Setting when UART3 is used.



Port P4 Direction Register (PD4)

PD4_0	Port P4_0 Direction Bit 1: Output
PD4_2	Port P4_2 Direction Bit 0: Input

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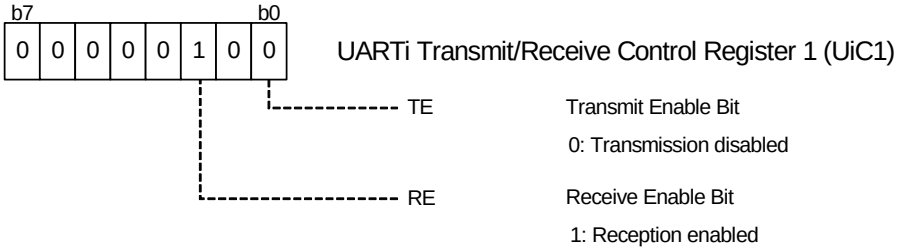
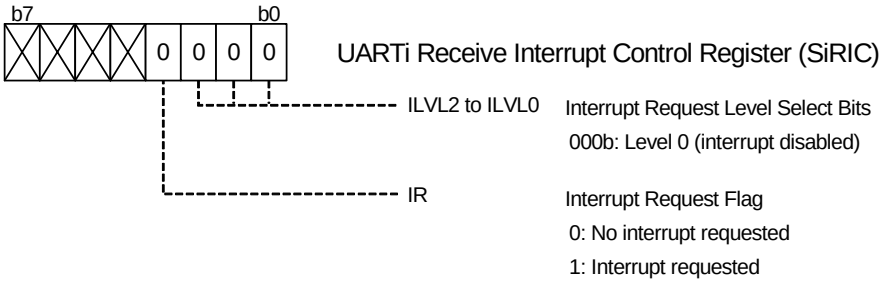
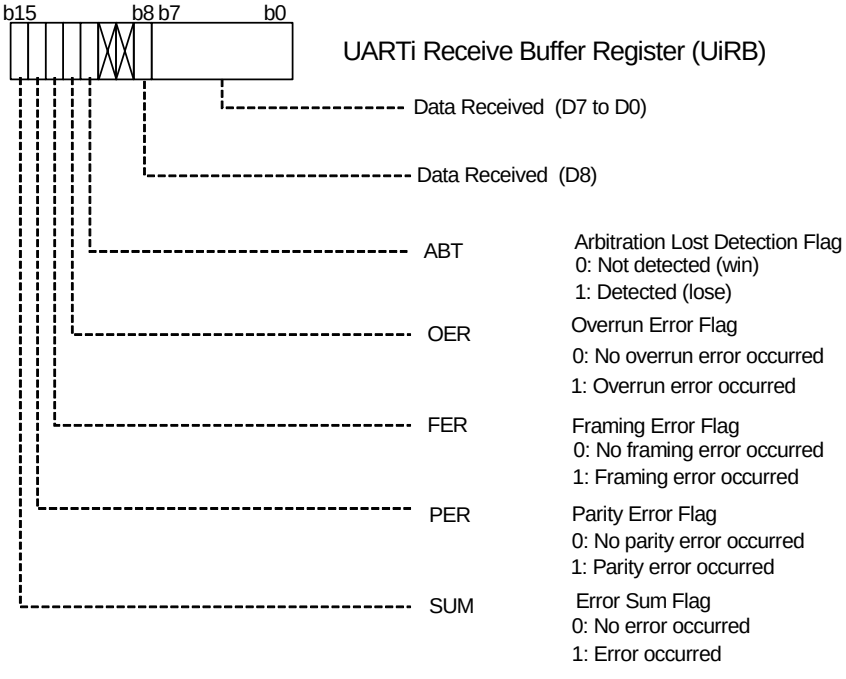
Set the UARTi transmit/receive control register 1 (i = 0 to 6).



Read the interrupt request bit and set the interrupt control register.



Read the receive data and check error.



4. Sample Programs

A sample program can be downloaded from the Renesas Technology website.

5. Reference Documents

Hardware Manual
R32C/111 Group Hardware Manual Rev.1.10
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

C compiler manual
R32C/100 Family C compiler package V.1.02 C compiler user manual Rev.1.00
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		Page	Summary
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