RL78/L1A

12-BIT A/D CONVERTER

(Single scan mode, Software trigger) CC-RL

R01AN3510EJ0100
Rev.1.00
2017.6.23

Introduction

This application note describes a method for A/D conversion of analog voltage using the RL78/L1A 12-bit A/D converter (single scan mode, software trigger).
In this application note, in addition to single conversion of analog voltage, average mode is used and average value of A/D conversion is stored in internal RAM.

Target Device

RL78/L1A

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specification

This application note shows the single scan mode of the 12-bit A / D converter and the use example of the software trigger. Set the 12-bit A / D converter to single scan mode and convert the analog signal input level of P101 / ANI00 pin, P106 / ANI03 pin to digital value. Also, ANI00 stores the result of one conversion, ANI03 stores the average value of conversion four times in internal RAM.

Table 1.1 lists the Peripheral Function to be Used and its Use and Figure 1.1 shows the outline of the conversion operation of the A/D converter.

Table 1.1 Peripheral Function to be Used and its Use

Peripheral Function	Use
12-bit A/D converter	Convert the analog signal input level of the P101 / ANI00, P106 / ANI03 pins

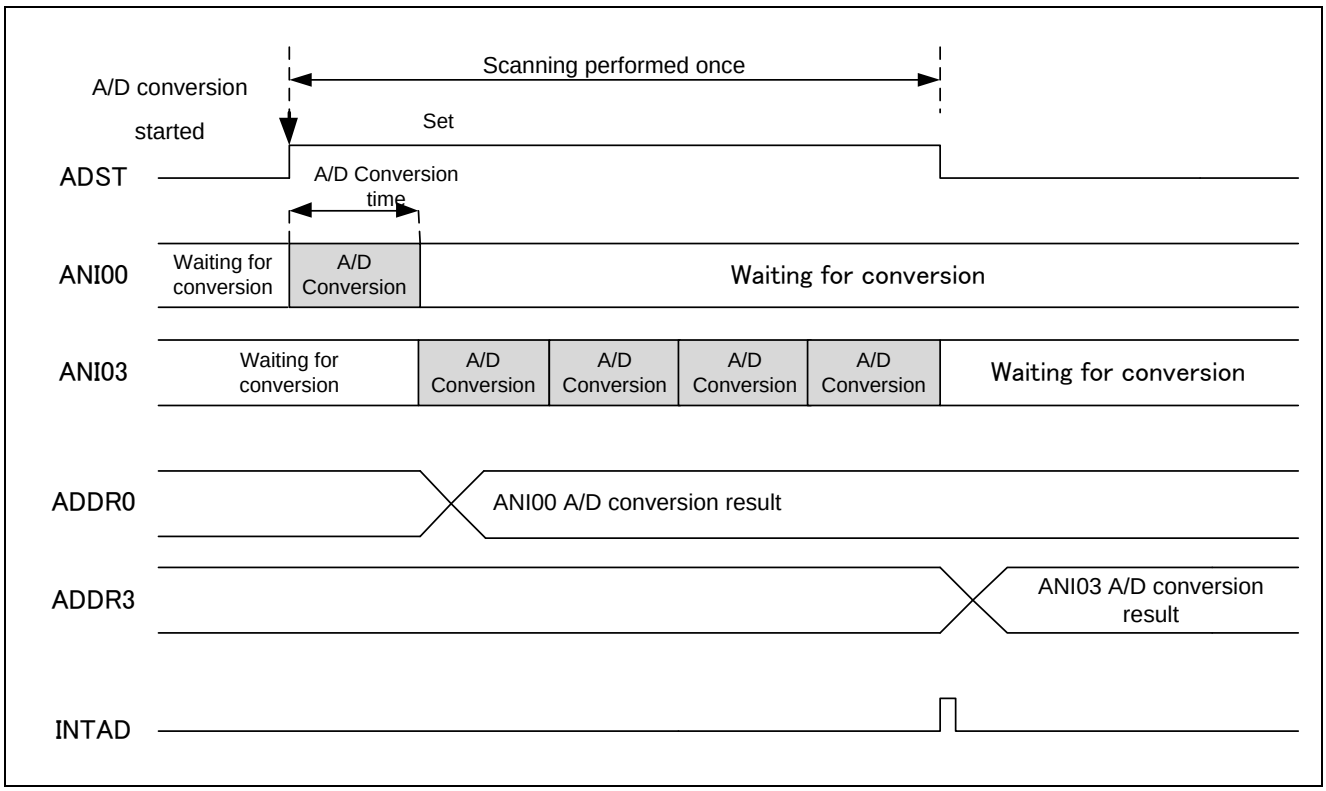

Figure 1.1 Outline of the A/D Converter Conversion Processing

2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/L1A (R5F11MPG)
Operating frequency	● High-speed on-chip oscillator (HOCO) clock: 24 MHz ● CPU/peripheral hardware clock: 24 MHz
Operating voltage	3.3V（can run on a voltage range of 1.8V to 3.6V） LVD operation (V_{LVD})：Reset mode 3.13V+/− 0.07V
Integrated development environment (CS+)	CS+ for CC V5.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.04.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e2studio 5.3 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.04.00 from Renesas Electronics Corp.

3. Description of the Hardware

3.1 Hardware Configuration Example

Figure 3.1 shows an example of hardware configuration that is used for this application note.

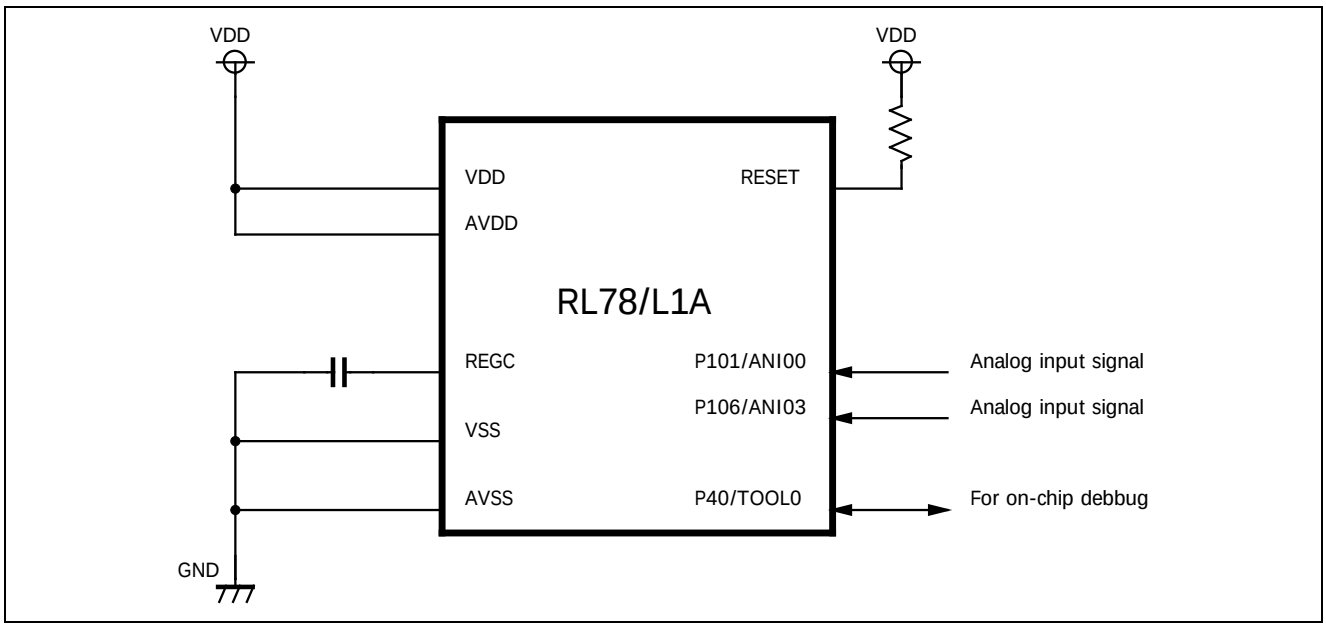

Figure 3.1 Hardware Configuration

Notes: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-dedicated ports separately to V_{DD} or V_{SS} via a resistor).
2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

3.2 List of Pins to be Used

Table 3.1 lists the pins to be used and their function.

Table 3.1 Pin to be Used and its Function

Pin Name	I/O	Description
P101/ANI00	Input	A/D converter analog input port
P106/ANI03	Input	A/D converter analog input port

4. Description of the Software

4.1 Operation Outline

In this sample code, analog voltage input to ANI00, ANI03 is A/D converted using A/D converter single scan mode and software trigger. The conversion result is stored in each A/D data register.

(1) Initialize the A/D converter.
<Setup conditions>

- ANI00, ANI03 are used for A/D conversion channels.
- Conversion operation is normal used for A/D conversion.
- Scan mode uses single scan mode.
- Software trigger is used for A/D conversion start trigger.
- A/D converted value average mode, 4 times conversion (3 times addition) is used.
- Use the A/D conversion completion interrupt (INTAD).

(2) Set the ADST bit in the ADCSR register to 1 (A/D conversion start), start A/D conversion, execute the HALT instruction, enter HALT mode, and wait for the A/D conversion completion interrupt.

(3) When the A/D conversion of the voltage input from ANI 0 is completed, the A/D converter transfers the A/D conversion result to the ADDR 0 register, followed by 4 A/D conversion of the voltage input from ANI03, the average , An A/D conversion completion interrupt is generated. The result is stored in the ADDR3 register.

(4) When the HALT mode is canceled by the A/D conversion completion interrupt, the A/D conversion result is read from the ADDR0 and ADDR3 registers and stored in the internal RAM.

4.2 List of Option Byte Settings

Table 4.1 summarizes the settings of the option bytes.

Table 4.1 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release of the reset state.)
000C1H/010C1H	01010011B	LVD reset mode 3.13V +/- 0.07V
000C2H/010C2H	11101000B	HS mode, HOCO : 24MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

4.3 List of Variables

Table 4.2 lists the global variable that is used by this sample program.

Table 4.1 Global Variable

Type	Variable Name	Contents	Function Used
unsigned short	result_buffer_00	Area for storing the ANI00 A/D conversion results	main()
unsigned short	result_buffer_03	Area for storing the ANI03 A/D conversion results	main()

4.4 List of Functions

Table 4.3 lists the functions that are used by this sample program.

Table 4.3 Functions

Function Name	Outline
R_12ADC_Start	Starts A/D conversion
R_12ADC_Get_ValueResult	Gets A/D conversion results

4.5 Function Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name] R_12ADC_Start	
Synopsis	Start A/D conversion.
Header	r_cg_12adc.h
Declaration	void R_12ADC_Start (void)
Explanation	Enables A/D conversion end interrupts and starts A/D conversion processing.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_12ADC_Get_ValueResult		
Synopsis	Get A/D conversion results.	
Header	r_cg_macrodriver.h	
Declaration	void R_12ADC_Get_ValueResult(ad_channel_t channel, uint16_t * const buffer)	
Explanation	Read the A / D conversion result.	
	I : ad_channel_t channel	Channel number
	O : uint16_t * const buffer;	Pointer to the area storing the read A / D conversion result
Return value	MD_OK	Successful completion
	MD_ARGERROR	Invalid argument specification
Remarks	none	

4.6 Flowcharts

Figure 4.1 shows the overall flow of the sample program described in this application note.

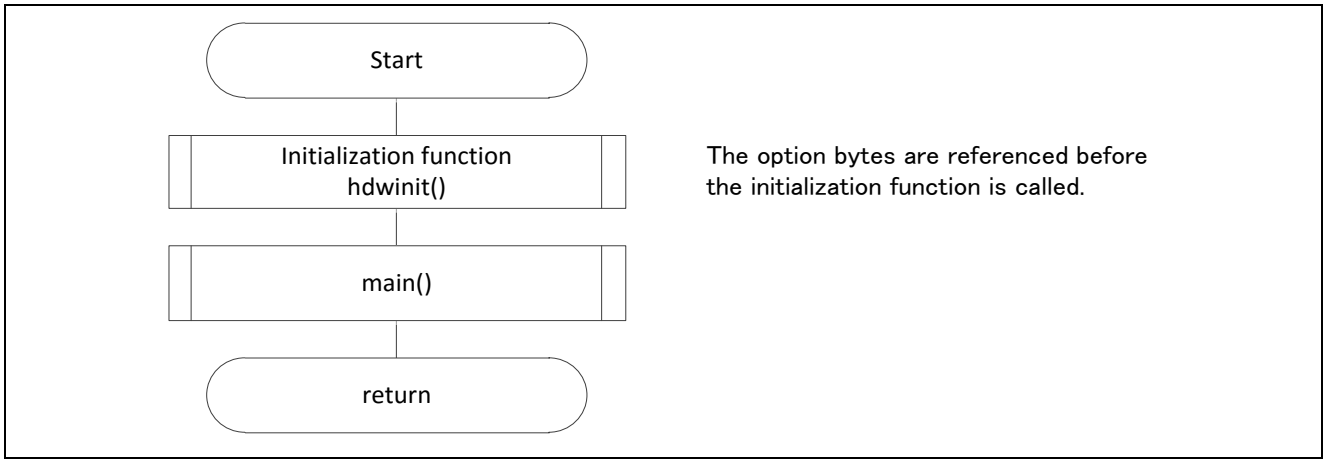

Figure 4.1 Overall Flow

Note: Startup routine is executed before and after the initialization function.

4.6.1 Initialization Function

Figure 4.2 shows the flowchart for the initialization function.

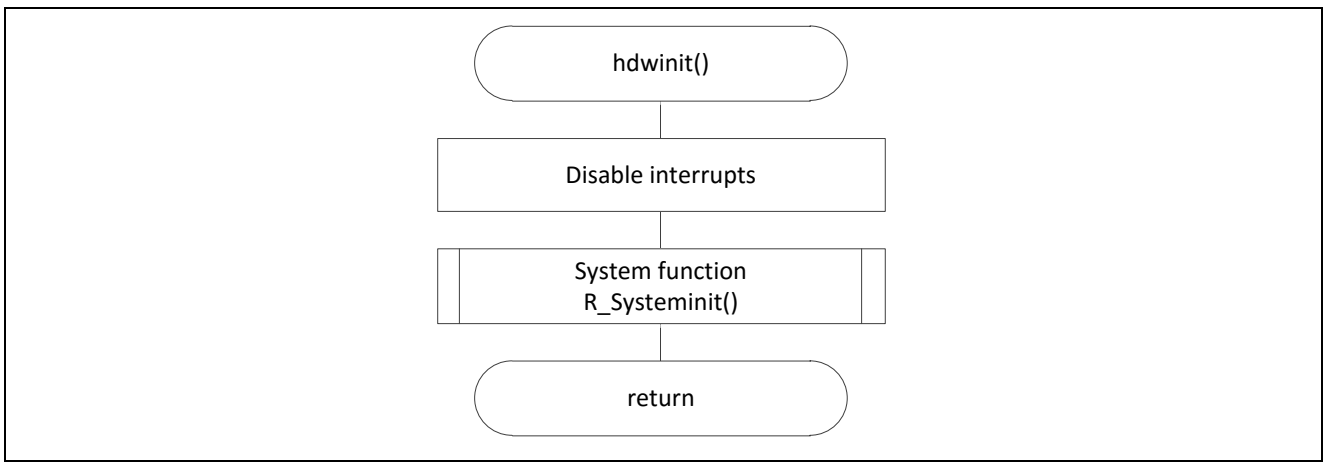

Figure 4.2 Initialization Function

4.6.2 System Function

Figure 4.3 shows the flowchart for the system function.

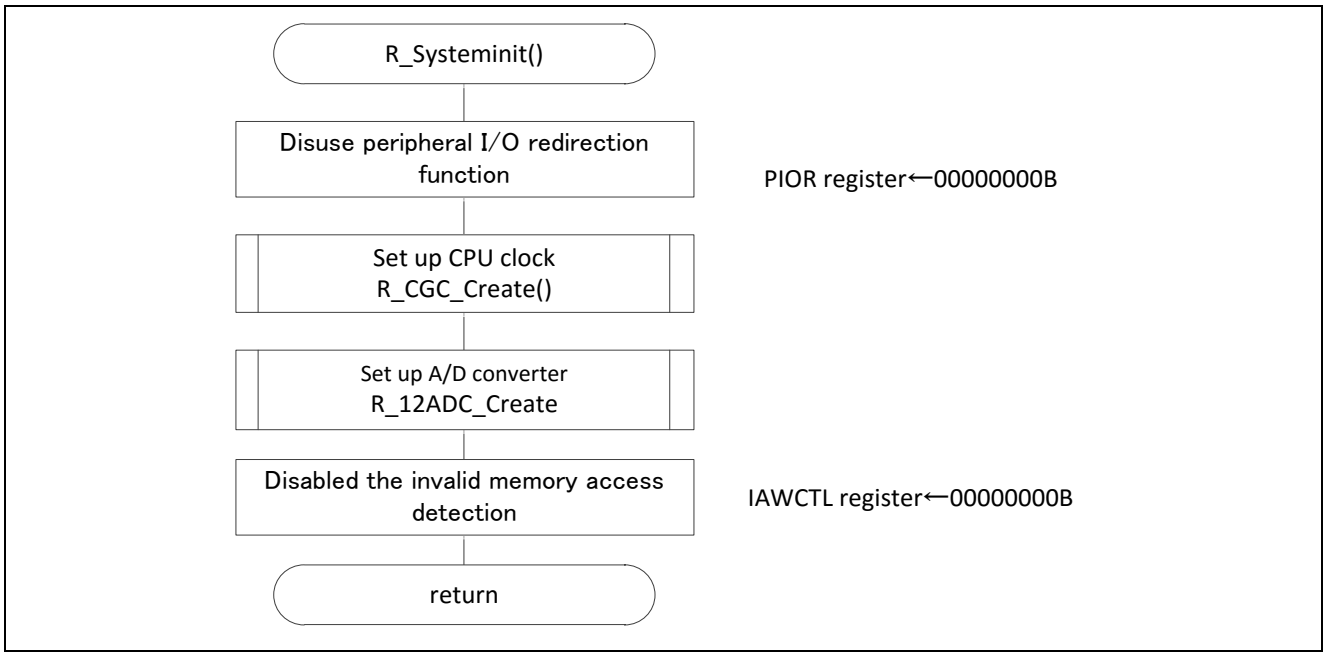

Figure 4.3 System Function

4.6.3 CPU Clock Setup

Figure 4.4 shows the flowchart for setting up the CPU clock.

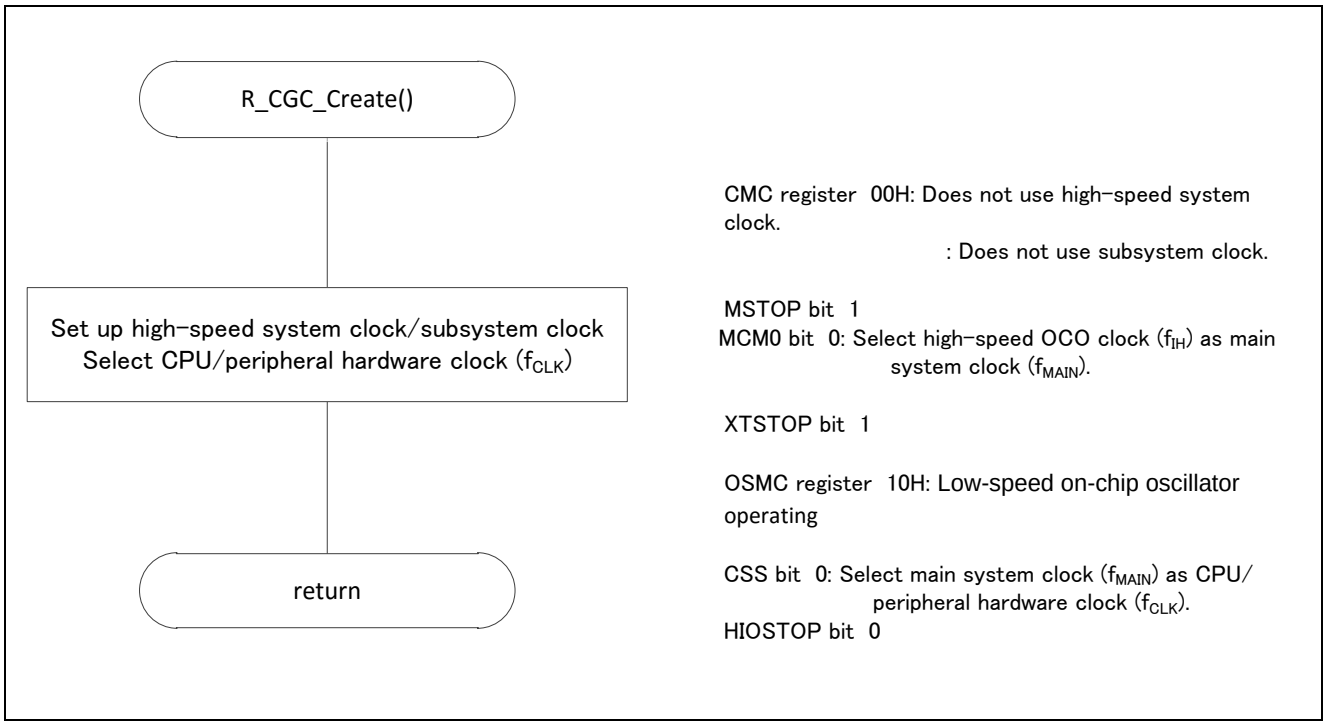

Figure 4.4 CPU Clock Setup

4.6.4 Setting up the A/D Converter

Figure 4.5 shows the flowchart for setting up the A/D converter.

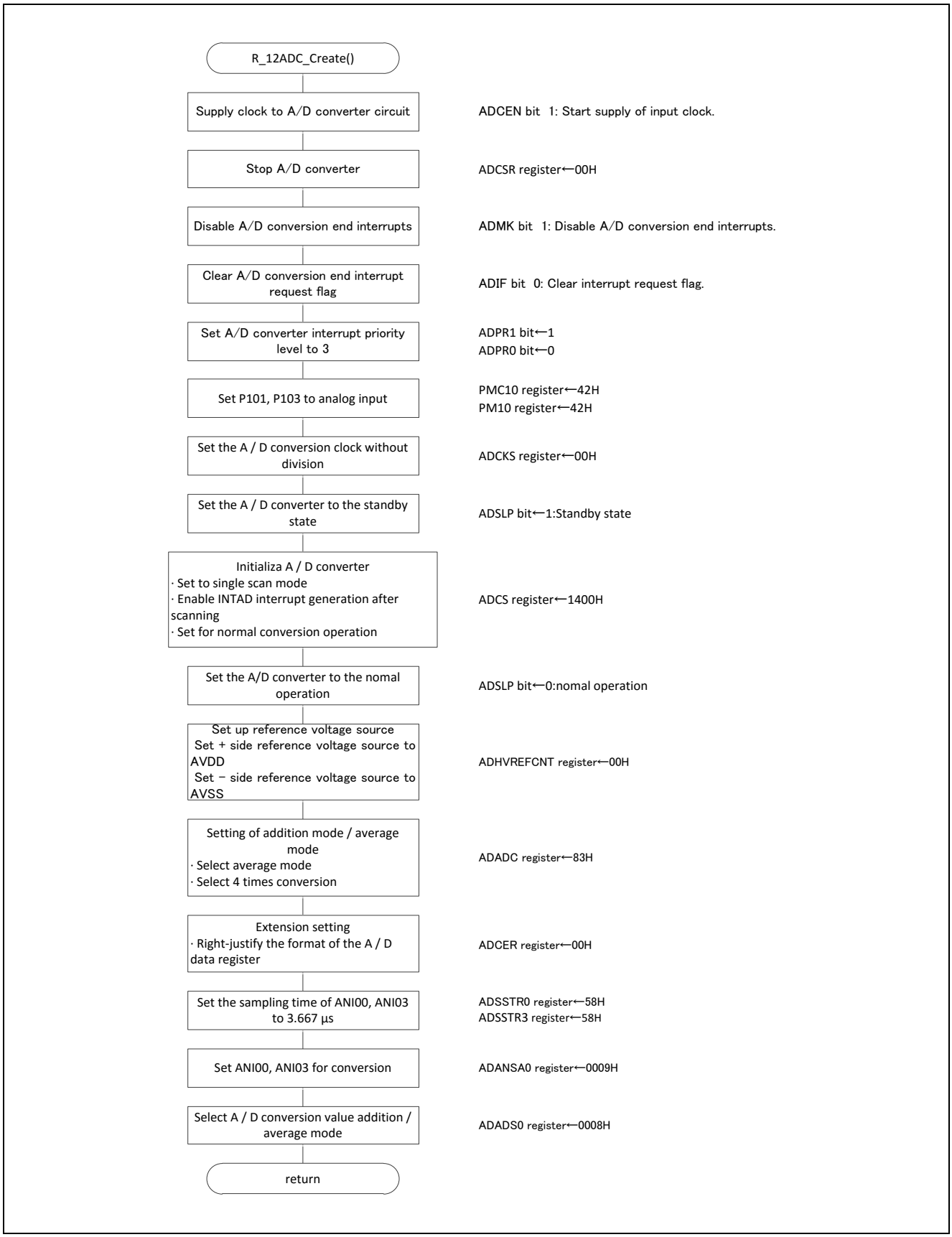

Figure 4.5 A/D Converter Setup

Starting the supply of clock to the A/D converter.

・Peripheral enable register 0 (PER0)
Starts the supply of the clock to the A/D converter.

Symbol	7	6	5	4	3	2	1	0
PER0	RTCWEN	0	**ADCEN**	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN
	×	0	**1**	×	×	×	0	×

× : Don't care

Bit 5

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply. • SFRs used by the A/D converter cannot be written. • The A/D converter is in the reset status.
1	Enables input clock supply. • SFRs used by the A/D converter can be read and written.

Note: For details on the register setup procedures, refer to RL78/L1A User's Manual: Hardware.

Setting up the A/D conversion time and operation mode.

・A/D control register (ADCSR)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCSR	ADST	**ADCS**		**ADIE**	0		TRGE	EXTRG	0	0	0	0	0	0	0	0
	0	**00**		**1**	0		0	×	0	0	0	0	0	0	0	0

× : Don't care

Bits 14,13

ADCS	Scan mode select bit
00	Single scan mode
01	Setting prohibited
10	Continuous scan mode
11	Setting prohibited

Bit 12

ADIE	Scan end interrupt enable bit
0	Disables INTAD interrupt generation upon scan completion.
1	Enables INTAD interrupt generation upon scan completion.

Bit 10

ADHSC	A/D conversion select bit
0	High-speed conversion
1	Normal conversion

・A/D channel select register A0 (ADANSA0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADANSA0	0	**ANSA0**														
	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	**1**

× : Don't care

Bit 14-0

ANSA0[14:0]	A/D conversion channel select bit
0	ANI00 to ANI14 are not subjected to conversion
1	ANI00 to ANI14 are subjected to conversion.

・A/D-converted value addition/average function select register 0 (ADADS0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADADS0	0	**ADS0**														
	×	×	×	×	×	×	×	×	×	×	×	×	**1**	×	×	×

× : Don't care

Bit 14-0

ADS0[14:0]	A/D-converted value addition/average channel select
0	A/D-converted value addition/average mode for ANI00 to ANI14 is not selected.
1	A/D-converted value addition/average mode for ANI00 to ANI14 is selected.

・A/D-converted value addition/average count select register (ADADC)

Symbol	7	6	5	4	3	2	1	0
ADADC	AVEE	0	0	0	0	**ADC**		
	1	×	×	×	×	**0**	**1**	**1**

× : Don't care

Bit 7

AVEE	Average mode enable bit
0	Addition mode is selected.
1	Average mode is selected.

Bit 2-0

ADC	Addition count select bit
000	1-time conversion (no addition; same as normal conversion)
001	2-time conversion (addition once)
010	3-time conversion (addition twice)
011	**4-time conversion (addition three times)**
101	16-time conversion (addition 15 times)
Other than above	Setting prohibited

・A/D high-potential/low-potential reference voltage control register(ADHVREFCNT)

Symbol	7	6	5	4	3	2	1	0
ADHVREFCNT	**ADSLP**	0	0	**LVSEL**	0	0	**HVSEL[1:0]**	
	1	0	0	**0**	0	0	**0**	**0**

Bit 7

ADSLP	Sleep bit
0	Normal operation
1	**Standby state**

Bit 4

LVSEL	Low-potential reference voltage select bit
0	**AVSS is selected as the low-potential reference voltage.**
1	AVREFM is selected as the low-potential reference voltage

Bit 1,0

HVSEL[1:0]	High-potential reference voltage select bit
00	**AVDD is selected as the high-potential reference voltage.**
01	AVREFP or VREFOUT is selected as the high-potential reference voltage
10	VBGR is selected as the high-potential reference voltage
11	Discharges the internal reference voltage (the high-potential reference voltage is not selected).

4.6.5 Main Processing

Figure 4.6 shows the flowchart for the main processing routine.

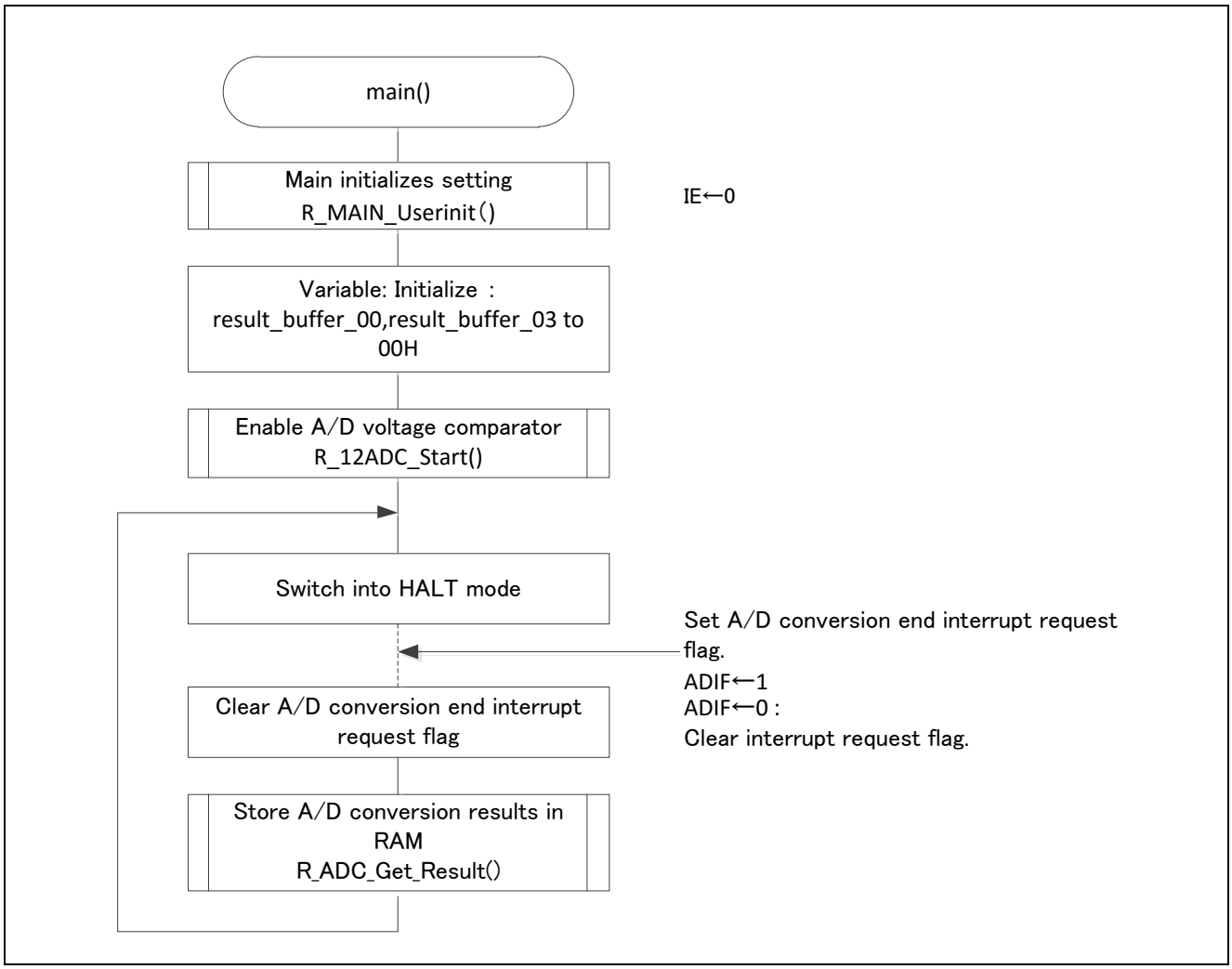

Figure 4.6 Main Processing

4.6.5 Main initializes settings

Figure 4.7 shows the flowchart for the main initializes settings.

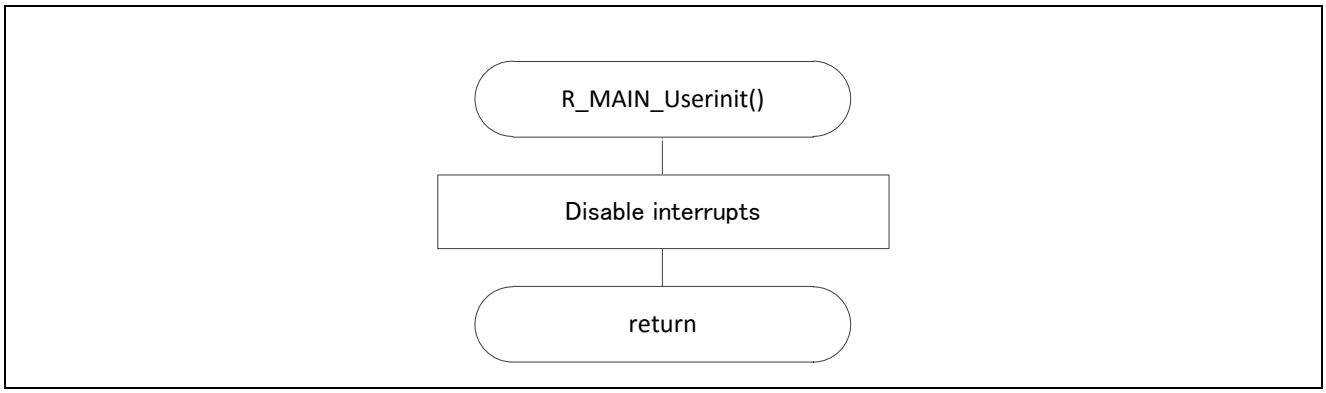

Figure 4.7 Main initializes settings

4.6.6 Starting A/D Conversion

Figure 4.8 shows the flowchart for starting A/D conversion processing.

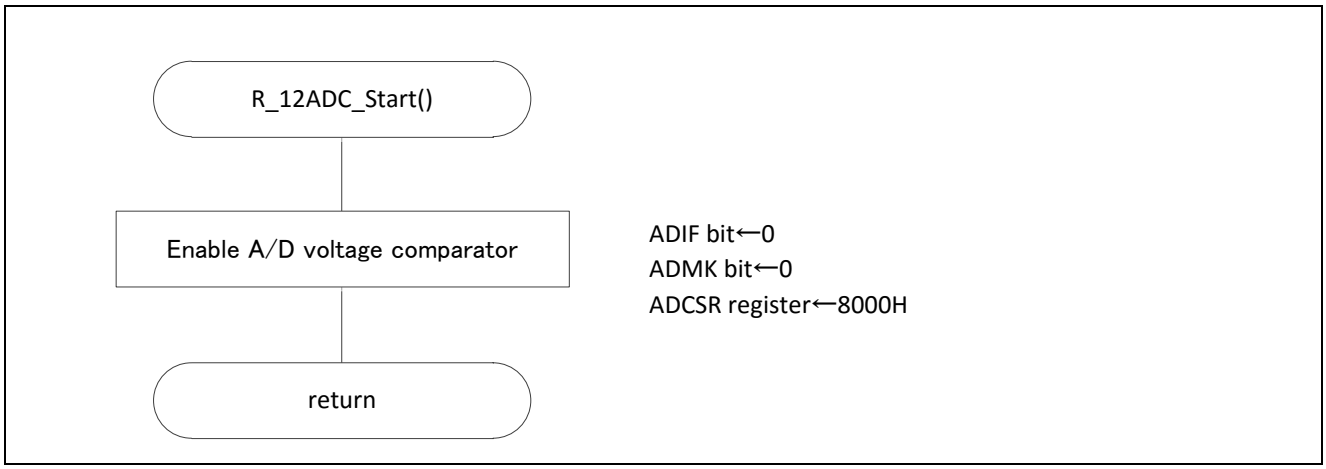

Figure 4.8 Starting A/D Conversion

・A/D control register (ADCSR)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCSR	ADST	ADCS		ADIE	0		TRGE	EXTRG	0	0	0	0	0	0	0	0
	1	0	0	0	0		0	0	0	0	0	0	0	0	0	0

Bit 15

ADST	A/D conversion start bit
0	Stops A/D conversion process.
1	**Starts A/D conversion process.**

4.6.7 Storing A/D Conversion Results in RAM

Figure 4.9 shows the flowchart for storing the A/D conversion results in RAM.

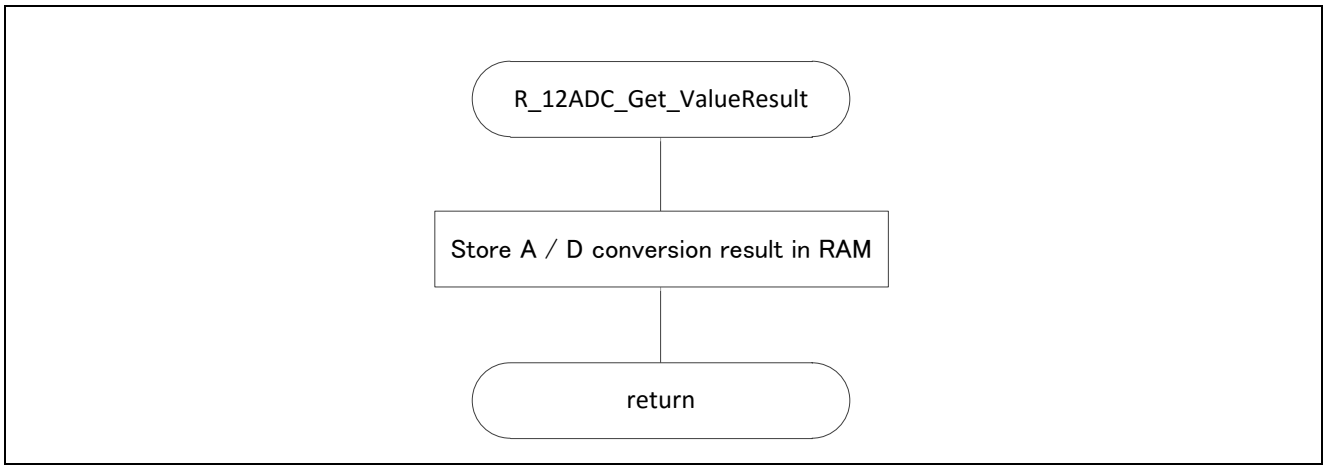

Figure 4.9 Storing the A/D Conversion Results in RAM

5. Sample Code

The sample code is available on the Renesas Electronics Website.

6. Documents for Reference

RL78/L1A User's Manual: Hardware （R01UH0636J）

RL78 Family User's Manual: Software （R01US0015J）

The latest version can be downloaded from the Renesas Electronics website.

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Revision History	RL78/L1A 12-BIT A/D CONVERTER (Single scan mode, Software trigger) CC-RL

Rev.	Date	Description	
		Page	Summary
1.00	2017.06.23	—	First edition issued

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