RL78/G23

Voltage Detector

Introduction

This application note describes how to use the two voltage detectors (LVD) mounted on the RL78/G23 to detect two voltage values.

Set voltage detector 0 (LVD0) to reset mode and voltage detector 1 (LVD1) to interrupt mode. When the power supply voltage becomes lower than the voltage detected by voltage detector 1 (LVD1), the clock frequency for the CPU and peripheral hardware changes to the frequency of the subsystem clock to reduce power consumption.

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

1.1 Overview of Specifications

In this application note, three LEDs are used. When the CPU is operating, one LED keeps flashing. Each time the switch is pressed, the flashing LED changes to another LED.

Set voltage detector 0 (LVD0) to reset mode and voltage detector 1 (LVD1) to interrupt mode.

When the power supply voltage (V_{DD}) equals or exceeds the voltage detected by LVD0 (V_{LVD0}), the CPU operates at 32 MHz and flashes an LED. When V_{DD} falls below the voltage detected by LVD1 (V_{LVD1}), the CPU operation clock (f_{CLK}) changes to 32.768 kHz. As a result, the flashing interval of the LED becomes longer. When V_{DD} equals or exceeds V_{LVD1} again, f_{CLK} changes to 32 MHz. In this case, the flashing interval of the LED becomes shorter.

When V_{DD} equals or exceeds the voltage detected by the power-on reset (POR) circuit (V_{PDR}) and is lower than V_{LVD0}, LVD0 generates an internal reset signal and the LED goes off. In this voltage range, the data stored in the RAM is retained. When V_{DD} equals or exceeds V_{LVD0} again, the LED that used to flash before the reset resumes flashing.

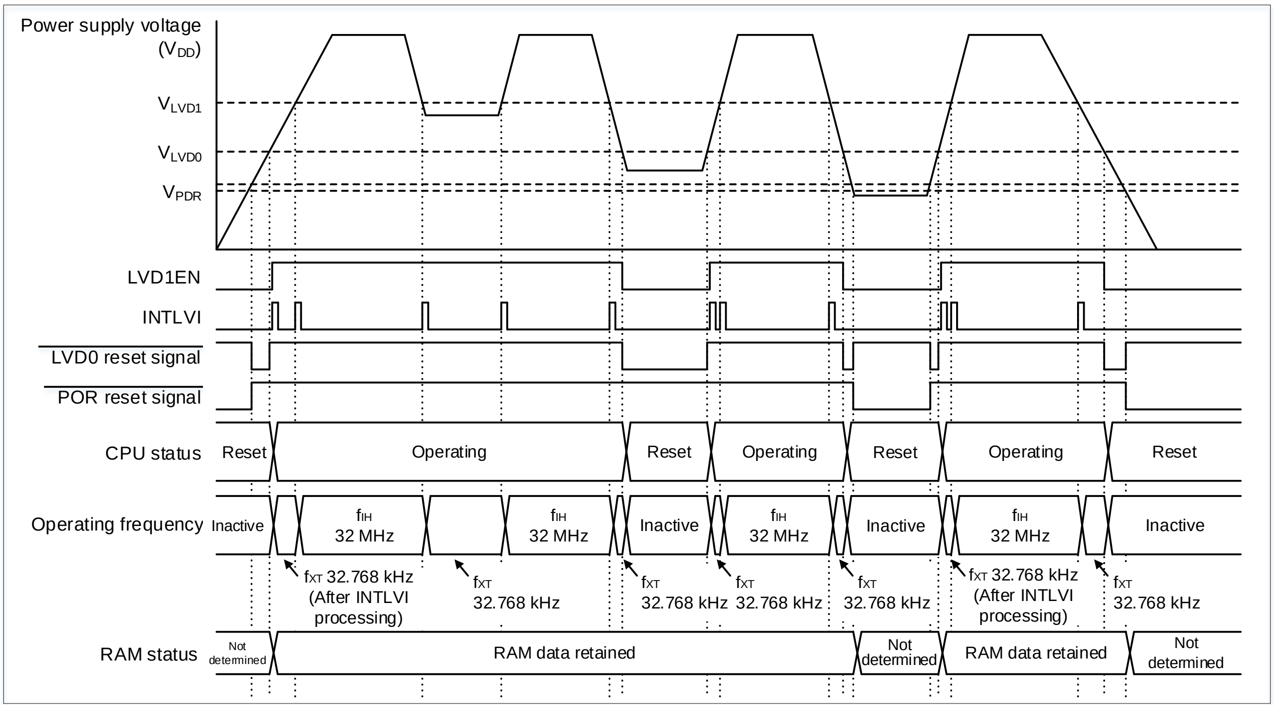
When V_{DD} falls below the voltage detected by the POR circuit (V_{PDR}), the POR circuit generates an internal reset signal and the LED goes off. In this case, the data stored in the RAM is not retained. When V_{DD} equals or exceeds V_{LVD0} again, LED1 starts flashing.

Table 1-1 lists the peripheral functions to be used and their uses, and Figure 1-1 gives an overview of the voltage detector (LVD) operation.

Table 1-1 Peripheral Functions Used and Their Uses

Peripheral Function	Use
Voltage detector (LVD0, LVD1)	Monitor the power supply voltage (V_{DD}).
External interrupt	Used as a pin edge detection interrupt (INTP0) by switch input. Receives switch input interrupts on the edge-detecting interrupt input pin (INTP0).
Port output	Controls the LEDs (LED1 to LED3) connected to P03, P02, and P43 pins.

Figure 1-1 Overview of the Voltage Detector (LVD) Operation



1.2 Outline of Operation

Set LVD0 to reset mode and LVD1 to interrupt mode.

f_{CLK} changes depending on V_{DD}. You can determine whether f_{CLK} is changed by checking the flashing interval of the LED.

When $V_{LVD1} \leqq V_{DD}$: f_{CLK} = 32 MHz, shorter LED flashing interval

When $V_{LVD0} \leqq V_{DD} < V_{LVD1}$: f_{CLK} = 32.768 kHz, longer LED flashing interval

The LEDs cycle as follows each time the switch is pressed.

LED1 → LED2 → LED3 → LED1 →・・・

Table 1-2 LED On/Off Status

Operation	LED On/Off Status		
	LED1	LED2	LED3
(1)	OFF	OFF	OFF
(2)	ON (flashing)	OFF	OFF
(3)	OFF	ON (flashing)	OFF
(4)	OFF	OFF	ON (flashing)

Operations (2) to (4) cycle each time the switch is pressed.

When LVD0 generates a reset signal, the data stored in the RAM (the number of switch inputs) is retained. When the CPU resumes operation, the LED that used to flash before the reset is selected.

When the POR circuit generates a reset signal, the data stored in the RAM (the number of switch inputs) is not retained. When the CPU resumes operation, LED1 is selected.

(1) Initialize the voltage detector (LVD).

<Setting conditions>

- At power-on or after a reset release, the option bytes are automatically referenced and LVD0 is set to reset mode.
- Set the LVD0 detection voltage to 1.875 V (rising) and to 1.835 V (falling).
- Set LVD1 to interrupt mode.
- Set the LVD1 detection voltage to 2.400 V (rising) and to 2.350 V (falling).

(2) Set the I/O ports.

- P03, P02, and P43 pins: Set as output ports (to be used for LED control).
- P137 / INTP0 pin: Set as an input port (to be used for switch input).

(3) Initialize external interrupt processing.

- Set the falling edge as the valid edge for the INTP0 pin and enable switch input.
- Enable INTP0 interrupts.

(4) Flash the LED corresponding to the input count of the switch.

- When the switch is pressed, the falling edge of the P137 / INTP0 pin is detected and interrupt processing is performed.
- To prevent chattering, the voltage applied to the P137 pin is checked approximately every 5 ms. When the switch is determined to be pressed, the switch input count is updated and the LED corresponding to the switch input count flashes (see Table 1-2).

(5) f_{CLK} changes based on the voltage detected by LVD1.

- When $V_{LVD1} \leqq V_{DD}$: f_{CLK} = 32 MHz
- When $V_{LVD0} \leqq V_{DD} < V_{LVD1}$: f_{CLK} = 32.768 kHz

When LVD0 generates a reset signal, the data stored in the RAM (switch input count) is retained. However, if you use the startup routine prepared in CS+ or e2studio without modifying it, the data in the internal RAM is initialized before the main functions. To prevent this, comment out the initialization program for the internal RAM data.

```
        ;--------------------------------------------------
        ; initializing BSS
        ;--------------------------------------------------
        ; clear external variables which doesn't have initial value (near)
;       MOVW    HL,#LOWW(STARTOF(.bss))
;       MOVW    AX,#LOWW(STARTOF(.bss) + SIZEOF(.bss))
;       BR      $.L2_BSS
;.L1_BSS:
;       MOV     [HL+0],#0                                  Comment out
;       INCW    HL
;.L2_BSS:
;       CMPW    AX,HL
;       BNZ     $.L1_BSS
```

If you use the startup routine prepared in IAR Embedded Workbench without modifying it, the data in the internal RAM is initialized before the main functions. To prevent this, add __no_init when you declare variables, and place the data in the area for holding variable values.

```
__no_init uint8_t g_SwCount;          /* Counter for KEY pushed */
```

Caution For details about the cautions on using the device, see the RL78/G23 User’s Manual: Hardware.

2. Operation Confirmation Conditions

The operation of the sample code provided with this application note has been tested under the following conditions.

Table 2-1 Operation Confirmation Conditions

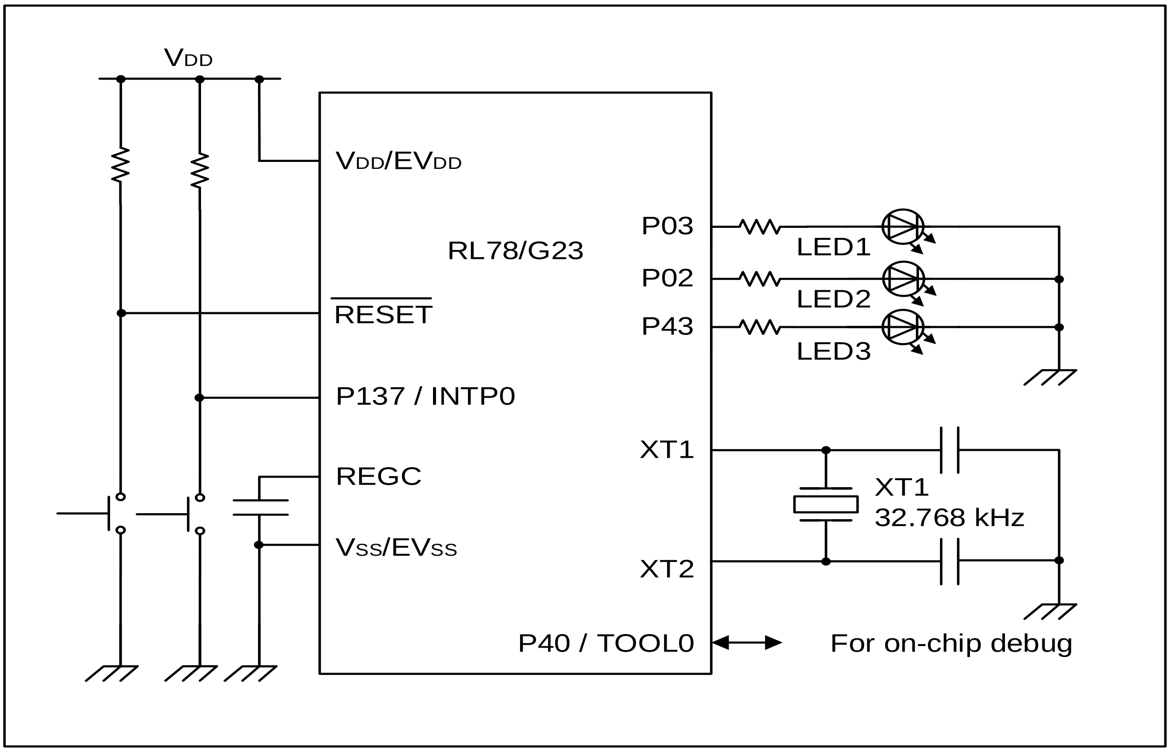
Item	Description
MCU used	RL78/G23 (R7F100GLG)
Board used	RL78/G23-64p Fast Prototyping Board (RTK7RLG230CLG000BJ)
Operating frequency	• High-speed on-chip oscillator clock (f_{IH}): 32 MHz • Subsystem clock (XT1 clock (f_{XT})): 32.768 kHz
Operating voltage	5.0 V (can be operated at 2.0 V to 5.5 V) LVD0 detection voltage: Reset mode At rising edge TYP. 1.90 V (1.84 V to 1.95 V) At falling edge TYP. 1.86 V (1.80 V to 1.91 V) LVD1 detection voltage: Interrupt mode At rising edge TYP. 2.40 V (2.35 V to 2.45 V) At falling edge TYP. 2.35 V (2.30 V to 2.40 V)
Integrated development environment (CS+)	CS+ V8.10.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.12.01 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2studio V2023-10 (23.10.0) from Renesas Electronics Corp.
C compiler (e2studio)	CC-RL V1.12.01 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V5.10.1 from IAR Systems Corp.
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V5.10.1 from IAR Systems Corp.
Smart configurator (SC)	V1.8.0 from Renesas Electronics Corp.
Board support package (BSP)	V1.00 from Renesas Electronics Corp.

3. Hardware Descriptions

3.1 Example of Hardware Configuration

Figure 3-1 shows an example of the hardware configuration used in the application note.

Figure 3-1 Hardware Configuration



Note 1. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes appropriate pin handling and meets electrical characteristic requirements (connect each input-only port to V_{DD} or V_{SS} through a resistor.)

Note 2. Connect any pins whose name begins with EV_{SS} to V_{SS}, and any pins whose name begins with EV_{DD} to V_{DD}, respectively.

Note 3. V_{DD} must not be lower than the interrupt generation voltage (V_{LVD1}) that is specified for the LVD1.

3.2 List of Pins to be Used

Table 3-1 lists the pins to be used and their functions.

Table 3-1 Pins to be Used and Their Functions

Pin name	I/O	Function
P03	Output	LED1 control
P02	Output	LED2 control
P43	Output	LED3 control
P137 / INTP0	Input	LED status switching
XT1	Input	Subsystem clock input: 32.768 kHz
XT2	Input	Subsystem clock input: 32.768 kHz

Caution In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software Explanation

4.1 Setting of Option Byte

Table 4-1 shows the option byte settings. Set the values that are most suited to your system as necessary.

Table 4-1 Option Byte Settings

Address	Setting Value	Contents
000C0H / 040C0H	11101111B	Disables the watchdog timer. (Counting stopped after reset)
000C1H / 040C1H	11111110B	LVD0 detection voltage: reset mode At rising edge TYP. 1.90 V (1.84 V to 1.95 V) At falling edge TYP. 1.86 V (1.80 V to 1.91 V)
000C2H / 040C2H	11101000B	HS mode, High-speed on-chip oscillator clock (f_{IH}): 32 MHz
000C3H / 040C3H	10000100B	Enables on-chip debugging

4.2 List pf Constants

Table 4-2 lists the constants that are used in the sample code.

Table 4-2 Constants

Constant Name	Setting Value	Description
LED_ON	01H	LED control: On
LED_OFF	00H	LED control: Off
WAITCOUNT_32M	8000	Wait count for 5 ms when the high-speed on-chip oscillator clock operates at 32 MHz
WAITCOUNT_32K	8	Wait count for 5 ms when the subsystem clock operates at 32.768 kHz

4.3 List of Variables

Table 4-3 lists global variables.

Table 4-3 Global Variables

Type	Variable Name	Description	Function Used
uint8_t	g_SwCount	Switch transition status variable	main (),r_Config_INTC_intp0_interrupt ()
uint8_t	aLedNumberTable	LED ON pattern table	main ()

4.4 List of Functions

Table 4-4 shows a list of functions.

Table 4-4 Functions

Function Name	Outline
r_Config_INTC_intp0_interrupt()	External interrupt (INTP0) processing.
r_lvd_interrupt()	Voltage detector (LVD1) interrupt processing.

4.5 Specification of Functions

The function specifications of the sample code are shown below.

r_Config_INTC_intp0_interrupt()

Outline	External interrupt (INTP0) processing.
Header	r_cg_macrodriver.h, r_cg_userdefine.h, Config_INTC.h
Declaration	static void __near r_Config_INTC_intp0_interrupt (void)
Description	Changes the LEDs to flash each time the switch is pressed.
Argument	None
Return Value	None

r_lvd_interrupt()

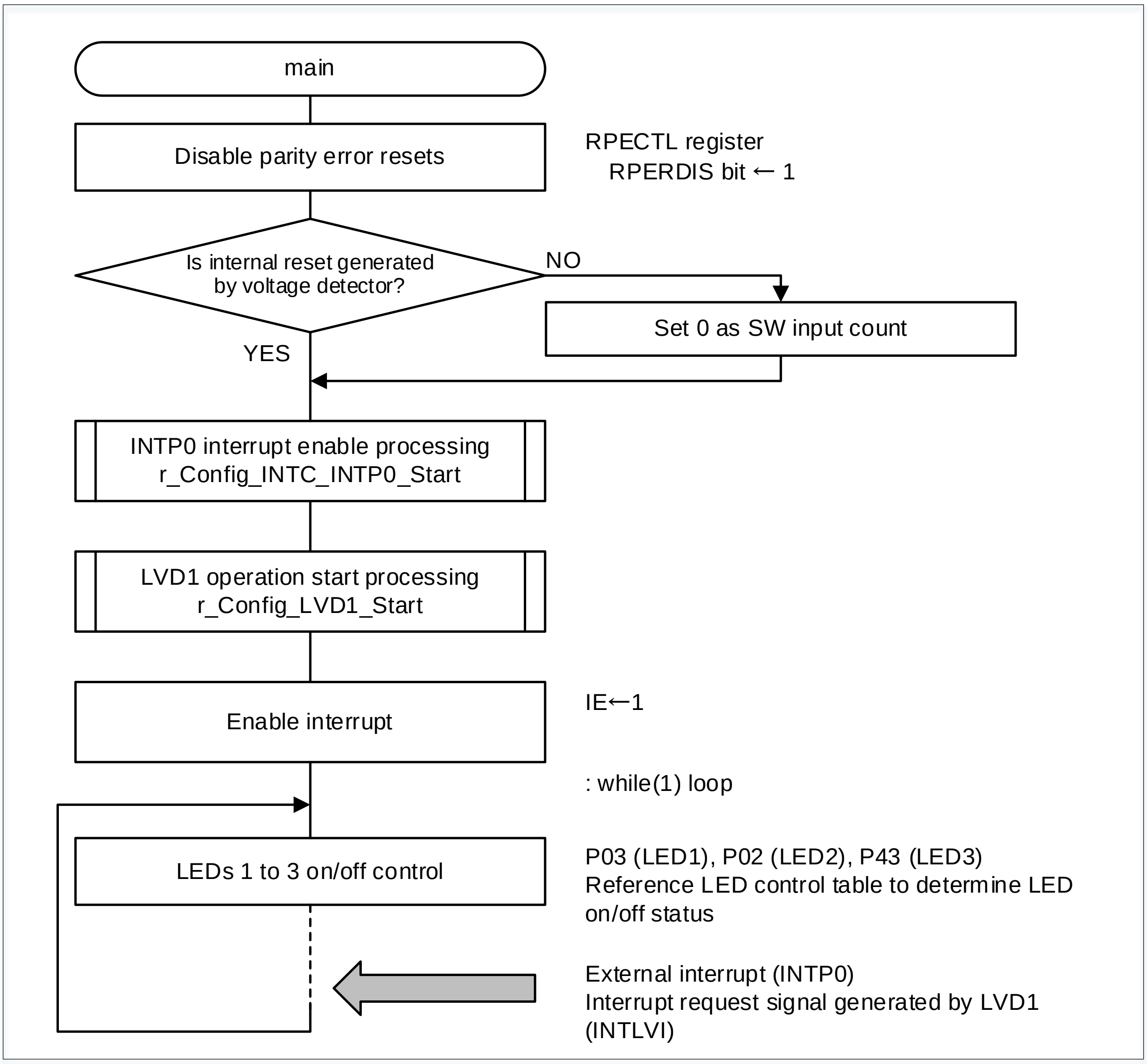
Outline	Voltage detector (LVD1) interrupt processing.
Header	r_cg_macrodriver.h, r_cg_userdefine.h
Declaration	static void __near r_lvd_interrupt (void)
Description	Changes the operating clock depending on the value of V_{DD}. When $V_{DD} < V_{LVD1}$, the high-speed on-chip oscillator clock is replaced by the subsystem clock. When $V_{DD} \geqq V_{LVD1}$, the subsystem clock is replaced by the high-speed on-chip oscillator clock.
Argument	None
Return Value	None

4.6 Flowcharts

4.6.1 Main Processing

Figure 4-1 shows the flowchart of the main processing.

Figure 4-1 Main Processing



4.6.2 Voltage Detector (LVD1) Interrupt Processing

Figure 4-2 and Figure 4-3 show flowcharts of the Voltage detector (LVD1) interrupt processing.

Figure 4-2 Voltage Detector (LVD1) Interrupt Processing. (1/2)

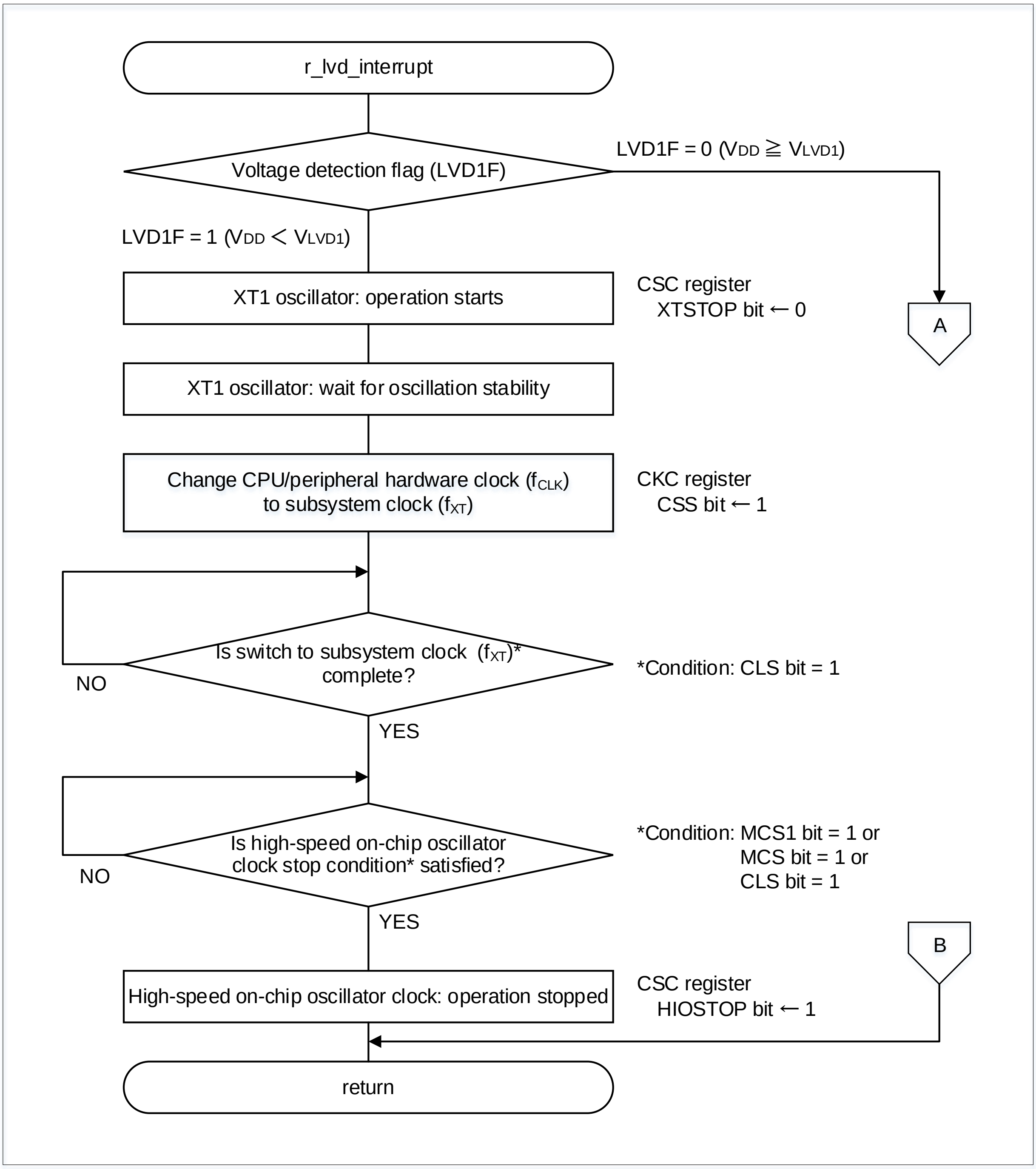
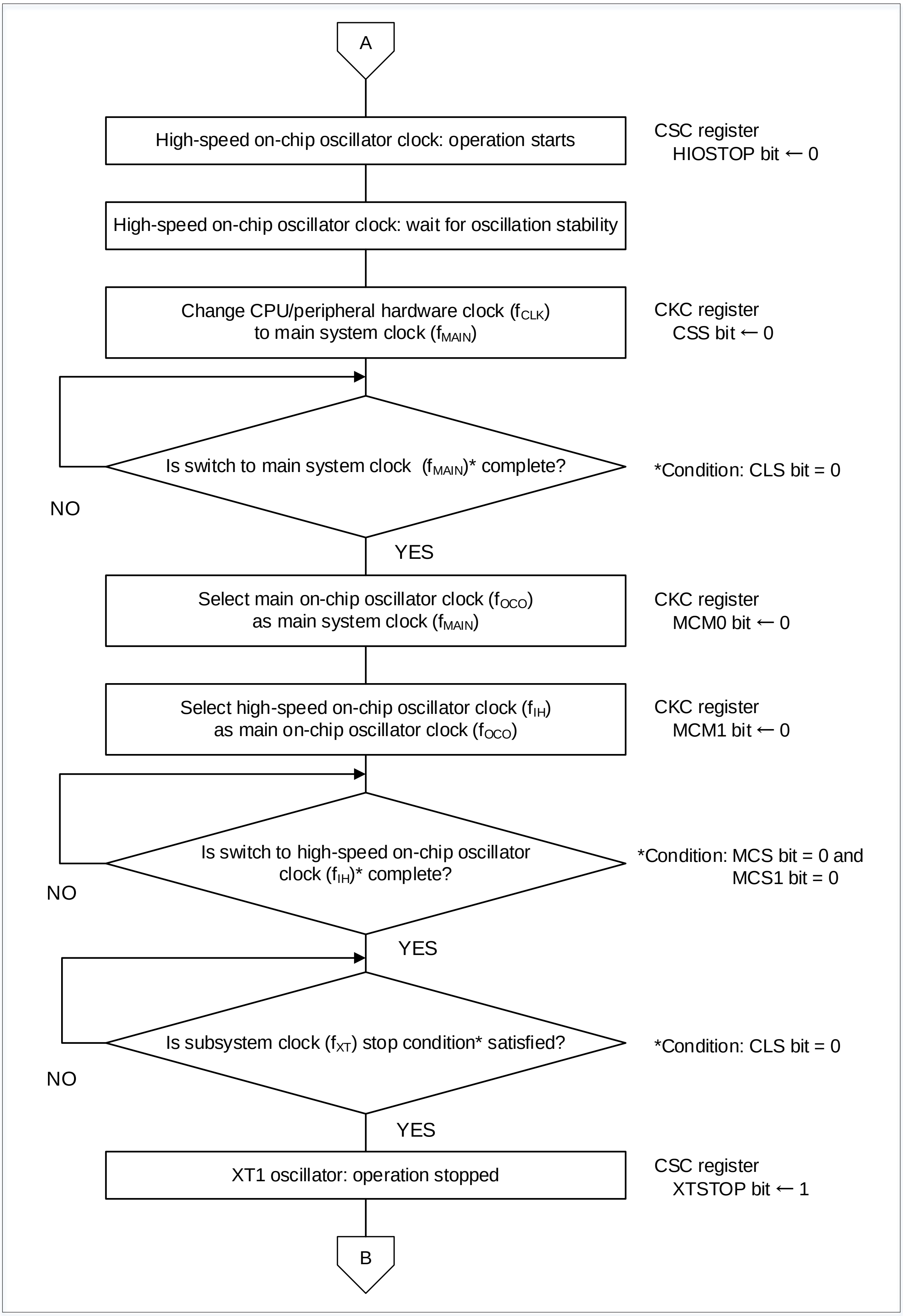


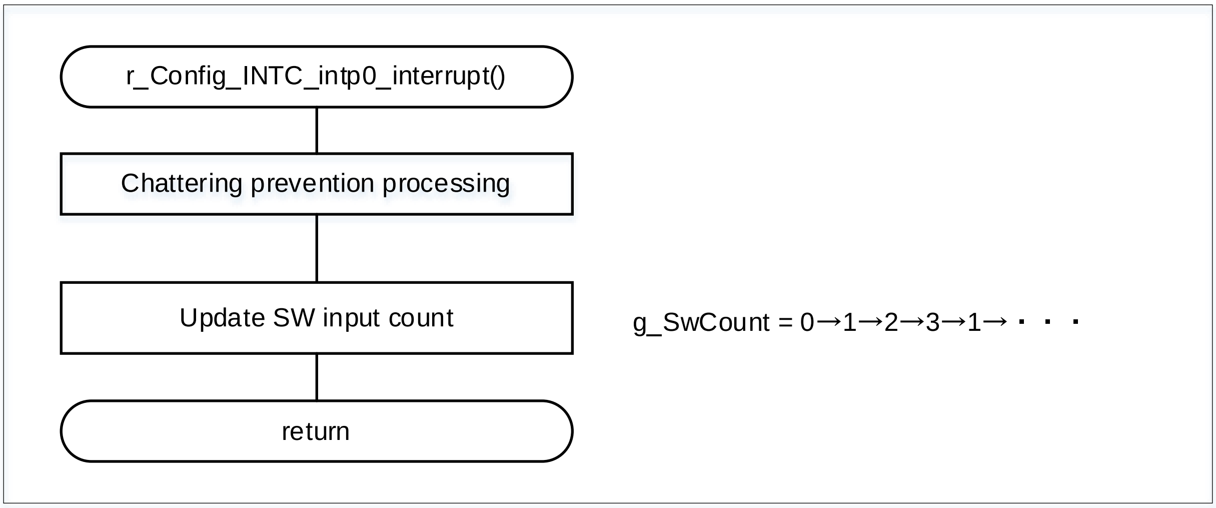
Figure 4-3 Voltage Detector (LVD1) Interrupt Processing (2/2)



4.6.3 External Interrupt (INTP0) Processing

Figure 4-4 shows the flowchart of the external interrupt (INTP0) processing

Figure 4-4 External Interrupt (INTP0) Processing



5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G23 User’s Manual: Hardware (R01UH0896J)
RL78 family user's manual software (R01US0015J)
The latest versions can be downloaded from the Renesas Electronics website.

Technical update
The latest versions can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2021.04.13	—	First Edition
1.01	2021.07.12	6	Updated the Operation Confirmation Conditions
1.02	2023.12.1	6	Updated the Operation Confirmation Conditions
		7	Figure 3-1: Reset Circuit Modification

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

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