RL78/G23

How to Use the Output Current Control Ports

Introduction

This application note describes how to use the output current control ports.

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

1.1 Overview of specifications

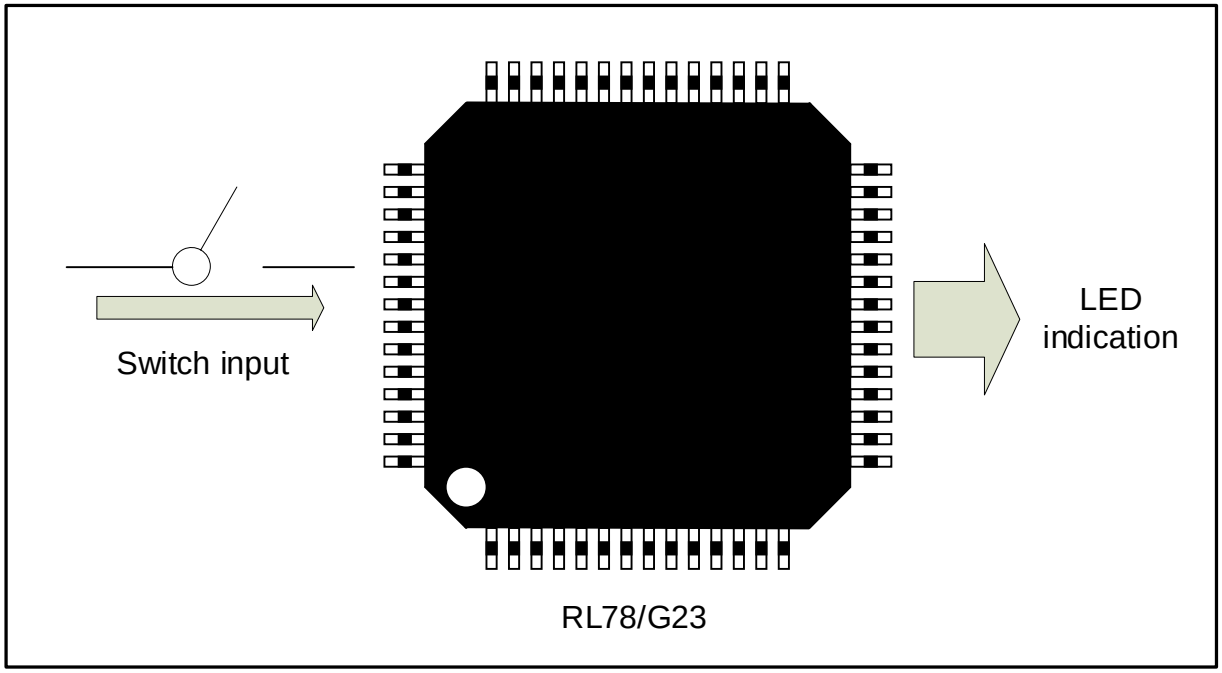
This application note describes an example of using the output current control ports. Each time the switch is pressed, the output currents of P60 and P61 are changed to shift the brightness of LEDs.

Table 1-1 lists the peripheral functions to be used and their uses, and Figure 1-1 gives an overview of the output current control port operation.

Table 1-1 Peripheral Functions Used and Their Uses

Peripheral Function	Use
Port output P60 / CCD04、P61 / CCD05	Control the brightness of the LEDs connected to P60/CCD04 and P61/CCD05 pins.
External interrupt INTP0	Receives switch input (SW1) interrupts on the edge-detecting interrupt input pin.

Figure 1-1 Overview of Output Current Control Ports



1.2 Outline of Operation

The sample code changes the output currents of the output current control ports each time the switch is pressed. Table 1-2 shows the changes in output currents.

Table 1-2 Changes in Output Currents

Operation	Output Current of P60/CCD04	Output Current of P61/CCD05
0	Hi-Z	Hi-Z
1	Output current control (2 mA)	Output current control (2 mA)
2	Output current control (5 mA)	Output current control (5 mA)
3	Output current control (10 mA)	Output current control (10 mA)
4	Output current control (15 mA)	Output current control (15 mA)
5	(Return to operation 0)	(Return to operation 0)

The major settings for this peripheral function are as follows.

（1） Initialize the output current control ports.

- Set the CCDE04 bit and CCDE05 bit in the CCDE register to 1 to enable output current control for P60 / CCD04 and P61 / CCD05.
- Set 00H in the CCS4 register and CCS5 register, and set the output of P60 / CCD04 and P61 / CCD05 to Hi-Z.
- Clear the PMCE60 bit and PMCE61 bit in the PMCE6 register (set 0), and set digital input/output for P60 / CCD04 and P61 / CCD05.
- Clear the P60 bit and P61 bit in the P6 register (set 0), and set the output of P60/CCD04 and P61 / CCD05 to 0.
- Clear the PM60 bit and PM61 bit in the PM6 register (set 0), and place P60 / CCD04 and P61 / CCD05 in output mode.

（2） Initialize the edge-detecting external interrupt pin.

- Clear the EGN0 bit in the EGN0 register (set 0), set the EGP0 bit in the EGP0 register to 1, and set the falling edge as the valid edge for the INTP0 pin.
- To determine whether switch input is made, the voltage applied to the pin is checked approximately every 5 ms. When the applied voltages match 2 consecutive times, the switch input is determined to be valid (this step is required to remove chattering).

2. Operation Confirmation Conditions

The operation of the sample code provided with this application note has been tested under the following conditions.

Table 2-1 Operation Confirmation Conditions

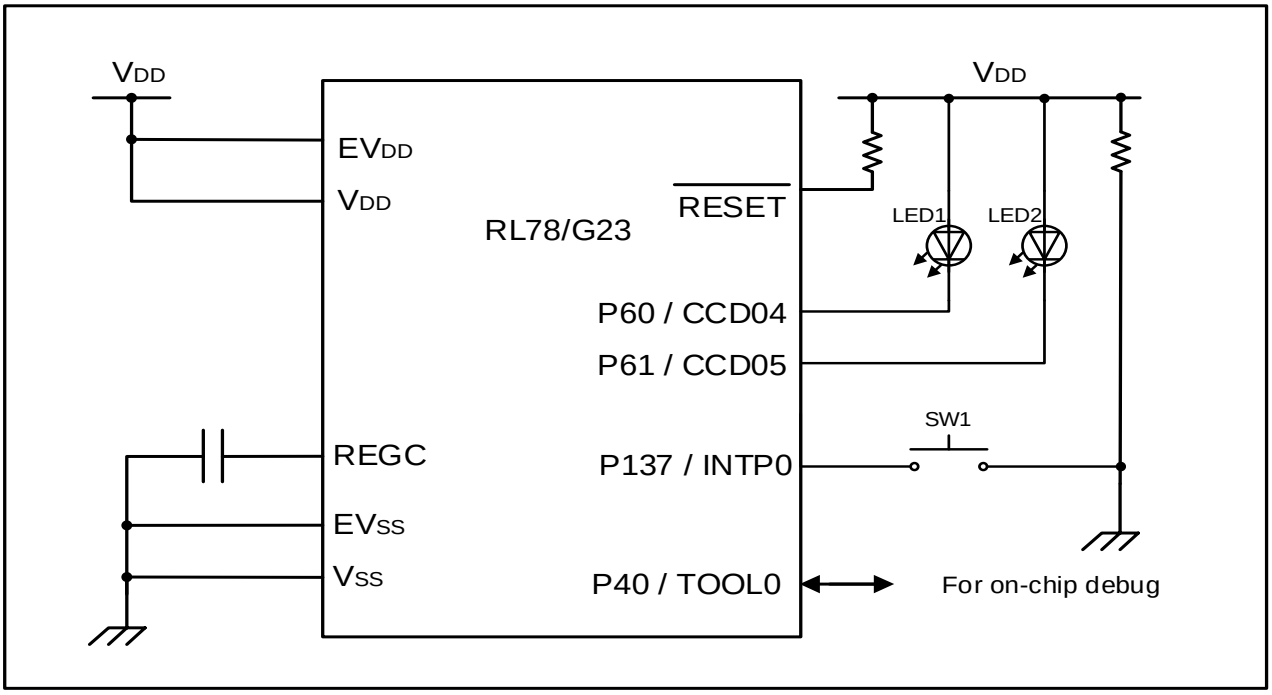
Item	Description
MCU used	RL78/G23 (R7F100GLG)
Board used	RL78/G23-64p Fast Prototyping Board (RTK7RLG230CLG000BJ)
Operating frequency	High-speed on-chip oscillator clock (f_{IH}): 32 MHz
Operating voltage	5.0 V (can be operated at 2.0 V to 5.5 V) LVD0 operations (V_{LVD0}): Reset mode At rising edge TYP. 1.90 V (1.84 V to 1.95 V) At falling edge TYP. 1.86 V (1.80 V to 1.91 V)
Integrated development environment (CS+)	CS+ for CC E8.09.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.12.00 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2studio V2023-04 (23.4.0) from Renesas Electronics Corp.
C compiler (e2studio)	CC-RL V1.12.00 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.2 from IAR Systems Corp.
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V4.21.2.2420 from IAR Systems Corp.
Smart configurator (SC)	V1.6.0 from Renesas Electronics Corp.
Board support package (BSP)	V1.60 from Renesas Electronics Corp.

3. Hardware Descriptions

3.1 Example of Hardware Configuration

Figure 3-1 shows an example of the hardware configuration used in the application note.

Figure 3-1 Hardware Configuration



Note 1. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes appropriate pin handling and meets electrical characteristic requirements (connect each input-only port to V_{DD} or V_{SS} through a resistor.)

Note 2. Connect any pins whose name begins with EV_{SS} to V_{SS}, and any pins whose name begins with EV_{DD} to V_{DD}, respectively.

Note 3. V_{DD} must not be lower than the reset generation voltage (V_{LVD0}) that is specified for the LVD0.

3.2 List of Pins to be Used

Table 3-1 lists the pins to be used and their functions.

Table 3-1 Pins to be Used and Their Functions

Pin name	I/O	Function
P60 / CCD04	Output	Output current control port
P61 / CCD05	Output	Output current control port
P137 / INTP0	Input	Input pin for the switch (SW) (external interrupt request input pin)

Caution In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software Explanation

4.1 Setting of Option Byte

Table 4-1 shows the option byte settings.

Table 4-1 Option Byte Settings

Address	Setting Value	Contents
000C0H / 040C0H	11101111B	Disables the watchdog timer. (Counting stopped after reset)
000C1H / 040C1H	11111110B	LVD0 detection voltage: reset mode At rising edge TYP. 1.90 V (1.84 V to 1.95 V) At falling edge TYP. 1.86 V (1.80 V to 1.91 V)
000C2H / 040C2H	11101000B	HS mode, High-speed on-chip oscillator clock (f_{IH}): 32 MHz
000C3H / 040C3H	10000100B	Enables on-chip debugging

4.2 List of Constants

Table 4-2 lists the constants that are used in the sample code.

Table 4-2 Constants

Constant Name	Setting Value	Description
WAITCOUNT_32M	8000	Wait count for 5 ms when the MCU operates in HS mode at 32 MHz

4.3 List of Variables

Table 4-3 lists global variables.

Table 4-3 Global Variables

Type	Variable Name	Description	Function Used
uint8_t	s_ccs_index	CCSn register setting value index	r_Config_INTC_intp0_interrupt

4.4 List of Functions

Table 4-4 shows a list of functions.

Table 4-4 Functions

Function Name	Outline
R_Config_PORT_Create_UserInit()	Port initialization processing (defined by the user)
r_Config_INTC_intp0_interrupt()	External interrupt (INTP0) processing.

4.5 Specification of Functions

The function specifications of the sample code are shown below.

R_Config_PORT_Create_UserInit()	
Outline	Port initialization processing (defined by the user)
Header	Config_PORT.h
Declaration	void R_Config_PORT_Create_UserInit(void)
Description	Sets P60 / CCD04 and P61 / CCD05 as output current control ports.
Argument	None
Return Value	None

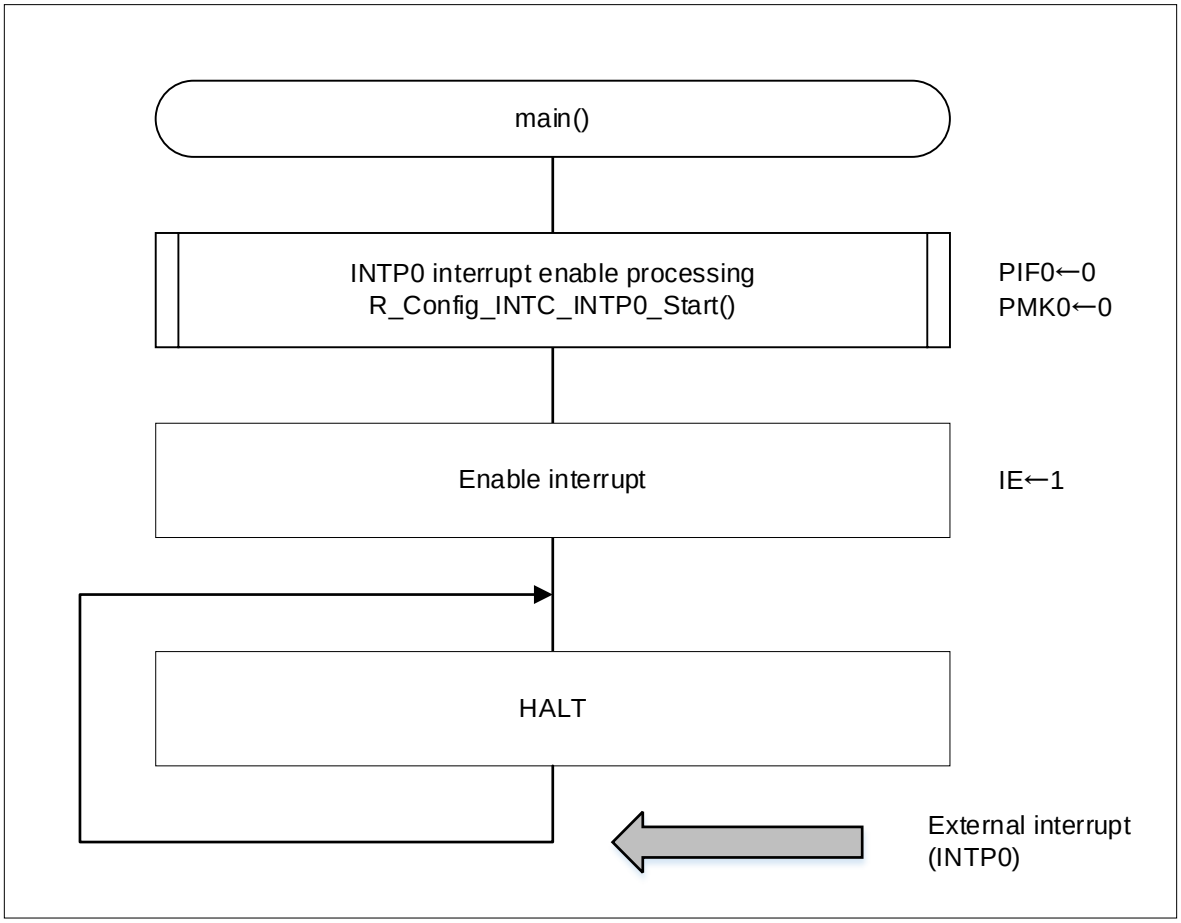
r_Config_INTC_intp0_interrupt()	
Outline	External interrupt (INTP0) processing.
Header	Config_INTC.h
Declaration	static void __near r_Config_INTC_intp0_interrupt(void)
Description	Increments s_ccs_index and sets the corresponding CCSn register setting values in the CCS4 register and CCS5 register after chattering removal processing.
Argument	None
Return Value	None

4.6 Flowcharts

4.6.1 Main Processing

Figure 4-1 shows the flowchart of the main processing in this application note.

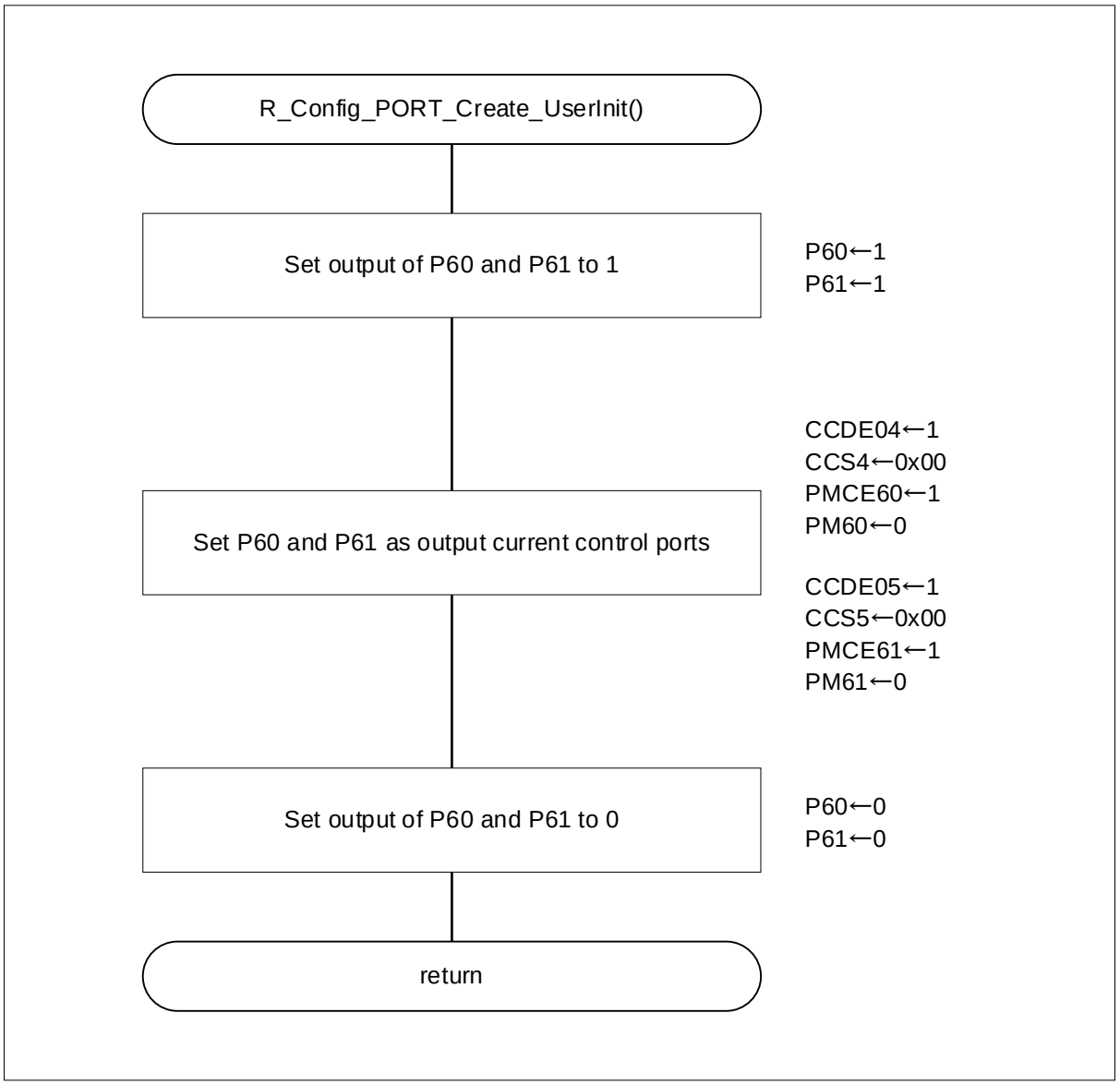
Figure 4-1 Main Processing



4.6.2 Port Initialization Processing (Defined by the User)

Figure 4-2 shows the flowchart of the port initialization processing (defined by the user).

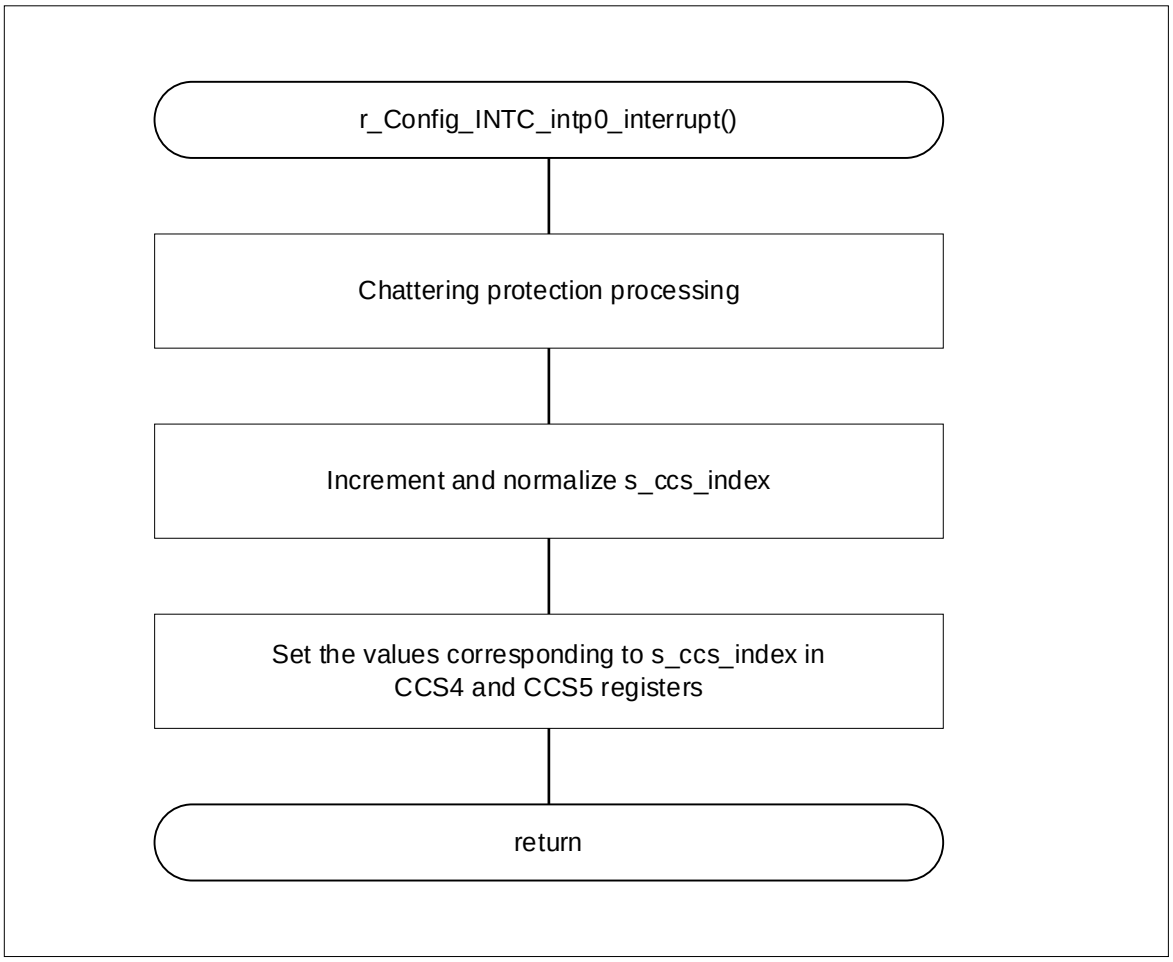
Figure 4-2 Port Initialization Processing (Defined by the User)



4.6.3 External Interrupt (INTP0) Processing

Figure 4-3 shows the flowchart of the external interrupt (INTP0) processing.

Figure 4-3 External Interrupt (INTP0) Processing



5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G23 User’s Manual: Hardware (R01UH0896)
RL78 family user's manual software (R01US0015)
The latest versions can be downloaded from the Renesas Electronics website.

Technical update
The latest versions can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2021.04.13	—	First Edition
1.01	2021.07.12	5	Updated the Operation Confirmation Conditions
1.02	2023.10.6	5	Updated the Operation Confirmation Conditions

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1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

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