RL78/G23

ELCL Edge Detection Thinning Function

Introduction

This application note describes how to use the logic and event link controller (ELCL) to thin out edge detection on an input signal. By using ELCL, the functions realized by software can be realized by hardware, and resources (ROM, RAM, etc.) can be reduced.

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

This application note describes an example of using ELCL to thin out the edge detection of the input signal and enable the input signal once every two times.

Figure 1-1 shows the system configuration for thinning edge detection using ELCL. The external input signal is INPUT A, the clock that creates the thinning interval is CLOCK B, and the thinned output signal is OUTPUT C.

Edge detection of the input signal from INPUT A is masked the first time and enabled the second time.

Figure 1-1 System Configuration

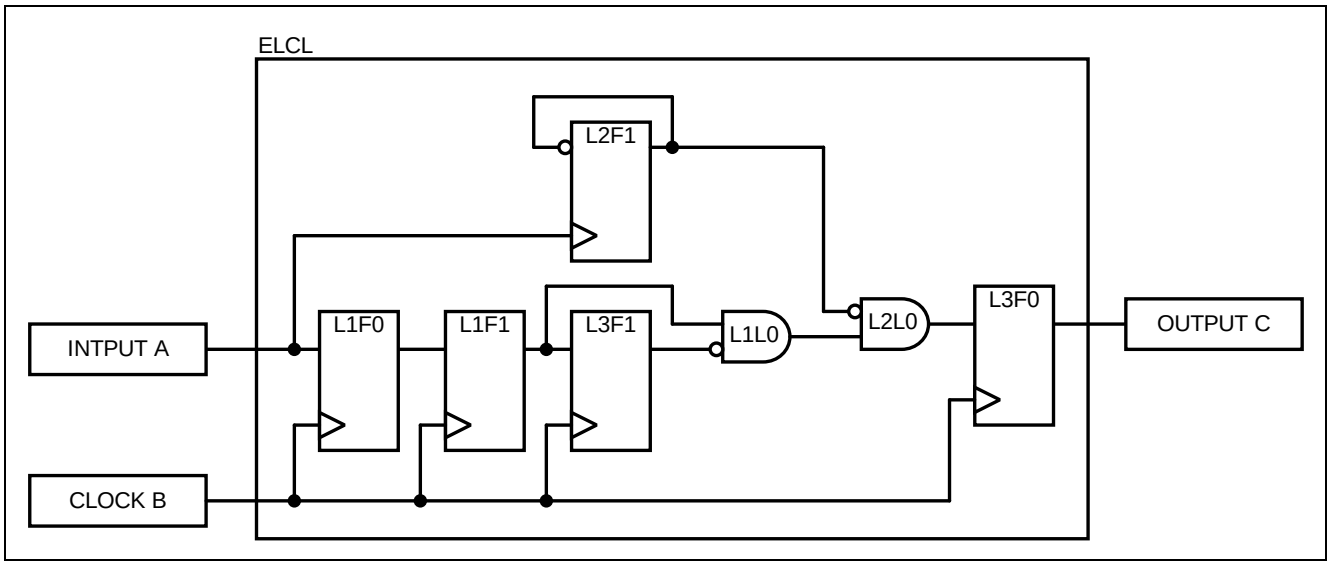
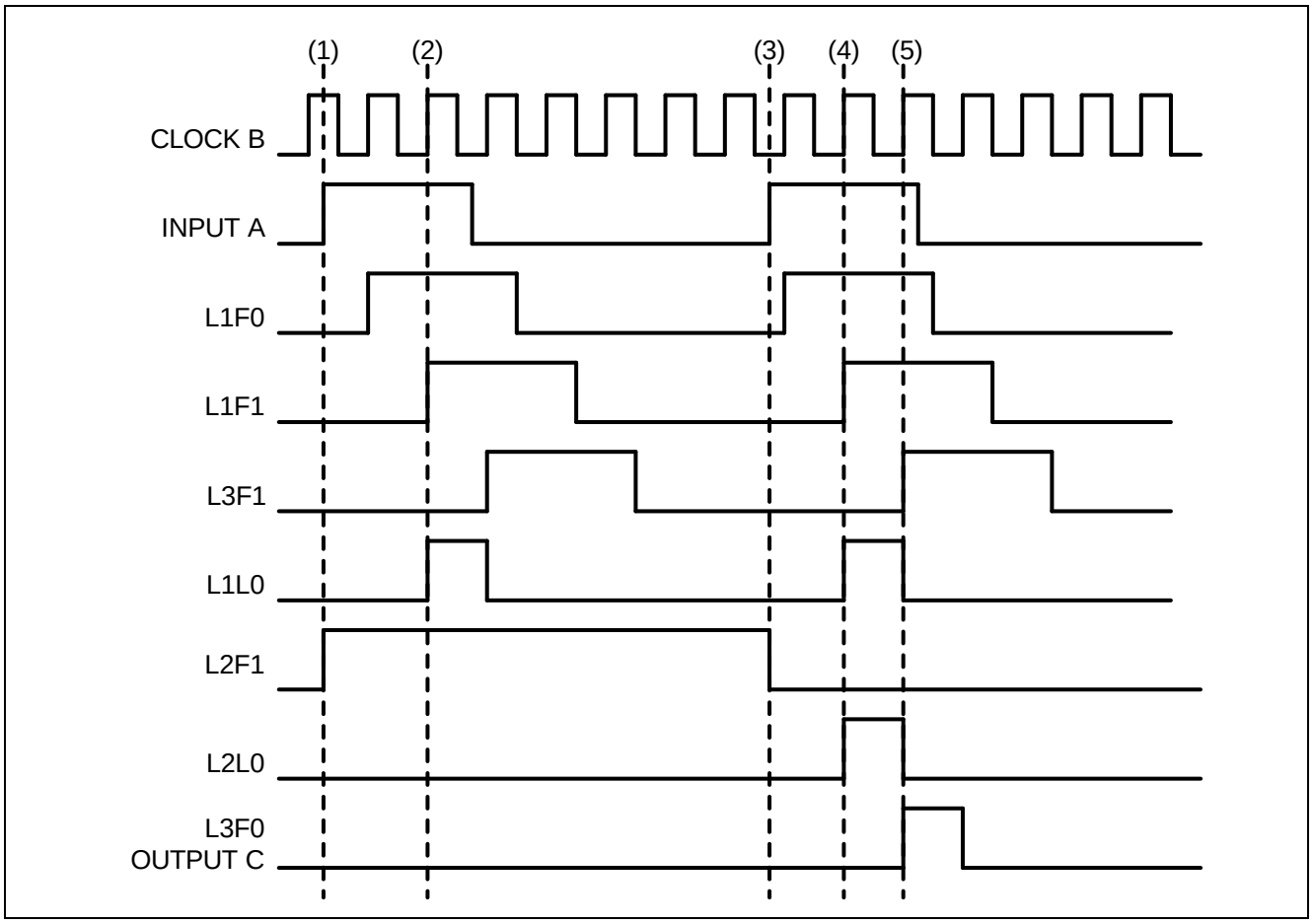


Figure 1-2 shows the timing chart of Figure 1-1.

(1) Inputs the pulse signal from input A (first time)
(2) Detects rising edges
(3) Inputs the pulse signal from input A (second time)
(4) Detects rising edges
(5) Outputs a pulse signal from output C.

Figure 1-2 Timing chart of Edge detection thinning



2. Conditions for Operation Confirmation Test

The sample code with this application note runs properly under the condition below.

Table 2-1 Operation Confirmation Conditions

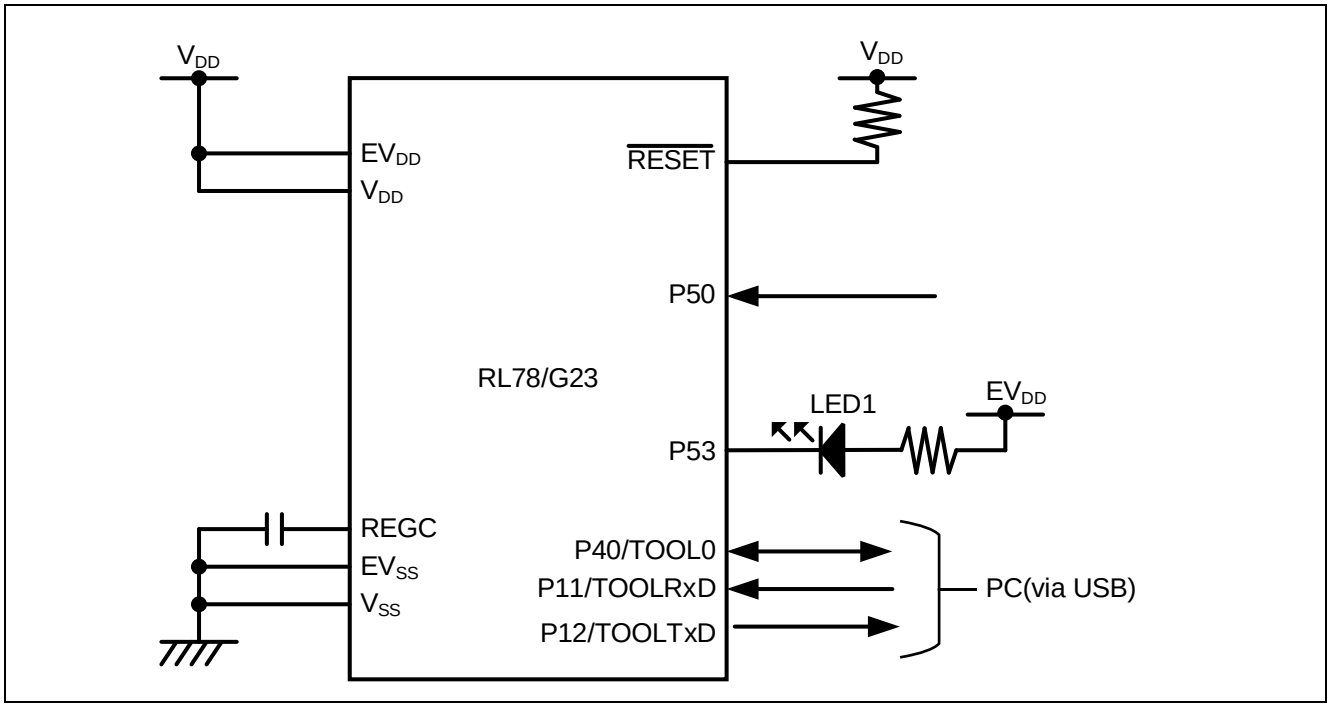
Items	Contents
MCU	RL78/G23 (R7F100GLG)
Operating frequencies	• High-speed on-chip oscillator clock: 16 MHz • CPU/peripheral hardware clock: 16 MHz
Operating voltage	• 3.3V • LVD0 operations (V_{LVD0}) : Reset mode Rising edge TYP.1.90V Falling edge TYP.1.86V
Integrated development environment (CS+)	CS+ for CC V8.07.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.11 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio 2022-01 (22.01.0) from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.11 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.1 from IAR Systems
C compiler (IAR)	
Smart Configurator	V.1.2.0
Board support package (r_bsp)	V.1.13
Emulator	CS＋, e^2 studio: COM port IAR: E2 Emulator Lite
Board	RL78/G23 Fast Prototyping Board (RTK7RLG230CLG000BJ)

3. Hardware

3.1 Example of Hardware Configuration

Figure 3-1 shows an example of the hardware configuration in this application.

Figure 3-1 Hardware Configuration



Caution 1. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements. (Connect each input-only port to V_{DD} or V_{SS} through a resistor.)

Caution 2. Connect the EV_{SS} pin to V_{SS} and the EV_{DD} pin to V_{DD}.

Caution 3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD0}) that is specified as LVD.

3.2 Used Pins

Table 3-1 shows list of used pins and assigned functions.

Table 3-1 List of Pins and Functions

Pin name	Input/Output	Function
P53	Output	LED1 lights (Low Active)
P50	Input	Input pin

Caution. In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software

4.1 Overview of the sample program

This sample code detects the edge of the input signal to the P50 pin and enables the edge once every two times.

Figure 4-1 shows the system configuration of the sample code, and Figure 4-2 shows the timing chart.

Select P50 as the ELCL input signal and INTELCL as the ELCL output signal.

Figure 4-1 System configuration of the sample code

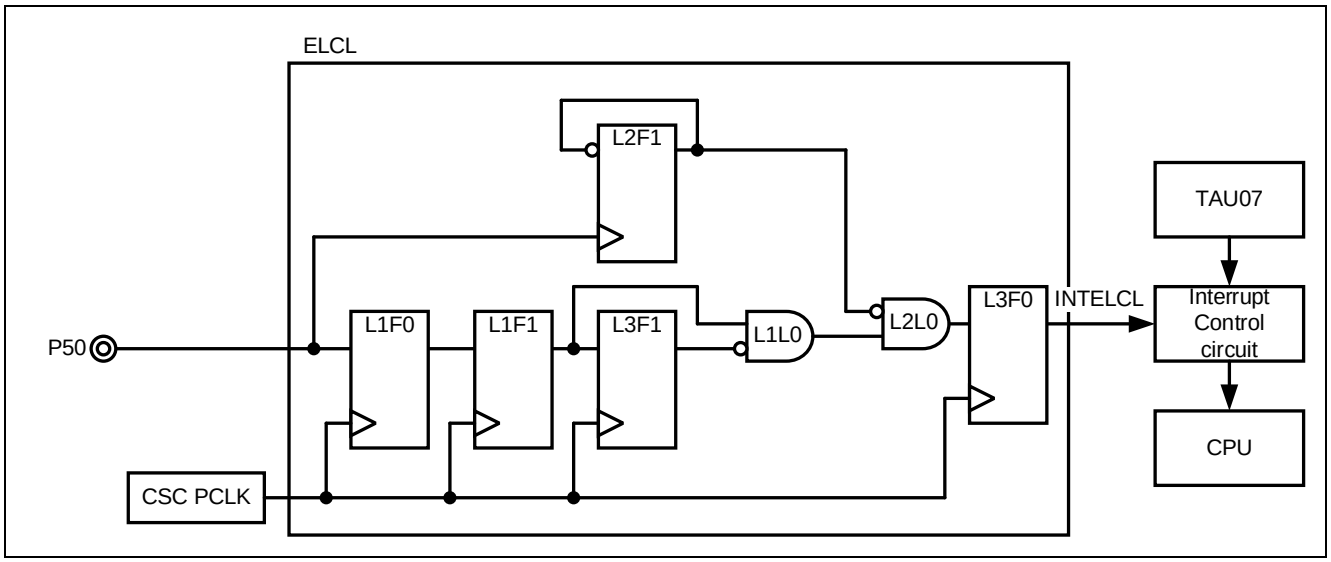
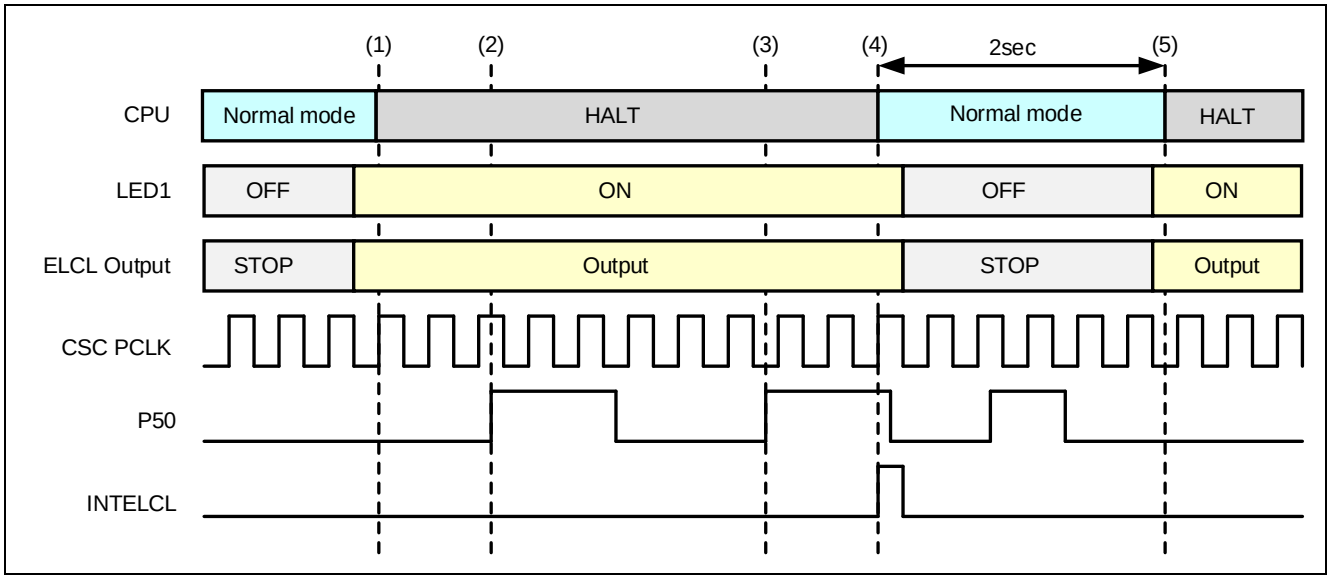


Figure 4-2 Timing chart of the sample code



(1) Turns on LED1 and enables to output of ELCL output signal, and shifts to HALT mode.
(2) Detects the edge when a pulse signal inputs to P50. (first time) HALT mode is not canceled because INTELCL is not output.
(3) Detects the edge when a pulse signal inputs to P50. (second time)
(4) Outputs INTELCL and cancels HALT mode. Turns off LED1 and disables ELCL output.
(5) After about 2 seconds has passed, initializes the ELCL settings and return to (1).

During the period from (4) to (5), INTELCL does not occur because the ELCL output stops even if a pulse signal is input to P50.

4.2 Folder Configuration

Table 4-1 shows folder configuration of source file and header files using by sample code except the files generated by integrated development environment and the files in the bsp environment.

Table 4-1 Folder configuration

Folder/File configuration	Outline	Created by Smart configurator
¥r01an5613_elcl_edge<DIR>Note 3	Root folder of this sample code	
¥src<DIR>	Folder for program source	
main.c	Sample code source file	
¥smc_gen<DIR>	Folder created by Smart Configurator	√
¥Config_EdgeDetectionThinningFunction<DIR>	Folder for ELCL program	√
Config_EdgeDetectionThinningFunction.c	Source file for ELCL	√
Config_EdgeDetectionThinningFunction.h	Header file for ELCL	√
Config_EdgeDetectionThinningFunction_user.c	Interrupt source file for ELCL	√Note 2
¥Config_PORT<DIR>	Folder for PORT program	√
Config_PORT.c	Source file for PORT	√
Config_PORT.h	Header file for PORT	√
Config_PORT_user.c	Interrupt source file for PORT	√Note 1
¥Config_TAU0_7<DIR>	Folder for TAU0 channel 7 program	√
Config_TAU0_7.c	Source file for TAU0 channel 7	√
Config_TAU0_7.h	Header file for TAU0 channel 7	√
Config_TAU0_7_user.c	Interrupt source file for TAU0 channel 7	√Note 2
¥general<DIR>	Folder for initialize or common program	√
¥r_bsp<DIR>	Folder for BSP program	√
¥r_config<DIR>	Folder for program	√

Note. <DIR> means directory.

Note 1. Not used in this sample code.

Note 2. Added the interrupt handling routine to the file generated by the Smart Configurator.

Note 3. The IAR version of the sample code contains r01an5613_elcl_edge.ipcf. For the ipcf file, refer to "RL78 Smart Configurator User Guide: IAR (R20AN0581)".

4.3 Option Byte Settings

Table 4-2 shows the option byte settings.

Table 4-2 Option Byte Settings

Address	Setting Value	Contents
000C0H/040C0H	1110 1111B (EFH)	Operation of Watchdog timer is stopped (counting is stopped after reset)
000C1H/040C1H	1111 1110B (FEH)	LVD0 operating mode: reset mode Detection voltage: Rising edge 1.90V Falling edge 1.86V
000C2H/040C2H	1110 1001B (E9H)	Flash operating mode: HS mode High-speed on-chip oscillator clock: 16MHz
000C3H/040C3H	1000 0101B (85H)	On-chip debugging is enabled

4.4 Constants

Table 4-3 shows the constants that are used in this sample code.

Table 4-3 Constants used in the sample code

Constant Name	Setting Value	Contents	File
LED1	P5_bit.no3	P53	main.c
LED_ON	0	Setting value for turning on the LED	main.c
LED_OFF	1	Setting value for turning off the LED	main.c
WAIT_TIME	2000	Interval to transition to HALT mode again after HALT mode release (every 2 seconds)	main.c

4.5 Variables

Table 4-4 shows the global variables used in this sample code.

Table 4-4 Global variables used in the sample code

Type	Variable name	Contents	Functions used in
volatile uint16_t	g_ms_timer	Count value of the wait process	r_ms_delay, r_Config_TAU0_7_interrupt
uint8_t	g_elcl_interrupt	ELCL interrupt occurrence flag	main r_Config_EdgeDetectionThinningFunction_interrupt

4.6 Functions

Table 4-5 shows the functions used in the sample code. However, the unchanged functions generated by the Smart Configurator are excluded.

Table 4-5 Functions

Function name	Outline	Source file
main	Main process	main.c
r_Config_EdgeDetectionThinningFunction_interrupt	ELCL interrupt process (For HALT mode release)	Config_EdgeDetectionThinningFunction_user.c
r_elcl_reset_flipflop	ELCL flip-flop reset process	Config_EdgeDetectionThinningFunction_user.c
r_ms_delay	Wait process after HALT mode is released (For HALT mode interval)	Config_TAU0_7_user.c
r_Config_TAU0_7_interrupt	TAU0 channel 7 interrupt process (For HALT mode interval)	Config_TAU0_7_user.c

4.7 Function Specifications

This part describes function specifications of the sample code.

[Function name] main

Outline	Main process
Header	r_smc_entry.h
Declaration	void main (void);
Description	This function initializes ELCL, sets ELCL output and sets interrupts. Turns on LED1 and shifts to HALT mode. When a pulse is input to P50 twice, HALT mode is canceled, LED1 turns off, and the flip-flop is initialized. After the time set by WAIT_TIME (about 2 seconds) has passed, CPU shifts to the HALT mode again.
Arguments	None
Return value	None
Remarks	None

[Function name] r_Config_EdgeDetectionThinningFunction_interrupt

Outline	ELCL interrupt process
Header	platform.h
Declaration	#pragma interrupt r_Config_EdgeDetectionThinningFunction_interrupt (vect=INTELCL)
Description	Sets g_elcl_interrupt = 1
Arguments	None
Return value	None
Remarks	None

[Function name] r_elcl_reset_flipflop

Outline	ELCL flip-flop reset process
Header	platform.h
Declaration	void r_elcl_reset_flipflop (void);
Description	This function initializes the flip-flops in the ELCL.
Arguments	None
Return value	None
Remarks	Flip-flops are reset when bit 6 and bit 7 of ELLnCTL are set to 0.

[Function name] r_ms_delay

Outline	Wait process
Header	r_cg_macrodriver.h, r_cg_userdefine.h, Config_TAU0_7.h
Declaration	void r_ms_delay (uint16_t msec);
Description	This function waits for the time (ms) specified by the argument msec. This function counts using channel 7. Polls if g_ms_timer is less than WAIT_TIME, completes wait process if more than WAIT_TIME.
Arguments	Msec
Return value	None
Remarks	None

[Function name] r_Config_TAU0_7_interrupt

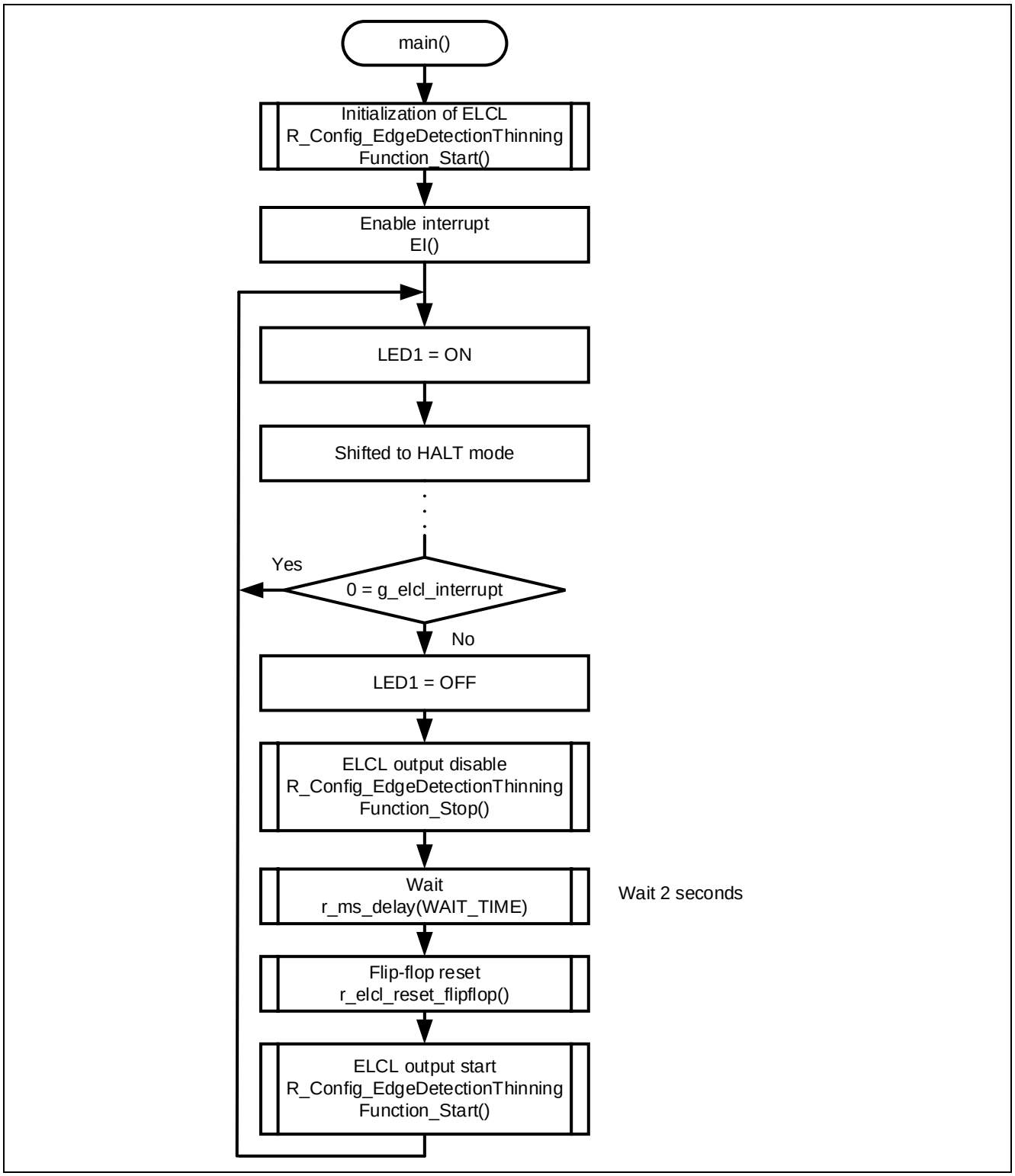
Outline	TAU0 channel 7 interrupt process
Header	r_cg_macrodriver.h, r_cg_userdefine.h, Config_TAU0_7.h
Declaration	#pragma interrupt r_Config_TAU0_7_interrupt (vect=INTTM07)
Description	This function is an interrupt process by INTTM07 on TAU0 channel 7. After HALT mode release, count the time until the transition to the HALT mode again.
Arguments	None
Return value	None
Remarks	None

4.8 Flow Charts

4.8.1 Main Process

Figure 4-3 shows flowchart of main process.

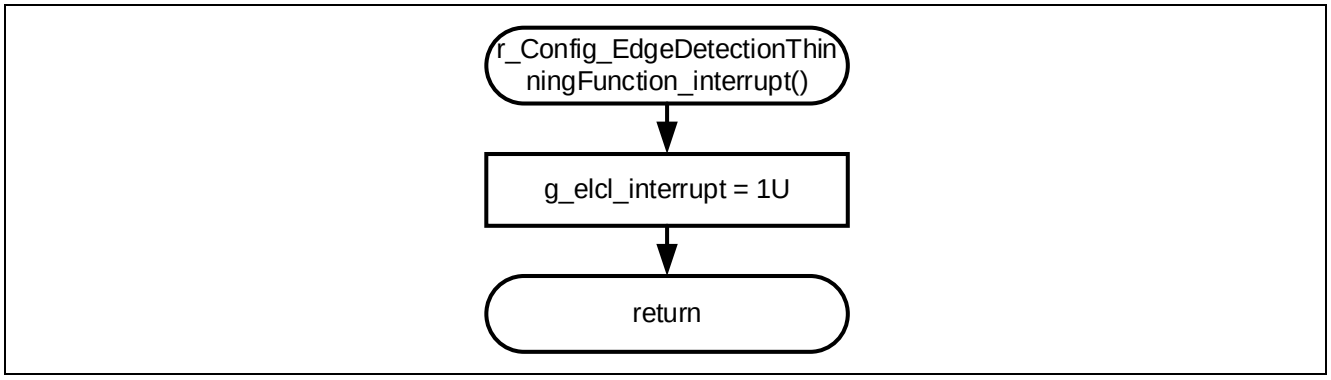
Figure 4-3 Main process



4.8.2 ELCL interrupt process

Figure 4-4 shows the flow chart for ELCL interrupt processing.

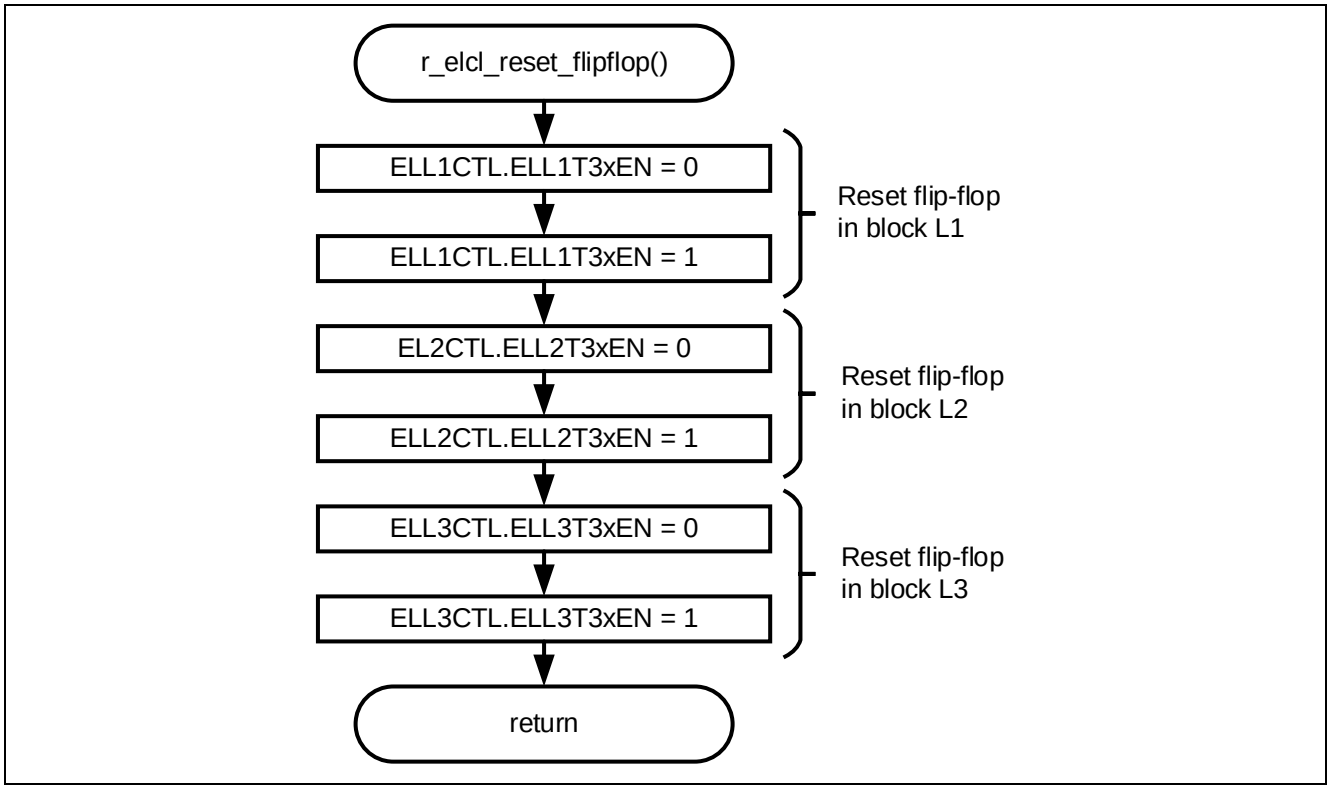
Figure 4-4 ELCL interrupt process



4.8.3 ELCL flip-flop reset process

Figure 4-5 shows the flow chart for ELCL flip-flop reset process.

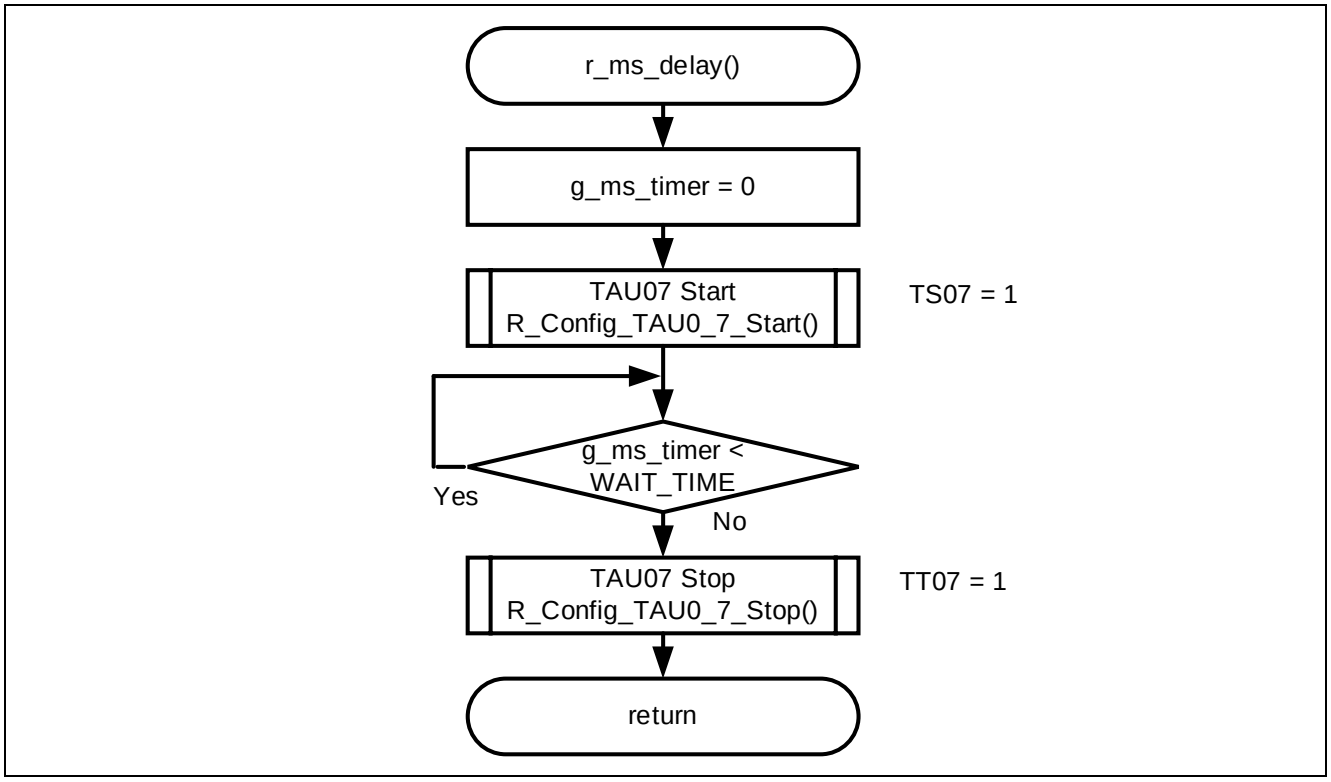
Figure 4-5 ELCL flip-flop reset process



4.8.4 Wait process

Figure 4-6 shows the flow chart for wait processing.

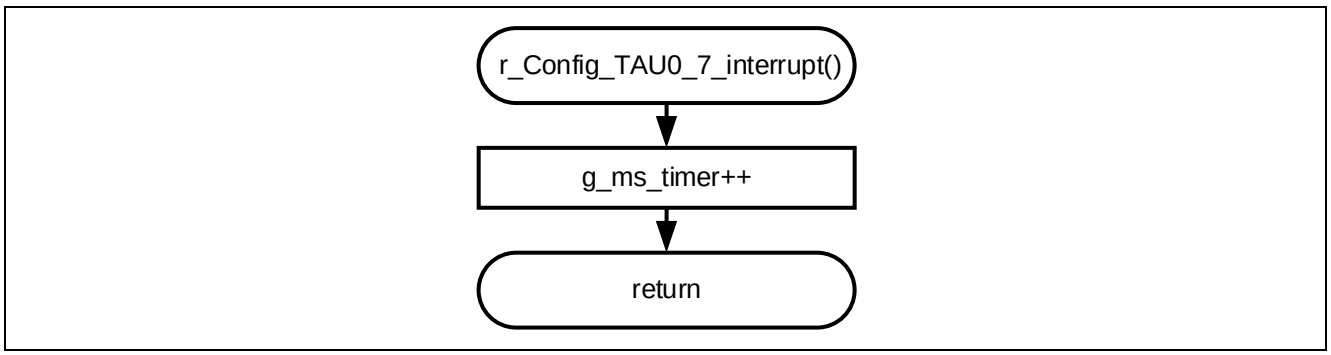
Figure 4-6 Wait process



4.8.5 TAU0 channel 7 interrupt process

Figure 4-7 shows the flow chart for interrupt processing of TAU0 channel 7.

Figure 4-7 TAU0 channel 7 interrupt process



5. Application example

In addition to the sample code, this application note contains the following Smart Configurator configuration files

r01an5613_elcl_edge.scfg

The following is a description of the file and examples of settings and notes for use.

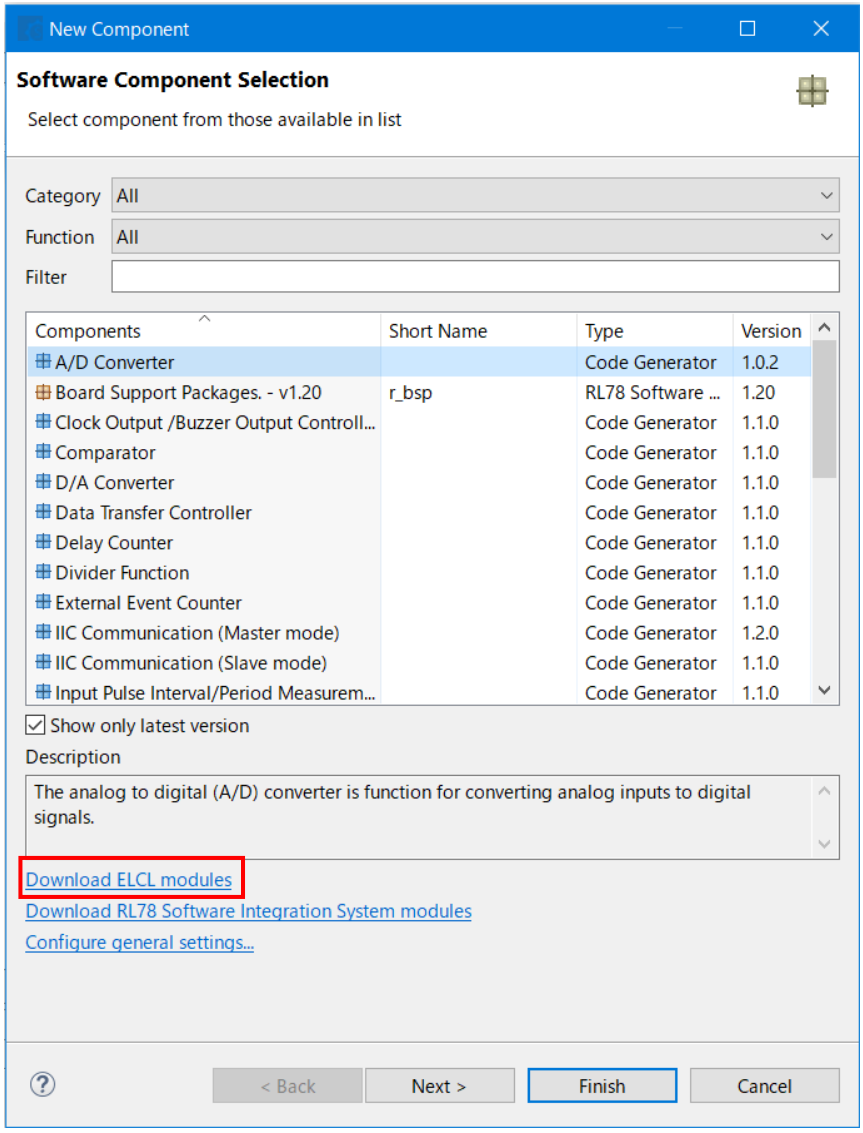
5.1 Setting up the ELCL components

To use the ELCL component, you need to install the ELCL content file.

The procedure is shown below.

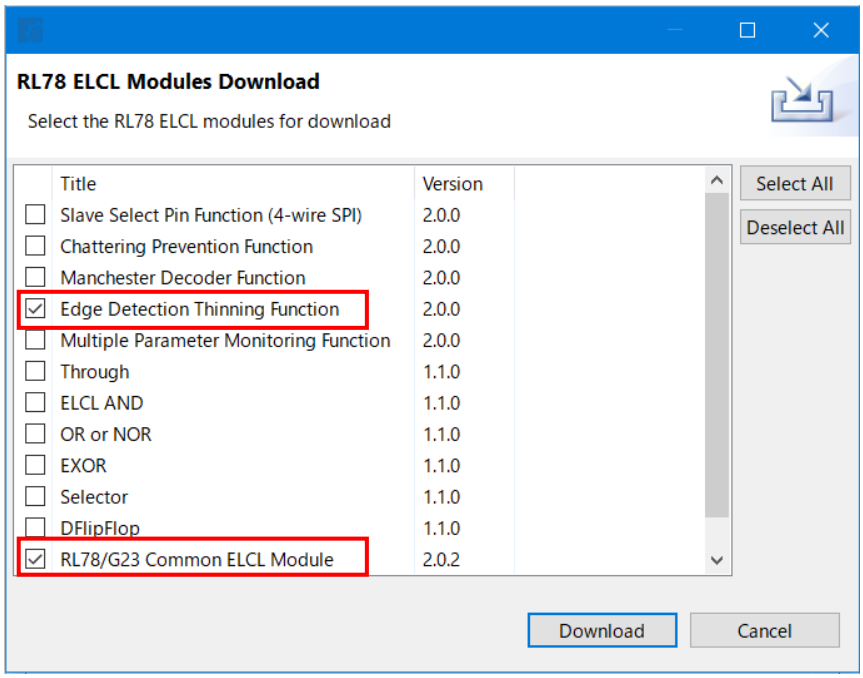
1. Start the Smart Configurator.
2. Click on the "Components" tag, and then click "Add component".
3. When the "New Component" window shown in Figure 5-1 opens, click on "Download ELCL modules".

Figure 5-1 Add component



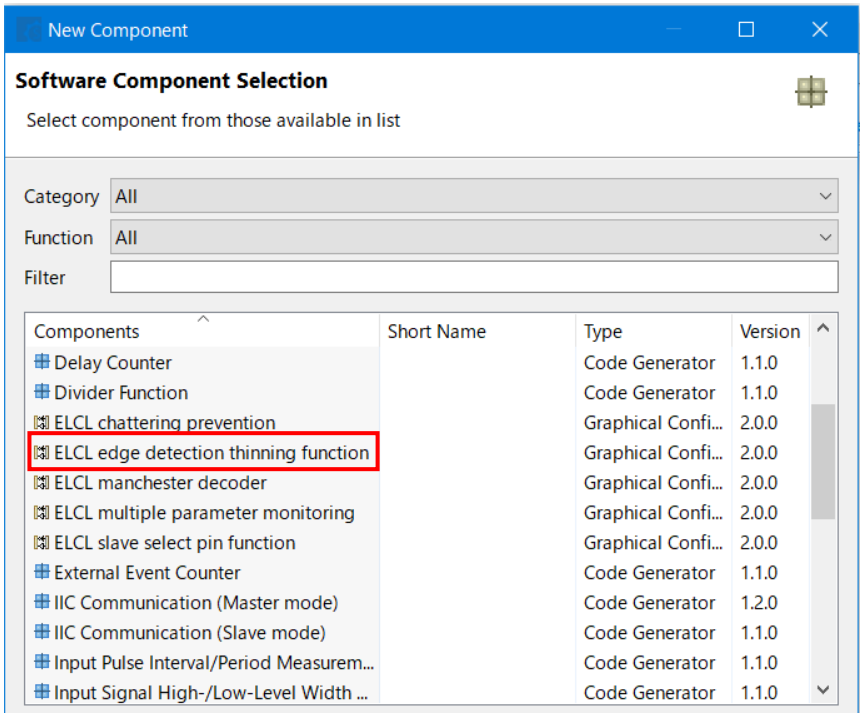
4. Select "Edge Detection Thinning Function" and download it. Please download the common setting file "RL78/G23 Common ELCL Module" as well.

Figure 5-2 Download the module



5. After the download is complete, make sure that "ELCL edge detection thinning function" is available for selection.

Figure 5-3 Select the module



5.2 r01an5613_elcl_edge.scfg

This is the Smart Configurator configuration file used in the sample code. It contains all the features configured in the Smart Configurator. The sample code settings are as follows.

Table 5-1 Parameters of Smart Configurator (1/2)

Tag name	Component	Contents
Clocks	-	Operation mod: High-speed main mode 2.4 (V)~5.5 (V) EV_{DD} setting: $1.8V \leqq EV_{DD0} < 5.5V$ High-speed on-chip oscillator: 16MHz f_{IHP}: 16MHz f_{CLK}: 16MHz (High-speed on-chip oscillator) f_{SXP}: 32.768kHz (Low-speed on-chip oscillator)
System	-	On-chip debug operation setting: COM port Note Pseudo-RRM/DMM function setting: Used Start/Stop function setting: Unused Trace function setting: Used Security ID setting: Use security ID Security ID：0x00000000000000000000 Security ID authentication failure setting: Do not erase flash memory data
Components	r_bsp	Start up select : Enable (use BSP startup) Control of invalid memory access detection : Disable RAM guard space (GRAM0-1) : Disabled Guard of control registers of port function (GPORT) : Disabled Guard of registers of interrupt function (GINT) : Disabled Guard of control registers of clock control function, voltage detector, and RAM parity error detection function (GCSC) : Disabled Data flash access control (DFLEN) : Disables Initialization of peripheral functions by Code Generator/Smart Configurator : Enable API functions disable : Enable Parameter check enable : Enable Setting for starting the high-speed on-chip oscillator at the times of release from STOP mode and of transitions to SNOOZE mode : High-speed Enable user warm start callback (PRE) : Unused Enable user warm start callback (POST) : Unused Watchdog Timer refresh enable : Unused
	Config_LVD0	Operation mode setting: Reset mode Voltage detection setting: Reset generation level (V_{LVD0}): 1.86 (V)
	Config_TAU0_7	Components: Interval timer Operating mode: 16 bit count mode Resource: TAU0_7 Operation clock: CK00 Clock source: f_{CLK} Interval value: 1 ms Interrupt setting: use Priority: Level 3

Table 5-2 Parameters of Smart Configurator (2/2)

Tag name	Component	Contents
Components	Config_EdgeDetectionThinningFunction	Components: ELCL edge detection thinning function Input signal selector: P50 Input signal selector: CSC PCLK Output signal selector: INTELCL
	Config_PORT	Components: Port Port selection: PORT5 P53: Out (Output 1)

Note. When using IAR, use by the following settings.
On-chip debug operation setting: Use emulator
Emulator setting: E2 Emulator Lite

5.2.1 Clocks

Set the clock used in the sample code.

5.2.2 System

Set the on-chip debug of the sample code.

"Control of on-chip debug operation" and "Security ID authentication failure setting" affect "On-chip debugging is enabled" in "Table 4-2 Option Byte Settings". Note that changing the settings.

5.2.3 r_bsp

Set the startup of the sample code.

5.2.4 Config_LVD0

Set the power management of the sample code.

Affects "Setting of LVD0" in "Table 4-2 Option Byte Settings". Note that changing the settings.

5.2.5 Config_TAU0_7

Set the TAU0_7 of the sample code.

In the sample code, HALT Mode Used to count the time until HALT mode is re-entered after being released.

5.2.6 Config_EdgeDetectionThinningFunction

Initialize and output the ELCL of the sample code.

The sample code uses P50 as the pin to perform edge detection and INTELCL as the output destination.

For details, please refer to 5.3 Component "ELCL edge detection thinning function".

5.2.7 Config_PORT

Set the port of the sample code.

In the sample code, P53 is used to control LED1.

5.3 Component "ELCL edge detection thinning function"

Figure 5-4 shows the component ELCL edge detection thinning function" and Table 5-3 shows the options for this component.

Figure 5-4 Component "ELCL edge detection thinning function"

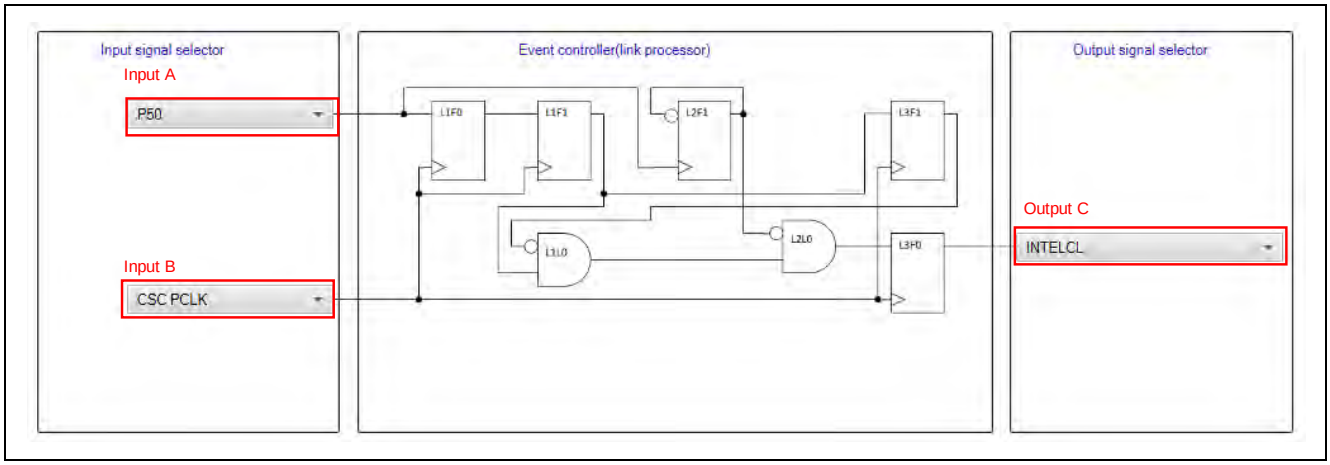


Table 5-3 Choices of component "ELCL edge detection thinning function"

Item	Choices	Description
Input A	P10	Select the edge detection pin
	P11	
	P12	
	P50	
	P51	
Input B Note	CSC PCLK	Select the edge detection clock
	HOCO HCLK_out	
	MOCO HCLK_out	
	SUB CLK SUBCLK_out	
Output C	INTELCL	Select the output destination
	DTC Start Trigger	
	SMS Start Trigger	
	A/D HW Trigger	
	D/A 0 HW Trigger	
	D/A 1 HW Trigger	
	CTSU HW Trigger	
	ITL Capture Trigger	

Note. Input B must be 16MHz or less.

5.3.1 Setting the ELCL Register

Table 5-4 to Table 5-8 show the initial settings of the ELCL register, and Figure 5-5 to Figure 5-9 show the ELCL configuration at that time. Refer to Figure 4-1 for the overall ELCL configuration.

Table 5-4 ELCL register settings (Inputs)

Register Symbol	Register Name	Setting	Description
ELISEL0	Input signal select register 0	05H	Input pin P50 is selected
ELISEL1	Input signal select register 1	1CH	Output from flip-flop 0 of logic cell block L1 in the ELCL is selected
ELISEL2	Input signal select register 2	1DH	Output from flip-flop 1 of logic cell block L1 in the ELCL is selected
ELISEL3	Input signal select register 3	1EH	Output from flip-flop 1 of logic cell block L2 in the ELCL is selected
ELISEL4	Input signal select register 4	1FH	Output from flip-flop 1 of logic cell block L3 in the ELCL is selected
ELISEL6	Input signal select register 6	05H	Input pin P50 is selected
ELISEL10	Input signal select register 10	1BH	CSC PCLK is selected

Figure 5-5 Setting of ELCL input

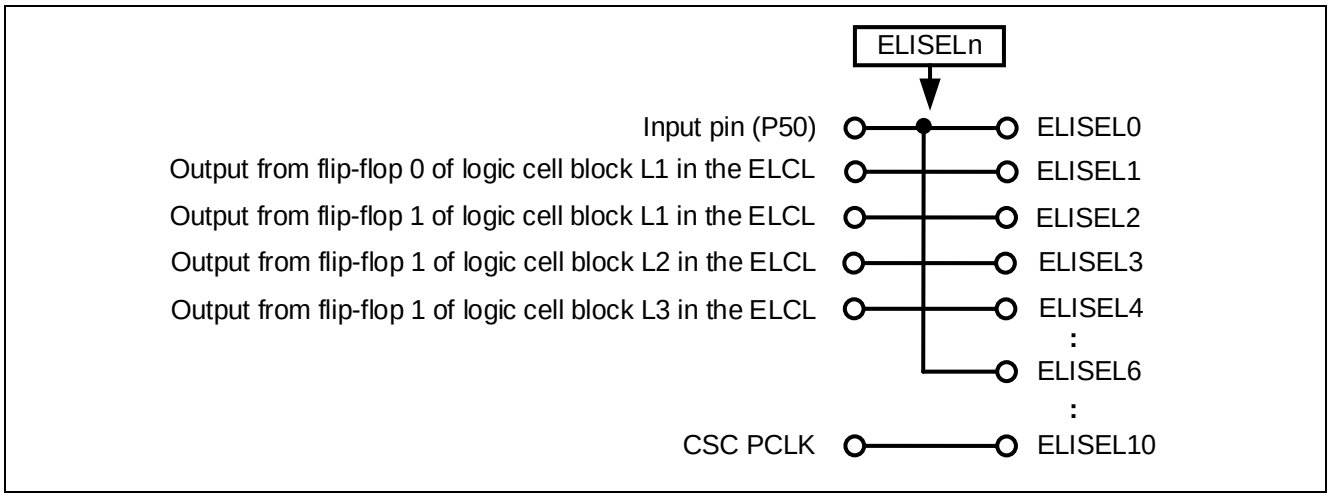


Table 5-5 ELCL register settings (Logic cell block L1)

Register Symbol	Register Name	Setting	Description
ELL1SEL0	Event link L1 signal select register 0	01H	Select the signal selected by ELISEL0 as the link target of L1
ELL1SEL1	Event link L1 signal select register 1	02H	Select the signal selected by ELISEL1 as the link target of L1
ELL1SEL2	Event link L1 signal select register 2	03H	Select the signal selected by ELISEL2 as the link target of L1
ELL1SEL3	Event link L1 signal select register 3	85H	Select the signal selected by ELISEL4 as the link target of L1 (Negative logic)
ELL1SEL6	Event link L1 signal select register 6	05H	Select the signal selected by ELISEL10 as the link target of L1
ELL1LNK0	Event link L1 output select register 0	08H	Link target selected by ELL1SEL0 to input of flip-flop 0 in logic cell block L1
ELL1LNK1	Event link L1 output select register 1	09H	Link target selected by ELL1SEL1 to input of flip-flop 1 in logic cell block L1
ELL1LNK2	Event link L1 output select register 2	02H	Link target selected by ELL1SEL2 to input 1 of logic cell 0 in logic cell block L1
ELL1LNK3	Event link L1 output select register 3	01H	Link target selected by ELL1SEL3 to input 0 of logic cell 0 in logic cell block L1
ELL1LNK6	Event link L1 output select register 6	03H	Link target selected by ELL1SEL6 to clock of flip-flop 0 and 1 in logic cell block L1
ELL1CTL	Logic cell block L1 control register	C1H	Enable use of logic cell block L1 flip-flops 0 and 1, logic cell 0 selects AND circuit

Figure 5-6 Setting of logic cells L1

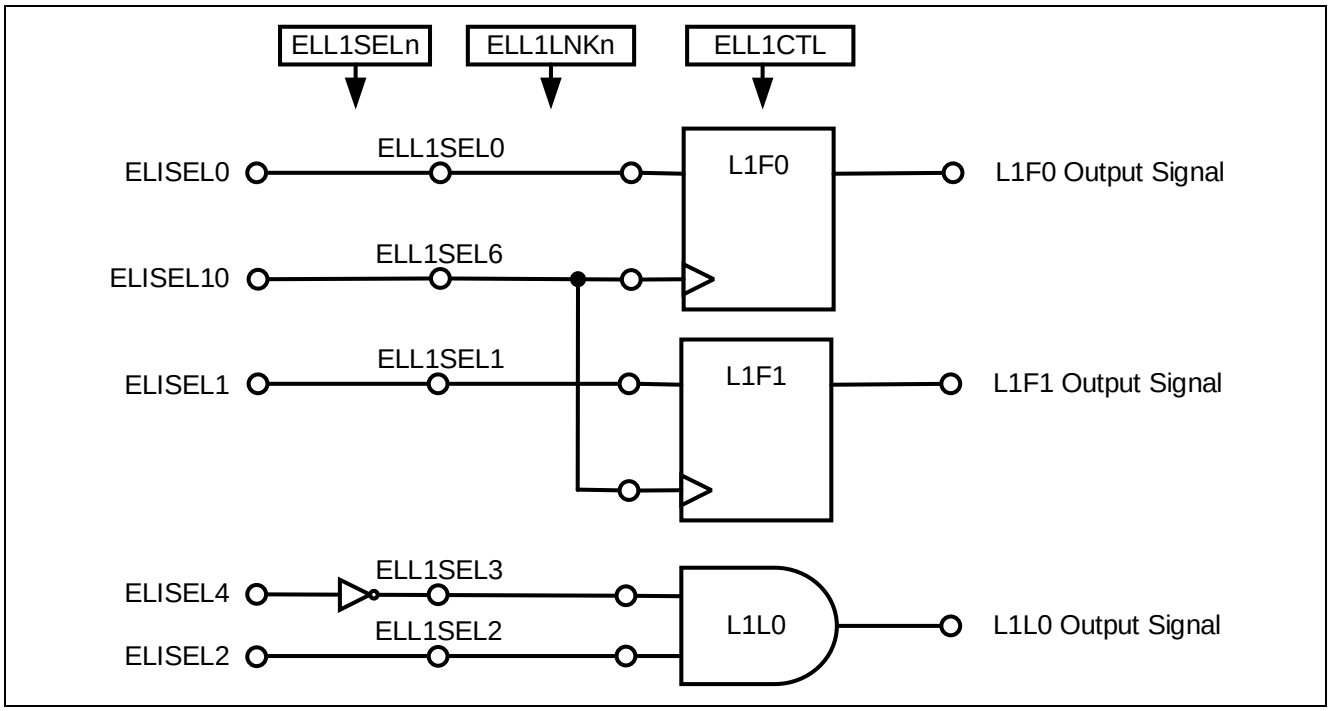


Table 5-6 ELCL register settings (Logic cell block L2)

Register Symbol	Register Name	Setting	Description
ELL2SEL0	Event link L2 signal select register 0	84H	Select the signal selected by ELISEL3 as the link target of L2 (Negative logic)
ELL2SEL1	Event link L2 signal select register 1	84H	Select the signal selected by ELISEL3 as the link target of L2 (Negative logic)
ELL2SEL2	Event link L2 signal select register 2	0DH	Output signal 0 in logic cell block L1 is selected as the link target of L2
ELL2SEL6	Event link L2 signal select register 6	01H	Select the signal selected by ELISEL6 as the link target of L2
ELL2LNK0	Event link L2 output select register 0	09H	Link target selected by ELL2SEL0 to input of flip-flop 1 in logic cell block L2
ELL2LNK1	Event link L2 output select register 1	01H	Link target selected by ELL2SEL1 to input 0 of logic cell 0 in logic cell block L2
ELL2LNK2	Event link L2 output select register 2	02H	Link target selected by ELL2SEL2 to input 1 of logic cell 0 in logic cell block L2
ELL2LNK6	Event link L2 output select register 6	02H	Link target selected by ELL2SEL6 to clock of flip-flop 1 in logic cell block L2
ELL2CTL	Logic cell block L2 control register	81H	Enable use of logic cell block L2 flip-flops 1, logic cell 0 selects AND circuit

Figure 5-7 Setting of logic cells L2

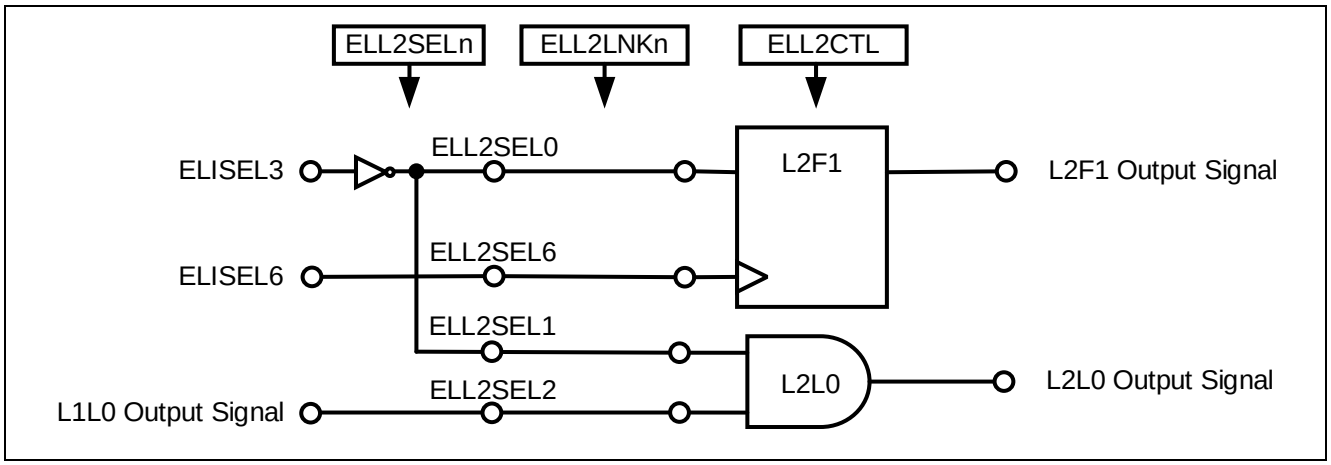


Table 5-7 ELCL register settings (Logic cell block L3)

Register Symbol	Register Name	Setting	Description
ELL3SEL0	Event link L3 signal select register 0	0DH	Output signal 0 in logic cell block L2 is selected as the link target of L3
ELL3SEL1	Event link L3 signal select register 1	03H	Select the signal selected by ELISEL2 as the link target of L3
ELL3SEL6	Event link L3 signal select register 6	05H	Select the signal selected by ELISEL10 as the link target of L3
ELL3LNK0	Event link L3 output select register 0	08H	Link target selected by ELL3SEL0 to input of flip-flop 0 in logic cell block L3
ELL3LNK1	Event link L3 output select register 1	09H	Link target selected by ELL3SEL1 to input of flip-flop 1 in logic cell block L3
ELL3LNK6	Event link L3 output select register 6	03H	Link target selected by ELL3SEL6 to clock of flip-flop 0 and 1 in logic cell block L3
ELL3CTL	Logic cell block L3 control register	C0H	Enable use of logic cell block L3 flip-flops 0 and 1

Figure 5-8 Setting of logic cells L3

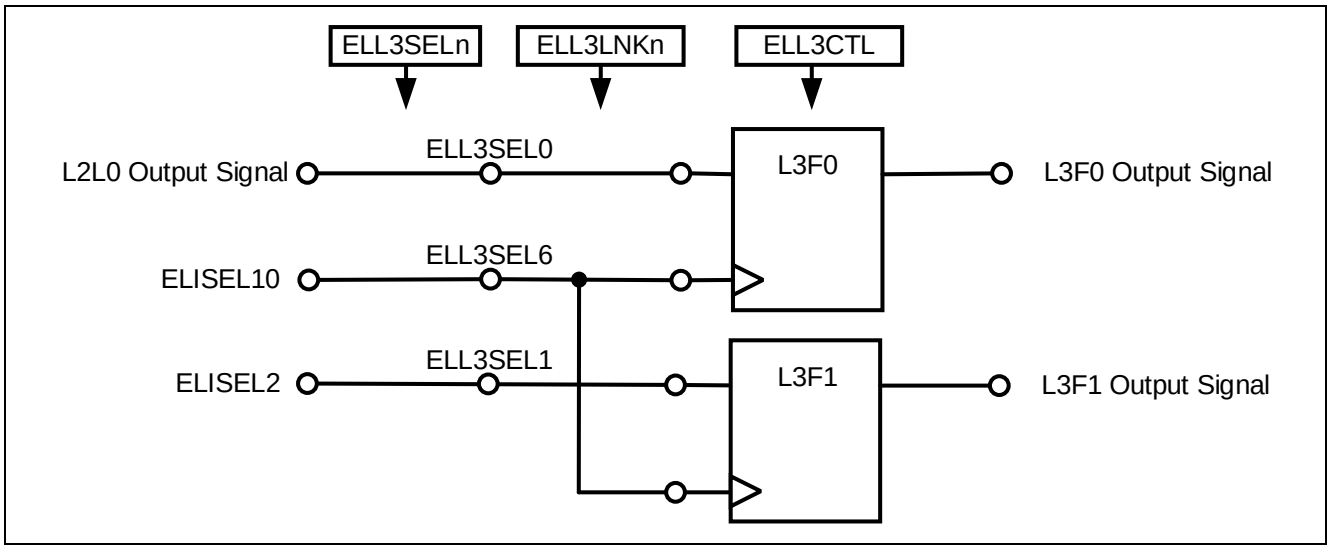
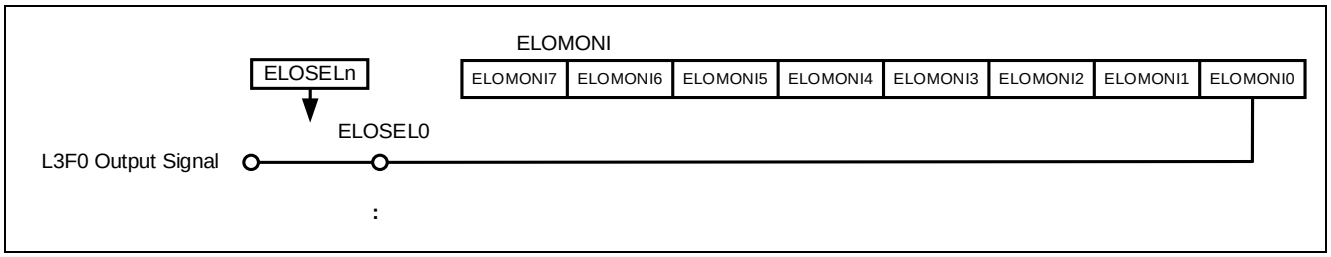


Table 5-8 ELCL register settings (Output)

Register Symbol	Register Name	Setting	Description
ELOSEL0	Output signal select register 0	0EH	Select the output signal [3] from logic cell block L3.

Figure 5-9 Settings of ELCL output



6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference

RL78/G23 User's Manual: Hardware (R01UH0896E)

RL78 Family User's Manual: Software (R01US0015E)

RL78 Smart Configurator User's Guide: CS+ (R20AN0580E)

RL78 Smart Configurator User's Guide: e^2 studio (R20AN0579E)

RL78 Smart Configurator User's Guide: IAREW (R20AN0581E)

(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update / Technical News

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr.13.21	-	First edition
2.00	Mar.24.22	5	Table 2-1 Operation Confirmation Conditions Operating voltage Rising edge TYP.1.875V -> 1.90V Falling edge TYP.1.835V -> 1.86V
		5	Updated tool version Table 2-1 Operation Confirmation Conditions Integrated development environment (CS+) : E8.05.00f -> V8.07.00 C compiler (CS+) : V1.09.00 -> V1.11 Integrated development environment (e^2 studio) : 2021-01 (21.01.0) -> 2022-01 (22.1.0) C compiler (e^2 studio) : V1.09.00 -> V1.11 Integrated development environment (IAR) : V4.20.1 -> V4.21.1 Smart Configurator : V.1.0.0 -> V.1.2.0 Board support package (r_bsp) : V.1.0.0 -> V.1.13
		5,6, 18,19	Changed due to COM port support Table 2-1 Operation Confirmation Conditions Emulator: E2 Emulator Lite -> CS＋, e^2 studio: COM port IAR: E2 Emulator Lite Figure 3-1 Hardware Configuration Added P11/TOOLRxD and P12/TOOLTxD Table 5-1 Smart Configurator Settings Note added
		5,10,18	Changes according to the operating conditions of the user manual Table 2-1 Operation Confirmation Conditions Operating frequencies High-speed on-chip oscillator clock:32MHz -> 16 MHz CPU/peripheral hardware clock: 32MHz -> 16 MHz Table 4-2 Option Byte Settings Setting Value 1110 1000B(E8H) -> 1110 1001B(E9H) Contents High-speed on-chip oscillator clock:32MHz -> 16MHz Table 5-1 Parameters of Smart Configurator Clocks Component High-speed on-chip oscillator: 32MHz -> 16 MHz fIHP: 32MHz -> 16 MHz fCLK: 32000kHz -> 16MHz (High-speed on-chip oscillator)
		9	Updated the folder structure in Table 4-1 due to the sample program update. Added Note 3 due to the update of the IAR version sample code.
		10	Table 4-2 Option byte setting Detection voltage Rise 1.875V / Fall 1.835V -> Rise 1.90V / Fall 1.86V

Rev.	Date	Description	
		Page	Summary
2.00	Mar.24.22	10	Updated the functions used in the sample code with the update of the component "ELCL edge detection thinning function" Table 4-4 Global variables used in the sample code Variable name: g_elcl_interrupt Function used r_elcl_interrupt -> r_Config_EdgeDetectionThinningFunction_interrupt
		11	Updated the contents in Table4-5 due to the component "ELCL edge detection thinning function" update. Table 4-5 Functions Deleted r_elcl_start, r_elcl_stop, r_elcl_interrupt Added r_Config_EdgeDetectionThinningFunction_interrupt r_elcl_reset_flipflop, source file elcl_support.c -> Config_EdgeDetectionThinningFunction_user.c
		11	Changes due to IAR version sample code update 4.7 Function specifications [function name] main, Header e^2 studio, CS +: r_smc_entry.h IAR: ior7f100g.h, ior7f100g_ext.h, r_cg_macrodriver.h, Config_SMS.h, Config_ITL000_ITL001.h -> r_smc_entry.h
		11	[Function name] r_Config_EdgeDetectionThinningFunction_interrupt, Description This function releases HALT mode when INTELCL occurs. -> Sets g_elcl_interrupt = 1
		11-12	Changed the header file due to the IAR version sample code update. 4.7 Function specifications Delete r_elcl_start, r_elcl_stop, r_elcl_interrupt Added r_Config_EdgeDetectionThinningFunction_interrupt [Function name] r_elcl_reset_flipflop, header r_cg_macrodriver.h, elcl_support.h -> platform.h
		13	Figure 4-3 Main process Corrected the branch condition in the flowchart.

Rev.	Date	Description	
		Page	Summary
2.00	Mar.24.22	13-15, 17-17, 20	Updated some figures as follows due to the component "ELCL edge detection thinning function" update. Figure 4-3 Main process Function name: R_Config_ EdgeDetectionThinningFunction _Create () -> R_Config_ EdgeDetectionThinningFunction _Start () Figure 4-6 ELCL interrupt process Function name: r_elcl_interrupt() -> r_Config_EdgeDetectionThinningFunction_interrupt() Figure 4-4 ELCL output start process Figure 4-5 ELCL output stop process Delete flowchart Figure 4-6 ELCL interrupt process Figure number: Figure 4-6 -> Figure 4-4 Figure 4-7 ELCL flip flop reset process Figure number: Figure 4-7 -> Figure 4-5 Figure 4-8 Weight process Figure number: Figure 4-8 -> Figure 4-6 Figure 4-9 TAU0 channel 7 interrupt process Figure number: Figure 4-9 -> Figure 4-7 Figure 5-1 Add of components Figure 5-2 Download the module Figure 5-3 Select the module Figure 5-4 Component "ELCL edge detection thinning function" Figure update
		17,19-20	ELCL Edge Detection Thinning Function -> ELCL edge detection thinning function
		18	Table 5-1 Parameters of Smart Configurator Clock: f_{SXL} -> f_{SXP} Component: Config_LVD0 Reset generation voltage (V_{LVD0}): 1.835 (V) -> 1.86 (V)
		20	Updated the contents in Table5-3 with the component "ELCL chattering prevention" update. Table 5-3 Choices for component "ELCL edge detection thinning function" Added Input A, Input B, Output C choices
		26	Added of RL78 Smart Configurator User's Guide 7. Reference RL78 Smart Configurator User's Guide: CS+ (R20AN0580E) RL78 Smart Configurator User's Guide: e² studio (R20AN0579E) RL78 Smart Configurator User's Guide: IAREW (R20AN0581E)

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1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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