RL78/G14

Timer RD in Timer Mode (PWM Function) CC-RL

R01AN2851EJ0100
Rev. 1.00
July 01, 2015

Abstract

This document describes a method to output a PWM waveform using the timer mode's PWM function (hereinafter referred to as PWM function) in the RL78/G14 timer RD.

Product

RL78/G14

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

Three PWM waveforms with 100 µs periods are output.

Table 1.1 lists the Peripheral Function and Its Application. Figure 1.1 shows the Output Timing Diagram.

Table 1.1 Peripheral Function and Its Application

Peripheral Function	Application
Timer RD (timer RD0)	PWM waveform output

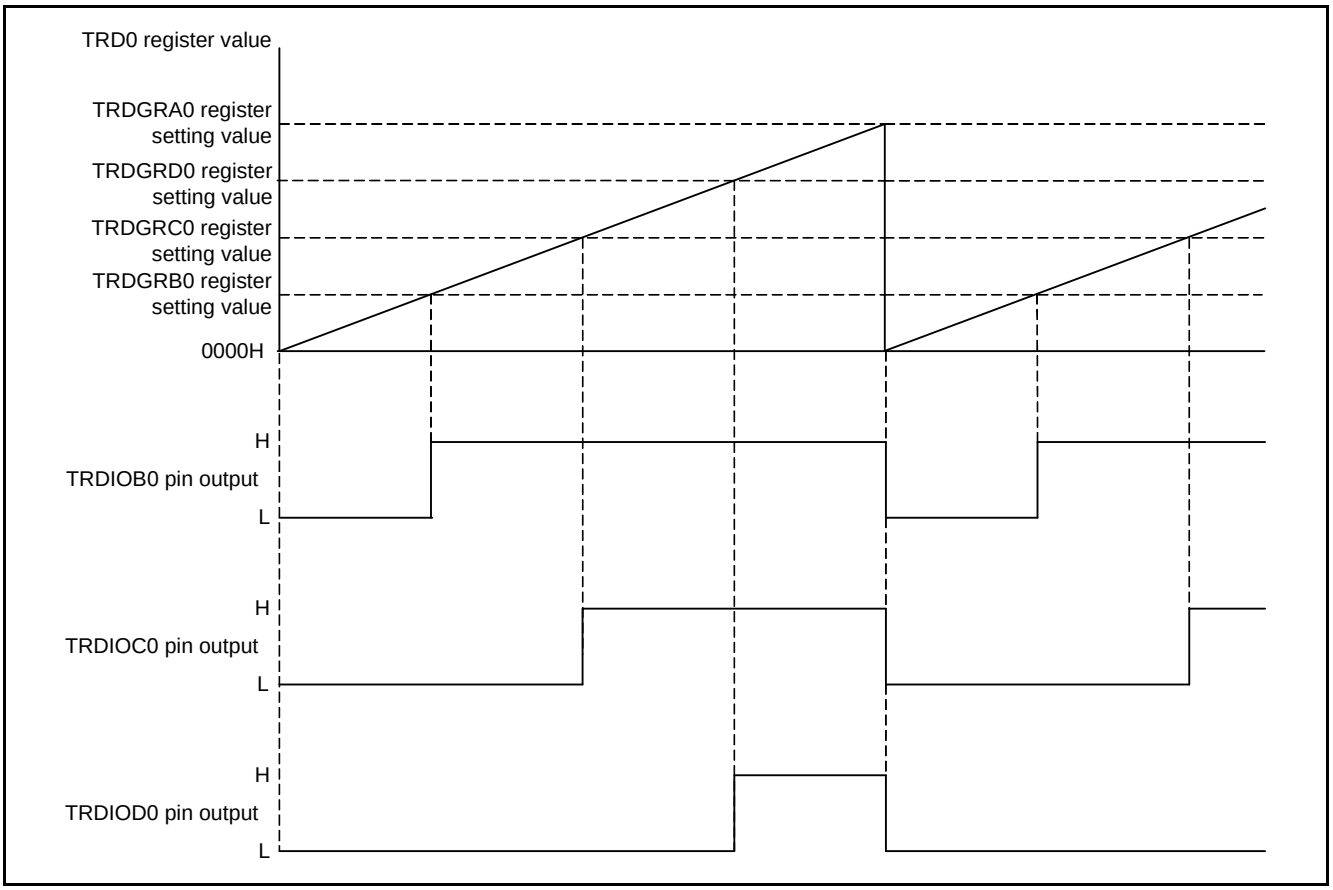


Figure 1.1 Output Timing Diagram

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

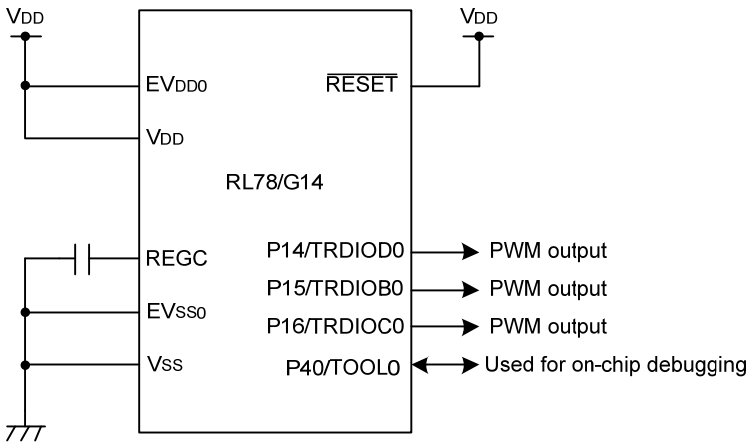
Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	RL78/G14 (R5F104LEA)
Operating frequencies	• High-speed on-chip oscillator clock (f_{HOCO}): 16 MHz (typical) • CPU/peripheral hardware clock (f_{CLK}): 16 MHz
Operating voltage	5.0 V (2.9 to 5.5 V) LVD operation (V_{LVD}): 2.81 V at the rising edge or 2.75 V at the falling edge in reset mode
Integrated development environment (CS+)	Renesas Electronics Corporation CS+ V3.01.00
C compiler (CS+)	Renesas Electronics Corporation CC-RL V1.01.00
Integrated development environment (e^2 studio)	Renesas Electronics Corporation e^2 studio V4.0.0.26
C compiler (e^2 studio)	Renesas Electronics Corporation CC-RL V1.01.00

3. Hardware

3.1 Hardware Configuration

Figure 3.1 shows the Hardware Configuration used in this document.



Notes:
1. The above figure is simplified to show an overview of the hardware connection. When designing application circuits, make sure to handle unused pins appropriately to satisfy the electrical characteristics (connect input-only ports independently to either VDD or VSS via resistors).
2. Connect pins with names that begin with EVSS to VSS, and pins with names that begin with EVDD to VDD.
3. Make sure to set VDD greater than the detection voltage (VLVD) specified by the LVD.

Figure 3.1 Hardware Configuration

3.2 Pins Used

Table 3.1 lists the Pins Used and Their Functions.

Table 3.1 Pins Used and Their Functions

Pin Name	I/O	Function
P14/TRDIOD0	Output	PWM output
P15/TRDIOB0	Output	PWM output
P16/TRDIOC0	Output	PWM output

4. Software

4.1 Operation Overview

Three PWM waveforms with 100 µs periods are output using the PWM function.

Output signals are shown below.

• TRDIOB0 pin output: Inactive level low period (25 µs) → Active level high period (75 µs)
• TRDIOC0 pin output: Inactive level low period (50 µs) → Active level high period (50 µs)
• TRDIOD0 pin output: Inactive level low period (75 µs) → Active level high period (25 µs)

The timer RD settings are shown below.

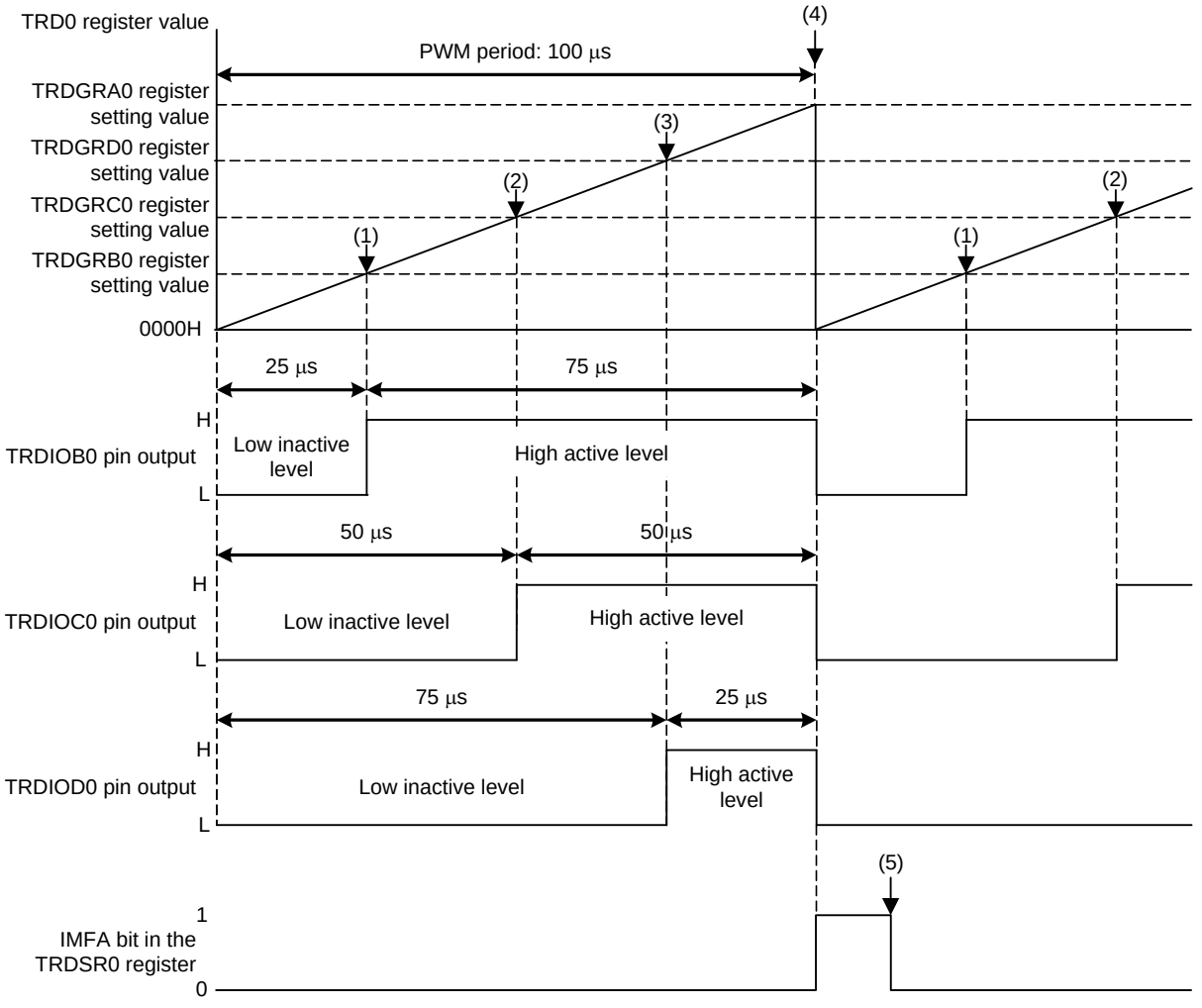
Settings:
• Use f_{CLK} (16 MHz) as the count source.
• Use timer RD0.
• Continue counting the TRD0 register after the compare match with the TRDGRA0 register.
• Use the TRDGRC0 register as the general register.
• Use the TRDGRD0 register as the general register.
• Enable output for pins TRDIOB0, TRDIOC0, and TRDIOD0.
• Select TRDIOB0, TRDIOC0, and TRDIOD0 pin output levels as high active level and the initial output level as low inactive level.
• Timer RD0 and timer TRD1 operate independently.
• Do not use the pulse output forced cutoff input function.
• Enable the compare match interrupt of registers TRD0 and TRDGRA0.

4.1.1 Output Waveform

Below is a description for calculating the PWM period and PWM waveform output from each pin.

(1) PWM period:
Calculate the PWM period as follows:
100 µs = 1/16 MHz × (TRDGRA0 + 1)
= 62.5 ns × 1600
(2) PWM output of the TRDIOB0 pin
Calculate the low inactive level period of the TRDIOB0 pin as follows:
25 µs = 1/16 MHz × (TRDGRB0 + 1)
= 62.5 ns × 400
(3) PWM output of the TRDIOC0 pin
Calculate the low inactive level period of the TRDIOC0 pin as follows:
50 µs = 1/16 MHz × (TRDGRC0 + 1)
= 62.5 ns × 800
(4) PWM output of the TRDIOD0 pin
Calculate the low inactive level period of the TRDIOD0 pin as follows:
75 µs = 1/16 MHz × (TRDGRD0 + 1)
= 62.5 ns × 1200

Figure 4.1 shows the PWM Output Waveform.



(1) Since the TRD0 register count value and the TRDGRB0 register setting value are compare matched, the TRDIOB0 pin output is changed.
(2) Since the TRD0 register count value and the TRDGRC0 register setting value are compare matched, the TRDIOC0 pin output is changed.
(3) Since the TRD0 register count value and the TRDGRD0 register setting value are compare matched, the TRDIOD0 pin output is changed.
(4) Since the TRD0 register count value and the TRDGRA0 register setting value are compare matched, the TRD0 register is cleared and an INTTRD0 interrupt is generated.
(5) Clear compare match flag A (IMFA bit) in timer RD status register 0 (TRDSR0 register) in the INTTRD0 interrupt service routine by a program.

Figure 4.1 PWM Output Waveform

4.2 Option Byte Settings

Table 4.1 lists the Option Byte Settings. When necessary, set a value suited to the user system.

Table 4.1 Option Byte Settings

Address	Setting Value	Contents
000C0H/010C0H	11101111B	Watchdog timer operation is stopped (count is stopped after reset)
000C1H/010C1H	01111111B	LVD reset mode Detection voltage: Rising edge 2.81 V/falling edge 2.75 V
000C2H/010C2H	11101001B	Internal high-speed oscillation HS mode: 16 MHz
000C3H/010C3H	10000100B	On-chip debugging enabled

4.3 Functions

Table 4.2 lists the Functions.

Table 4.2 Functions

Function Name	Outline
hdwinit	Initial setting
R_Systeminit	Initial setting of peripheral functions
R_CGC_Create	Initial setting of the CPU
R_TMR_RD0_Create	Initial setting of timer RD
main	Main processing
timer_rd0_start	Timer RD count start setting
r_tmr_rd0_interrupt	Timer RD0 interrupt

4.4 Function Specifications

The following tables list the sample code function specifications.

hdwinit	
Outline	Initial setting
Header	None
Declaration	void hdwinit(void)
Description	Perform the initial setting of peripheral functions.
Argument	None
Return Value	None

R_Systeminit	
Outline	Initial setting of peripheral functions
Header	None
Declaration	void R_Systeminit(void)
Description	Perform the initial setting of peripheral functions used in this document.
Argument	None
Return Value	None

R_CGC_Create	
Outline	Initial setting of the CPU
Header	None
Declaration	void R_CGC_Create(void)
Description	Perform the initial setting of the CPU.
Argument	None
Return Value	None

R_TMR_RD0_Create	
Outline	Initial setting of timer RD
Header	None
Declaration	void R_TMR_RD0_Create(void)
Description	Perform the initial setting to use the PWM function of timer RD.
Argument	None
Return Value	None

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	Perform main processing.
Argument	None
Return Value	None

timer_rd0_start	
Outline	Timer RD count start setting
Header	None
Declaration	void timer_rd0_start(void)
Description	Perform timer RD count start setting.
Argument	None
Return Value	None

r_tmr_rd0_interrupt	
Outline	Timer RD0 interrupt
Header	None
Declaration	static void __near r_tmr_rd0_interrupt(void)
Description	• Perform timer RD0 interrupt service routine. • Clear compare match flag A.
Argument	None
Return Value	None

4.5 Flowcharts

4.5.1 Overall Flowchart

Figure 4.2 shows the Overall Flowchart.

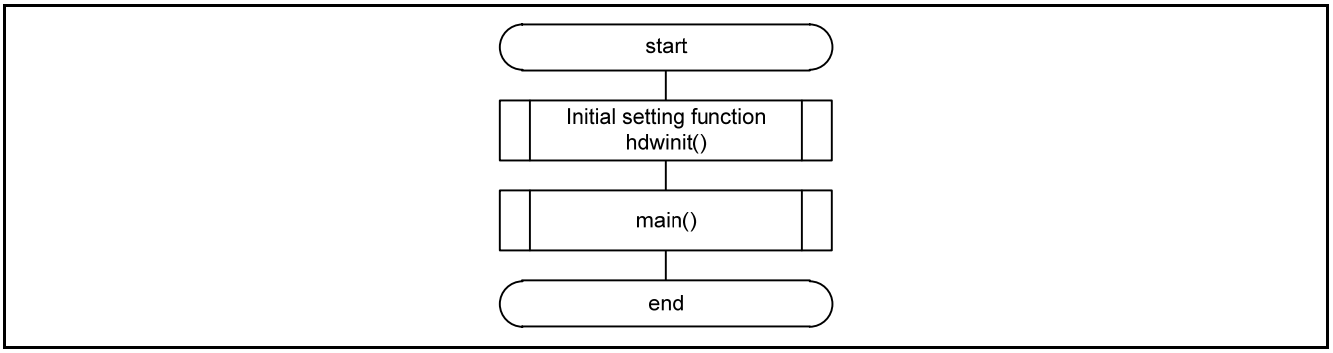


Figure 4.2 Overall Flowchart

4.5.2 Initial Setting

Figure 4.3 shows the Initial Setting.

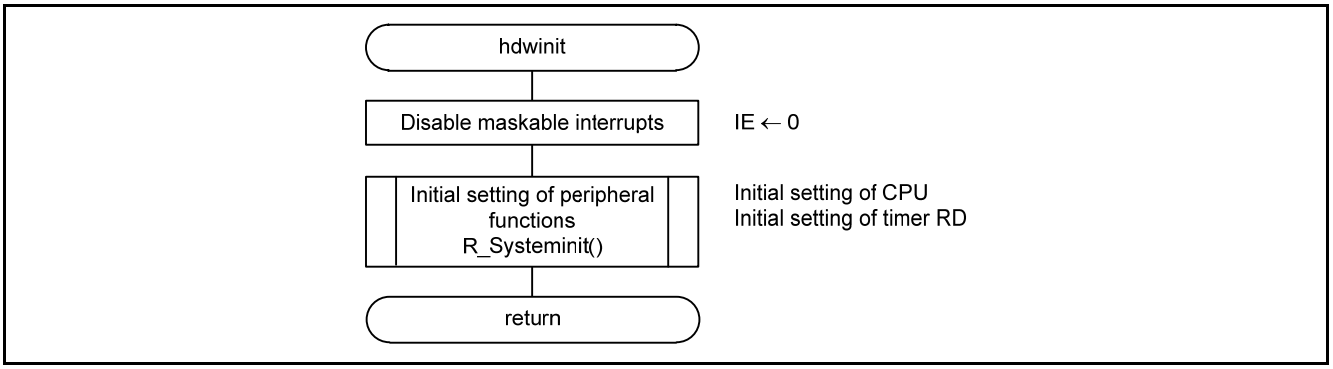


Figure 4.3 Initial Setting

4.5.3 Initial Setting of Peripheral Functions

Figure 4.4 shows the Initial Setting of Peripheral Functions.

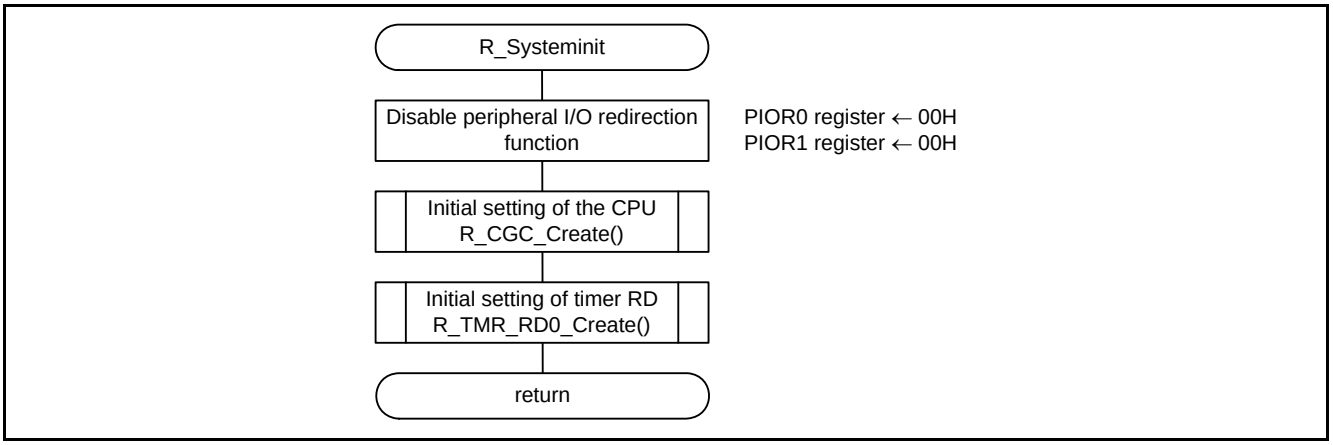


Figure 4.4 Initial Setting of Peripheral Functions

4.5.4 Initial Setting of the CPU

Figure 4.5 shows the Initial Setting of the CPU.

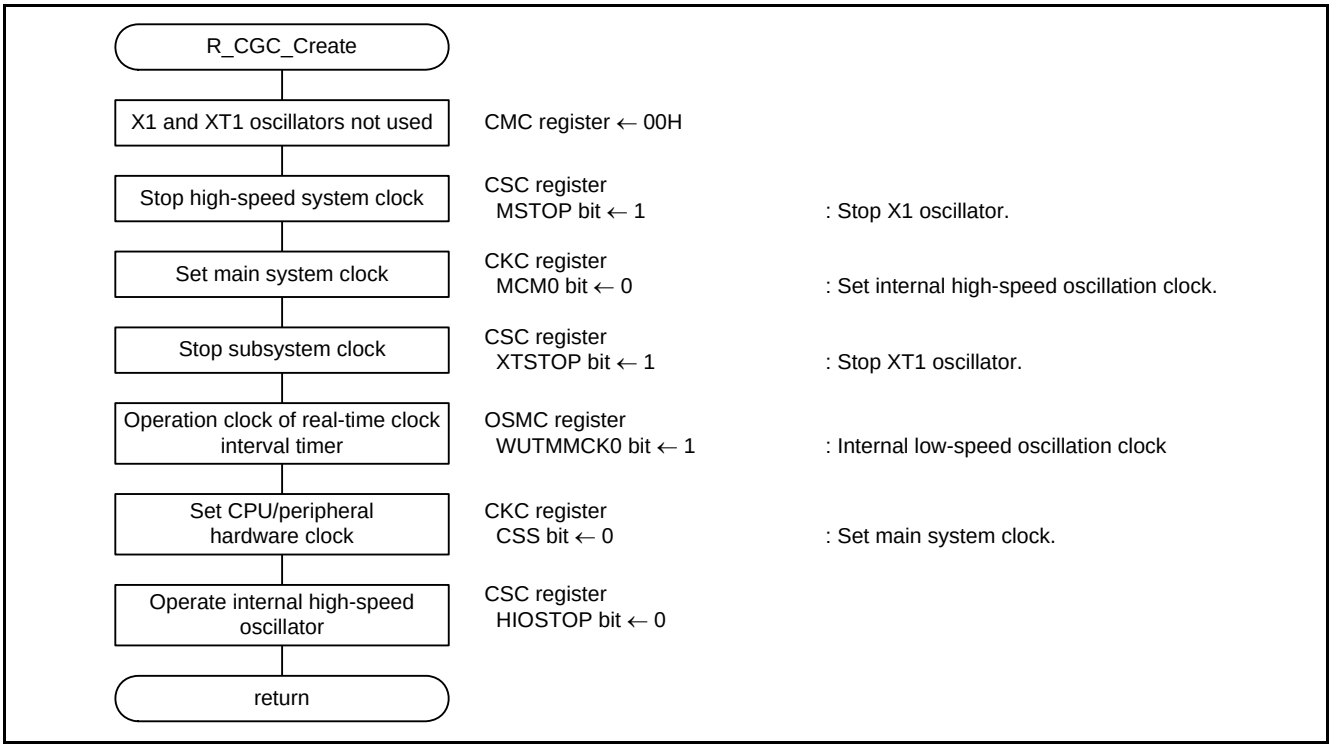


Figure 4.5 Initial Setting of the CPU

4.5.5 Initial Setting of Timer RD

Figure 4.6 and Figure 4.7 show the Initial Setting of Timer RD.

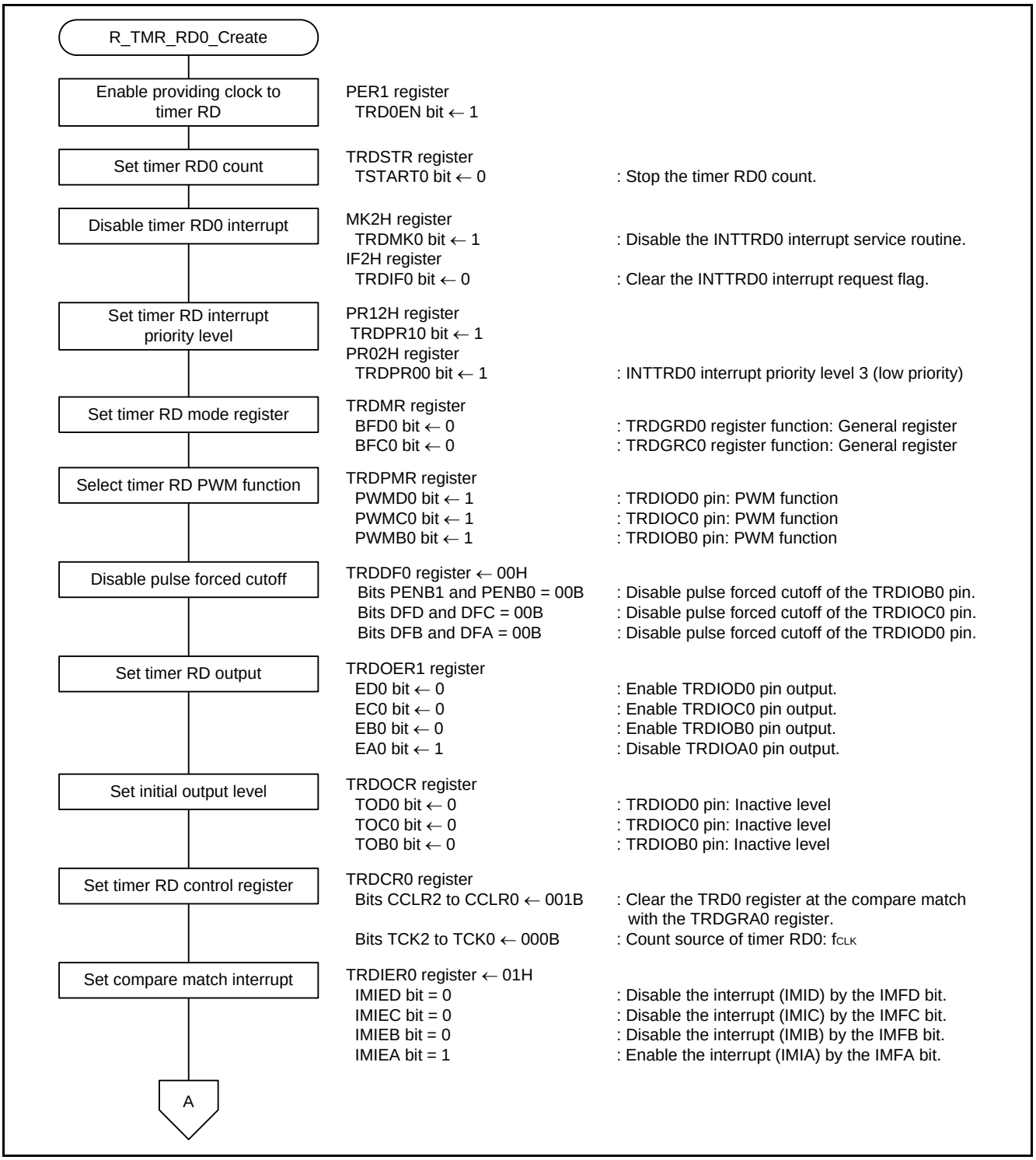


Figure 4.6 Initial Setting of Timer RD (1/2)

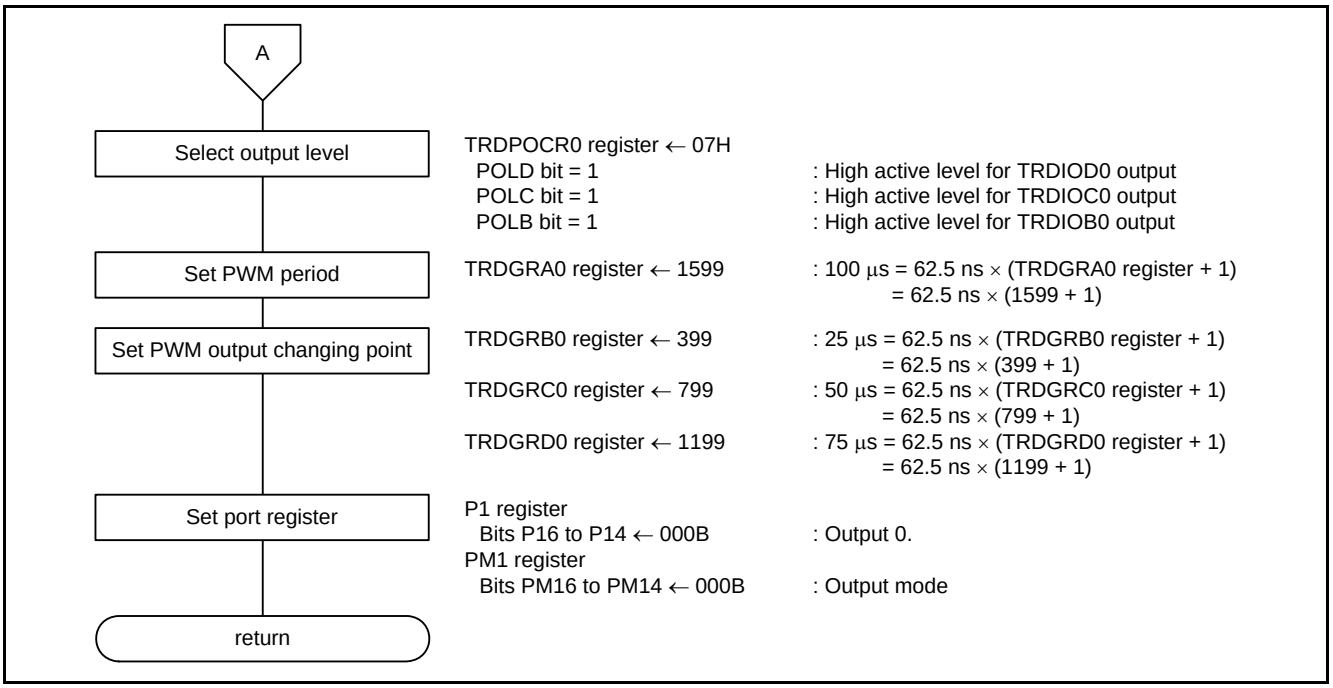


Figure 4.7 Initial Setting of Timer RD (2/2)

Enable providing a clock to timer RD.

- Peripheral Enable Register 1 (PER1)
  Enable providing a clock to timer RD.

Symbol	7	6	5	4	3	2	1	0
PER1	DACEN	TRGEN	CMPEN	TRD0EN	DTCEN	0	0	TRJ0EN
Setting Value	x	x	x	1	x	—	—	x

Bit 4

TRD0EN	Control of timer RD input clock supply
0	Stops input clock supply. • SFR used by timer RD cannot be written. • Timer RD is in the reset status.
1	Enables input clock supply. • SFR used by timer RD can be read and written.

Set the timer RD0 count.

- Timer RD Mode Register (TRDSTR)
  Stop the timer RD0 count.

Symbol	7	6	5	4	3	2	1	0
TRDSTR	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
Setting Value	—	—	—	—	x		x	0

Bit 2

CSEL0	TRD0 count operation select
0	Count stops at compare match with TRDGRA0 register
1	Count continues after compare match with TRDGRA0 register

Bit 0

TSTART0	TRD0 count start flag
0	Count stops
1	Count starts

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Disable the timer RD0 interrupt.

- Interrupt Mask Flag Register (MK2H)
  Disable the INTTRD0 interrupt.

Symbol	7	6	5	4	3	2	1	0
MK2H	FLMK	IICAMK1	1	SREMK3 TMMK13H	TRGMK	TRDMK1	TRDMK0	PMK11 CMPMK1
Setting Value	x	x	—	x	x	x	1	x

Bit 1

TRDMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

- Interrupt Request Flag Register (IF2H)
  Clear the INTTRD0 interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF2H	FLIF	IICAIF1	0	SREIF3 TMIF13H	TRGIF	TRDIF1	TRDIF0	PIF11 CMPIF1
Setting Value	x	x	—	x	x	x	0	x

Bit 1

TRDIF0	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the timer RD interrupt priority level.

- Priority Specification Flag Registers (PR02H and PR12H)
  Set to level 3 (low priority).

Symbol	7	6	5	4	3	2	1	0
PR02H	FLPR0	IICAPR01	1	SREPR03 TMPR013H	TRGPR0	TRDPR01	TRDPR00	PPR011 CMPPR01
Setting Value	x	x	—	x	x	x	1	x

Symbol	7	6	5	4	3	2	1	0
PR12H	FLPR1	IICAPR11	1	SREPR13 TMPR113H	TRGPR1	TRDPR11	TRDPR10	PPR111 CMPPR11
Setting Value	x	x	—	x	x	x	1	x

TRDPR10	TRDPR00	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	1	Specify level 3 (low priority level)

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the timer RD mode register.

- Timer RD Mode Register (TRDMR)
  Use registers TRDGRC0 and TRDGRD0 as the general registers.

Symbol	7	6	5	4	3	2	1	0
TRDMR	BFD1	BFC1	BFD0	BFC0	—	—	—	SYNC
Setting Value	x	x	0	0	—	—	—	

Bit 5

BFD0	TRDGRD0 register function select
0	General register
1	Buffer register for TRDGRB0 register

Bit 4

BFC0	TRDGRC0 register function select
0	General register
1	Buffer register for TRDGRA0 register

Bit 0

SYNC	Timer RD Synchronous
0	TRD0 and TRD1 operate independently
1	TRD0 and TRD1 operate synchronously

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Select the timer RD PWM function.

- Timer RD PWM Function Select Register (TRDPMR)
  Set the PWM function to pins TRDIOB0, TRDIOC0, and TRDIOD0.

Symbol	7	6	5	4	3	2	1	0
TRDPMR	—	PWMD1	PWMC1	PWMB1	—	PWMD0	PWMC0	PWMB0
Setting Value	—	x	x	x	—	1	1	1

Bit 2

PWMD0	PWM function of TRDIOD0 select
0	Input capture function or output compare function
1	PWM function

Bit 1

PWMC0	PWM function of TRDIOC0 select
0	Input capture function or output compare function
1	PWM function

Bit 0

PWMB0	PWM function of TRDIOB0 select
0	Input capture function or output compare function
1	PWM function

Disable pulse forced cut-off.

- Timer RD Digital Filter Function Select Register 0 (TRDDF0)
  Disable pulse forced cut-off of pins TRDIOB0, TRDIOC0, and TRDIOD0.

Symbol	7	6	5	4	3	2	1	0
TRDDF0	DFCK1	DFCK0	PENB1	PENB0	DFD	DFC	DFB	DFA
Setting Value	x	x	0	0	0	0	0	0

Bits 5 and 4

PENB1	PENB0	TRDIOB0 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output
Set these bits to 00B (forced cutoff disabled) if the corresponding pin is not used as a timer RD output port in these modes. Also, set these bits while the count is stopped.		

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Bits 3 and 2

DFD	DFC	TRDIOC0 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output
Set these bits to 00B (forced cutoff disabled) if the corresponding pin is not used as a timer RD output port in these modes. Also, set these bits while the count is stopped.		

Bits 1 and 0

DFB	DFA	TRDIOD0 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output
Set these bits to 00B (forced cutoff disabled) if the corresponding pin is not used as a timer RD output port in these modes. Also, set these bits while the count is stopped.		

Set timer RD output.

- Timer RD Output Master Enable Register 1 (TRDOER1)
  Disable TRDIOA0 pin output, and enable output of pins TRDIOB0, TRDIOC0, and TRDIOD0.

Symbol	7	6	5	4	3	2	1	0
TRDOER1	ED1	EC1	EB1	EA1	ED0	EC0	EB0	EA0
Setting Value	x	x	x	x	0	0	0	1

Bit 3

ED0	TRDIOD0 output disable
0	Output enabled
1	Output disabled (TRDIOD0 pin functions as an I/O port.)

Bit 2

EC0	TRDIOC0 output disable
0	Output enabled
1	Output disabled (TRDIOC0 pin functions as an I/O port.)

Bit 1

EB0	TRDIOB0 output disable
0	Output enabled
1	Output disabled (TRDIOB0 pin functions as an I/O port.)

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Bit 0

EA0	TRDIOA0 output disable
0	Output enabled
1	Output disabled (TRDIOA0 pin functions as an I/O port.)

Set to 1 for the PWM function.

Set initial output levels.

- Timer RD Output Control Register (TRDOCR)
  Set initial output levels of pins TRDIOB0, TRDIOC0, and TRDIOD0.

Symbol	7	6	5	4	3	2	1	0
TRDOCR	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0
Setting Value	x	x	x	x	0	0	0	x

Bit 3

TOD0	TRDIOD0 initial output level select
0	Initial output is not active level
1	Initial output is active level

Bit 2

TOC0	TRDIOC0 initial output level select
0	Initial output is not active level
1	Initial output is active level

Bit 1

TOB0	TRDIOB0 initial output level select
0	Initial output is not active level
1	Initial output is active level

Set the timer RD control register.

- Timer RD Control Register 0 (TRDCR0)
  Set the timing to clear the TRD0 register at compare match with the TRDGRA0 register. Set f_{CLK} to the count source of timer RD0.

Symbol	7	6	5	4	3	2	1	0
TRDCR0	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
Setting Value	0	0	1	x	x	0	0	0

Bits 7 to 5

CCLR2	CCLR1	CCLR0	TRD0 counter clear select
Set to 001B (TRD0 register is cleared at compare match with TRDGRA0 register).			

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Bits 2 to 0

TCK2	TCK1	TCK0	Count source select
0	0	0	f_{CLK}, f_{HOCO}
0	0	1	$f_{CLK}/2$
0	1	0	$f_{CLK}/4$
0	1	1	$f_{CLK}/8$
1	0	0	$f_{CLK}/32$
1	0	1	TRDCLK input
1	1	0	Do not set.
1	1	1	Do not set.

Set the compare match interrupt.

- Timer RD Interrupt Enable Register 0 (TRDIER0)
  Set the IMFA bit to enable the interrupt (IMIA).

Symbol	7	6	5	4	3	2	1	0
TRDIER0	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA
Setting Value	—	—	—	x	0	0	0	1

Bit 3

IMIED	Input capture/compare match interrupt enable D
0	Interrupt (IMID) by the IMFD bit is disabled
1	Interrupt (IMID) by the IMFD bit is enabled

Bit 2

IMIEC	Input capture/compare match interrupt enable C
0	Interrupt (IMIC) by the IMFC bit is disabled
1	Interrupt (IMIC) by the IMFC bit is enabled

Bit 1

IMIEB	Input capture/compare match interrupt enable B
0	Interrupt (IMIB) by the IMFB bit is disabled
1	Interrupt (IMIB) by the IMFB bit is enabled

Bit 0

IMIEA	Input capture/compare match interrupt enable A
0	Interrupt (IMIA) by the IMFA bit is disabled
1	Interrupt (IMIA) by the IMFA bit is enabled

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Select output levels.

- Timer RD PWM Function Output Level Control Register 0 (TRDPOCR0)
  Set output levels of pins TRDIOC0, TRDIOB0, and TRDIOD0 to high active level.

Symbol	7	6	5	4	3	2	1	0
TRDPOCR0	—	—	—	—	—	POLD	POLC	POLB
Setting Value	—	—	—	—	—	1	1	1

Bit 2

POLD	PWM function output level control D
0	TRDIOD0 output level is low active
1	TRDIOD0 output level is high active

Bit 1

POLC	PWM function output level control C
0	TRDIOC0 output level is low active
1	TRDIOC0 output level is high active

Bit 0

POLB	PWM function output level control B
0	TRDIOB0 output level is low active
1	TRDIOB0 output level is high active

Set the PWM period.

- Timer RD General Register A0 (TRDGRA0)
  Set the PWM period to 100 µs.

Symbol	15	14	13	12	11	10	9	8
TRDGRA0	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	1	1	0

Symbol	7	6	5	4	3	2	1	0
TRDGRA0	—	—	—	—	—	—	—	—
Setting Value	0	0	1	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.3 TRDGRA0 register function in PWM function.	0000H to FFFFH

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the PWM output changing point.

- Timer RD General Register B0 (TRDGRB0)
  Set this register after 25 µs from the count start to change the output of the TRDIOB0 pin.

Symbol	15	14	13	12	11	10	9	8
TRDGRB0	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	0	0	1

Symbol	7	6	5	4	3	2	1	0
TRDGRB0	—	—	—	—	—	—	—	—
Setting Value	1	0	0	0	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.3 TRDGRB0 register function in PWM function.	0000H to FFFFH

- Timer RD General Register C0 (TRDGRC0)
  Set this register after 50 µs from the count start to change the output of the TRDIOC0 pin.

Symbol	15	14	13	12	11	10	9	8
TRDGRC0	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	0	1	1

Symbol	7	6	5	4	3	2	1	0
TRDGRC0	—	—	—	—	—	—	—	—
Setting Value	0	0	0	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.3 TRDGRC0 register function in PWM function.	0000H to FFFFH

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

- Timer RD General Register D0 (TRDGRD0)
  Set this register after 75 μs from the count start to change the output of the TRDIOD0 pin.

Symbol	15	14	13	12	11	10	9	8
TRDGRD0	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	1	0	0

Symbol	7	6	5	4	3	2	1	0
TRDGRD0	—	—	—	—	—	—	—	—
Setting Value	1	0	1	0	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.3 TRDGRD0 register function in PWM function.	0000H to FFFFH

Table 4.3 General Register Functions in PWM Function

Register	Setting	Register Function	PWM Output Pin
TRDGRA0	—	General register. Set the PWM period.	—
TRDGRB0	—	General register. Set the changing point of PWM output.	TRDIOB0
TRDGRC0	BFC0 = 0	General register. Set the changing point of PWM output.	TRDIOC0
TRDGRD0	BFD0 = 0		TRDIOD0
TRDGRC0	BFC0 = 1	Buffer register. Set the next PWM period.	—
TRDGRD0	BFD0 = 1	Buffer register. Set the changing point of the next PWM output.	TRDIOB0

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the port register.

- Port Register 1 (P1)
  Set port register 1.

Symbol	7	6	5	4	3	2	1	0
P1	P17	P16	P15	P14	P13	P12	P11	P10
Setting Value	x	0	0	0	x	x	x	x

Bit 6

P16	Output data control
0	Output 0
1	Output 1

Bit 5

P15	Output data control
0	Output 0
1	Output 1

Bit 4

P14	Output data control
0	Output 0
1	Output 1

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

• Port Mode Register 1 (PM1)
Set pins P16 to P14 to output mode.

Symbol	7	6	5	4	3	2	1	0
PM1	P17	P16	P15	P14	P13	P12	P11	P10
Setting Value	x	0	0	0	x	x	x	x

Bit 6

PM16	P16 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Bit 5

PM15	P15 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Bit 4

PM14	P14 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

4.5.6 Main Processing

Figure 4.8 shows the Main Processing.

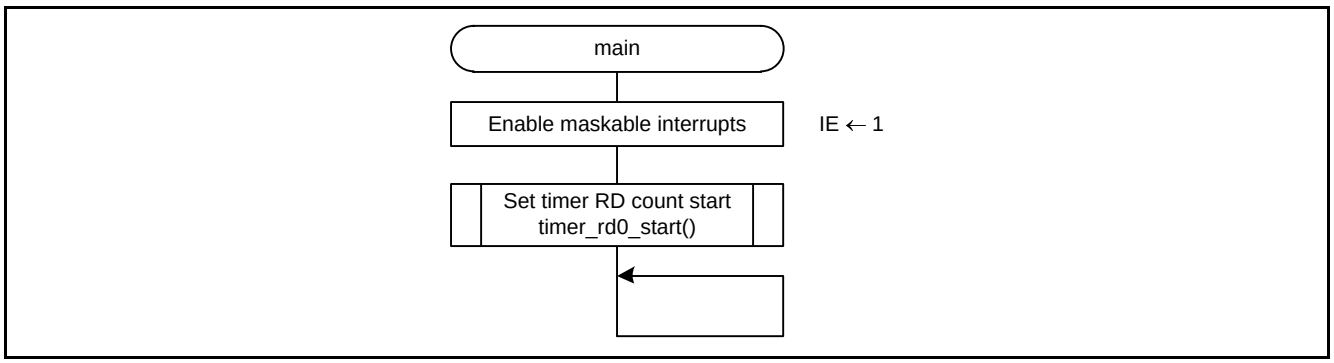


Figure 4.8 Main Processing

4.5.7 Timer RD Count Start Setting

Figure 4.9 shows the Timer RD Count Start Setting.

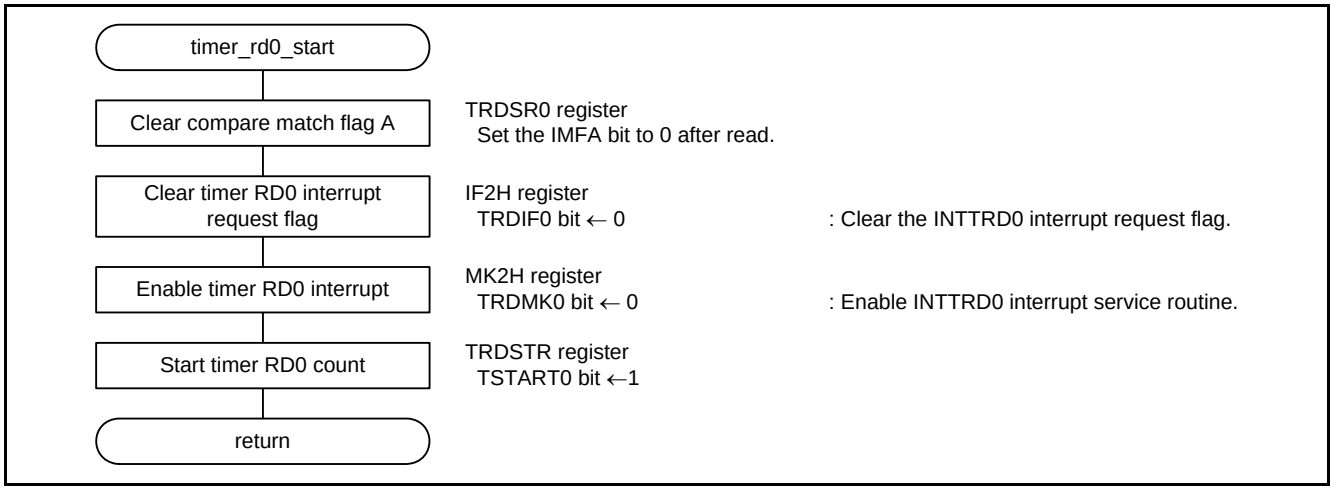


Figure 4.9 Timer RD Count Start Setting

Clear compare match flag A.

- Timer RD Status Register 0 (TRDSR0)
  Clear compare match flag A after reading timer RD status register 0.

Symbol	7	6	5	4	3	2	1	0
TRDSR0	—	—	—	OVF	IMFD	IMFC	IMFB	IMFA
Setting Value	—	—	—	x	x	x	x	0

Bit 0

IMFA	Input capture/compare match flag A
[Source for setting to 0] Write 0 after reading. [Source for setting to 1] When the values of TRD0 and TRDGRA0 match.	

Clear the timer RD0 interrupt request flag.

- Interrupt Request Flag Register (IF2H)
  Clear the INTTRD0 interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF2H	FLIF	IICAIF1	0	SREIF3 TMIF13H	TRGIF	TRDIF1	TRDIF0	PIF11 CMPIF1
Setting Value	x	x	—	x	x	x	0	x

Bit 1

TRDIF0	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Enable the timer RD0 interrupt.

- Interrupt Mask Flag Register (MK2H)
  Enable the INTTRD0 interrupt.

Symbol	7	6	5	4	3	2	1	0
MK2H	FLMK	IICAMK1	1	SREMK3 TMMK13H	TRGMK	TRDMK1	TRDMK0	PMK11 CMPMK1
Setting Value	x	x	—	x	x	x	0	x

Bit 1

TRDMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Start the timer RD count.

- Timer RD Mode Register (TRDSTR)
  Start the timer RD count.

Symbol	7	6	5	4	3	2	1	0
TRDSTR	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
Setting Value	—	—	—	—	x		x	1

Bit 0

TSTART0	TRD0 count start flag
0	Count stops
1	Count starts

4.5.8 Timer RD0 Interrupt

Figure 4.10 shows the Timer RD0 Interrupt.

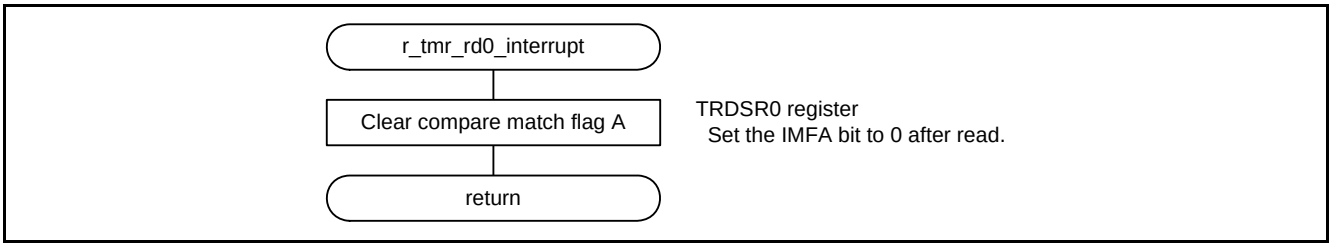


Figure 4.10 Timer RD0 Interrupt

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

User's Manual: Hardware
RL78/G14 Group User's Manual: Hardware (R01UH0186E)
RL78 Family User's Manual: Software (R01US0015E)
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com

Inquiries
http://www.renesas.com/contact/

REVISION HISTORY	RL78/G14 Timer RD in Timer Mode (PWM Function)

Rev.	Date	Description	
		Page	Summary
1.00	July 01, 2015	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
3. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics product.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; and safety equipment etc.
   Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (nuclear reactor control systems, military equipment etc.). You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application for which it is not intended. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
6. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You should not use Renesas Electronics products or technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. When exporting the Renesas Electronics products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the contents and conditions set forth in this document, Renesas Electronics assumes no responsibility for any losses incurred by you or third parties as a result of unauthorized use of Renesas Electronics products.
11. This document may not be reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

RENESAS

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HALII Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 5.0