RL78/G14

Timer RD in Complementary PWM Mode

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Abstract

This document describes a method to output a PWM waveform and an inverted waveform every half period of the PWM using the RL78/G14 timer RD in complementary PWM mode.

Product

RL78/G14

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

Three normal-phases, three counter-phases of the PWM waveform every 350 µs (three-phase, triangular wave modulation, and with dead time), and the inverted output every half period of the PWM are output. The PWM waveform is switched using a buffer operation every constant period. The three normal-phases output the same signal and three counter-phases output the same signal.

Table 1.1 lists the Peripheral Function and Its Application. Figure 1.1 shows the Output Waveform of the Complementary PWM.

Table 1.1 Peripheral Function and Its Application

Peripheral Function	Application
Timer RD (timer RD0 and timer RD1)	PWM waveform output

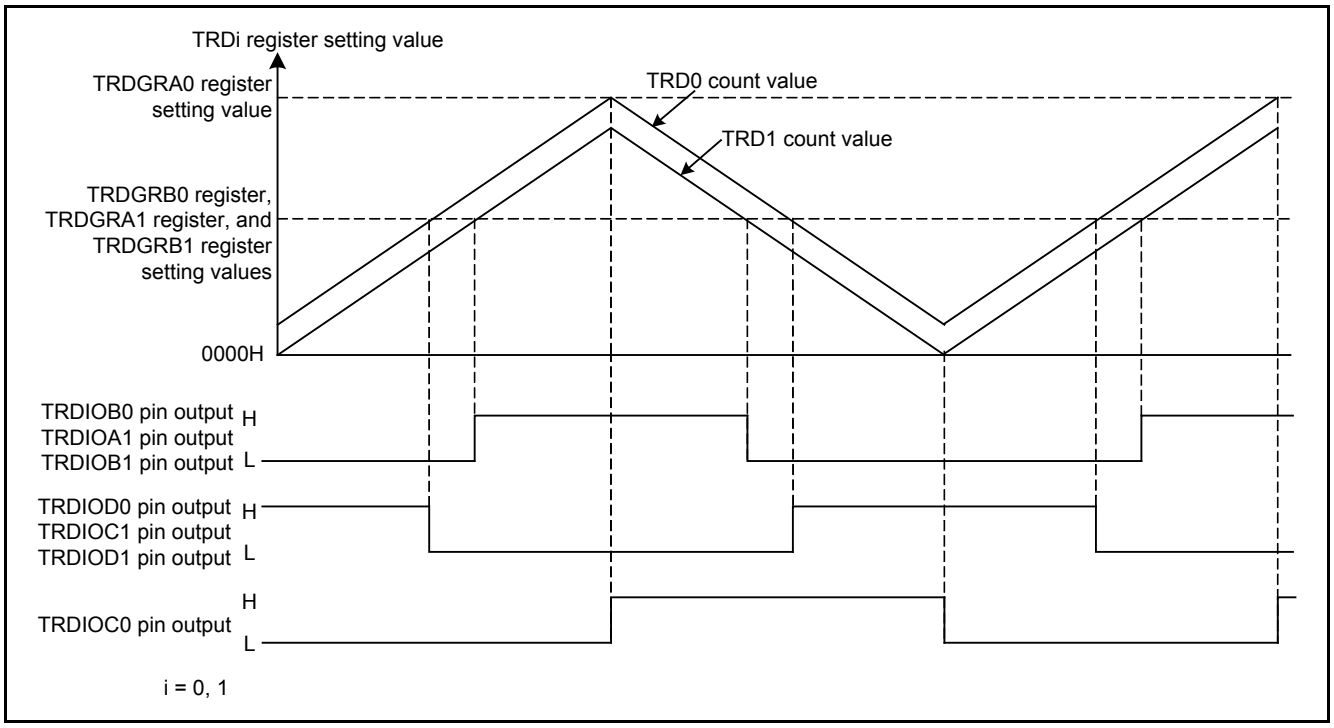


Figure 1.1 Output Waveform of the Complementary PWM

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

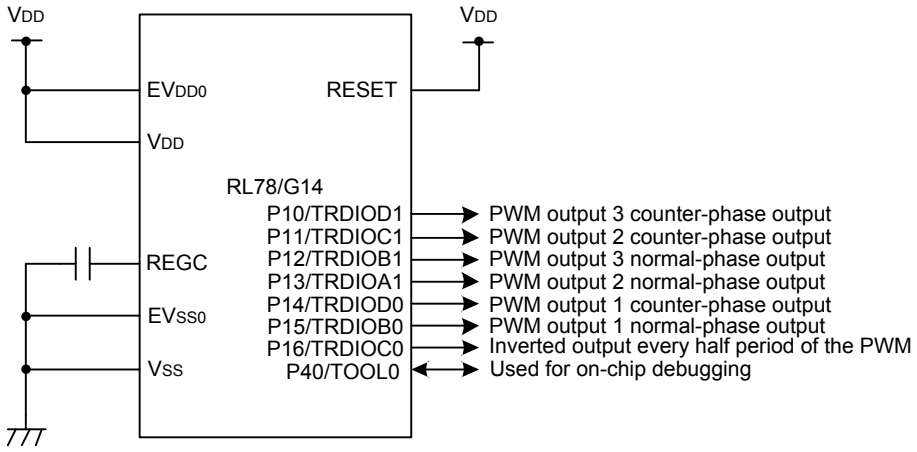
Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	RL78/G14 (R5F104LEA)
Operating frequencies	• High-speed on-chip oscillator clock (f_{HOCO}): 16 MHz (typical) • CPU/peripheral hardware clock (f_{CLK}): 16 MHz
Operating voltage	5.0 V (2.9 to 5.5 V) LVD operation (V_{LVI}): 2.81 V at the rising edge or 2.75 V at the falling edge in reset mode
Integrated development environment	Renesas Electronics Corporation CubeSuite+ V1.01.00
C compiler	Renesas Electronics Corporation CA78K0R V1.30
RL78/G14 code library	Renesas Electronics Corporation CodeGenerator for RL78/G14 V1.01.01

3. Hardware

3.1 Hardware Configuration

Figure 3.1 shows the Hardware Configuration used in this document.



Notes 1. The above figure is simplified to show an overview of the hardware connection. When designing application circuits, make sure to handle unused pins appropriately to satisfy the electrical characteristics. Connect input-only ports independently to VDD or VSS via resistors.
2. Connect pins with names that begin with EVSS to VSS, and pins with names that begin with EVDD to VDD.
3. Make sure to set VDD greater than the detection voltage (VLVI) specified by the LVD.

Figure 3.1 Hardware Configuration

3.2 Pins Used

Table 3.1 lists the Pins Used and Their Functions.

Table 3.1 Pins Used and Their Functions

Pin Name	I/O	Function
P15/TRDIOB0	Output	PWM output 1 normal-phase output
P14/TRDIOD0	Output	PWM output 1 counter-phase output
P13/TRDIOA1	Output	PWM output 2 normal-phase output
P11/TRDIOC1	Output	PWM output 2 counter-phase output
P12/TRDIOB1	Output	PWM output 3 normal-phase output
P10/TRDIOD1	Output	PWM output 3 counter-phase output
P16/TRDIOC0	Output	Inverted output every half period of PWM

4. Software

4.1 Operation Overview

Three normal-phases of the PWM waveform with 350 µs periods are output from pins TRDIOB0, TRDIOA1, and TRDIOB1; three counter-phases are output from TRDIOD0, TRDIOC1, and TRDIOD1; and inverted output every half period of the PWM is output from the TRDIOC0 pin using complementary PWM mode. The four kinds of PWM waveforms output are shown in Figures 4.1 to 4.4. When the compare match interrupt for registers TRD0 and TRDGRA0 has been generated 10 times, use the buffer operation to switch the PWM waveform. The waveforms are repeatedly switched in the following order:
PWM waveform 1 → PWM waveform 2 → PWM waveform 3 → PWM waveform 2 → PWM waveform 4 → PWM waveform 1

The timer RD settings are shown below.

Settings:
- Use f_{CLK} (16 MHz) as the count source.
- Continue counting the TRD0 register after the compare match with the TRDGRA0 register.
- Continue counting the TRD1 register after the compare match with the TRDGRA1 register.
- Use the TRDGRD0 register as the buffer register of the TRDGRB0 register.
- Use the TRDGRC1 register as the buffer register of the TRDGRA1 register.
- Use the TRDGRD1 register as the buffer register of the TRDGRB1 register.
- Transfer data from the buffer register to the general register when the TRD1 register underflows.
- Enable output for pins TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, and TRDIOD1.
- Select TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, and TRDIOD1 pin output levels as low active level and the initial output level as high inactive level.
- Do not use the pulse output forced cutoff input function.
- Enable the compare match interrupt of registers TRD0 and TRDGRA0.

4.1.1 Description of Output Waveform

The kind of the PWM waveform output from each pin, and calculating active/inactive level and dead time is shown below.
PWM period: 350 µs = 1/16 MHz × (TRDGRA0 + 2 - TRD0) × 2
= 62.5 ns × (3200 - 400) × 2

(1) PWM waveform 1

Normal-phase output: High inactive level period (50 µs) → Low active level period (250 µs) → High inactive level period (50 µs)

Counter-phase output: Low active level period (25 µs) → Dead time (25 µs) → High inactive level period (250 µs) → Dead time (25 µs) → Low active level period (25 µs)

The formula below shows how to calculate the low active level period/high inactive level period and dead time when PWM waveform 1 is output.

PWM waveform 1 normal-phase output: Pins TRDIOB0, TRDIOA1, TRDIOB1 (Note 1)

Low active level period: 250 µs = 1/16 MHz × (TRDGRA0 - n - TRD0 + 1) × 2
= 62.5 ns × (3198 - 799 - 400 + 1) × 2

High inactive level period: 50 µs = 1/16 MHz × (n + 1)
= 62.5 ns × (799 + 1)

PWM waveform 1 counter-phase output: Pins TRDIOD0, TRDIOC1, TRDIOD1 (Note 1)

Low active level period: 25 µs = 1/16 MHz × (n + 1 - TRD0)
= 62.5 ns × (799 + 1 - 400)

High inactive level period: 250 µs = 1/16 MHz × (TRDGRA0 - n - TRD0 + 1) × 2
= 62.5 ns × (3198 - 799 - 400 + 1) × 2

Dead time (High): 25 µs = 1/16 MHz × TRD0
= 62.5 ns × 400

n: TRDGRB0 register setting value (PWM output 1)
TRDGRA1 register setting value (PWM output 2)
TRDGRB1 register setting value (PWM output 3)

Note 1. In this sample code, the same signal is output.

Figure 4.1 shows PWM Waveform 1.

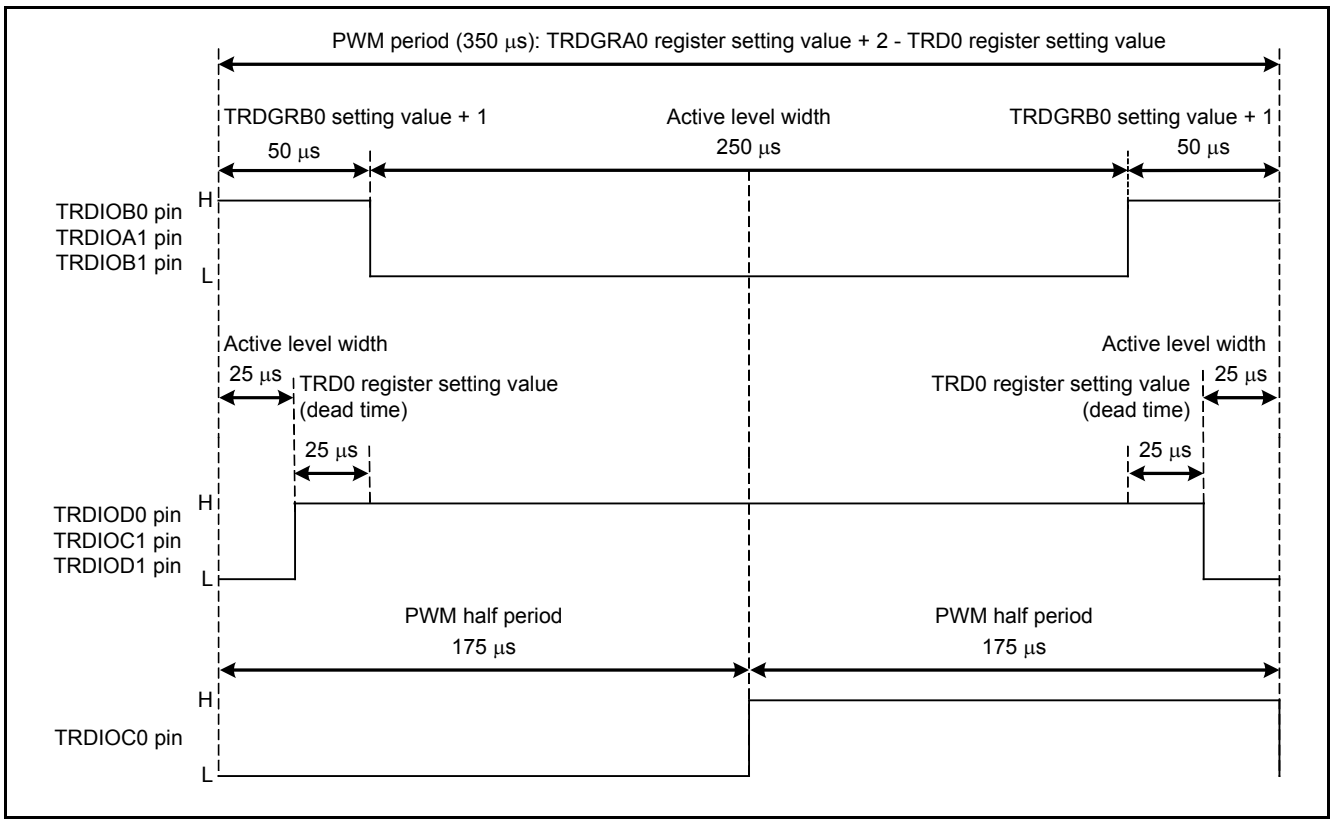


Figure 4.1 PWM Waveform 1

(2) PWM waveform 2

Normal-phase output: High inactive level period (125 µs) → Low active level period (100 µs) → High inactive level period (125 µs)

Counter-phase output: Low active level period (100 µs) → Dead time (25 µs) → High inactive level period (100 µs) → Dead time (25 µs) → Low active level period (100 µs)

The formula below shows how to calculate the low active level period/high inactive level period and dead time when PWM waveform 2 is output.

PWM waveform 2 normal-phase output: Pins TRDIOB0, TRDIOA1, TRDIOB1 (Note 1)

Low active level period: 100 µs = 1/16 MHz × (TRDGRA0 - n - TRD0 + 1) × 2
= 62.5 ns × (3198 - 1999 - 400 + 1) × 2

High inactive level period: 125 µs = 1/16 MHz × (n + 1)
= 62.5 ns × (1999 + 1)

PWM waveform 2 counter-phase output: Pins TRDIOD0, TRDIOC1, TRDIOD1 (Note 1)

Low active level period: 100 µs = 1/16 MHz × (n + 1 - TRD0)
= 62.5 ns × (1999 + 1 - 400)

High inactive level period: 100 µs = 1/16 MHz × (TRDGRA0 - n - TRD0 + 1) × 2
= 62.5 ns × (3198 - 1999 - 400 + 1) × 2

Dead time (H): 25 µs = 1/16 MHz × TRD0
= 62.5 ns × 400

n: TRDGRB0 register setting value (PWM output 1)
TRDGRA1 register setting value (PWM output 2)
TRDGRB1 register setting value (PWM output 3)

Note 1. In this sample code, the same signal is output.

Figure 4.2 shows PWM Waveform 2.

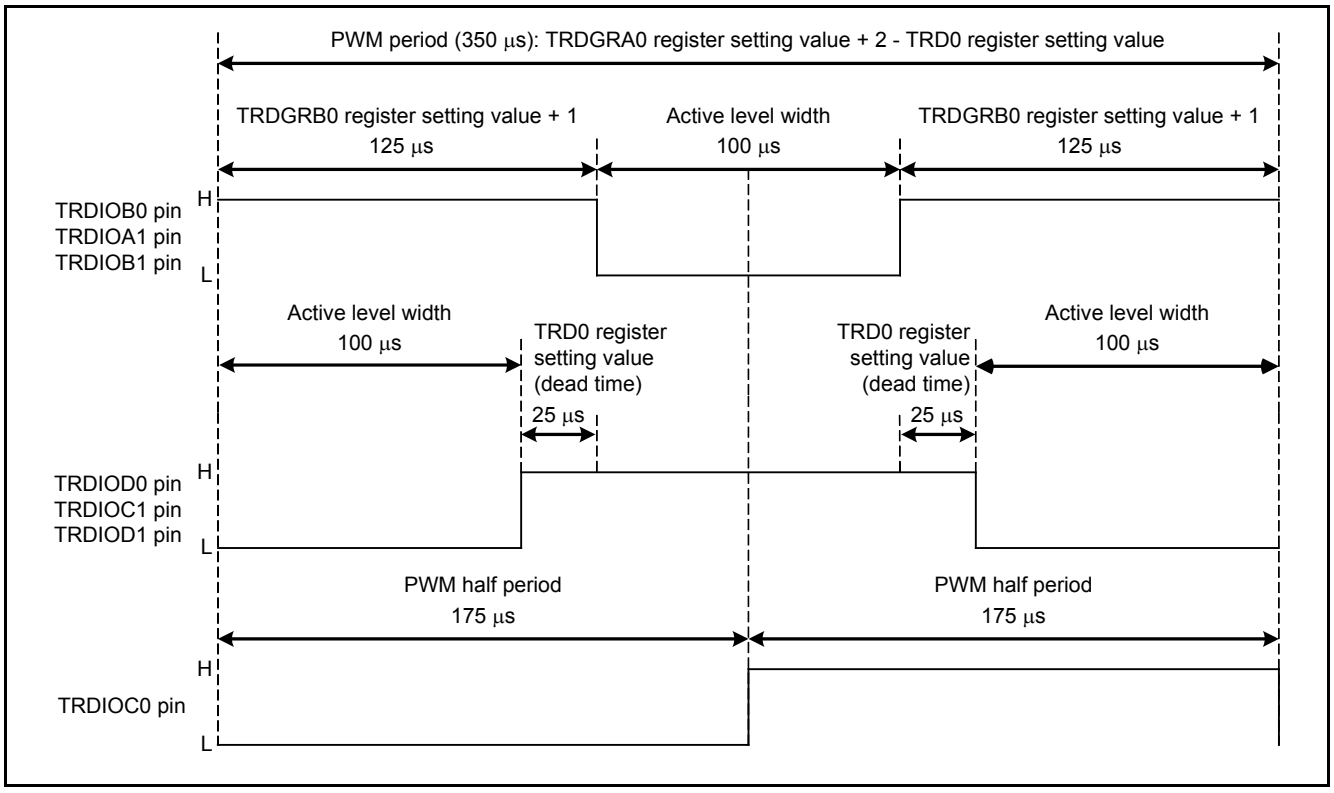


Figure 4.2 PWM Waveform 2

(3) PWM waveform 3
Normal-phase output: Low active level period (350 μs)
Counter-phase output: High inactive level period (350 μs)
After setting the buffer registers (registers TRDGRD0, TRDGRC1, and TRDGRD1) to 0000H, if the TRD0 and TRDGRA0 registers are compare matched, the levels below are output.

PWM waveform 3 normal-phase output: Pins TRDIOB0, TRDIOA1, TRDIOB1 (Note 1)
Low active level period: 350 μs

PWM waveform 3 counter-phase output: Pins TRDIOD0, TRDIOC1, TRDIOD1 (Note 1)
High inactive level period: 350 μs

Note 1. In this sample code, the same signal is output.

Figure 4.3 shows PWM Waveform 3.

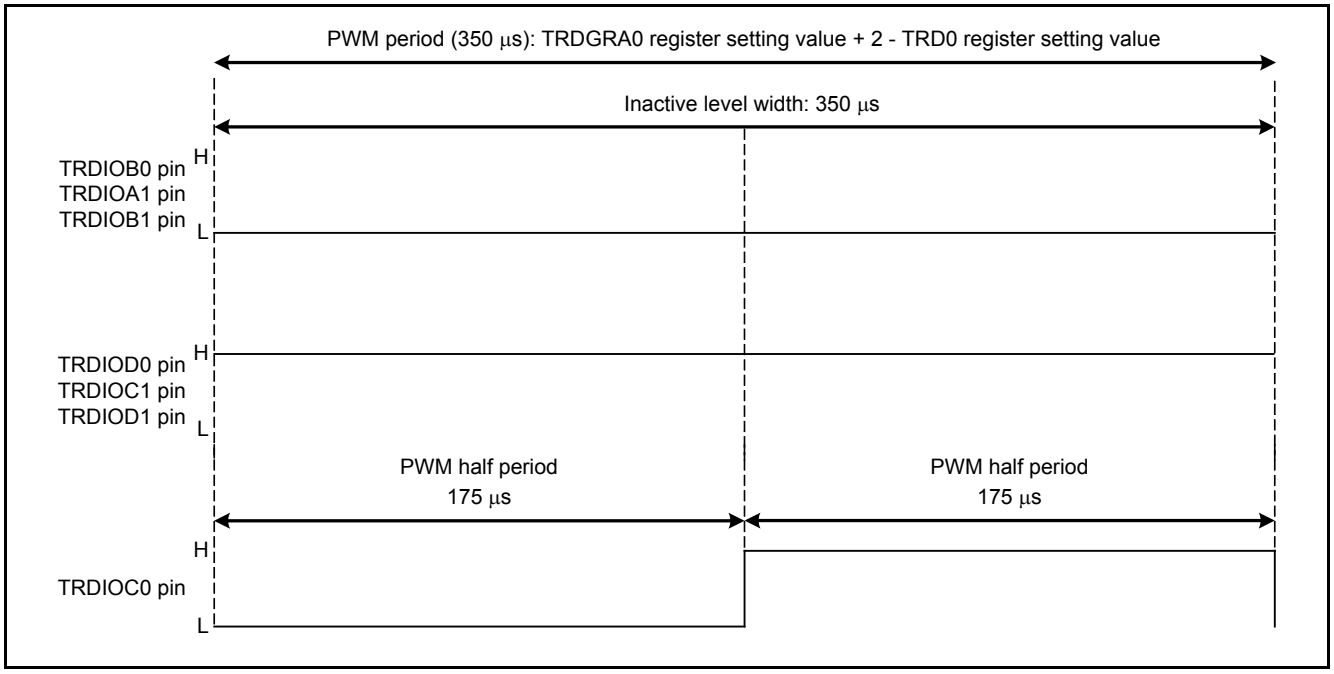


Figure 4.3 PWM Waveform 3

(4) PWM waveform 4
Normal-phase output: High inactive level period (350 µs)
Counter-phase output: Low active level period (350 µs)
When the TRD1 register underflows after setting the value more than the TRDGRA0 register setting value to the buffer registers (registers TRDGRD0, TRDGRC1, and TRDGRD1), levels below are output.

PWM waveform 4 normal-phase output: Pins TRDIOB0, TRDIOA1, TRDIOB1 (Note 1)
High inactive level period: 350 µs

PWM waveform 4 counter-phase output: Pins TRDIOD0, TRDIOC1, TRDIOD1 (Note 1)
Low active level period: 350 µs

Note 1. In this sample code, the same signal is output.

Figure 4.4 shows PWM Waveform 4.

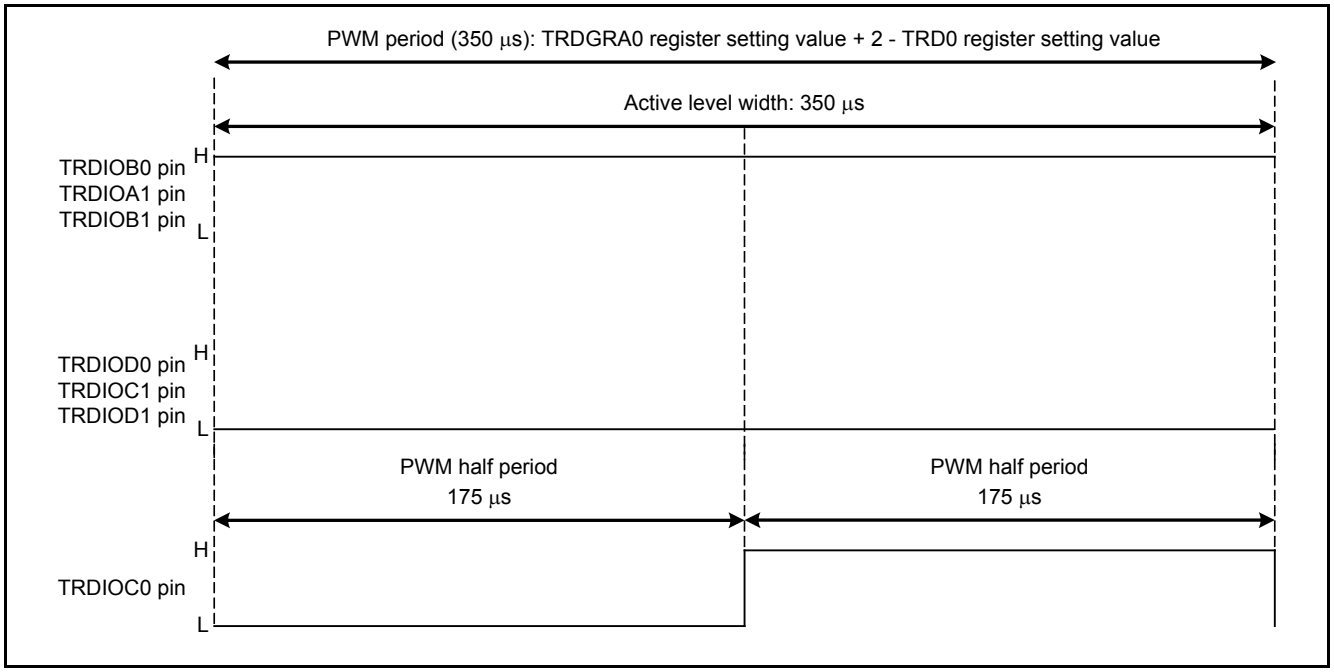


Figure 4.4 PWM Waveform 4

4.1.2 Timing Diagram

When the compare match interrupt is generated for registers TRD0 and TRDGRA0 for the 10th time, a buffer operation is used to switch the PWM waveform.
The figures below show timing diagrams for PWM waveform switching.

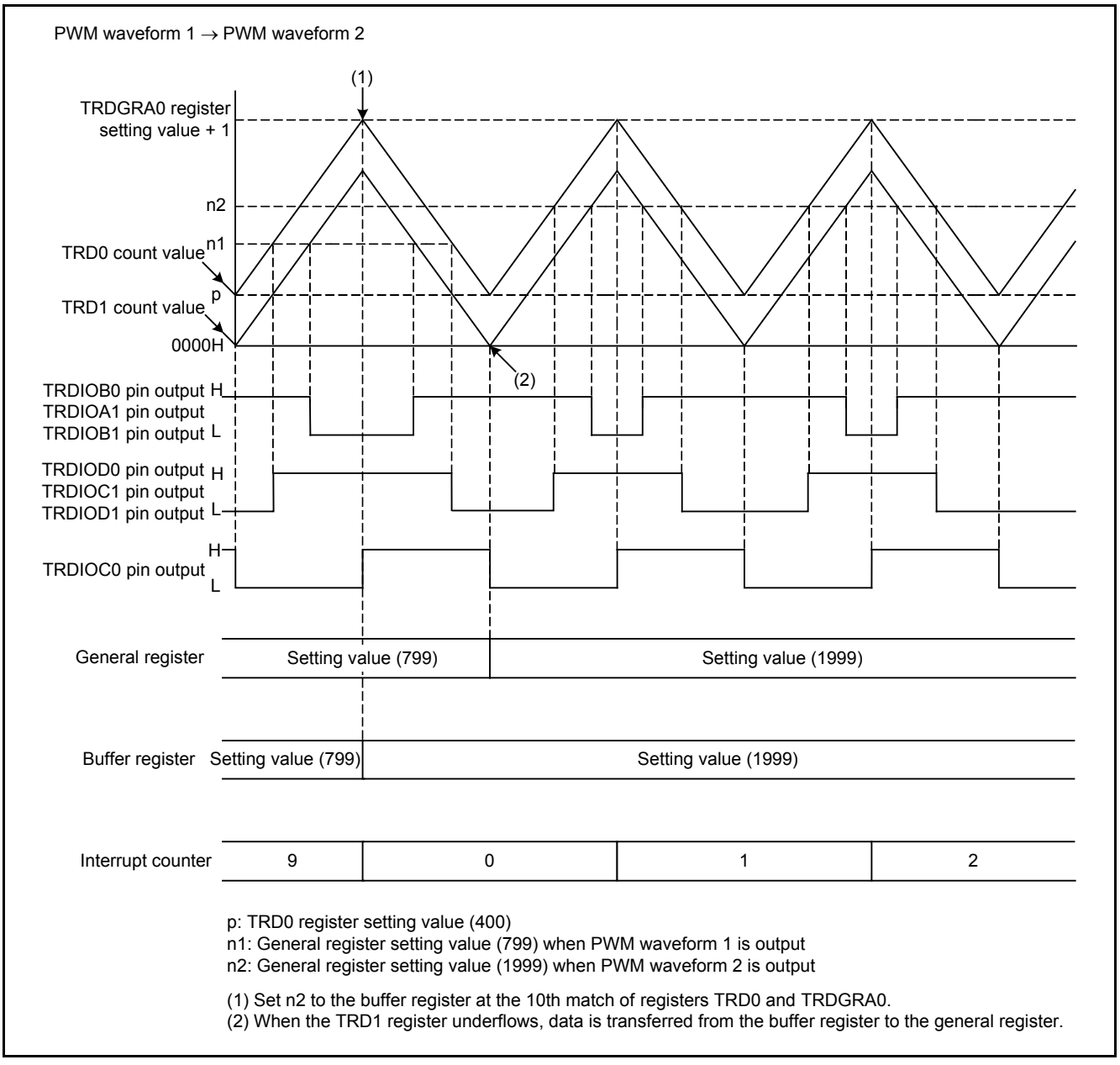
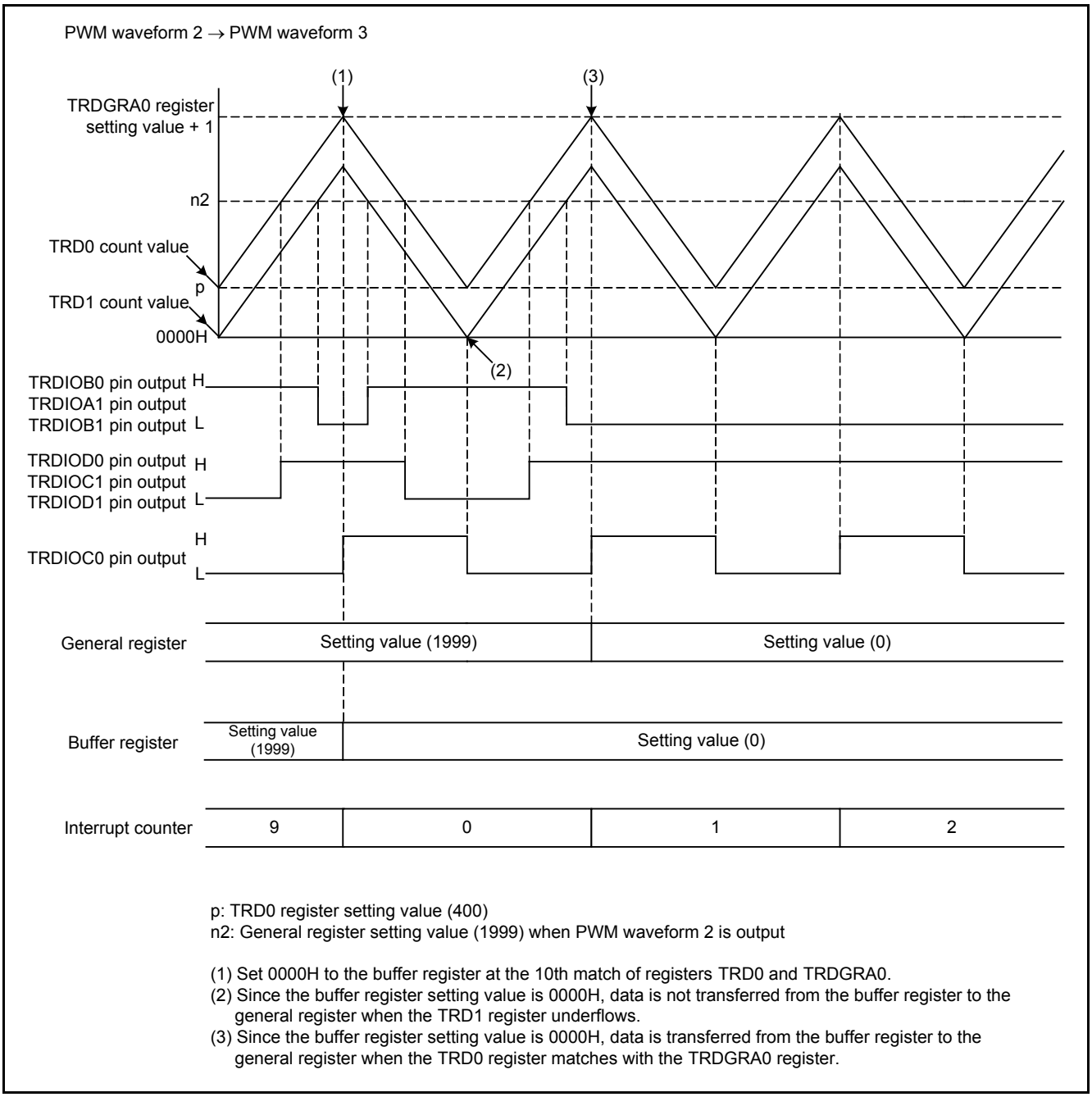


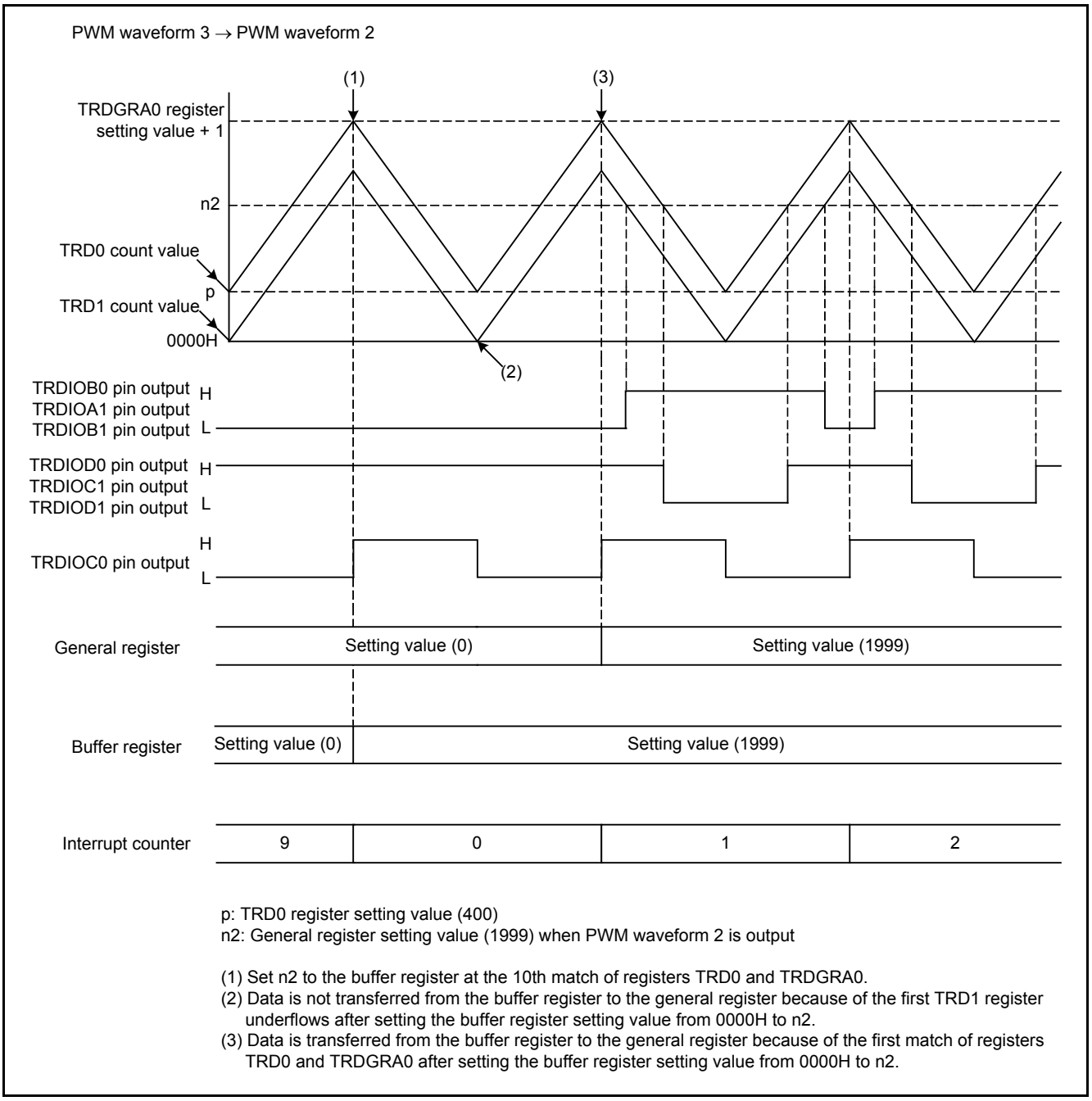
Figure 4.5 Switch Timing From PWM Waveform 1 to PWM Waveform 2



p: TRD0 register setting value (400)
n2: General register setting value (1999) when PWM waveform 2 is output

(1) Set 0000H to the buffer register at the 10th match of registers TRD0 and TRDGRA0.
(2) Since the buffer register setting value is 0000H, data is not transferred from the buffer register to the general register when the TRD1 register underflows.
(3) Since the buffer register setting value is 0000H, data is transferred from the buffer register to the general register when the TRD0 register matches with the TRDGRA0 register.

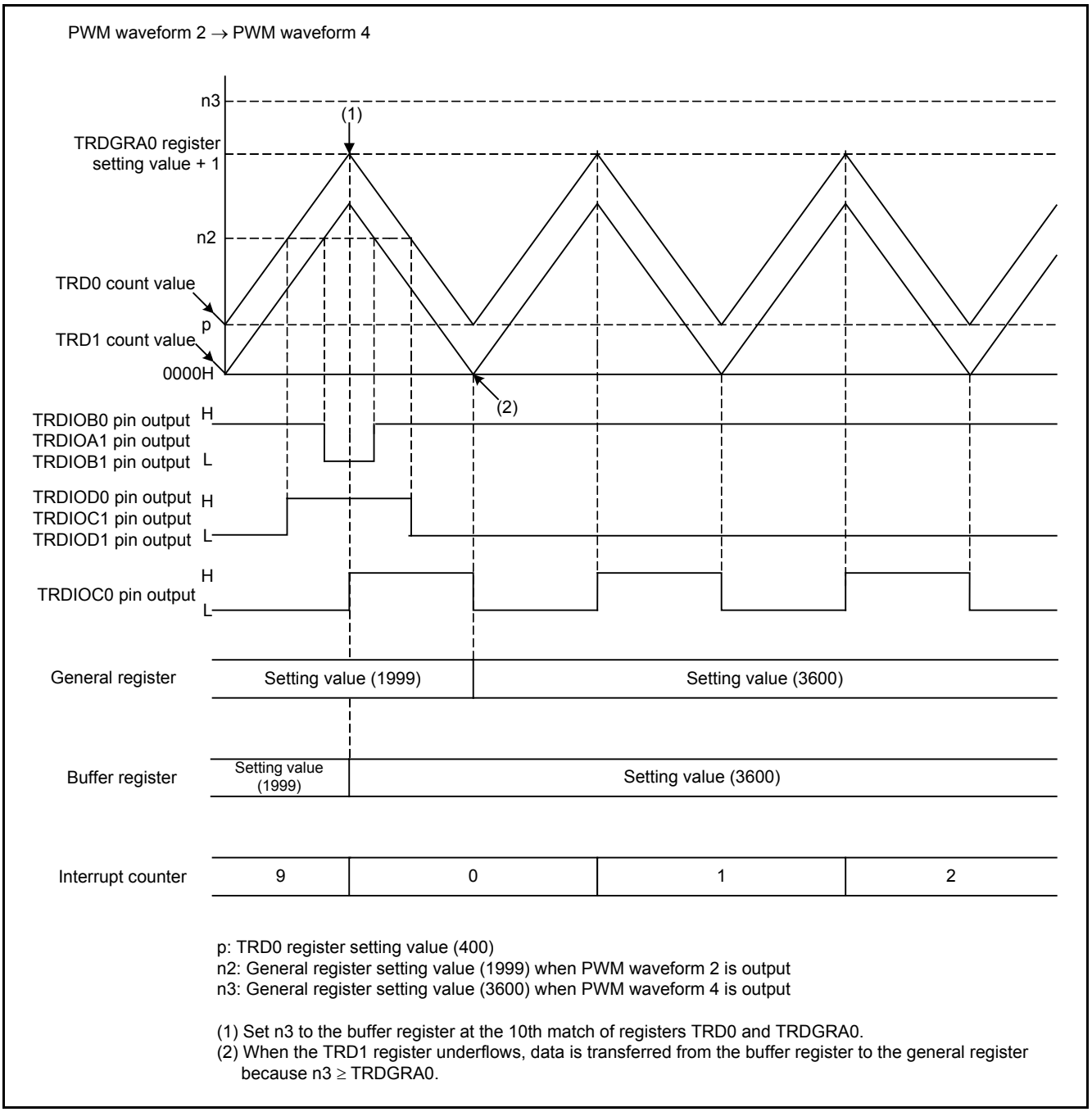
Figure 4.6 Switch Timing From PWM Waveform 2 to PWM Waveform 3



p: TRD0 register setting value (400)
n2: General register setting value (1999) when PWM waveform 2 is output

(1) Set n2 to the buffer register at the 10th match of registers TRD0 and TRDGRA0.
(2) Data is not transferred from the buffer register to the general register because of the first TRD1 register underflows after setting the buffer register setting value from 0000H to n2.
(3) Data is transferred from the buffer register to the general register because of the first match of registers TRD0 and TRDGRA0 after setting the buffer register setting value from 0000H to n2.

Figure 4.7 Switch Timing From PWM Waveform 3 to PWM Waveform 2



p: TRD0 register setting value (400)
n2: General register setting value (1999) when PWM waveform 2 is output
n3: General register setting value (3600) when PWM waveform 4 is output

(1) Set n3 to the buffer register at the 10th match of registers TRD0 and TRDGRA0.
(2) When the TRD1 register underflows, data is transferred from the buffer register to the general register because n3 ≥ TRDGRA0.

Figure 4.8 Switch Timing From PWM Waveform 2 to PWM Waveform 4

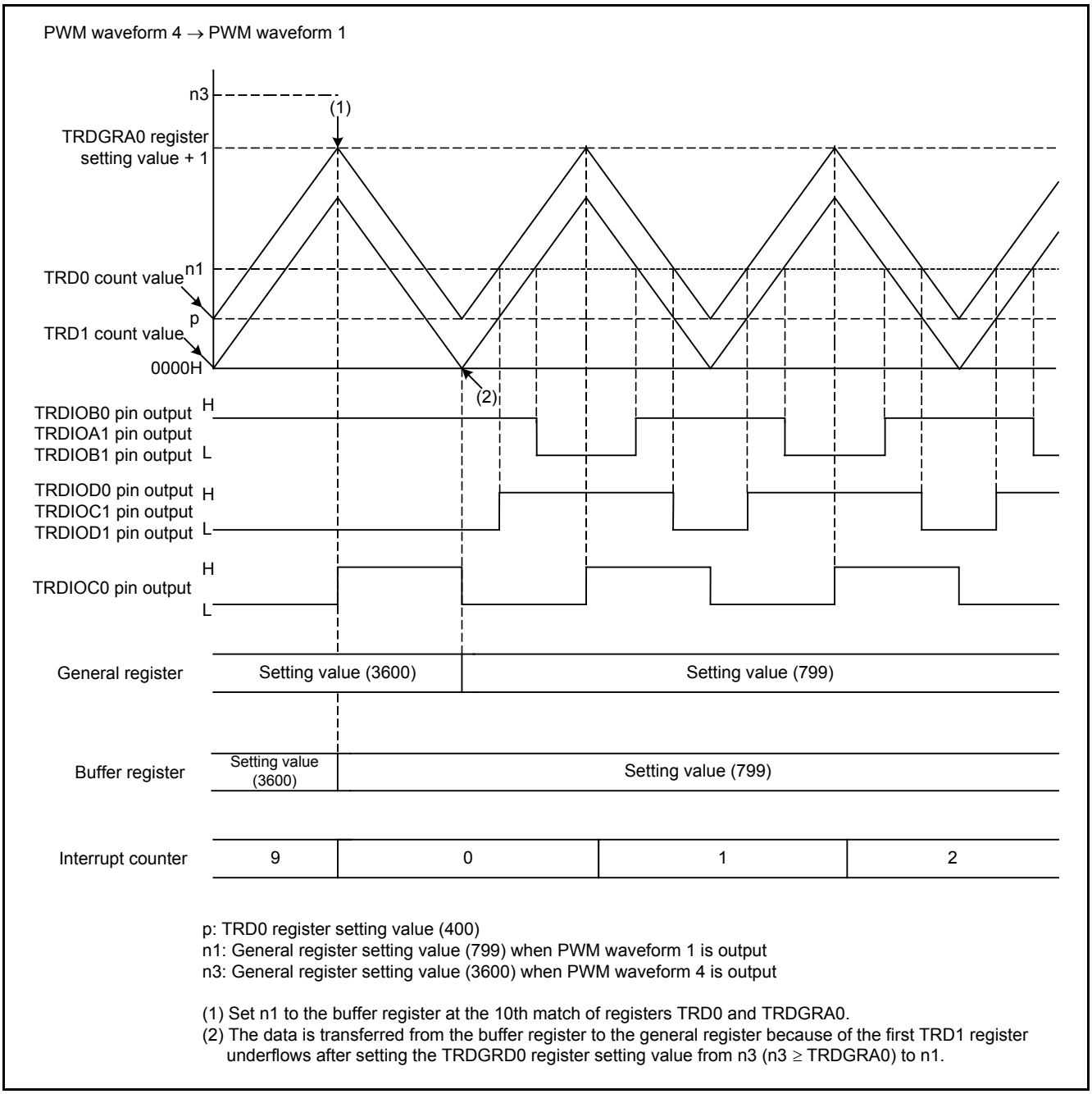


Figure 4.9 Switch Timing From PWM Waveform 4 to PWM Waveform 1

4.2 Option Byte Settings

Table 4.1 lists the Option Byte Settings. When necessary, set a value suited to the user system.

Table 4.1 Option Byte Settings

Address	Setting Value	Contents
000C0H/010C0H	11101111B	Watchdog timer operation is stopped (count is stopped after reset)
000C1H/010C1H	01111111B	LVD reset mode Detection voltage: Rising edge 2.81 V/falling edge 2.75 V
000C2H/010C2H	11101001B	Internal high-speed oscillation HS mode: 16 MHz
000C3H/010C3H	10000100B	On-chip debugging enabled

4.3 Constants

Table 4.2 lists the Constants Used in the Sample Code.

Table 4.2 Constants Used in the Sample Code

Constant Name	Setting Value	Contents
ACT_250us_100us	0	Waveform switch mode: PWM waveform 1 → PWM waveform 2
ACT_100us_LOUT	1	Waveform switch mode: PWM waveform 2 → PWM waveform 3
ACT_LOUT_100us	2	Waveform switch mode: PWM waveform 3 → PWM waveform 2
ACT_100us_HOUT	3	Waveform switch mode: PWM waveform 2 → PWM waveform 4
ACT_HOUT_250us	4	Waveform switch mode: PWM waveform 4 → PWM waveform 1
ACT_250us	0	Register setting value index of PWM waveform 1
ACT_100us	1	Register setting value index of PWM waveform 2
ACT_HOUT	2	Register setting value index of PWM waveform 4
ACT_LOUT	3	Register setting value index of PWM waveform 3

4.4 Variables

Table 4.3 lists the Global Variables and Table 4.4 lists the const Variable.

Table 4.3 Global Variables

Type	Variable Name	Contents	Function Used
unsigned char	int_cnt	Interrupt counter	r_tmr_rd0_interrupt
unsigned char	output_chg_mode	Waveform switch mode	r_tmr_rd0_interrupt

Table 4.4 const Variable

Type	Variable Name	Contents	Function Used
unsgined short const	TRDGRB0_VALUE_TBL[]	Active level setting value table	r_tmr_rd0_interrupt

4.5 Functions

Table 4.5 lists the Functions.

Table 4.5 Functions

Function Name	Outline
hdwinit	Initial setting
R_Systeminit	Initial setting of peripheral functions
R_CGC_Create	Initial setting of CPU
R_TMR_RD0_Create	Initial setting of timer RD
main	Main processing
timer_rd0_start	Timer RD count start setting
r_tmr_rd0_interrupt	Timer RD0 interrupt

4.6 Function Specifications

The following tables list the sample code function specifications.

hdwinit	
Outline	Initial setting
Header	None
Declaration	void hdwinit(void)
Description	Perform the initial setting of peripheral functions.
Argument	None
Return Value	None

R_Systeminit	
Outline	Initial setting of peripheral functions
Header	None
Declaration	void R_Systeminit(void)
Description	Perform the initial setting of peripheral functions used in this document.
Argument	None
Return Value	None

R_CGC_Create	
Outline	Initial setting of CPU
Header	None
Declaration	void R_CGC_Create(void)
Description	Perform the initial setting of the CPU.
Argument	None
Return Value	None

R_TMR_RD0_Create	
Outline	Initial setting of timer RD
Header	None
Declaration	void R_TMR_RD0_Create(void)
Description	Perform the initial setting to use timer RD in complementary PWM mode.
Argument	None
Return Value	None

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	Perform main processing.
Argument	None
Return Value	None

timer_rd0_start	
Outline	Timer RD count start setting
Header	None
Declaration	void timer_rd0_start(void)
Description	Perform timer RD count start setting.
Argument	None
Return Value	None

r_tmr_rd0_interrupt	
Outline	Timer RD0 interrupt
Header	None
Declaration	void r_tmr_rd0_interrupt(void)
Description	• Perform timer RD0 interrupt service routine. • When the 10th interrupt is generated, set the buffer register value.
Argument	None
Return Value	None

4.7 Flowcharts

4.7.1 Overall Flowchart

Figure 4.10 shows the Overall Flowchart.

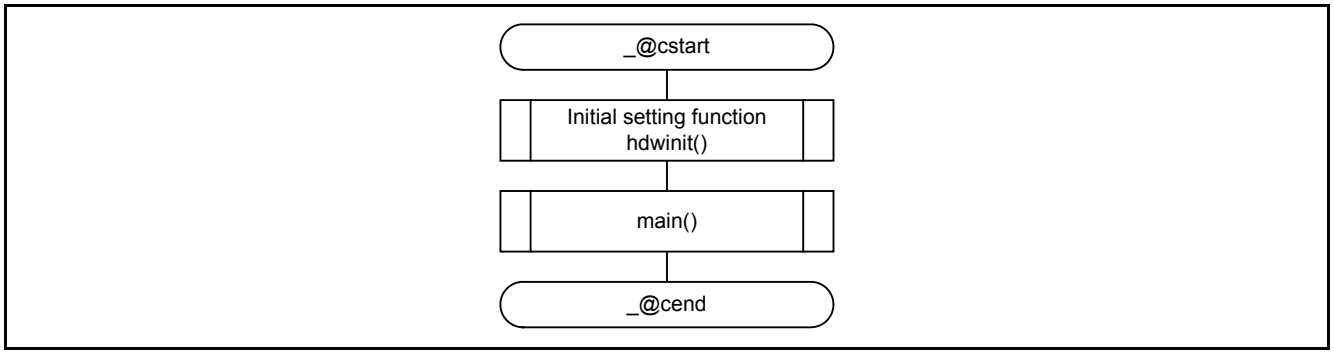


Figure 4.10 Overall Flowchart

4.7.2 Initial Setting

Figure 4.11 shows the Initial Setting.

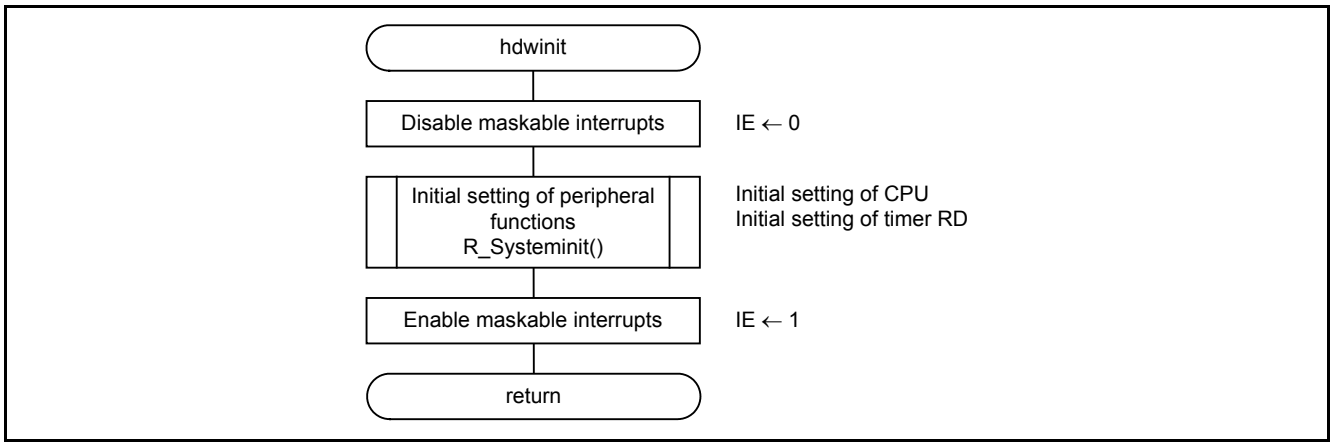


Figure 4.11 Initial Setting

4.7.3 Initial Setting of Peripheral Functions

Figure 4.12 shows the Initial Setting of Peripheral Functions.

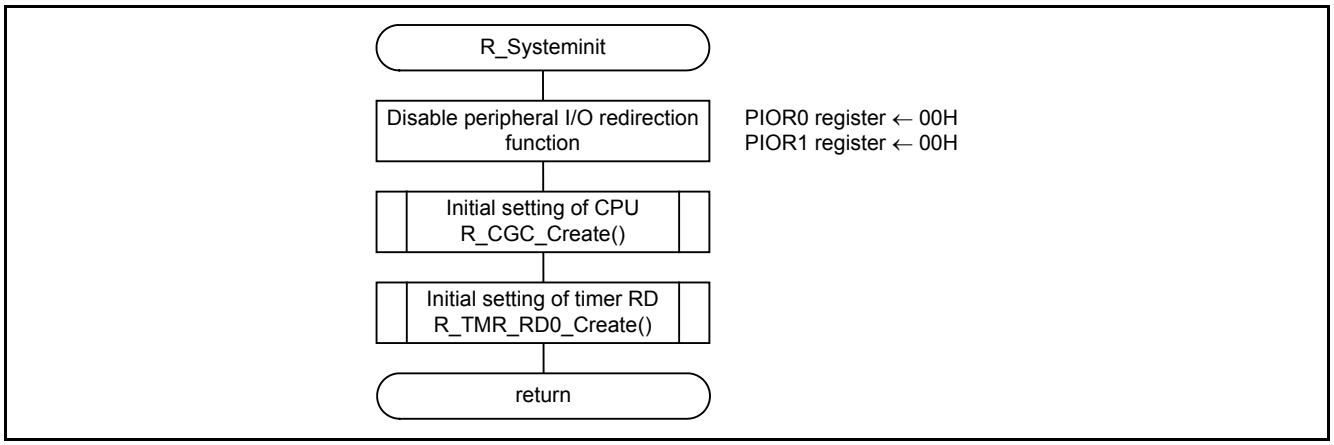


Figure 4.12 Initial Setting of Peripheral Functions

4.7.4 Initial Setting of the CPU

Figure 4.13 shows the Initial Setting of the CPU.

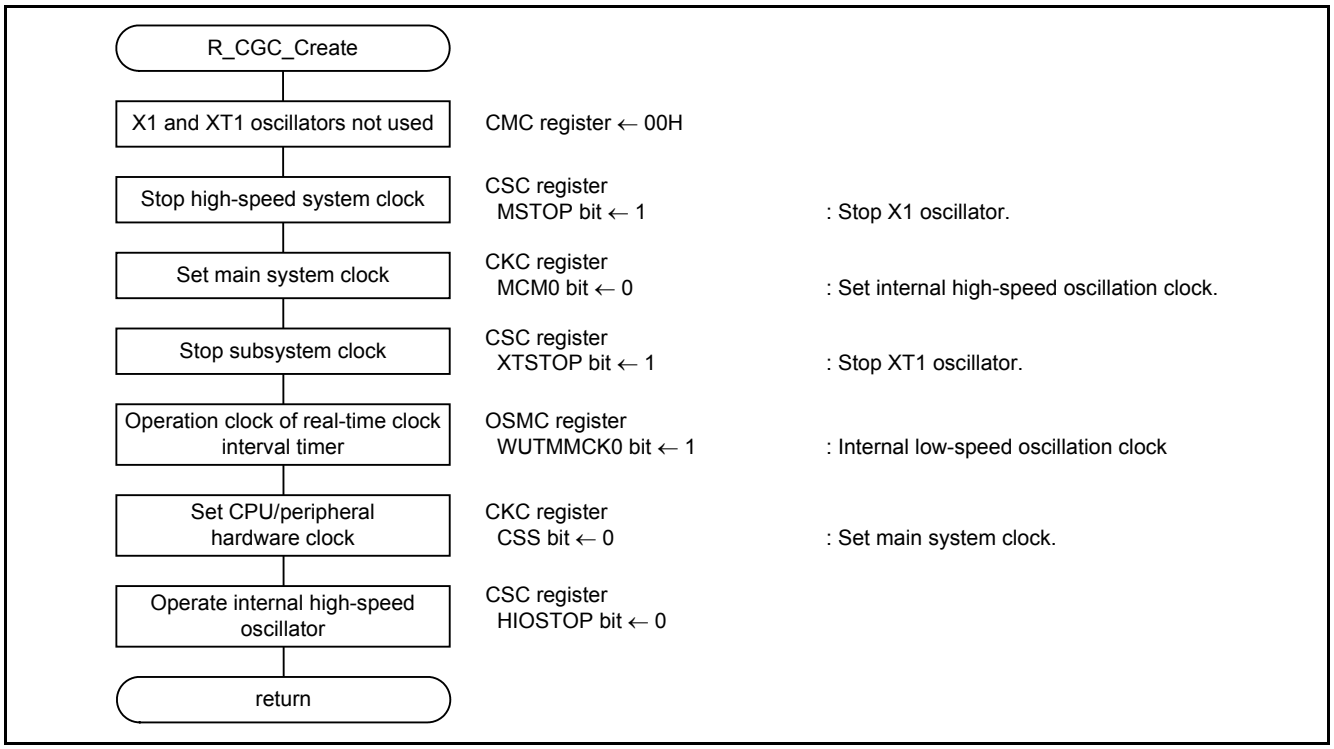


Figure 4.13 Initial Setting of the CPU

4.7.5 Initial Setting of Timer RD

Figure 4.14 and Figure 4.15 show the Initial Setting of Timer RD.

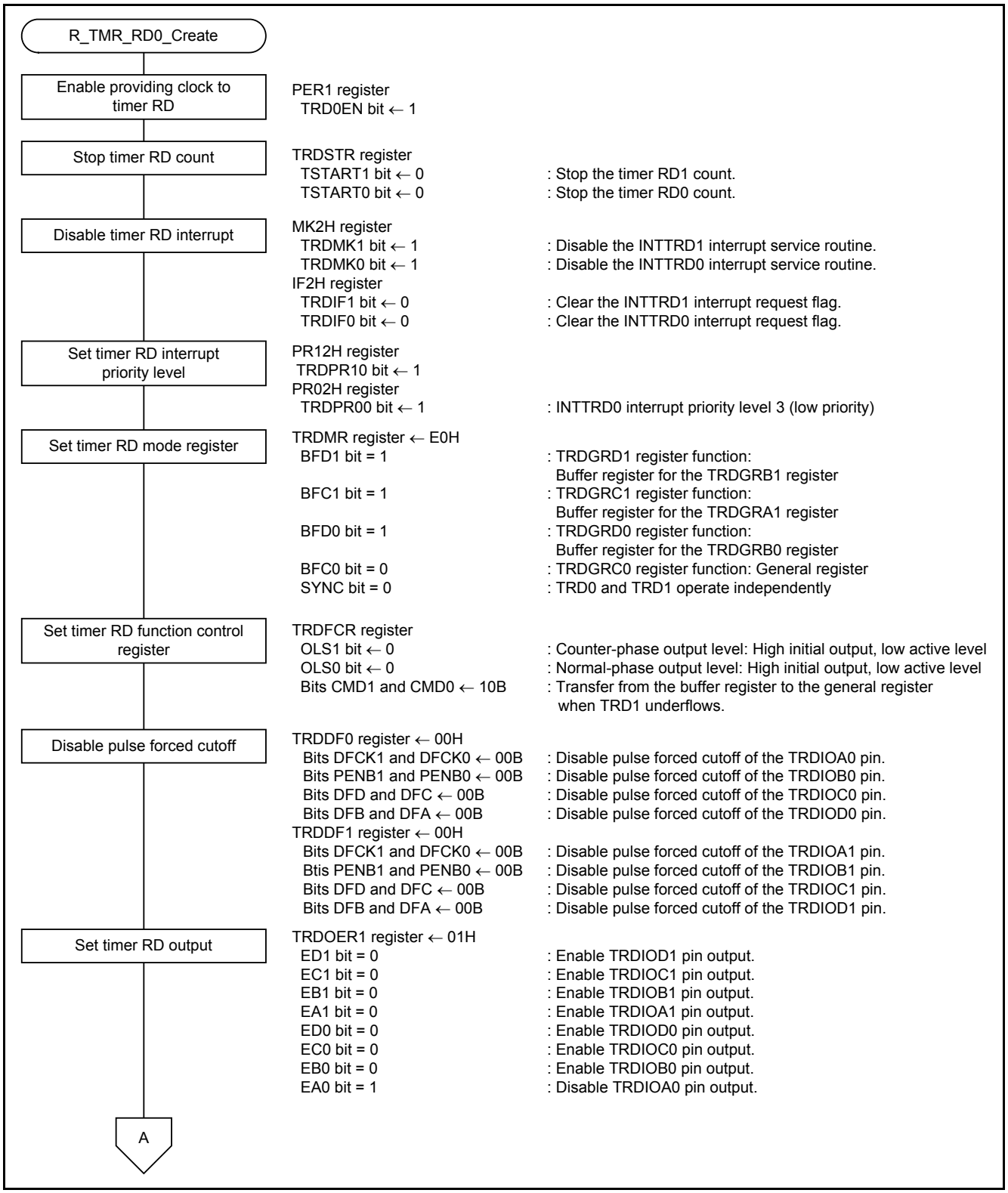


Figure 4.14 Initial Setting of Timer RD (1/2)

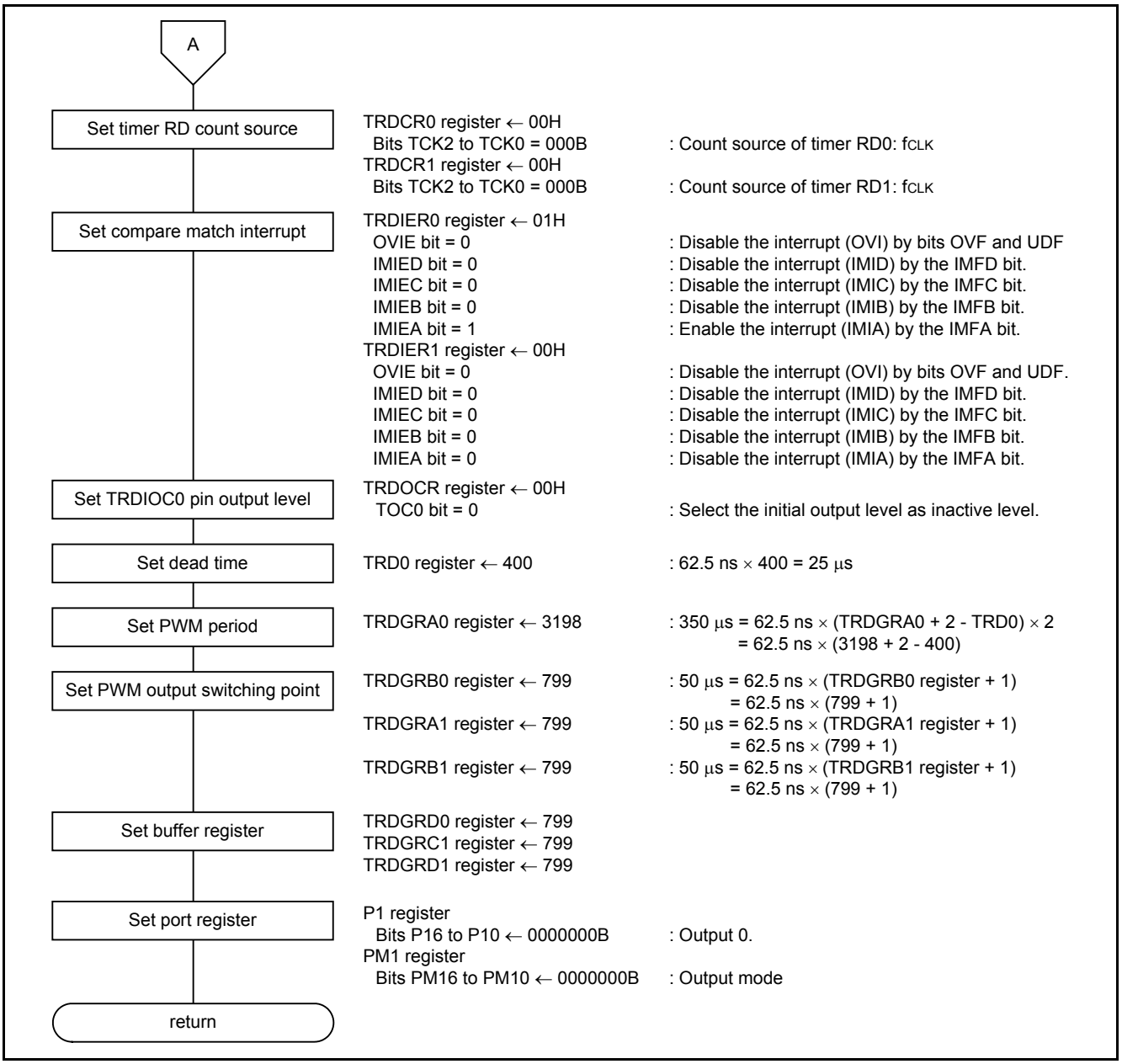


Figure 4.15 Initial Setting of Timer RD (2/2)

Enable providing a clock to timer RD.

- Peripheral Enable Register 1 (PER1)
  Enable providing a clock to timer RD.

Symbol	7	6	5	4	3	2	1	0
PER1	DACEN	TRGEN	CMPEN	TRD0EN	DTCEN	0	0	TRJ0EN
Setting Value	x	x	x	1	x	—	—	x

Bit 4

TRD0EN	Control of timer RD input clock supply
0	Stops input clock supply. • SFR used by timer RD cannot be written. • Timer RD is in the reset status.
1	Enables input clock supply. • SFR used by timer RD can be read and written.

Stop the timer RD count.

- Timer RD Mode Register (TRDSTR)
  Stop the timer RD count.

Symbol	7	6	5	4	3	2	1	0
TRDSTR	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
Setting Value	—	—	—	—			0	0

Bit 3

CSEL1	TRD1 count operation select
0	Count stops at compare match with TRDGRA1 register
1	Count continues after compare match with TRDGRA1 register

Bit 2

CSEL0	TRD0 count operation select
0	Count stops at compare match with TRDGRA0 register
1	Count continues after compare match with TRDGRA0 register

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Bit 1

TSTART1	TRD1 count start flag
0	Count stops
1	Count starts

Bit 0

TSTART0	TRD0 count start flag
0	Count stops
1	Count starts

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Disable the timer RD interrupt.

- Interrupt Mask Flag Register (MK2H)
  Disable INTTRD0 and INTTRD1 interrupts.

Symbol	7	6	5	4	3	2	1	0
MK2H	FLMK	IICAMK1	1	SREMK3 TMMK13H	TRGMK	TRDMK1	TRDMK0	PMK11 CMPMK1
Setting Value	x	x	—	x	x	1	1	x

Bit 2

TRDMK1	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Bit 1

TRDMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

- Interrupt Request Flag Register (IF2H)
  Clear the INTTRD0 interrupt request flag and INTTRD1 interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF2H	FLIF	IICAIF1	0	SREIF3 TMIF13H	TRGIF	TRDIF1	TRDIF0	PIF11 CMPIF1
Setting Value	x	x	—	x	x	0	0	x

Bit 2

TRDIF1	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Bit 1

TRDIF0	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the timer RD interrupt priority level.

- Priority Specification Flag Registers (PR02H and PR12H)
  Set to level 3 (low priority).

Symbol	7	6	5	4	3	2	1	0
PR02H	FLPR0	IICAPR01	1	SREPR03 TMPR013H	TRGPR0	TRDPR01	TRDPR00	PPR011 CMPPR01
Setting Value	x	x	—	x	x	x	1	x

Symbol	7	6	5	4	3	2	1	0
PR12H	FLPR1	IICAPR11	1	SREPR13 TMPR113H	TRGPR1	TRDPR11	TRDPR10	PPR111 CMPPR11
Setting Value	x	x	—	x	x	x	1	x

TRDPR10	TRDPR00	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	1	Specify level 3 (low priority level)

Set timer RD mode register.

- Timer RD Mode Register (TRDMR)
  Use registers TRDGRD0, TRDGRC1, and TRDGRD1 as the buffer registers.

Symbol	7	6	5	4	3	2	1	0
TRDMR	BFD1	BFC1	BFD0	BFC0	—	—	—	SYNC
Setting Value	1	1	1	0	—	—	—	0

Bit 7

BFD1	TRDGRD1 register function select
0	General register
1	Buffer register for TRDGRB1 register

Bit 6

BFC1	TRDGRC1 register function select
0	General register
1	Buffer register for TRDGRA1 register

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Bit 5

BFD0	TRDGRD0 register function select
0	General register
1	Buffer register for TRDGRB0 register

Bit 4

BFC0	TRDGRC0 register function select
0	General register
1	Buffer register for TRDGRA0 register

Set to 0 in complementary PWM mode.

Bit 0

SYNC	Timer RD synchronous
0	TRD0 and TRD1 operate independently
1	TRD0 and TRD1 operate synchronously

Set to 0 in complementary PWM mode.

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the timer RD function control register.

- Timer RD Function Control Register (TRDFCR)

Use normal-phase output level, counter-phase output level, and combination mode.

Symbol	7	6	5	4	3	2	1	0
TRDFCR	PWM3	STCLK	0	0	OLS1	OLS0	CMD1	CMD0
Setting Value	x	x	—	—	0	0	1	0

Bit 3

OLS1	Counter-phase output level select (in reset synchronous PWM mode or complementary PWM mode)
• In reset synchronous and complementary PWM modes, 0: High initial output and low active level 1: Low initial output and high active level • Disabled in timer and PWM3 modes.	

Bit 2

OLS0	Normal-phase output level select (in reset synchronous PWM mode or complementary PWM mode)
• In reset synchronous and complementary PWM modes, 0: High initial output and low active level 1: Low initial output and high active level • Disabled in timer and PWM3 modes.	

Bits 1 and 0

CMD1	CMD0	Combination mode select
• In timer and PWM3 modes, set to 00B (timer mode or PWM3 mode). • In reset synchronous PWM mode, set to 01B (reset synchronous PWM mode). • In complementary PWM mode, CMD1 CMD0 1 0: Complementary PWM mode (transfer from the buffer register to the general register when TRD1 underflows) 1 1: Complementary PWM mode (transfer from the buffer register to the general register at compare match between registers TRD0 and TRDGRA0) Other than the above: Do not set.		

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Disable pulse forced cut-off.

- Timer RD Digital Filter Function Select Register 0 (TRDDF0)
  Disable pulse forced cut-off of pins TRDIOA0, TRDIOB0, TRDIOC0, and TRDIOD0.

Symbol	7	6	5	4	3	2	1	0
TRDDF0	DFCK1	DFCK0	PENB1	PENB0	DFD	DFC	DFB	DFA
Setting Value	0	0	0	0	0	0	0	0

Bits 7 and 6

DFCK1	DFCK0	TRDIOA0 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output
Set these bits to 00B (forced cutoff disabled) if the corresponding pin is not used as a timer RD output port in these modes. Also, set these bits while the count is stopped.		

Bits 5 and 4

PENB1	PENB0	TRDIOB0 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output
Set these bits to 00B (forced cutoff disabled) if the corresponding pin is not used as a timer RD output port in these modes. Also, set these bits while the count is stopped.		

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Bits 3 and 2

DFD	DFC	TRDIOC0 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output
Set these bits to 00B (forced cutoff disabled) if the corresponding pin is not used as a timer RD output port in these modes. Also, set these bits while the count is stopped.		

Bits 1 and 0

DFB	DFA	TRDIOD0 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output
Set these bits to 00B (forced cutoff disabled) if the corresponding pin is not used as a timer RD output port in these modes. Also, set these bits while the count is stopped.		

- Timer RD Digital Filter Function Select Register 0 (TRDDF1)
  Disable pulse forced cut-off of pins TRDIOA1, TRDIOB1, TRDIOC1, and TRDIOD1.

Symbol	7	6	5	4	3	2	1	0
TRDDF1	DFCK1	DFCK0	PENB1	PENB0	DFD	DFC	DFB	DFA
Setting Value	0	0	0	0	0	0	0	0

Bits 7 and 6

DFCK1	DFCK0	TRDIOA0 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output
Set these bits to 00B (forced cutoff disabled) if the corresponding pin is not used as a timer RD output port in these modes. Also, set these bits while the count is stopped.		

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Bits 5 and 4

PENB1	PENB0	TRDIOB1 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output
Set these bits to 00B (forced cutoff disabled) if the corresponding pin is not used as a timer RD output port in these modes. Also, set these bits while the count is stopped.		

Bits 3 and 2

DFD	DFC	TRDIOC1 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output
Set these bits to 00B (forced cutoff disabled) if the corresponding pin is not used as a timer RD output port in these modes. Also, set these bits while the count is stopped.		

Bits 1 and 0

DFB	DFA	TRDIOD1 pin pulse forced cutoff control
0	0	Forced cutoff disabled
0	1	High-impedance output
1	0	Low output
1	1	High output
Set these bits to 00B (forced cutoff disabled) if the corresponding pin is not used as a timer RD output port in these modes. Also, set these bits while the count is stopped.		

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set timer RD output.

- Timer RD Output Master Enable Register 1 (TRDOER1)
  Disable TRDIOA0 pin output, and enable output of pins TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, and TRDIOD1.

Symbol	7	6	5	4	3	2	1	0
TRDOER1	ED1	EC1	EB1	EA1	ED0	EC0	EB0	EA0
Setting Value	0	0	0	0	0	0	0	1

Bit 7

ED1	TRDIOD1 output disable
0	Output enabled
1	Output disabled (TRDIOD1 pin functions as an I/O port.)

Bit 6

EC1	TRDIOC1 output disable
0	Output enabled
1	Output disabled (TRDIOC1 pin functions as an I/O port.)

Bit 5

EB1	TRDIOB1 output disable
0	Output enabled
1	Output disabled (TRDIOB1 pin functions as an I/O port.)

Bit 4

EA1	TRDIOA1 output disable
0	Output enabled
1	Output disabled (TRDIOA1 pin functions as an I/O port.)

Bit 3

ED0	TRDIOD0 output disable
0	Output enabled
1	Output disabled (TRDIOD0 pin functions as an I/O port.)

Bit 2

EC0	TRDIOC0 output disable
0	Output enabled
1	Output disabled (TRDIOC0 pin functions as an I/O port.)

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Bit 1

EB0	TRDIOB0 output disable
0	Output enabled
1	Output disabled (TRDIOB0 pin functions as an I/O port.)

Bit 0

EA0	TRDIOA0 output disable
0	Output enabled
1	Output disabled (TRDIOA0 pin functions as an I/O port.)

Set to 1 in complementary PWM mode

Set the timer RD count source.

- Timer RD Control Register 0 (TRDCR0)
  Set f_{CLK} to the count source of timer RD0.

Symbol	7	6	5	4	3	2	1	0
TRDCR0	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
Setting Value	x	x	x	x	x	0	0	0

Bits 2 and 0

TCK2	TCK1	TCK0	Count source select
0	0	0	f_{CLK}, f_{HOCO}
0	0	1	$f_{CLK}/2$
0	1	0	$f_{CLK}/4$
0	1	1	$f_{CLK}/8$
1	0	0	$f_{CLK}/32$
1	0	1	TRDCLK input
1	1	0	Do not set.
1	1	1	Do not set.

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the compare match interrupt.

- Timer RD Interrupt Enable Register 0 (TRDIER0)
  Enable the interrupt (IMIA) by the IMFA bit.

Symbol	7	6	5	4	3	2	1	0
TRDIER0	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA
Setting Value	—	—	—	0	0	0	0	1

Bit 4

OVIE	Overflow/underflow interrupt enable
0	Interrupt (OVI) by bits OVF and UDF disabled
1	Interrupt (OVI) by bits OVF and UDF enabled

Bit 3

IMIED	Input capture/compare match interrupt enable D
0	Interrupt (IMID) by the IMFD bit is disabled
1	Interrupt (IMID) by the IMFD bit is enabled

Bit 2

IMIEC	Input capture/compare match interrupt enable C
0	Interrupt (IMIC) by the IMFC bit is disabled
1	Interrupt (IMIC) by the IMFC bit is enabled

Bit 1

IMIEB	Input capture/compare match interrupt enable B
0	Interrupt (IMIB) by the IMFB bit is disabled
1	Interrupt (IMIB) by the IMFB bit is enabled

Bit 0

IMIEA	Input capture/compare match interrupt enable A
0	Interrupt (IMIA) by the IMFA bit is disabled
1	Interrupt (IMIA) by the IMFA bit is enabled

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

- Timer RD Interrupt Enable Register 1 (TRDIER1)
  Disable the timer RD1 interrupt.

Symbol	7	6	5	4	3	2	1	0
TRDIER1	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA
Setting Value	—	—	—	0	0	0	0	0

Bit 4

OVIE	Overflow/underflow interrupt enable
0	Interrupt (OVI) by bits OVF and UDF disabled
1	Interrupt (OVI) by bits OVF and UDF enabled

Bit 3

IMIED	Input capture/compare match interrupt enable D
0	Interrupt (IMID) by the IMFD bit is disabled
1	Interrupt (IMID) by the IMFD bit is enabled

Bit 2

IMIEC	Input capture/compare match interrupt enable C
0	Interrupt (IMIC) by the IMFC bit is disabled
1	Interrupt (IMIC) by the IMFC bit is enabled

Bit 1

IMIEB	Input capture/compare match interrupt enable B
0	Interrupt (IMIB) by the IMFB bit is disabled
1	Interrupt (IMIB) by the IMFB bit is enabled

Bit 0

IMIEA	Input capture/compare match interrupt enable A
0	Interrupt (IMIA) by the IMFA bit is disabled
1	Interrupt (IMIA) by the IMFA bit is enabled

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the TRDIOC0 pin output level.

- Timer RD Output Control Register 0 (TRDOCR)
  Set low for initial output of the TRDIOC0 pin.

Symbol	7	6	5	4	3	2	1	0
TRDOCR	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0
Setting Value	x	x	x	x	x	0	x	x

Bit 2

TOC0	TRDIOC0 initial output level select
0	Initial output is not active level
1	Initial output is active level
Enabled in reset synchronous and complementary PWM modes.	

Set dead time.

- Timer RD Counter 0 (TRD0)
  Set dead time to 25 μs.

Symbol	15	14	13	12	11	10	9	8
TRD0	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	0	0	1

Symbol	7	6	5	4	3	2	1	0
TRD0	—	—	—	—	—	—	—	—
Setting Value	1	0	0	1	0	0	0	0

—	Function	Setting Range
Bits 15 to 0	Dead time must be set. Count the count source. Count operation is incremented or decremented. When an overflow occurs, the OVF bit in the TRDSR0 register is set to 1.	0001H to FFFFH

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the PWM period.

- Timer RD General Register A0 (TRDGRA0)
  Set the PWM period to 350 µs.

Symbol	15	14	13	12	11	10	9	8
TRDGRA0	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	1	1	0	0

Symbol	7	6	5	4	3	2	1	0
TRDGRA0	—	—	—	—	—	—	—	—
Setting Value	0	1	1	1	1	1	1	0

—	Function	Setting Range
Bits 15 to 0	See Table 4.6 General Register Functions in Complementary PWM Mode.	0000H to FFFFH

Set the PWM output changing point.

- Timer RD General Register B0 (TRDGRB0)
  Set this register after 50 µs from the count start to change the output of PWM output 1.

Symbol	15	14	13	12	11	10	9	8
TRDGRB0	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	0	1	1

Symbol	7	6	5	4	3	2	1	0
TRDGRB0	—	—	—	—	—	—	—	—
Setting Value	0	0	0	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.6 General Register Functions in Complementary PWM Mode.	0000H to FFFFH

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

• Timer RD General Register A1 (TRDGRA1)
Set this register after 50 µs from the count start to change the output of PWM output 2.

Symbol	15	14	13	12	11	10	9	8
TRDGRA1	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	0	1	1

Symbol	7	6	5	4	3	2	1	0
TRDGRA1	—	—	—	—	—	—	—	—
Setting Value	0	0	0	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.6 General Register Functions in Complementary PWM Mode.	0000H to FFFFH

• Timer RD General Register B1 (TRDGRB1)
Set this register after 50 µs from the count start to change the output of PWM output 3.

Symbol	15	14	13	12	11	10	9	8
TRDGRB1	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	0	1	1

Symbol	7	6	5	4	3	2	1	0
TRDGRB1	—	—	—	—	—	—	—	—
Setting Value	0	0	0	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.6 General Register Functions in Complementary PWM Mode.	0000H to FFFFH

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Set the buffer register.

- Timer RD General Register D0 (TRDGRD0)
  Set 31FH to the buffer register of the TRDGRB0 register (TRDGRD0).

Symbol	15	14	13	12	11	10	9	8
TRDGRD0	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	0	1	1

Symbol	7	6	5	4	3	2	1	0
TRDGRD0	—	—	—	—	—	—	—	—
Setting Value	0	0	0	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.6 General Register Functions in Complementary PWM Mode.	0000H to FFFFH

- Timer RD General Register C1 (TRDGRC1)
  Set 31FH to the buffer register of the TRDGRA1 register (TRDGRC1).

Symbol	15	14	13	12	11	10	9	8
TRDGRC1	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	0	1	1

Symbol	7	6	5	4	3	2	1	0
TRDGRC1	—	—	—	—	—	—	—	—
Setting Value	0	0	0	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.6 General Register Functions in Complementary PWM Mode.	0000H to FFFFH

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned

- Timer RD General Register D1 (TRDGRD1)
  Set 31FH to the buffer register of the TRDGRB1 register (TRDGRD1).

Symbol	15	14	13	12	11	10	9	8
TRDGRD1	—	—	—	—	—	—	—	—
Setting Value	0	0	0	0	0	0	1	1

Symbol	7	6	5	4	3	2	1	0
TRDGRD1	—	—	—	—	—	—	—	—
Setting Value	0	0	0	1	1	1	1	1

—	Function	Setting Range
Bits 15 to 0	See Table 4.6 General Register Functions in Complementary PWM Mode.	0000H to FFFFH

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned

Table 4.6 General Register Functions in Complementary PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRA0	—	General register. Set the PWM period at initialization. Setting range: ≥ Value set in TRD0 register ≥ FFFFh - value set in TRD0 register Do not write to this register when bits TSTART0 and TSTART1 in the TRDSTR register are set to 1 (count starts).	(TRDIOC0, output inverted every half period)
TRDGRB0	—	General register. Set the changing point of PWM1 output at initialization. Setting range: ≥ Value set in TRD0 register ≤ Value set in TRDGRA0 register - value set in TRD0 register Do not write to this register when bits TSTART0 and TSTART1 in the TRDSTR register are set to 1 (count starts).	TRDIOB0 TRDIOD0
TRDGRA1	—	General register. Set the changing point of PWM2 output at initialization. Setting range: ≥ Value set in TRD0 register ≤ Value set in TRDGRA0 register - value set in TRD0 register Do not write to this register when bits TSTART0 and TSTART1 in the TRDSTR register are set to 1 (count starts).	TRDIOA1 TRDIOC1
TRDGRB1	—	General register. Set the changing point of PWM3 output at initialization. Setting range: ≥ Value set in TRD0 register ≤ Value set in TRDGRA0 register - value set in TRD0 register Do not write to this register when bits TSTART0 and TSTART1 in the TRDSTR register are set to 1 (count starts).	TRDIOB1 TRDIOD1
TRDGRC0	—	(Not used in complementary PWM mode.)	—
TRDGRD0	BFD0 = 1	Buffer register. Set the changing point of next PWM1 output Setting range: ≥ Value set in TRD0 register □□□□□□□□□□□□□□≤ Value set in TRDGRA0 register - value set in TRD0 register Set this register to the same value as the TRDGRB0 register for initialization.	TRDIOB0 TRDIOD0
TRDGRC1	BFC1 = 1	Buffer register. Set the changing point of next PWM2 output Setting range: ≥ Value set in TRD0 register □□□□□□□□□□□□□□□□□□□□□□□□□□□□≤ Value set in TRDGRA0 register - value set in TRD0 register Set this register to the same value as the TRDGRA1 register for initialization.	TRDIOA1 TRDIOC1
TRDGRD1	BFD1 = 1	Buffer register. Set the changing point of next PWM3 output Setting range: ≥ Value set in TRD0 register □□□□□□□□□□□□□□□□□□□□□□□□□□□□≤ Value set in TRDGRA0 register - value set in TRD0 register Set this register to the same value as the TRDGRB1 register for initialization.	TRDIOB1 TRDIOD1

Set the port register.

- Port Register 1 (P1)
  Set port register 1.

Symbol	7	6	5	4	3	2	1	0
P1	P17	P16	P15	P14	P13	P12	P11	P10
Setting Value	x	0	0	0	0	0	0	0

Bit 6

P16	Output data control
0	Output 0
1	Output 1

Bit 5

P15	Output data control
0	Output 0
1	Output 1

Bit 4

P14	Output data control
0	Output 0
1	Output 1

Bit 3

P13	Output data control
0	Output 0
1	Output 1

Bit 2

P12	Output data control
0	Output 0
1	Output 1

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned

Bit 1

P11	Output data control
0	Output 0
1	Output 1

Bit 0

P10	Output data control
0	Output 0
1	Output 1

- Port Mode Register 1 (PM1)
  Set pins P16 to P11 to output mode.

Symbol	7	6	5	4	3	2	1	0
P1	P17	P16	P15	P14	P13	P12	P11	P10
Setting Value	x	0	0	0	0	0	0	0

Bit 6

PM16	P16 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Bit 5

PM15	P15 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Bit 4

PM14	P14 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Bit 3

PM13	P13 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned

Bit 2

PM12	P12 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Bit 1

PM11	P11 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Bit 0

PM10	P10 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

4.7.6 Main Processing

Figure 4.16 shows the Main Processing.

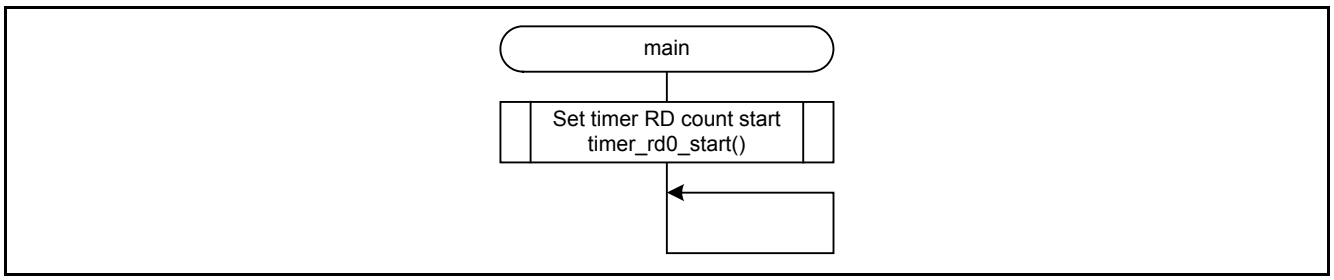


Figure 4.16 Main Processing

4.7.7 Timer RD Count Start Setting

Figure 4.17 shows the Timer RD Count Start Setting.

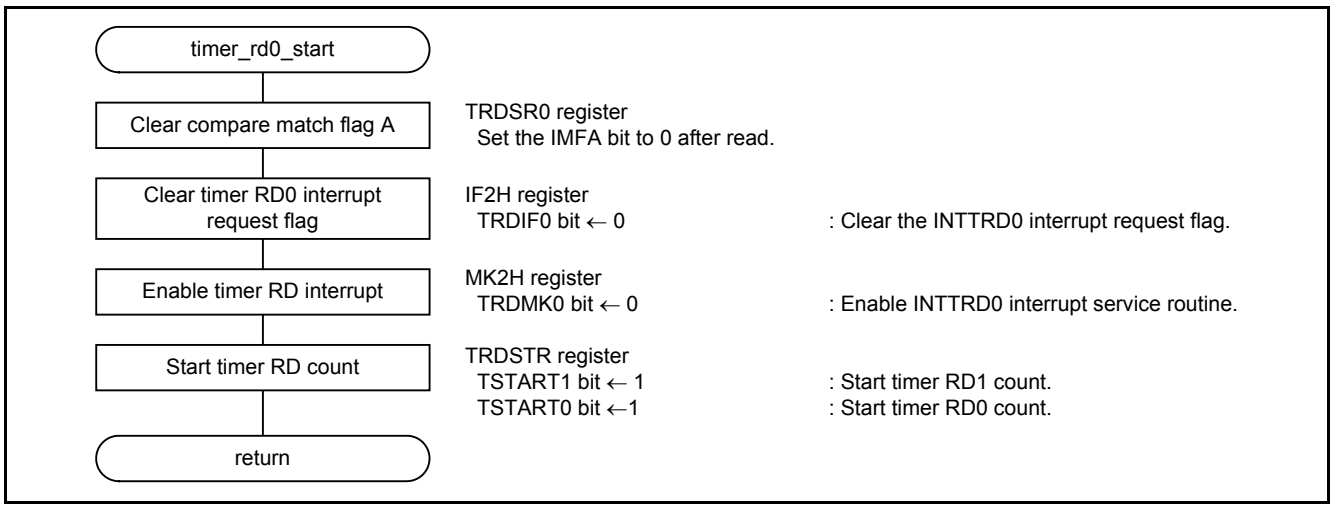


Figure 4.17 Timer RD Count Start Setting

Clear compare match flag A.

- Timer RD Status Register 0 (TRDSR0)
  Clear compare match flag A after reading timer RD status register 0.

Symbol	7	6	5	4	3	2	1	0
TRDSR0	—	—	—	OVF	IMFD	IMFC	IMFB	IMFA
Setting Value	—	—	—	x	x	x	x	0

Bit 0

IMFA	Input capture/compare match flag A
[Source for setting to 0] Write 0 after reading. [Source for setting to 1] When the values of TRD0 and TRDGRA0 match.	

Clear the timer RD0 interrupt request flag.

- Interrupt Request Flag Register (IF2H)
  Clear the INTTRD0 interrupt request flag.

Symbol	7	6	5	4	3	2	1	0
IF2H	FLIF	IICAIF1	0	SREIF3 TMIF13H	TRGIF	TRDIF1	TRDIF0	PIF11 CMPIF1
Setting Value	x	x	—	x	x		0	x

Bit 1

TRDIF0	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Enable the timer RD0 interrupt.

- Interrupt Mask Flag Register (MK2H)
  Enable the INTTRD0 interrupt.

Symbol	7	6	5	4	3	2	1	0
MK2H	FLMK	IICAMK1	1	SREMK3 TMMK13H	TRGMK	TRDMK1	TRDMK0	PMK11 CMPMK1
Setting Value	x	x	—	x	x		0	x

Bit 1

TRDMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

Start the timer RD count.

- Timer RD Mode Register (TRDSTR)
  Start the timer RD count.

Symbol	7	6	5	4	3	2	1	0
TRDSTR	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
Setting Value	—	—	—	—			1	1

Bit 1

TSTART1	TRD1 count start flag
0	Count stops
1	Count starts

Bit 0

TSTART0	TRD0 count start flag
0	Count stops
1	Count starts

Refer to the RL78/G14 user's manual (hardware) for details on individual registers.
Initial values of individual bits
x: Bits not used in this application; blank spaces: bits that do not change; —: reserved bits or bits that have nothing assigned.

4.7.8 Timer RD0 Interrupt

Figure 4.18 shows the Timer RD0 Interrupt.

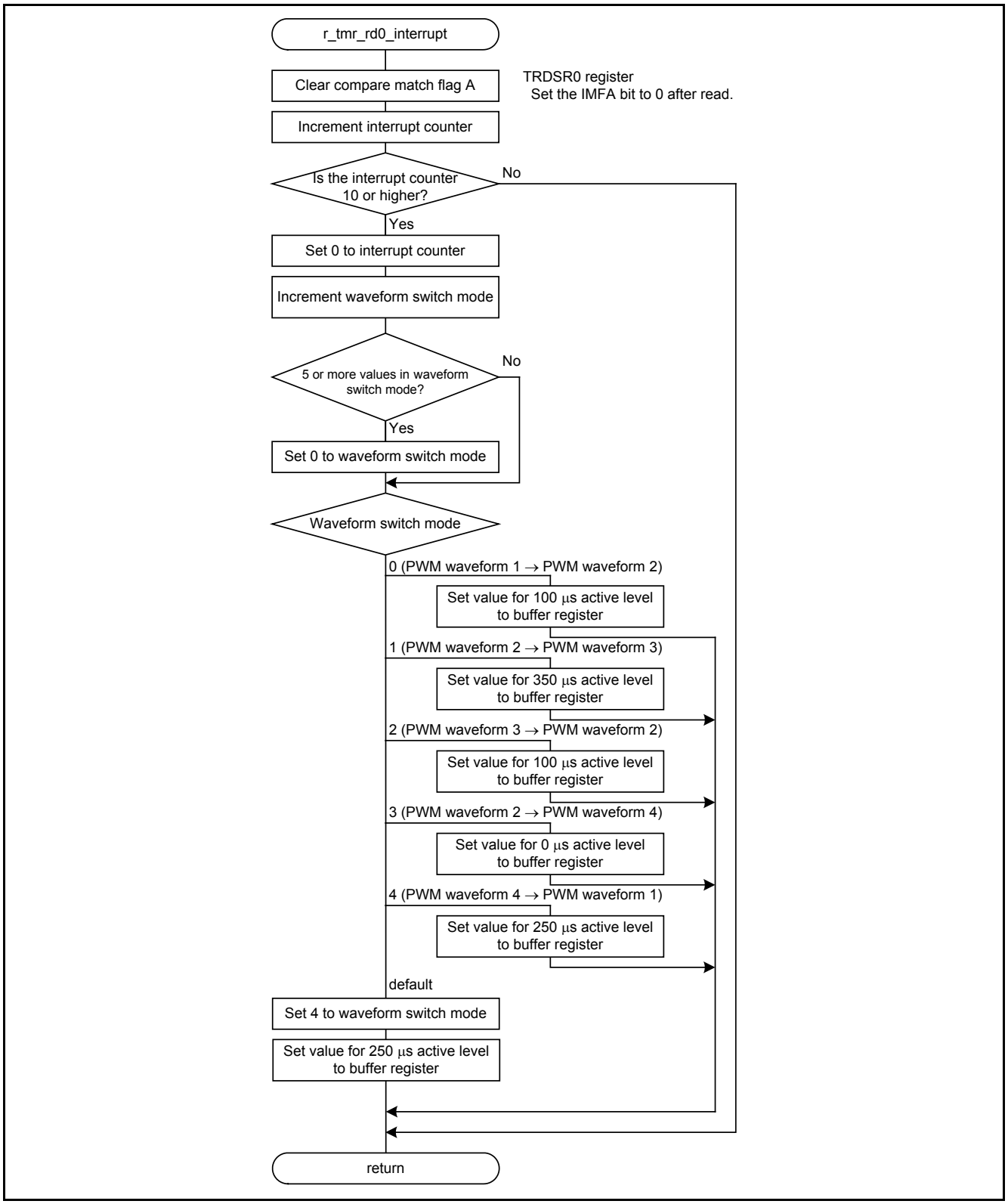


Figure 4.18 Timer RD0 Interrupt

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

User's Manual: Hardware
RL78/G14 Group User's Manual: Hardware Rev.0.02
RL78 Family User's Manual: Software Rev.1.00
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	RL78/G14 Timer RD in Complementary PWM Mode

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 1, 2012	—	First edition issued
1.10	June 1, 2013	4	Fixed typo in Table 2.1
		5	Fixed typo in Figure 3.1

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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