RL78/G14, R8C/36M Group

Migration Guide from R8C to RL78: Timer RD

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Introduction

This document describes how to migrate from timer RD in R8C/36M Group to timer RD in RL78/G14 (This document is described in 64-pin package as an example).

Target Device

RL78/G14, R8C/36M Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Migration Method from R8C Family to RL78 Family

This application note explains how to achieve each mode (timer mode, PWM mode, reset synchronous PWM mode, complementary PWM mode and PWM3 mode) in timer RD of R8C/36M using RL78/G14.
Table 1.1 shows the mode in timer RD of R8C/36M Group, and Table 1.2 shows the mode in timer RD of RL78/G14.

In R8C/36M Group, timer RD has 2 16-bit timers (timer RD0 and timer RD1). Timer RDi has five modes: timer mode, PWM mode, reset synchronous PWM mode, complementary PWM mode and PWM3 mode. In timer mode, there are two functions: input capture function and output compare function. In input capture function, transfer the counter value to a register with an external signal as the trigger. In output compare function, detect register value matches with a counter (Pin output can be changed at detection). And the other 4 modes use the output compare function. In PWM mode, output pulse of any width continuously. In reset synchronous PWM mode, output three-phase waveforms (6) with sawtooth wave modulation and without dead time. In complementary PWM mode, output three-phase waveforms (6) with triangular wave modulation and dead time. In PWM3 mode, output PWM waveforms (2) with a fixed period.

In RL78/G14, timer RD also has two 16-bit timers (timer RD0, timer RD1). Timer RDi has four modes: timer mode, reset synchronous PWM mode, complementary PWM mode and PWM3 mode. In timer mode, there are three functions: input capture function, output compare function and PWM function. In input capture function, transfer the counter value to a register with an external signal as the trigger. In output compare function, detect register value matches with a counter (Pin output can be changed at detection). In PWM function, output pulse of any width continuously. And the other 3 modes use the PWM function. In reset synchronous PWM mode, output three-phase waveforms (6) with sawtooth wave modulation and without dead time. In complementary PWM mode, output three-phase waveforms (6) with triangular wave modulation and dead time. In PWM3 mode, output PWM waveforms (2) with a fixed period.

The same operation as that each mode (timer mode, reset synchronous PWM mode, complementary PWM mode and PWM3 mode) in timer RD of R8C/36M group can be realized by using timer RD of RL78/G14.
("PWM mode" in timer RD of R8C/36M group is same function with "PWM function" in timer RD of RL78/G14.)

About the detailed differences of timer RD, please refer to "2. Differences between RL78/G14 and R8C/36M Group" in this application note.

For sample programs using timer RD of RL78/G14, please refer to the application notes in each operation mode in "3. Reference Application Note".

Remark i = 0 or 1

Table 1.1 Operation Mode of Timer RD in R8C/36M

Timer RD in R8C/36M		
Mode		**Function**
Timer mode	- Input capture function	Transfer the counter value to a register with an external signal as the trigger.
	- Output compare function	Detect register value matches with a counter (Pin output can be changed at detection).
PWM mode		Output pulse of any width continuously.
Reset synchronous PWM mode		Output three-phase waveforms (6) with sawtooth wave modulation and without dead time.
Complementary PWM mode		Output three-phase waveforms (6) with triangular wave modulation and dead time.
PWM3 mode		Output PWM waveforms (2) with a fixed period.

Table 1.2 Corresponding Mode of Timer RD in RL78/G14

Timer RD in RL78/G14		
Mode		**Function**
Timer mode	- Input capture function	Transfer the counter value to a register with an external signal as the trigger.
	- Output compare function	Detect register value matches with a counter (Pin output can be changed at detection).
	- PWM function	Output pulse of any width continuously.
Reset synchronous PWM mode		Output three-phase waveforms (6) with sawtooth wave modulation and without dead time.
Complementary PWM mode		Output three-phase waveforms (6) with triangular wave modulation and dead time.
PWM3 mode		Output PWM waveforms (2) with a fixed period.

2. Differences between RL78/G14 and R8C/36M Group

2.1 Differences in Function Overview

Table 2.1 and Table 2.2 list the differences between timer RD in R8C/36M Group and timer RD in RL78/G14.

Table 2.1 Differences (1/2)

Item	R8C/36M Group Timer RD	RL78/G14 Timer RD
Count source	f1, f2, f4, f8, f32, fC2 Note 1 fOCO40M, fOCO-F TRDCLK Note 2 (Max. 40 MHz Note 3)	f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, $f_{CLK}/32$, f_{HOCO} Note 4 TRDCLK Note 2 (Max. 64 MHz Note 5)
How to execute the forced cutoff of the pulse output	• Input low level signals to the $\overline{INT0}$ pin The output pin of timer RD (the TRDIOji pin) can be forcibly set to a programmable I/O port, and pulse output can be cut off.	• Input low level signals to the INTP0 pin • The pulse output forced cutoff by ELC event input The pulse output from the output pin of timer RD (the TRDIOji pin) can be cut off. The output pin used as a timer RD output port outputs the output value set by the TRDDFi register.
How to cancel the forced cutoff of the pulse output	Input high level signals to the $\overline{INT0}$ pin while the count is stopped (TSTARTi = 0).	After inputting high level signals to the INTP0 pin, set the TRDSHUTS bit to 0 while the count is stopped (TSTARTi = 0). (Set the TRDSHUTS bit when a pulse forced cutoff by ELC event input is not generated.)
Operation mode that enable forcibly cut off	• Output compare function • PWM mode • Reset synchronous PWM mode • Complementary PWM mode • PWM3 mode	• PWM function • Reset synchronous PWM mode • Complementary PWM mode • PWM3 mode
Pin state setting on the forced cutoff of pulse output	Set registers P2 and PD2	Set the TRDDFi register

Notes: 1. fC2 cannot be selected in PWM mode, reset synchronous PWM mode, complementary PWM mode, or PWM3 mode.

2. TRDCLK cannot be selected in PWM3 mode.

3. Count source of Timer RD in R8C/36M: Max. 40 MHz
   Set the Timer RD count source select to fOCO40M.

4. f_{CLK} is selected when FRQSEL4 = 0 and f_{HOCO} is selected when FRQSEL4 = 1 in the user option byte (000C2H). When selecting f_{HOCO} as the count source for timer RD, set f_{CLK} to f_{IH} before setting bit 4 (TRD0EN) in peripheral enable register 1 (PER1). When changing f_{CLK} to a clock other than f_{IH}, clear bit 4 (TRD0EN) in peripheral enable register 1 (PER1) before changing.

5. Count source of Timer RD in RL78/G14: Max. 64 MHz (set as follows.)
   • Setting CPU clock
   When supplying 64 MHz or 48 MHz to timer RD, set f_{CLK} to f_{IH}.
   f_{IH} is controlled by hardware to be set to two frequency division of f_{HOC}O when f_{HOCO} is set to 64 MHz or 48 MHz, and the same clock frequency as f_{HOCO} when f_{HOCO} is set to 32 MHz or less.
   • Setting count source of Timer RD
   When supplying 64 MHz or 48 MHz to timer RD, set the count source select to f_{HOCO}.

Remark i = 0 or 1
j = A, B, C, or D

Table 2.2 Differences (2/2)

Item	R8C/36M Group Timer RD	RL78/G14 Timer RD
Switch between TRDIOA0 and fOCO128 for the input capture function	Yes (set by the TRDIORA0 register)	No
Timer RD pins	P2_0 to P2_7 Note 1	P10 to P17 Note 1
A/D trigger generation function	Yes Note 2	YES (The A/D converter can be operated by using the ELC.)
Event input from Event Link Controller (ELC)	No	Yes

Notes: 1. See "Table 2.17 R8C/36M Group and RL78/G14 I/O Pins".
2. This function is not available in the input capture function.

2.2 Differences in Input Capture Function

The operation of input capture function in timer RD of RL78/G14 corresponds to input capture function in timer RD of R8C/36M Group.
Table 2.3 and Table 2.4 list the differences between input capture function in timer RD of R8C/36M Group and input capture function in timer RD of RL78/G14.

Table 2.3 Differences of Timer RD (Input Capture Function) (1/2)

Item	R8C/36M Group (Input Capture Function)	RL78/G14 (Input Capture Function)
Count sources	f1, f2, f4, f8, f32, fC2, fOCO40M, fOCO-F External signal input to the TRDCLK pin (valid edge selected by a program) (Max. 40 MHz Note 1)	f_{HOCO} Note 2, f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, $f_{CLK}/32$ External signal input to the TRDCLK pin (active edge selected by a program) (Max. 64 MHz Note 3)
Count operation	Increment	Increment
Count period	When bits CCLR2 to CCLR0 in the TRDCRi register are set to 000b (freerunning operation). 1/fk × 65536 fk: Frequency of count source	When bits CCLR2 to CCLR0 in the TRDCRi register are set to 000B (free-running operation). 1/fk × 65536 fk: Frequency of count source
Count start condition	1 (count starts) is written to the TSTARTi bit in the TRDSTR register.	1 (count starts) is written to the TSTARTi bit in the TRDSTR register.
Count stop condition	0 (count stops) is written to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1.	0 (count stops) is written to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1.
Interrupt request generation timing	• Input capture (valid edge of TRDIOji input or fOCO128 signal edge) • TRDi register overflows	• Input capture (active edge of TRDIOji input) • TRDi register overflow

Note 1: Count source of Timer RD in R8C/36M: Max. 40 MHz
Set the Timer RD count source select to fOCO40M.

Note 2: f_{HOCO} is selected only when FRQSEL4 = 1 in the user option byte (000C2H). When selecting f_{HOCO} as the count source for timer RD, set f_{CLK} to f_{IH} before setting bit 4 (TRD0EN) in peripheral enable register 1 (PER1). When changing f_{CLK} to a clock other than f_{IH}, clear bit 4 (TRD0EN) in peripheral enable register 1 (PER1) before changing.

Note 3: Count source of Timer RD in RL78/G14: Max. 64 MHz (set as follows.)
- Setting CPU clock
  When supplying 64 MHz or 48 MHz to timer RD, set f_{CLK} to f_{IH}.
  f_{IH} is controlled by hardware to be set to two frequency division of $f_{HOC}O$ when f_{HOCO} is set to 64 MHz or 48 MHz, and the same clock frequency as f_{HOCO} when f_{HOCO} is set to 32 MHz or less.
- Setting count source of Timer RD
  When supplying 64 MHz or 48 MHz to timer RD, set the count source select to f_{HOCO}.

Remark i = 0 or 1
j = A, B, C, or D

Table 2.4 Differences of Timer RD (Input Capture Function) (2/2)

Item	R8C/36M Group (Input Capture Function)	RL78/G14 (Input Capture Function)
TRDIOA0 pin function	Programmable I/O port, input-capture input, or TRDCLK (external clock) input	I/O port, input-capture input, or TRDCLK (external clock) input
TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1 to TRDIOD1 pin functions	Programmable I/O port, or input-capture input (selectable by pin)	I/O port or input-capture input (selectable for each pin)
$\overline{INT0}$/INTP0 pin function	Programmable I/O port or $\overline{INT0}$ interrupt input	Not used (input-only port or INTP0 interrupt input)
Read from timer	The count value can be read by reading the TRDi register.	The count value can be read by reading the TRDi register.
Write to timer	• When the SYNC bit in the TRDMR register is set to 0 (timer RD0 and timer RD1 operate independently). Data can be written to the TRDi register. • When the SYNC bit in the TRDMR register is set to 1 (timer RD0 and timer RD1 operate synchronously). Data can be written to both the TRD0 and TRD1 registers by writing to the TRDi register.	• When the TRDSYNC bit in the TRDMR register is 0 (timer RD0 and timer RD1 operate independently). Data can be written to the TRDi register. • When the TRDSYNC bit in the TRDMR register is 1 (timer RD0 and timer RD1 operate synchronously). Data can be written to both the TRD0 and TRD1 registers by writing to the TRDi register.
Selectable functions	• Input-capture input pin selection • Input-capture input valid edge selection • Timing for setting the TRDi register to 0000h • Buffer operation • Synchronous operation • Digital filter • Input-capture trigger selection	• Input-capture input pin selection • Input-capture input active edge selection • Timing for setting the TRDi register to 0000H • Buffer operation • Synchronous operation • Digital filter • Input capture operation by event input from ELC

Remark i = 0 or 1

2.3 Differences in Output Compare Function

The operation of output compare function in timer RD of RL78/G14 corresponds to output compare function in timer RD of R8C/36M Group.
Table 2.5, Table 2.6 and Table 2.7 list the differences between output compare function in timer RD of R8C/36M Group and operation as output compare function in timer RD of RL78/G14.

Table 2.5 Differences of Timer RD (Output Compare Function) (1/3)

Item	R8C/36M Group (Output Compare Function)	RL78/G14 (Output Compare Function)
Count sources	f1, f2, f4, f8, f32, fC2, fOCO40M, fOCO-F External signal input to the TRDCLK pin (valid edge selected by a program) (Max. 40 MHz Note 1)	f_{HOCO} Note 2, f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, $f_{CLK}/32$ External signal input to the TRDCLK pin (active edge selected by a program) (Max. 64 MHz Note 3)
Count operation	Increment	Increment
Count period	• When bits CCLR2 to CCLR0 in the TRDCRi register are set to 000b (free-running operation). 1/fk × 65536 fk: Frequency of count source • Bits CCLR1 to CCLR0 in the TRDCRi register are set to 01b or 10b (set the TRDi register to 0000h at the compare match in the TRDGRji register). Frequency of count source × (n+1) n: Setting value in the TRDGRji register	• When bits CCLR2 to CCLR0 in the TRDCRi register are set to 000B (free-running operation). 1/fk × 65536 fk: Frequency of count source • When bits CCLR1 and CCLR0 in the TRDCRi register are set to 01B or 10B (TRDi register is set to 0000H at compare match with TRDGRji register). 1/fk × (n + 1) n: Value set in the TRDGRji register
Waveform output timing	Compare match	Compare match (contents of registers TRDi and TRDGRji match)
Count start condition	1 (count starts) is written to the TSTARTi bit in the TRDSTR register.	1 (count starts) is written to the TSTARTi bit in the TRDSTR register.

Note 1: Count source of Timer RD in R8C/36M: Max. 40 MHz
Set the Timer RD count source select to fOCO40M.

Note 2: f_{HOCO} is selected only when FRQSEL4 = 1 in the user option byte (000C2H). When selecting f_{HOCO} as the count source for timer RD, set f_{CLK} to f_{IH} before setting bit 4 (TRD0EN) in peripheral enable register 1 (PER1). When changing f_{CLK} to a clock other than f_{IH}, clear bit 4 (TRD0EN) in peripheral enable register 1 (PER1) before changing.

Note 3: Count source of Timer RD in RL78/G14: Max. 64 MHz (set as follows.)
• Setting CPU clock
When supplying 64 MHz or 48 MHz to timer RD, set f_{CLK} to f_{IH}.
f_{IH} is controlled by hardware to be set to two frequency division of f_{HOC}O when f_{HOCO} is set to 64 MHz or 48 MHz, and the same clock frequency as f_{HOCO} when f_{HOCO} is set to 32 MHz or less.
• Setting count source of Timer RD
When supplying 64 MHz or 48 MHz to timer RD, set the count source select to f_{HOCO}.

Remark i = 0 or 1
j = A, B, C, or D

Table 2.6 Differences of Timer RD (Output Compare Function) (2/3)

Item	R8C/36M Group (Output Compare Function)	RL78/G14 (Output Compare Function)
Count stop condition	• 0 (count stops) is written to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1. The output compare output pin holds output level before the count stops. • When the CSELi bit in the TRDSTR register is set to 0, the count stops at the compare match in the TRDGRAi register. The output compare output pin holds level after output change by the compare match.	• 0 (count stops) is written to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1. The output compare output pin holds the output level before the count stops. • When the CSELi bit in the TRDSTR register is set to 0, the count stops at the compare match with the TRDGRAi register. The output compare output pin holds the level after output change by compare match.
Interrupt request generation timing	• Compare match (content of the TRDi register matches content of the TRDGRji register) • TRDi register overflows	• Compare match (contents of registers TRDi and TRDGRji match) • TRDi register overflow
TRDIOA0 pin function	Programmable I/O port, output-compare output, or TRDCLK (external clock) input	I/O port, output-compare output, or TRDCLK (external clock) input
TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1 to TRDIOD1 pin functions	Programmable I/O port or output-compare output (selectable by pin)	I/O port or output-compare output (selectable for each pin)
$\overline{\text{INT0}}$/INTP0 pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input	Not used (input-only port or INTP0 interrupt input)

Remark i = 0 or 1
j = A, B, C, or D

Table 2.7 Differences of Timer RD (Output Compare Function) (3/3)

Item	R8C/36M Group (Output Compare Function)	RL78/G14 (Output Compare Function)
Read from timer	The count value can be read by reading the TRDi register.	The count value can be read by reading the TRDi register.
Write to timer	• When the SYNC bit in the TRDMR register is set to 0 (timer RD0 and timer RD1 operate independently). Data can be written to the TRDi register. • When the SYNC bit in the TRDMR register is set to 1 (timer RD0 and timer RD1 operate synchronously). Data can be written to both the TRD0 and TRD1 registers by writing to the TRDi register.	• When the TRDSYNC bit in the TRDMR register is set to 0 (timer RD0 and timer RD1 operate independently). Data can be written to the TRDi register. • When the TRDSYNC bit in the TRDMR register is set to 1 (timer RD0 and timer RD1 operate synchronously). Data can be written to both the TRD0 and TRD1 registers by writing to the TRDi register.
Selectable functions	• Output-compare output pin selection • Output level at the compare match selection • Initial output level selected • Timing for setting the TRDi register to 0000h • Buffer operation • Synchronous operation • Changing output pins for registers TRDGRCi and TRDGRDi • Pulse output forced cutoff signal input • Timer RD can be used as the internal timer without output • A/D trigger generation Note 1	• Output-compare output pin selection • Output level selection at compare match • Initial output level selection • Timing for setting the TRDi register to 0000H • Buffer operation • Synchronous operation • Changing output pins for registers TRDGRCi and TRDGRDi • Timer RD can be used as the internal timer without output • The A/D converter can be operated by using the ELC

Note 1: A compare match signal with registers TRDi and TRDGRji can be used as the conversion start trigger of the A/D converter. The TRDADCR register is used to select which compare match is used.

Remark i = 0 or 1
j = A, B, C, or D

2.4 Differences in PWM Function

The operation of PWM function in timer RD of RL78/G14 corresponds to PWM mode in timer RD of R8C/36M Group.
Table 2.8 and Table 2.9 list the differences between PWM mode in timer RD of R8C/36M Group and operation as PWM function in timer RD of RL78/G14.

Table 2.8 Differences of Timer RD (PWM Mode / PWM Function) (1/2)

Item	R8C/36M Group (PWM Mode)	RL78/G14 (PWM Function)
Count sources	f1, f2, f4, f8, f32, fOCO40M, fOCO-F External signal input to the TRDCLK pin (valid edge selected by a program) (Max. 40 MHz Note 1)	f_{HOCO} Note 2, f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, $f_{CLK}/32$ External signal input to the TRDCLK pin (active edge selected by a program) (Max. 64 MHz Note 3)
Count operations	Increment	Increment
PWM waveform	PWM period: 1/fk x (m+1) Active level width: 1/fk x (m-n) Inactive level width: 1/fk x (n+1) fk: Frequency of count source m: Value set in the TRDGRAi register n: Value set in the TRDGRji register	PWM period: 1/fk × (m + 1) Active level width: 1/fk × (m - n) Inactive level width: 1/fk × (n + 1) fk: Frequency of count source m: Value set in the TRDGRAi register n: Value set in the TRDGRji register
Count start condition	1 (count starts) is written to the TSTARTi bit in the TRDSTR register.	1 (count starts) is written to the TSTARTi bit in the TRDSTR register.
Count stop conditions	• 0 (count stops) is written to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1. The PWM output pin holds output level before the count stops. • When the CSELi bit in the TRDSTR register is set to 0, the count stops at the compare match in the TRDGRAi register. The PWM output pin holds level after output change by compare match.	• 0 (count stops) is written to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1. The PWM output pin holds the output level before the count stops. • When the CSELi bit in the TRDSTR register is set to 0, the count stops at the compare match with the TRDGRAi register. The PWM output pin holds the level after output change by compare match.

Note 1: Count source of Timer RD in R8C/36M: Max. 40 MHz
Set the Timer RD count source select to fOCO40M.

Note 2: f_{HOCO} is selected only when FRQSEL4 = 1 in the user option byte (000C2H). When selecting f_{HOCO} as the count source for timer RD, set f_{CLK} to f_{IH} before setting bit 4 (TRD0EN) in peripheral enable register 1 (PER1). When changing f_{CLK} to a clock other than f_{IH}, clear bit 4 (TRD0EN) in peripheral enable register 1 (PER1) before changing.

Note 3: Count source of Timer RD in RL78/G14: Max. 64 MHz (set as follows.)
- Setting CPU clock
  When supplying 64 MHz or 48 MHz to timer RD, set f_{CLK} to f_{IH}.
  f_{IH} is controlled by hardware to be set to two frequency division of f_{HOC}O when f_{HOCO} is set to 64 MHz or 48 MHz, and the same clock frequency as f_{HOCO} when f_{HOCO} is set to 32 MHz or less.
- Setting count source of Timer RD
  When supplying 64 MHz or 48 MHz to timer RD, set the count source select to f_{HOCO}.

Remark i = 0 or 1
j = B, C, or D
h = A, B, C, or D

Table 2.9 Differences of Timer RD (PWM Mode / PWM Function) (2/2)

Item	R8C/36M Group (PWM Mode)	RL78/G14 (PWM Function)
Interrupt request generation timing	• Compare match (the content of the TRDi register matches content of the TRDGRhi register) • TRDi register overflows	• Compare match (content of the TRDi register matches content of the TRDGRhi register) • TRDi register overflow
TRDIOA0 pin function	Programmable I/O port or TRDCLK (external clock) input	I/O port or TRDCLK (external clock) input
TRDIOA1 pin function	Programmable I/O port	I/O port
TRDIOB0, TRDIOC0, TRDIOD0, TRDIOB1, TRDIOC1, TRDIOD1 pin functions	Programmable I/O port or pulse output (selectable by pin)	I/O port or pulse output (selectable for each pin)
$\overline{\text{INT0}}$/INTP0 pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input	Pulse output forced cutoff signal input (input-only port or INTP0 interrupt input)
Read from timer	The count value can be read by reading the TRDi register.	The count value can be read by reading the TRDi register.
Write to timer	The value can be written to the TRDi register.	The value can be written to the TRDi register.
Selectable functions	• One to three PWM output pins selectable with timer RDi • Active level selectable for each pin • Initial output level selectable for each pin • Synchronous operation • Buffer operation • Pulse output forced cutoff signal input • A/D trigger generation Note 1	• One to three PWM output pins selectable with timer RDi • Active level selectable for each pin • Initial output level selectable for each pin • Synchronous operation • Buffer operation • Pulse output forced cutoff signal input • The A/D converter can be operated by using the ELC

Note 1: A compare match signal with registers TRDi and TRDGRji can be used as the conversion start trigger of the A/D converter. The TRDADCR register is used to select which compare match is used.

Remark i = 0 or 1
j = A, B, C, or D

2.5 Differences in Reset Synchronous PWM Mode

The operation of reset synchronous PWM mode in timer RD of RL78/G14 corresponds to reset synchronous PWM mode in timer RD of R8C/36M Group.
Table 2.10 and Table 2.11 list the differences between reset synchronous PWM mode in timer RD of R8C/36M Group and operation as reset synchronous PWM mode in timer RD of RL78/G14.

Table 2.10 Differences of Timer RD (Reset Synchronous PWM Mode) (1/2)

Item	R8C/36M Group (Reset Synchronous PWM Mode)	RL78/G14 (Reset Synchronous PWM Mode)
Count sources	f1, f2, f4, f8, f32, fOCO40M, fOCO-F External signal input to the TRDCLK pin (valid edge selected by a program) (Max. 40 MHz Note 1)	f_{HOCO} Note 2, f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, $f_{CLK}/32$ External signal input to the TRDCLK pin (active edge selected by a program) (Max. 64 MHz Note 3)
Count operations	The TRD0 register is incremented (the TRD1 register is not used).	The TRD0 register is incremented (the TRD1 register is not used).
PWM waveform	PWM period: 1/fk × (m+1) Active level width of normal-phase: 1/fk × (m-n) Active level width of counter-phase: 1/fk × (n+1) fk: Frequency of count source m: Value set in the TRDGRA0 register n: Value set in the TRDGRB0 register (PWM1 output) Value set in the TRDGRA1 register (PWM2 output) Value set in the TRDGRB1 register (PWM3 output)	PWM period: 1/fk × (m + 1) Active level of normal-phase: 1/fk × (m - n) Inactive level of counter-phase: 1/fk × (n + 1) fk: Frequency of count source m: Value set in the TRDGRA0 register n: Value set in the TRDGRB0 register (PWM1 output) Value set in the TRDGRA1 register (PWM2 output) Value set in the TRDGRB1 register (PWM3 output)
Count start condition	1 (count starts) is written to the TSTART0 bit in the TRDSTR register.	1 (count starts) is written to the TSTART0 bit in the TRDSTR register.

Note 1 Count source of Timer RD in R8C/36M: Max. 40 MHz
Set the Timer RD count source select to fOCO40M.

Note 2: f_{HOCO} is selected only when FRQSEL4 = 1 in the user option byte (000C2H). When selecting f_{HOCO} as the count source for timer RD, set f_{CLK} to f_{IH} before setting bit 4 (TRD0EN) in peripheral enable register 1 (PER1). When changing f_{CLK} to a clock other than f_{IH}, clear bit 4 (TRD0EN) in peripheral enable register 1 (PER1) before changing.

Note 3 Count source of Timer RD in RL78/G14: Max. 64 MHz (set as follows.)

- Setting CPU clock
  When supplying 64 MHz or 48 MHz to timer RD, set f_{CLK} to f_{IH}.
  f_{IH} is controlled by hardware to be set to two frequency division of $f_{HOC}O$ when f_{HOCO} is set to 64 MHz or 48 MHz, and the same clock frequency as f_{HOCO} when f_{HOCO} is set to 32 MHz or less.
- Setting count source of Timer RD
  When supplying 64 MHz or 48 MHz to timer RD, set the count source select to f_{HOCO}.

Table 2.11 Differences of Timer RD (Reset Synchronous PWM Mode) (2/2)

Item	R8C/36M Group (Reset Synchronous PWM Mode)	RL78/G14 (Reset Synchronous PWM Mode)
Count stop conditions	• 0 (count stops) is written to the TSTART0 bit when the CSEL0 bit in the TRDSTR register is set to 1. (The PWM output pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register.) • When the CSEL0 bit in the TRDSTR register is set to 0, the count stops at the compare match in the TRDGRA0 register. (The PWM output pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register.)	• 0 (count stops) is written to the TSTART0 bit when the CSEL0 bit in the TRDSTR register is set to 1. The PWM output pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register. • When the CSEL0 bit in the TRDSTR register is set to 0, the count stops at the compare match with the TRDGRA0 register. The PWM output pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register.
Interrupt request generation timing	• Compare match (the content of the TRD0 register matches content of registers TRDGRj0, TRDGRA1, and TRDGRB1) • The TRD0 register overflows	• Compare match (content of the TRD0 register matches content of registers TRDGRj0, TRDGRA1, and TRDGRB1) • TRD0 register overflow
TRDIOA0 pin function	Programmable I/O port or TRDCLK (external clock) input	I/O port or TRDCLK (external clock) input
TRDIOB0 pin function	PWM1 output normal-phase output	PWM1 output normal-phase output
TRDIOD0 pin function	PWM1 output counter-phase output	PWM1 output counter-phase output
TRDIOA1 pin function	PWM2 output normal-phase output	PWM2 output normal-phase output
TRDIOC1 pin function	PWM2 output counter-phase output	PWM2 output counter-phase output
TRDIOB1 pin function	PWM3 output normal-phase output	PWM3 output normal-phase output
TRDIOD1 pin function	PWM3 output counter-phase output	PWM3 output counter-phase output
TRDIOC0 pin function	Output inverted every PWM period	Output inverted every PWM period
$\overline{\text{INT0}}$/INTP0 pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input	Pulse output forced cutoff signal input (input-only port or INTP0 interrupt input)
Read from timer	The count value can be read by reading the TRD0 register.	The count value can be read by reading the TRD0 register.
Write to timer	The value can be written to the TRD0 register.	The value can be written to the TRD0 register.
Selectable functions	• The normal-phase and counter-phase active level and initial output level are selected individually • Buffer operation • Pulse output forced cutoff signal input • A/D trigger generation Note 1	• The normal-phase and counter-phase active level and initial output level are selected individually • Buffer operation • Pulse output forced cutoff signal input • The A/D converter can be operated by using the ELC

Note 1: A compare match signal with registers TRDi and TRDGRji can be used as the conversion start trigger of the A/D converter. The TRDADCR register is used to select which compare match is used.

Remark i = 0、1
j = A, B, C, or D

2.6 Differences in Complementary PWM Mode

The operation of complementary PWM mode in timer RD of RL78/G14 corresponds to complementary PWM mode in timer RD of R8C/36M Group.
Table 2.12, Table 2.13 and Table 2.14 list the differences between complementary PWM mode in timer RD of R8C/36M Group and operation as complementary PWM mode in timer RD of RL78/G14.

Table 2.12 Differences of Timer RD (Complementary PWM Mode) (1/3)

Item	R8C/36M Group (Complementary PWM Mode)	RL78/G14 (Complementary PWM Mode)
Count sources	f1, f2, f4, f8, f32, fOCO40M, fOCO-F External signal input to the TRDCLK pin (valid edge selected by a program) Set bits TCK2 to TCK0 in the TRDCR1 register to the same value (same count source) as bits TCK2 to TCK0 in the TRDCR0 register. (Max. 40 MHz Note 1)	f_{HOCO} Note 2, f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, $f_{CLK}/32$ External signal input to the TRDCLK pin (active edge selected by a program) Set bits TCK2 to TCK0 in the TRDCR1 register to the same value (same count source) as bits TCK2 to TCK0 in the TRDCR0 register. (Max. 64 MHz Note 3)
Count operations	Increment or decrement Registers TRD0 and TRD1 are decremented with the compare match in registers TRD0 and TRDGRA0 during increment operation. The TRD1 register value is changed from 0000h to FFFFh during decrement operation, and registers TRD0 and TRD1 are incremented.	Increment or decrement. Registers TRD0 and TRD1 are decremented with the compare match with registers TRD0 and TRDGRA0 during increment operation. When the TRD1 register changes from 0000H to FFFFH during decrement operation, and registers TRD0 and TRD1 are incremented.

Notes: 1. Count source of Timer RD in R8C/36M: Max. 40 MHz
Set the Timer RD count source select to fOCO40M.

2. f_{HOCO} is selected only when FRQSEL4 = 1 in the user option byte (000C2H). When selecting f_{HOCO} as the count source for timer RD, set f_{CLK} to f_{IH} before setting bit 4 (TRD0EN) in peripheral enable register 1 (PER1). When changing f_{CLK} to a clock other than f_{IH}, clear bit 4 (TRD0EN) in peripheral enable register 1 (PER1) before changing.

3. Count source of Timer RD in RL78/G14: Max. 64 MHz (set as follows.)
   - Setting CPU clock
     When supplying 64 MHz or 48 MHz to timer RD, set f_{CLK} to f_{IH}.
     f_{IH} is controlled by hardware to be set to two frequency division of f_{HOC}O when f_{HOCO} is set to 64 MHz or 48 MHz, and the same clock frequency as f_{HOCO} when f_{HOCO} is set to 32 MHz or less.
   - Setting count source of Timer RD
     When supplying 64 MHz or 48 MHz to timer RD, set the count source select to f_{HOCO}.

Table 2.13 Differences of Timer RD (Complementary PWM Mode) (2/3)

Item	R8C/36M Group (Complementary PWM Mode)	RL78/G14 (Complementary PWM Mode)
PWM operations	PWM period: 1/fk × (m+2-p) × 2 Note 1 Dead time: p Active level width of normal-phase: 1/fk × (m-n-p+1) × 2 Active level width of counter-phase: 1/fk × (n+1-p) × 2 fk: Frequency of count source m: Value set in the TRDGRA0 register n: Value set in the TRDGRB0 register (PWM1 output) Value set in the TRDGRA1 register (PWM2 output) Value set in the TRDGRB1 register (PWM3 output) p: Value set in the TRD0 register	PWM period: 1/fk × (m + 2 - p) × 2 Note 1 Dead time: p Active level width of normal-phase: 1/fk × (m - n - p + 1) × 2 Active level width of counter-phase: 1/fk × (n + 1 - p) × 2 fk: Frequency of count source m: Value set in the TRDGRA0 register n: Value set in the TRDGRB0 register (PWM1 output) Value set in the TRDGRA1 register (PWM2 output) Value set in the TRDGRB1 register (PWM3 output) p: Value set in the TRD0 register
Count start condition	1 (count starts) is written to bits TSTART0 and TSTART1 in the TRDSTR register.	1 (count starts) is written to bits TSTART0 and TSTART1 in the TRDSTR register.
Count stop conditions	0 (count stops) is written to bits TSTART0 and TSTART1 when the CSEL0 bit in the TRDSTR register is set to 1. (The PWM output pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register.)	0 (count stops) is written to bits TSTART0 and TSTART1 in the TRDSTR register when the CSEL0 bit in the TRDSTR register is set to 1. (The PWM output pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register.)
Interrupt request generation timing	• Compare match (the content of the TRDi register matches content of the TRDGRji register) • The TRD1 register underflows	• Compare match (content of the TRDi register matches content of the TRDGRji register) • TRD1 register underflow
TRDIOA0 pin function	Programmable I/O port or TRDCLK (external clock) input	I/O port or TRDCLK (external clock) input
TRDIOB0 pin function	PWM1 output normal-phase output	PWM1 output normal-phase output
TRDIOD0 pin function	PWM1 output counter-phase output	PWM1 output counter-phase output
TRDIOA1 pin function	PWM2 output normal-phase output	PWM2 output normal-phase output
TRDIOC1 pin function	PWM2 output counter-phase output	PWM2 output counter-phase output
TRDIOB1 pin function	PWM3 output normal-phase output	PWM3 output normal-phase output
TRDIOD1 pin function	PWM3 output counter-phase output	PWM3 output counter-phase output
TRDIOC0 pin function	Output inverted every 1/2 period of PWM	Output inverted every 1/2 period of PWM

Notes: 1. After a count starts, the PWM period is fixed.

Remark i = 0 or 1
j = A, B, C, or D

Table 2.14 Differences of Timer RD (Complementary PWM Mode) (3/3)

Item	R8C/36M Group (Complementary PWM Mode)	RL78/G14 (Complementary PWM Mode)
$\overline{\text{INT0}}$/INTP0 pin function	Programmable I/O port, pulse output forced cutoff signal input or $\overline{\text{INT0}}$ interrupt input	Pulse output forced cutoff signal input (input-only port or INTP0 interrupt input)
Read from timer	The count value can be read by reading the TRDi register.	The count value can be read by reading the TRDi register.
Write to timer	The value can be written to the TRDi register.	The value can be written to the TRDi register.
Selectable functions	• Pulse output forced cutoff signal input • The normal-phase and counter-phase active level and initial output level are selected individually • Transfer timing from the buffer register selection • A/D trigger generation Note 1	• Pulse output forced cutoff signal input • The normal-phase and counter-phase active level and initial output level are selected individually • Transfer timing from the buffer register selection • The A/D converter can be operated by using the ELC

Note 1: Compare match between registers TRD0 and TRDGRA0 and TRD1 underflow can be used as the conversion start trigger of the A/D converter. A compare match signal with registers TRDi and TRDGRji can be used as the conversion start trigger of the A/D converter. Use bits ADEG and ADTRG in the TRDFCR register and the TRDADCR register to make settings.

Remark i = 0 or 1
j = A, B, C, or D

2.7 Differences in PWM3 Mode

The operation of PWM3 mode in timer RD of RL78/G14 corresponds to PWM3 mode in timer RD of R8C/36M Group.
Table 2.15 and Table 2.16 list the differences between PWM3 mode in timer RD of R8C/36M Group and operation as PWM3 mode in timer RD of RL78/G14.

Table 2.15 Differences of Timer RD (PWM3 Mode) (1/2)

Item	R8C/36M Group (PWM3 Mode)	RL78/G14 (PWM3 Mode)
Count sources	f1, f2, f4, f8, f32, fOCO40M, fOCO-F (Max. 40 MHz Note 1)	f_{HOCO} Note 2, f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, $f_{CLK}/32$ (Max. 64 MHz Note 3)
Count operations	The TRD0 register is incremented (the TRD1 is not used).	The TRD0 register is incremented (the TRD1 register is not used).
PWM waveform	PWM period: 1/fk × (m+1) Active level width of TRDIOA0 output: 1/fk × (m-n) Active level width of TRDIOB0 output: 1/fk × (p-q) fk: Frequency of count source m: Value set in the TRDGRA0 register n: Value set in the TRDGRA1 register p: Value set in the TRDGRB0 register q: Value set in the TRDGRB1 register	PWM period: 1/fk × (m + 1) Active level width of TRDIOA0 output: 1/fk × (m - n) Active level width of TRDIOB0 output: 1/fk × (p - q) fk: Frequency of count source m: Value set in the TRDGRA0 register n: Value set in the TRDGRA1 register p: Value set in the TRDGRB0 register q: Value set in the TRDGRB1 register
Count start condition	1 (count starts) is written to the TSTART0 bit in the TRDSTR register.	1 (count starts) is written to the TSTART0 bit in the TRDSTR register.
Count stop conditions	• 0 (count stops) is written to the TSTART0 bit in the TRDSTR register when the CSEL0 bit in the TRDSTR register is set to 1. The PWM output pin holds output level before the count stops. • When the CSEL0 bit in the TRDSTR register is set to 0, the count stops at compare match with the TRDGRA0 register. The PWM output pin holds level after output change by compare match.	• 0 (count stops) is written to the TSTART0 bit in the TRDSTR register when the CSEL0 bit in the TRDSTR register is set to 1. The PWM output pin holds the output level before the count stops. • When the CSEL0 bit in the TRDSTR register is set to 0, the count stops at compare match with the TRDGRA0 register. The PWM output pin holds the level after output change by compare match.

Note 1: Count source of Timer RD in R8C/36M: Max. 40 MHz
Set the Timer RD count source select to fOCO40M.

Note 2: f_{HOCO} is selected only when FRQSEL4 = 1 in the user option byte (000C2H). When selecting f_{HOCO} as the count source for timer RD, set f_{CLK} to f_{IH} before setting bit 4 (TRD0EN) in peripheral enable register 1 (PER1). When changing f_{CLK} to a clock other than f_{IH}, clear bit 4 (TRD0EN) in peripheral enable register 1 (PER1) before changing.

Note 3: Count source of Timer RD in RL78/G14: Max. 64 MHz (set as follows.)
• Setting CPU clock
When supplying 64 MHz or 48 MHz to timer RD, set f_{CLK} to f_{IH}.
f_{IH} is controlled by hardware to be set to two frequency division of $f_{HOC}O$ when f_{HOCO} is set to 64 MHz or 48 MHz, and the same clock frequency as f_{HOCO} when f_{HOCO} is set to 32 MHz or less.
• Setting count source of Timer RD
When supplying 64 MHz or 48 MHz to timer RD, set the count source select to f_{HOCO}.

Table 2.16 Differences of Timer RD (PWM3 Mode) (2/2)

Item	R8C/36M Group (PWM3 Mode)	RL78/G14 (PWM3 Mode)
Interrupt request generation timing	• Compare match (the content of the TRDi register matches content of the TRDGRji register) • The TRD0 register overflows	• Compare match (content of the TRDi register matches content of the TRDGRji register) • TRD0 register overflow
TRDIOA0, TRDIOB0 pin functions	PWM output	PWM output
TRDIOC0, TRDIOD0, TRDIOA1 to TRDIOD1 pin functions	Programmable I/O port	I/O port
$\overline{\text{INT0}}$/INTP0 pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input	Pulse output forced cutoff signal input (input-only port or INTP0 interrupt input)
Read from timer	The count value can be read by reading the TRD0 register.	The count value can be read by reading the TRD0 register.
Write to timer	The value can be written to the TRD0 register.	The value can be written to the TRD0 register.
Selectable functions	• Pulse output forced cutoff signal input • Buffer operation • Active level selectable for each pin • A/D trigger generation Note 1	• Pulse output forced cutoff signal input • Active level selectable for each pin • Buffer operation • The A/D converter can be operated by using the ELC

Note 1: A compare match signal with registers TRDi and TRDGRji can be used as the conversion start trigger of the A/D converter. The TRDADCR register is used to select which compare match is used.

Remark i = 0 or 1
j = A, B, C, or D

2.8 Assigned I/O Pins

Table 2.17 lists the assigned I/O pins to use in timer RD in the R8C/36M Group and timer RD in RL78/G14.

Table 2.17 R8C/36M Group and RL78/G14 I/O Pins

Pin Name	R8C/36M Group	RL78/G14	I/O
TRDIOA0/TRDCLK	P2_0	P17	I/O
TRDIOB0	P2_2	P15	I/O
TRDIOC0	P2_1	P16	I/O
TRDIOD0	P2_3	P14	I/O
TRDIOA1	P2_4	P13	I/O
TRDIOB1	P2_5	P12	I/O
TRDIOC1	P2_6	P11	I/O
TRDIOD1	P2_7	P10	I/O

2.9 Register Compatibility

Register compatibilities between timer RD in R8C/36M Group and timer RD in RL78/G14 are listed in Table 2.18.

Table 2.18 Register Compatibility

Item	R8C/36M Group	RL78/G14
fC2 select for timer RDi	• TRDECR register ITCLKi bit	N/A
A/D trigger ji enable (Can be set in all modes except input capture function.)	• TRDADCR register	N/A
A/D trigger edge select (Can be set in complementary PWM mode.)	• TRDFCR register ADEG bit	N/A
A/D trigger enable (Can be set in complementary PWM mode.)	• TRDFCR register ADTRG bit	N/A
Timer RD synchronous	• TRDMR register SYNC bit	• TRDMR register TRDSYNC bit
General register/buffer register select	• TRDMR register BFki bit	• TRDMR register TRDBFki bit
Timer mode/PWM mode select	• TRDPMR register Bits PWMBi, PWMCi, and PWMDi	• TRDPMR register Bits TRDPWMBi, TRDPWMCi, and TRDPWMDi
$\overline{\text{INT0}}$ (INTP0) of pulse output forced cutoff signal input enable	• TRDOER2 register PTO bit	• TRDOER2 register TRDPTO bit
Digital filter function clock select	• TRDDFi register Bits DFCK0 and DFCK1	• TRDDFi register Bits DFCK0 and DFCK1
Count source select	• TRDCRi register Bits TCK0 to TCK2	• TRDCRi register Bits TCK0 to TCK2
Input capture input switch	• TRDIORAi register IOA3 bit	N/A
Timer RD pin select	• TRDPSR0, TRDPSR1 register	N/A
Interrupt priority level select	• TRDiIC register Bits ILVL0 to ILVL21	• PR02H register TRDPR0i bit • PR12H register TRDPR1i bit
Interrupt request bit	• TRDiIC register IR bit	• IF2H register TRDIFi bit
Interrupt enable/disable	N/A	• MK2H register TRDMKi bit
Forced cutoff flag	N/A	• TRDOER2 register TRDSHUTS bit
TRDIOB pin pulse forced cutoff control	N/A	• TRDDFi register Bits PENB0 and PENB1
ELC event input i select for input capture	N/A	• TRDELC register ELCICEi bit
ELC event input i enable for pulse output forced cutoff	N/A	• TRDELC register ELCOBEi bit

Remark i = 0 or 1
j = A, B, C, D
k = C, D

2.10 Changes in Registers

2.10.1 TRDECR Register (R8C/36M Group Only)

When using the R8C/36M Group MCU in timer mode, set the TRDECR register to select the count source from TRDCLK input or fC2. The RL78/G14 MCU has no equivalent register.

2.10.2 TRDADCR Register (R8C/36M Group Only)

In the R8C/36M Group MCU, a compare match signal specified by the TRDADCR register can be used as a conversion start trigger of the A/D converter.
Timer RD cannot be used as an A/D conversion start trigger in RL78/G14. However, the A/D converter can be operated by using the ELC.

2.10.3 TRDFCR Register

In the R8C/36M Group MCU, an A/D trigger is enabled or disabled by setting the ADTRG bit in the TRDFCR register, and an A/D trigger edge can be selected by the ADEG bit in the TRDFCR register. Timer RD cannot be used as an A/D conversion start trigger in RL78/G14. However, the A/D converter can be operated by using the ELC.

- TRDFCR (R8C/36M Group)

b7	b6	b5	b4	b3	b2	b1	b0
PWM3	STCLK	ADEG	ADTRG	OLS1	OLS0	CMD1	CMD0

- TRDFCR (RL78/G14)

b7	b6	b5	b4	b3	b2	b1	b0
PWM3	STCLK	–	–	OLS1	OLS0	CMD1	CMD0

2.10.4 TRDDFi Register (i = 0, 1)

The digital filter function clock is different between the R8C/36M Group MCU and RL78/G14. Table 2.19 lists the comparison of digital filter function clock.

Table 2.19 Comparison of Digital Filter Function Clock

DFCK1	DFCK0	R8C/36M Group	RL78/G14
0	0	f32	$f_{CLK}/32$ Note 1
0	1	f8	$f_{CLK}/8$ Note 1
1	0	f1	f_{CLK} Note 1
1	1	Count source (the clock set by bits TCK0 to TCK2 in the TRDCRi register)	Count source (the clock set by bits TCK0 to TCK2 in the TRDCRi register)

Note 1: When the FRQSEL4 bit in the user option byte (000C2H/010C2H) is 1, $f_{CLK}/32$, $f_{CLK}/8$, and f_{CLK} are set to $f_{HOCO}/32$, $f_{HOCO}/8$, and f_{HOCO}, respectively.

Remark i = 0 or 1

Bits PENB0 and PENB1 are newly added to the RL78/G14 for the TRDIOB pin pulse forced cutoff control.

- TRDDFi (R8C/36M Group)

b7	b6	b5	b4	b3	b2	b1	b0
DFCK1	DFCK0	–	–	DFD	DFC	DFB	DFA

- TRDDFi (RL78/G14)

b7	b6	b5	b4	b3	b2	b1	b0
DFCK1	DFCK0	PENB1	PENB0	DFD	DFC	DFB	DFA

2.10.5 TRDCRi Register (i = 0, 1)

Count source which can be specified is different between the R8C/36M Group MCU and RL78/G14. Table 2.20 lists the comparison of count sources.

Table 2.20 Comparison of Count Sources

TCK2	TCK1	TCK0	R8C/36M Group Note 1	RL78/G14 Note 2
0	0	0	f1	f_{CLK}, f_{HOCO}
0	0	1	f2	$f_{CLK}/2$
0	1	0	f4	$f_{CLK}/4$
0	1	1	f8	$f_{CLK}/8$
1	0	0	f32	$f_{CLK}/32$
1	0	1	TRDCLK input Note 3 or fC2 Note 4	TRDCLK input Note 3
1	1	0	fOCO40M	Do not set
1	1	1	fOCO-F	Do not set

Notes: 1. Count source of Timer RD in R8C/36M: Max. 40 MHz
Set the Timer RD count source select to fOCO40M.
2. Count source of Timer RD in RL78/G14: Max. 64 MHz (set as follows.)
• Setting CPU clock
When supplying 64 MHz or 48 MHz to timer RD, set f_{CLK} to f_{IH}.
f_{IH} is controlled by hardware to be set to two frequency division of $f_{HOC}O$ when f_{HOCO} is set to 64 MHz or 48 MHz, and the same clock frequency as f_{HOCO} when f_{HOCO} is set to 32 MHz or less.
• Setting count source of Timer RD
When supplying 64 MHz or 48 MHz to timer RD, set the count source select to f_{HOCO}.
3. TRDCLK input cannot be selected in PWM3 mode.
4. fC2 cannot be selected in PWM mode, reset synchronous PWM mode, complementary PWM mode, or PWM3 mode.

2.10.6 TRDIORAi Register (i = 0, 1)

When using the input capture function in the R8C/36M Group MCU, the input-capture input can be specified as the fOCO128 signal or the TRDIOA0 pin input by the IOA3 bit in the TRDIORA0 register. The RL78/G14 MCU has no equivalent bit.

- TRDIORA0 (R8C/36M Group)

b7	b6	b5	b4	b3	b2	b1	b0
–	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0

- TRDIORA0 (RL78/G14)

b7	b6	b5	b4	b3	b2	b1	b0
–	IOB2	IOB1	IOB0	–	IOA2	IOA1	IOA0

2.10.7 TRDPSRi Register (i = 0, 1) (R8C/36M Group Only)

In the R8C/36M Group MCU, set registers TRDPSR0 and TRDPSR1 to assign I/O pins. As I/O pins are fixed in the RL78/G14 MCU, input or output mode can be set by the port mode register.

2.10.8 TRDOER2 Register

The TRDSHUTS bit is newly added to the RL78/G14 MCU to indicate the forced cutoff. When the pulse output is forcibly cut off, the TRDSHUTS bit in the TRDOER2 register is set to 1.

- TRDOER2 (R8C/36M Group)

b7	b6	b5	b4	b3	b2	b1	b0
PTO	–	–	–	–	–	–	–

- TRDOER2 (RL78/G14)

b7	b6	b5	b4	b3	b2	b1	b0
TRDPTO	–	–	–	–	–	–	TRDSHUTS

2.10.9 TRDELC Register (RL78/G14 Only)

Bits ELCICEi and ELCOBEi are newly added to the RL78/G14 MCU to select the ELC event input for the input capture, and to enable the ELC event for pulse output forced cutoff (i = 0, 1).

- TRDELC (RL78/G14)

b7	b6	b5	b4	b3	b2	b1	b0
–	–	ELCOBE1	ELCICE1	–	–	ELCOBE0	ELCICE0

3. Reference Application Note

RL78/G14 Timer RD Using Input Capture Function and Output Compare Function CC-RL (R01AN2852)
RL78/G14 Timer RD in Timer Mode (PWM Function) CC-RL (R01AN2851)
RL78/G14 Timer RD in Reset Synchronous PWM Mode CC-RL (R01AN2506)
RL78/G14 Timer RD in Complementary PWM Mode CC-RL (R01AN2572)
RL78/G14 Timer RD in PWM3 Mode CC-RL (R01AN2781)
RL78/G14 Utilising the Timer RD Unit Sample Code for e2studio (R01AN1328)
RL78/G14 Utilising the Timer RD Unit Sample Code for Cubesuite+ (R01AN1311)

The latest versions can be downloaded from the Renesas Electronics website.

4. Reference Documents

User's Manual: Hardware
RL78/G14 User's Manual: Hardware (R01UH0186)
R8C/36M Group User's Manual: Hardware (R01UH0259)
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

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Revision History

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.
   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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