RL78/G14, M16C/62P Group

Migration Guide from M16C to RL78: Interrupts

R01AN1998EJ0100
Rev.1.00
Mar. 3, 2014

Abstract

This application note explains how to migrate the interrupt function of the M16C/62P Group to that in RL78/G14.

Target Devices

RL78/G14, M16C/62P Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Differences between the M16C/62P Group and RL78/G14

1.1 Interrupts

Table 1.1 lists the general differences in interrupts.

Table 1.1 General Differences in Interrupts

Item	M16C/62P Group	RL78/G14
Maskable interrupts	Peripheral function interrupts (Note 1)	Peripheral function interrupts
Non-maskable interrupts	• Software interrupt – Undefined instruction (UND instruction) – Overflow (INTO instruction – BRK instruction – INT instruction	• Software interrupt – BRK instruction
	• Special interrupts – $\overline{\text{NMI}}$ – $\overline{\text{DBC}}$ (Note 2) – Watchdog time – Oscillation stop detection and re-oscillation detection – Low voltage detection – Single step (Note 2) – Address match	–
Interrupt priority levels	0 to 7 (Note 3)	0 to 3 (Note 4)
Type of vector table	• Fixed vector table • Relocatable vector table	Vector table
Vector table address	• Fixed address is in the fixed vector table • Relocatable address is in the relocatable vector table: (optional)	Fixed address is in the vector table

Notes

1. Peripheral function interrupts are generated by the peripheral functions in the MCU.
2. Do not use these interrupts. These are provided exclusively for use by development tools.
3. Level 0 is given low priority (interrupt disabled) and level 7 is given high priority
4. Level 3 is given low priority and level 0 is given high priority.

1.2 Differences in $\overline{\text{INT}}$ Interrupts

Table 1.2 lists the differences in $\overline{\text{INT}}$ interrupts.

Table 1.2 Differences on $\overline{\text{INT}}$ Interrupts

Item	M16C/62P Group	RL78/G14
$\overline{\text{INT}}$ interrupt pin	$\overline{\text{INT0}}$ to $\overline{\text{INT5}}$ (refer to Table 1.3.)	INTP0 to INTP11 (refer to **Table 1.4**.)
Digital filter	N/A	N/A

Table 1.3 $\overline{\text{INT}}$ Interrupt Pin Configuration in the M16C/62P Group

Pin name	Assigned pin		
	80-pin product	100-pin product	128-pin product
$\overline{\text{INT0}}$	P8_2		
$\overline{\text{INT1}}$	P8_3		
$\overline{\text{INT2}}$	P8_4		
$\overline{\text{INT3}}$	N/A	P1_5	
$\overline{\text{INT4}}$	N/A	P1_6	
$\overline{\text{INT5}}$	N/A	P1_7	

Table 1.4 INTP Interrupt Pin Configuration in RL78/G14

Pin name	Assigned pin									
	30-pin product	32-pin product	36-pin product	40-pin product	44-pin product	48-pin product	52-pin product	64-pin product	80-pin product	100-pin product
INTP0	P137									
INTP1	P50							P50 (P52)		P46 (P56)
INTP2	P51							P51 (P53)		P47
INTP3	P30							P30 (P54)		P30 (P57)
INTP4	P31							P31 (P55)		P31 (P146)
INTP5	P16							P16 (P12)		
INTP6	N/A					P140				P140 (P84)
INTP7	N/A							P141		P141 (P85)
INTP8	N/A					P74		P74 (P42)		P74 (P86)
INTP9	N/A					P75		P75 (P43)		P75 (P87)
INTP10	N/A						P76	P76 (P05)		P76 (P100)
INTP11	N/A						P77	P77 (P06)		P77 (P110)

Note

1. Functions in parentheses can be assigned via settings in the peripheral I/O redirection register 0 (PIOR 0). For more details, refer to 3.2.2 in this application note or the RL78/G14 User's Manual: Hardware.

1.3 Differences in Key Input Interrupts

Differences in key input interrupts are shown in Table 1.5.

Table 1.5 Differences in Key Input Interrupts

Item	M16C/62P Group	RL78/G14	
Number of input channels	4 channels	30-pin product	N/A
		32-pin product	
		36-pin product	
		40-pin product	4 channels
		44-pin product	
		48-pin product	6 channels
		52-pin product	8 channels
		64-pin product	
		80-pin product	
		100-pin product	
Key input interrupt pin	$\overline{KI0}$ to $\overline{KI3}$ (refer to Table 1.6.)	KR0 to KR7 (refer to Table 1.7.)	
Key input polarity	Falling edge	Falling edge	

Table 1.6 Key Input Interrupt Pin Configuration in the M16C/62P Group

Pin name	Assigned pin
$\overline{KI0}$	P10_4
$\overline{KI1}$	P10_5
$\overline{KI2}$	P10_6
$\overline{KI3}$	P10_7

Table 1.7 Key Input Interrupt Pin Configuration in RL78/G14

Pin name	Assigned pin									
	30-pin product	32-pin product	36-pin product	40-pin product	44-pin product	48-pin product	52-pin product	64-pin product	80-pin product	100-pin product
KR0	N/A			P70						
KR1	N/A			P71						
KR2	N/A			P72						
KR3	N/A			P73						
KR4	N/A					P74				
KR5	N/A					P75				
KR6	N/A						P76			
KR7	N/A						P77			

2. Register Compatibility

2.1 Interrupts

Table 2.1 lists the compatibility of registers associated with interrupts.

Table 2.1 Compatibility of Registers Associated with Interrupts

Item	M16C/62P Group	RL78/G14
Interrupt priority level select	Bits ILVL0 to ILVL2 in the interrupt control register	Bits XXPR1X and XXPR0X in the priority specification flag register
Interrupt request flag	IR bit in the interrupt control register	XXIFX bit in the interrupt request flag register
Interrupt handling control	Bits ILVL0 to ILVL2 in the interrupt control register (Level 0: interrupt disabled)	XXMKX bit in the interrupt mask flag register
Maskable interrupt enable control	I flag in the FLG register	IE flag in the PSW register
Processor interrupt priority specification	FLG register IPL	ISP1 and ISP0 in the PSW register

Note: For details on bits XXPR1X, XXPR0X, XXIFX, and XXMKX, refer to 3.1.2 in this application note or the RL78/G14 User's Manual: Hardware.

2.2 Registers Associated with $\overline{\text{INT}}$ Interrupts

Table 2.2 lists the compatibility of registers associated with $\overline{\text{INT}}$ interrupts.

Table 2.2 Compatibility of Registers Associated with $\overline{\text{INT}}$ Interrupts

Item	M16C/62P Group	RL78/G14
$\overline{\text{INT}}$ input polarity switch	• POL bit in the INTiIC register • IFSRi bit in the IFSR register	• EGPn bit in the registers EGP0 and EGP1 • EGNn bit in the registers EGN0 and EGN1
$\overline{\text{INT}}$ pin select	–	PIOR0 register
$\overline{\text{INT}}$ input enable	– (Use the IFSRk bit in the IFSR regiter to select $\overline{\text{INT4}}$ and $\overline{\text{INT5}}$ as interrupt source.)	• EGPn bit in the registers EGP0 and EGP1 • EGNn bit in the registers EGN0 and EGN1 (Edge detection is disabled when bits EGPn and EGNn are 0.)

–: No register is applicable. i = 0 to 5, k = 6 to 7, n = 0 to 11

2.3 Registers Associated with Key Input Interrupts

Table 2.3 lists the compatibility of registers associated with key input interrupts.

Table 2.3 Compatibility of Registers Associated with Key Input Interrupts

Item	M16C/62P Group	RL78/G14
Key input enable	PD10_i bit in the PD10 register	KRMn bit in the KRM register PM7n bit in the PM7 register

i = 4 to 7, n = 0 to 7

3. Comparison of Interrupt Operation Settings

3.1 Maskable Interrupts

3.1.1 M16C/62P Group

In the M16C/62P Group, maskable interrupts are enabled or disabled by setting the I flag in the FLG register, IPL, and bits ILVL0 to ILVL2 in interrupt control registers. The IR bit in interrupt control registers indicates whether there is an interrupt request or not.

Table 3.1 lists the functions of the I flag. Table 3.2 lists the functions of IPL. Table 3.3 lists the functions of the IR bit in the interrupt control register. Table 3.4 lists the functions of the interrupt priority level select bits.

Table 3.1 I Flag Functions

I flag	Maskable interrupt enable/disable
0	Disable maskable interrupts.
1	Enable maskable interrupts.

Table 3.2 IPL Functions

IPL	Maskable interrupt enable/disable
000b	Maskable interrupts at interrupt level 1 and above are enabled.
001b	Maskable interrupts at interrupt level 2 and above are enabled.
010b	Maskable interrupts at interrupt level 3 and above are enabled.
011b	Maskable interrupts at interrupt level 4 and above are enabled.
100b	Maskable interrupts at interrupt level 5 and above are enabled.
101b	Maskable interrupts at interrupt level 6 and above are enabled.
110b	Maskable interrupts at interrupt level 7 and above are enabled.
111b	All maskable interrupts are disabled.

Table 3.3 Interrupt Request Bit Functions

IR	Function
0	No interrupt requested
1	Interrupt requested

Table 3.4 Interrupt Priority Level Select Bits Functions

ILVL2	ILVL1	ILVL0	Interrupt priority level	Priority
0	0	0	Level 0 (interrupt disabled)	–
0	0	1	Level 1	Low ↓ High
0	1	0	Level 2	
0	1	1	Level 3	
1	0	0	Level 4	
1	0	1	Level 5	
1	1	0	Level 6	
1	1	1	Level 7	

Interrupts are acknowledged when:

- I flag = 1,
- IR bit = 1, and
- Interrupt priority level > IPL

Example: Interrupts of the timer A0 are acknowledged when:

I flag: I flag in the FLG register is 1,
IR bit: IR bit (bit 3) in the TA0IC register is 1, and
Interrupt priority level: Bits ILV2 to ILV0 in the TA0IC register > IPL in the FLG register.

3.1.2 RL78/G14

In RL78/G14, maskable interrupts are enabled or disabled by setting the flags IE, ISP0, and ISP1 in the PSW register, bits XXPR1X and XXPR0X in the priority specification flag register and the XXMKX bit in the interrupt mask flag register. The XXIFX bit in the interrupt request flag registers indicates whether there is an interrupt request or not.

Table 3.5 lists the functions of the IE flag. Table 3.6 lists the functions of flags ISP1 and ISP0. Table 3.7 lists the functions of the interrupt request flag. Table 3.8 lists the functions of the interrupt servicing control bit. Table 3.9 lists the functions of priority level select bits.

Table 3.5 IE Flag Functions

IE flag	Interrupt request acknowledge enable/disable
0	Disabled
1	Enabled

Table 3.6 ISP1 and ISP0 Flag Functions

ISP1	ISP0	Priority of interrupts being handled
0	0	Interrupt at level 0 is enabled. (Interrupt at level 1 or 0 is being handled.)
0	1	Interrupts at levels 0 and 1 are enabled. (Interrupt at level 2 is being handled.)
1	0	Interrupts at level 0 to 2 are enabled. (Interrupt at level 3 is being handled.)
1	1	All interrupts are enabled. (Wait for an acknowledgment of interrupt)

Table 3.7 Interrupt Request Flag Functions

XXIFX	Interrupt request flag
0	No interrupt request signal is generated.
1	Interrupt request is generated, interrupt request status

Note: For details of the XXIFX bit, refer to the RL78/G14 User's Manual: Hardware.

Table 3.8 Interrupt Handling Control Bit Functions

XXMKX	Interrupt handling control
0	Interrupt handling enabled
1	Interrupt handling disabled

Note: For details of the XXMKX bit, refer to the RL78/G14 User's Manual: Hardware.

Table 3.9 Priority Level Select Bits Functions

XXPR1X	XXPR0X	Priority level select
0	0	Specify level 0 (high priority level).
0	1	Specify level 1.
1	0	Specify level 2.
1	1	Specify level 3 (low priority level).

Note: For details on bits XXPR1X and XXPR0X, refer to the RL78/G14 User's Manual: Hardware.

Interrupts are acknowledged when:

- Interrupt request flag = 1,
- Interrupt mask flag = 0,
- IE flag = 1, and
- Interrupt priority level ≤ (ISP1, ISP0)

Example: Interrupts of channel 0 of the timer array unit 0 are acknowledged when:

Interrupt request flag: TMIF00 bit (bit 4) in the IF1L register is 1,
Interrupt mask flag: TMMK00 bit (bit 4) in the MK1L register is 0,
IE flag: IE flag in PSW is 1, and
Interrupt priority level:
Bits TMPR100 and TMPR000 in the registers PR11L and PR01L ≤ Bits ISP1 and ISP0 in PSW

3.2 $\overline{\text{INT}}$ Interrupts

3.2.1 M16C/62P

In the M16C/62P Group, there is no setting to enable or disable $\overline{\text{INT}}$ interrupts. However, $\overline{\text{INT4}}$ sets the IFSR6 bit in the IFSR register to select SI/03 or the interrupt factor. Similarly, $\overline{\text{INT5}}$ sets the IFSR7 bit to specify SI/04 or the interrupt factor. Table 3.10 lists the functions of interrupt request factor select bit.

Input polarity can be specified by using the IFSRi bit in the IFSR register and the POL bit in the INTiIC register (i = 0 to 5). Table 3.11 lists the functions of $\overline{\text{INTi}}$ interrupt polarity switch bit. Table 3.12 shows the polarity switch bit functions.

Table 3.10 Interrupt Request Factor Select Bit Functions

IFSRk	Interrupt request factor select
0	SI / Ox
1	$\overline{\text{INTx}}$

k = 6 to 7

Table 3.11 $\overline{\text{INTi}}$ Interrupt Polarity Switch Bit Functions

IFSRi (Note 1)	$\overline{\text{INTi}}$ interrupt polarity switch
0	One edge
1	Both edges

i = 0 to 5

Note

1. When setting this bit to “1” (= both edges), make sure the POL bit in the corresponding INTiIC register is set to “0” (= falling edge).

Table 3.12 Polarity Switch Bit Functions

POL (Note 1)	Valid edge select
0	Falling edge selected
1	Rising edge selected (Note 2)

Note

1. When changing the POL bit, the IR bit may become "1" (= interrupt requested).
2. When setting the IFSRi bit to “1” (= both edges), make sure the POL bit in the INTiIC register is set to “0” (= falling edge). (i = 0 to 5)

3.2.2 RL78/G14

In RL78/G14, valid edges of pins INTP0 to INTP11 are specified by setting registers EGPm and EGNm (m = 0 and 1).

Table 3.13 lists the functions of the INTPn pin valid edge select bit, and Table 3.14 lists the ports corresponding to bits EGPn and EGNn (n = 0 to 11).

The input pins of INTP interrupt can be assigned via setting in the PIOR0 register. Table 3.15 to Table 3.18 show the allocation of INTP interrupt input pins

Table 3.13 INTPn Pin Valid Edge Select Bits Functions

EGPn	EGNn	INTPn pin valid edge select
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

n = 0 to 11

Table 3.14 Ports Corresponding to Bits EGPn and EGNn (n = 0 to 11)

Detection enable bit		Corresponding port
EGP0	EGN0	INTP0
EGP1	EGN1	INTP1
EGP2	EGN2	INTP2
EGP3	EGN3	INTP3
EGP4	EGN4	INTP4
EGP5	EGN5	INTP5
EGP6	EGN6	INTP6
EGP7	EGN7	INTP7
EGP8	EGN8	INTP8
EGP9	EGN9	INTP9
EGP10	EGN10	INTP10
EGP11	EGN11	INTP11

Table 3.15 INTP Interrupt Input Pin Select Bit Functions (1)

PIOR05		Pin select									
		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin
0	INTP1	Set to 0 (default value).									P46
	INTP3										P30
	INTP4										P31
	INTP6										P140
	INTP7										P141
	INTP8										P74
	INTP9										P75
1	INTP1	Do not set.									P56
	INTP3										P57
	INTP4										P146
	INTP6										P84
	INTP7										P85
	INTP8										P86
	INTP9										P87

Table 3.16 INTP Interrupt Input Pin Select Bit Functions (2)

PIOR04		Pin select									
		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin
0	INTP5	Set to 0 (default value).							P16		
1		Do not set.							P12		

Table 3.17 INTP Interrupt Input Pin Select Bit Functions (3)

PIOR01		Pin select									
		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin
0	INTP10	–						P76			
	INTP11	–							P05	P100	
1	INTP10	–						P77			
	INTP11	–							P06	P110	

Table 3.18 INTP Interrupt Input Pin Select Bit Functions (4)

PIOR00		Pin select								
		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin
0	INTP1	Set to 0 (default value).							P50		Set to 0 (default value).
	INTP2								P51		
	INTP3								P30		
	INTP4								P31		
	INTP8								P74		
	INTP9								P75		
1	INTP1	Do not set.							P52		Do not set.
	INTP2								P53		
	INTP3								P54		
	INTP4								P55		
	INTP8								P42		
	INTP9								P43		

3.3 Key Input Interrupts

3.3.1 M16C/62P Group

In the M16C/62P Group, the PD10_k bit in the PD10 register is used for controlling key input and port input/output. Table 3.19 lists the functions of bits to enable or disable key input. Table 3.20 lists the ports corresponding to PD10_k.

Table 3.19 Key Input Control Bit Functions

PD10_k	Key input enable/disable (port I/O select)
0	Enabled (input mode)
1	Disabled (output mode)

k = 4 to 7

Table 3.20 Key Input (Ports) Corresponding to PD10_k Bit

Direction bit	Corresponding key input (port)
PD10_4	$\overline{KI0}$ (P10_4)
PD10_5	$\overline{KI1}$ (P10_5)
PD10_6	$\overline{KI2}$ (P10_6)
PD10_7	$\overline{KI3}$ (P10_7)

k = 4 to 7

3.3.2 RL78/G14

In RL78/G14, set the KRMn bit in the KRM register to enable or disable the key interrupt. Table 3.21 lists the functions of key interrupt mode control bit.

Also, in RL78/G14, set the PM7 register to select input or output mode of the pin (I/O port). Table 3.22 lists the functions of port I/O mode select bit. To enable key input, set the pin (I/O port) to input mode.

Table 3.21 Key Interrupt Mode Control Bit Functions

KRMn	Key interrupt mode control
0	Does not detect key interrupt signal
1	Detects key interrupt signal

n = 0 to 7

Table 3.22 Port I/O Mode Select Bit Functions

PM7n	P7n pin I/O mode select
0	Output mode (functions as output port (output buffer on))
1	Input mode (functions as input port (output buffer off))

n = 0 to 7

3.4 Interrupt Priority Level

3.4.1 M16C/62P Group

In the M16C/62P Group, if two or more interrupt requests are sampled at the same sampling points (a timing to detect whether an interrupt request is generated or not), the interrupt with the highest priority is acknowledged.

For maskable interrupts (peripheral functions interrupt), any desired priority level can be selected using the ILVL2 to ILVL0 bits. However, if two or more maskable interrupts have the same priority level, the request with the highest priority set in hardware is accepted.

The watchdog timer and other special interrupts have their priority levels set in hardware.

Software interrupts are not affected by the interrupt priority.

3.4.2 RL78/G14

In RL78/G14, when two or more maskable interrupt requests are generated simultaneously, the request with a higher priority level specified in the priority specification flag is acknowledged first. If two or more interrupt requests have the same priority level, the request with the highest default priority is acknowledged first

3.5 Register Saving

3.5.1 M16C/62P Group

In the M16C/62P Group, the FLG register and the PC (program counter) are saved in the stack. To be more specific, the 4 high-order bits in the PC, and the 4 high-order bits (IPL) and 8 low-order bits in the FLG register (16 bits in total) are saved in the stack first, and then the 16 low-order bits in the PC are saved.

3.5.2 RL78/G14

In RL78/G14, when a maskable interrupt request is acknowledged, the PC is saved in the stack after the program status word (PSW) is saved.

3.6 $\overline{\text{NMI}}$ Interrupts

3.6.1 M16C/62P Group

An $\overline{\text{NMI}}$ interrupt is generated when input on the NMI pin changes state from high to low. The $\overline{\text{NMI}}$ interrupt is a non-maskable interrupt.

3.6.2 RL78/G14

In RL78/G14, there is no non-maskable interrupts generated in accordance with pin input status.

In RL78/G14, INTPn interrupt is used to execute $\overline{\text{NMI}}$ interrupt operation in the M16C/62P Group. Specifically, the falling edge is selected as the valid edge, INTPn interrupt is enabled, the interrupt priority level is set to 0 (high priority), and then multiple interrupts are enabled in handling interrupts other than INTPn (n = 0 to 11. Specify a smaller number. If possible, select 0.) In normal processing (other than interrupt handling) parts, interrupts must not be disabled. (Do not set the IE flag to 0.)

Figure 3.1 is a flowchart for setting INTP0 to use it as the alternative to $\overline{\text{NMI}}$ interrupts. Figure 3.2 shows a flow for handling interrupts other than INTP0. Figure 3.3 is a flowchart for main processing.

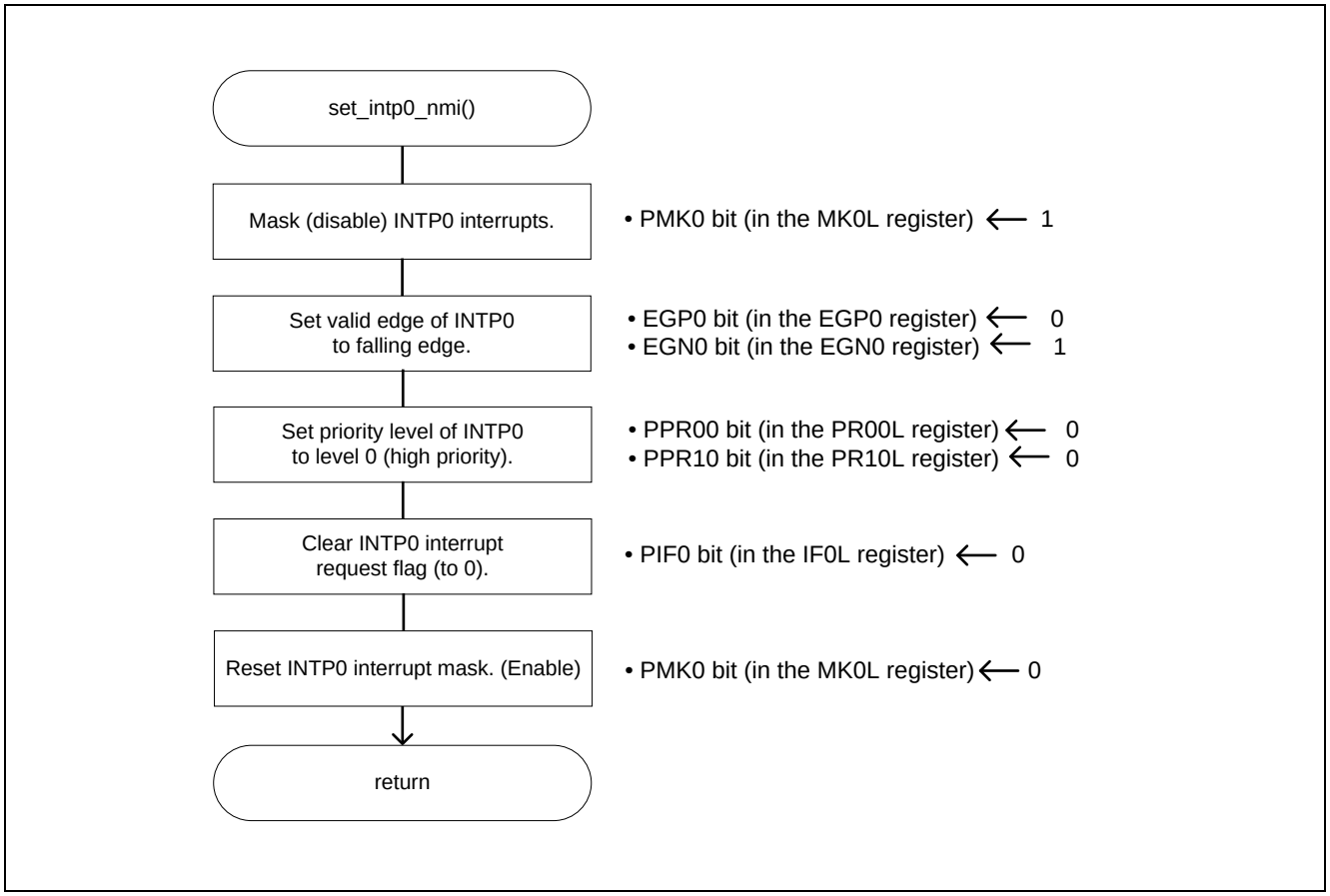

Figure 3.1 Setting to Use INTP0 as the Alternative to $\overline{\text{NMI}}$ Interrupts

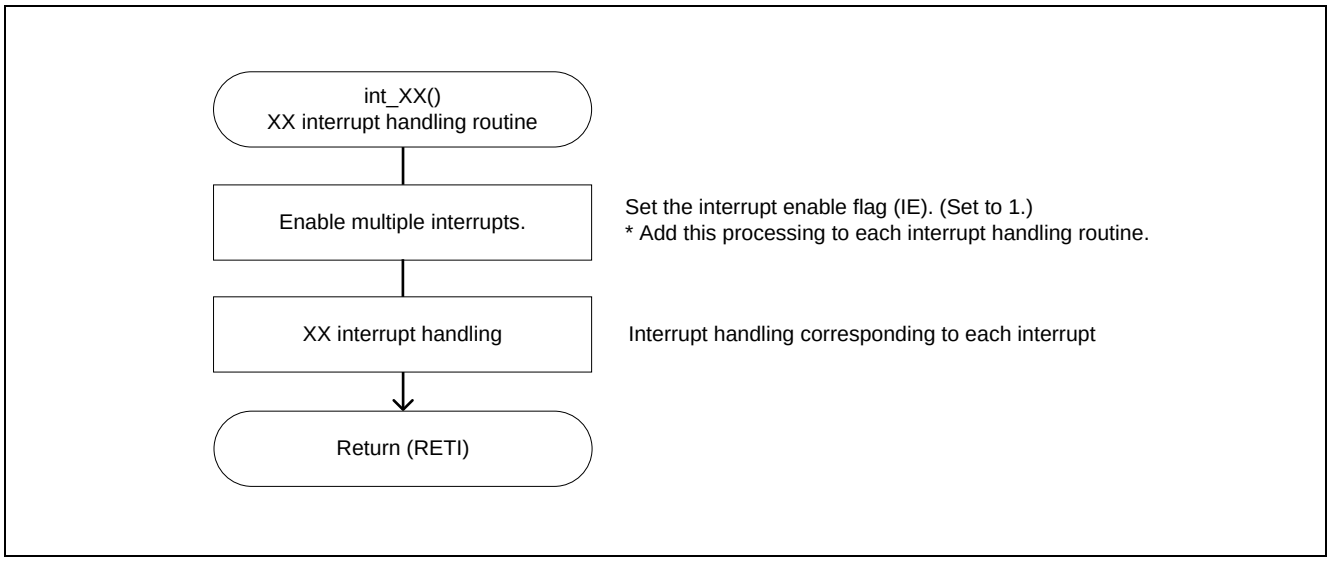

Figure 3.2 Handling Interrupts Other Than INTP0 Used as the Alternative to $\overline{\text{NMI}}$ Interrupts

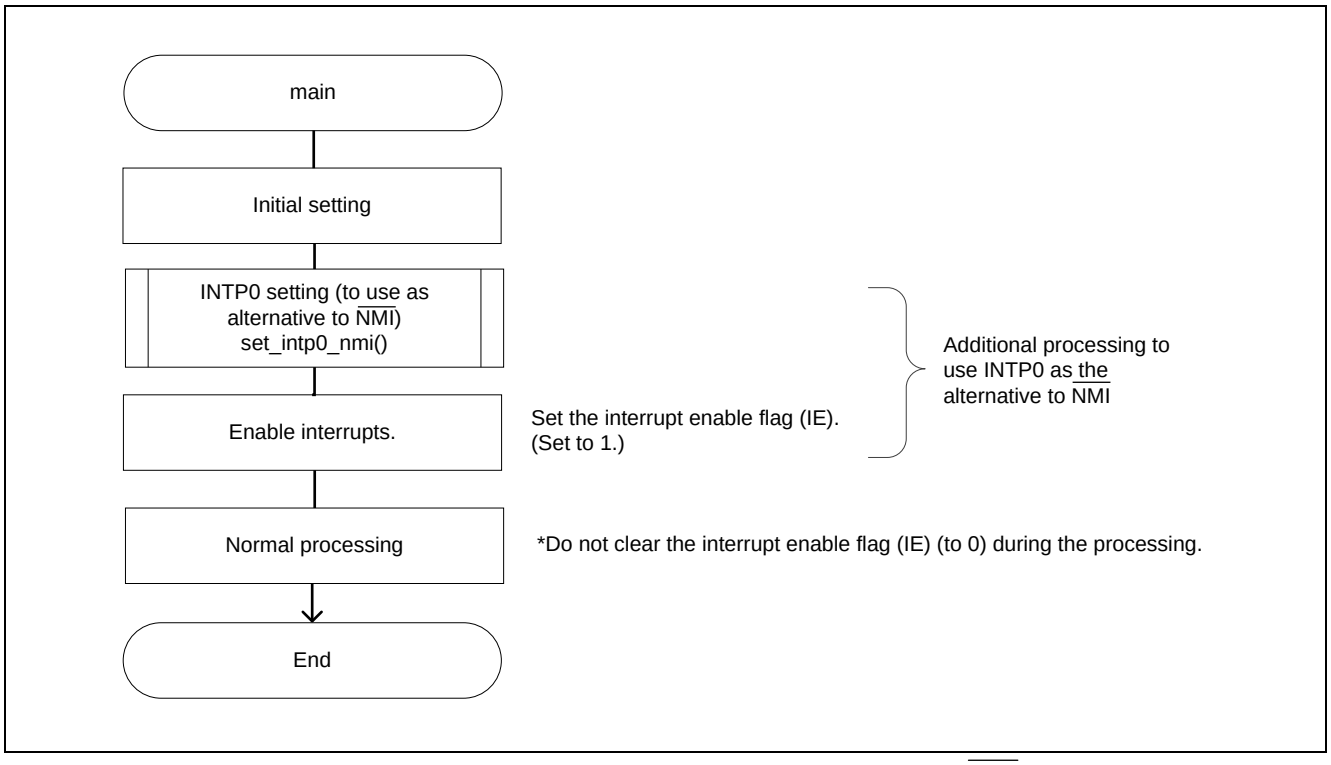

Figure 3.3 Main Processing to Use INTP0 as the Alternative to $\overline{\text{NMI}}$ Interrupts

4. Interrupt Vectors

The configuration of interrupt vectors varies between the M16C/62P Group and RL78/G14. The M16C/62P Group has fixed vector tables and relocatable vector tables, and RL78/G14 has address-fixed vector tables.

4.1 M16C/62P Group

4.1.1 Fixed Vector Tables

Fixed vector tables are allocated from addresses FFFDCh to FFFFFh. Table 4.1 shows the fixed vector tables.

Table 4.1 Fixed Vector Tables

Interrupt source	Vector address Address (L) to address (H)	Remarks
Undefined instruction	FFFDCh to FFFDFh	Interrupt with UND instruction
Overflow	FFFE0h to FFFE3h	Interrupt with INTO instruction
BRK instruction	FFFE4h to FFFE7h	If the value of address FFFE7h is FFH, program execution starts from the address shown by the vector in the relocatable vector table
Address match	FFFE8h to FFFEBh	
Single step (Note 1)	FFFECh to FFFEFh	
Watchdog timer, Oscillation stop, Re-oscillation detection, Low voltage detection	FFFF0h to FFFF3h	
$\overline{\text{DBC}}$ (Note 1)	FFFF4h to FFFF7h	
$\overline{\text{NMI}}$	FFFF8h to FFFFBh	
Reset	FFFFCh to FFFFFh	

Note

1. Do not use these interrupts. They are provided exclusively for use by development tools.

4.1.2 Relocatable Vector Table

Relocatable vector tables occupy 256 bytes beginning from the start address set in the INTB register. Table 4.2 lists the relocatable vector tables. Setting an even address in the INTB register causes the interrupt sequence to be executed faster than in the case of odd addresses.

Table 4.2 Relocatable Vector Tables

Interrupt source	Vector address Address (L) to address (H)	Software interrupt number	Interrupt control register
BRK instruction (Note 4)	+0 to +3 (0000h to 0003h)	0	
– (Reserved)		1 to 3	–
$\overline{\text{INT3}}$	+16 to +19 (0010h to 0013h)	4	INT3IC
Timer B5	+20 to +23 (0014h to 0017h)	5	TB5IC
Timer B4, UART1 bus collision detect (Notes 3, 5)	+24 to +27 (0018h to 001Bh)	6	TB4IC/U1BCNIC
Timer B3, UART0 bus collision detect (Notes 3, 5)	+28 to +31 (001Ch to 001Fh)	7	TB3IC/U0BCNIC
SI/O4, $\overline{\text{INT5}}$ (Note 1)	+32 to +35 (0020h to 0023h)	8	S4IC/ S4IC
SI/O3, $\overline{\text{INT4}}$ (Note 1)	+36 to +39 (0024h to 0027h)	9	S3IC/ INT4IC
UART2 bus collision detect (Note 5)	+40 to +43 (0028h to 002Bh)	10	BCNIC
DMA0	+44 to +47 (002Ch to 002Fh)	11	DM0IC
DMA1	+48 to +51 (0030h to 0033h)	12	DM1IC
Key input interrupt	+52 to +55 (0034h to 0037h)	13	KUPIC
A/D	+56 to +59 (0038h to 003Bh)	14	ADIC
UART2 transmit, NACK2 (Note 2)	+60 to +63 (003Ch to 003Fh)	15	S2TIC
UART2 receive, ACK2 (Note 2)	+64 to +67 (0040h to 0043h)	16	S2RIC
UART0 transmit, NACK0 (Note 2)	+68 to +71 (0044h to 0047h)	17	S0TIC
UART0 receive, ACK0 (Note 2)	+72 to +75 (0048h to 004Bh)	18	S0RIC
UART1 transmit, NACK1 (Note 2)	+76 to +79 (004Ch to 004Fh)	19	S1TIC
UART1 receive, ACK1 (Note 2)	+80 to +83 (0050h to 0053h)	20	S1RIC
Timer A0	+84 to +87 (0054h to 0057h)	21	TA0IC
Timer A1	+88 to +91 (0058h to 005Bh)	22	TA1IC
Timer A2	+92 to +95 (005Ch to 005Fh)	23	TA2IC
Timer A3	+96 to +99 (0060h to 0063h)	24	TA3IC
Timer A4	+100 to +103 (0064h to 0067h)	25	TA4IC
Timer B0	+104 to +107 (0068h to 006Bh)	26	TB0IC
Timer B1	+108 to +111 (006Ch to 006Fh)	27	TB1IC
Timer B2	+112 to +115 (0070h to 0073h)	28	TB2IC
$\overline{\text{INT0}}$	+116 to +119 (0074h to 0077h)	29	INT0IC
$\overline{\text{INT1}}$	+120 to +123 (0078h to 007Bh)	30	INT1IC
$\overline{\text{INT2}}$	+124 to +127 (007Ch to 007Fh)	31	INT2IC
INT instruction interrupt (Note 4)	+128 to +131 (0080h to 0083h) to +252 to +255 (00FCh to 00FFh)	32 to 63	–

Notes

1. Use the IFSR6 and IFSR7 bits in the IFSR register to select.
2. During I^2C mode, NACK and ACK interrupts comprise the interrupt source.
3. Use the IFSR26 and IFSR27 bits in the IFSR2A register to select.
4. These interrupts cannot be disabled using the I flag.
5. Bus collision detection: During IE mode, this bus collision detection constitutes the factor of an interrupt. During I2C mode, however, a start condition or a stop condition detection constitutes the factor of an interrupt.

4.2 RL78/G14

Set the program start address where the CPU branches when interrupts or reset sources are generated in the RL78/G14 vector tables. Since there are 2 bytes in each vector code, the destination start address is a 64 KB address from 00000H to 0FFFFH. The highest default priority is 0 and the lowest is 44. When an interrupt request is acknowledged, the CPU branches to the address set in the corresponding interrupt vector. Vector tables are listed in Table 4.3 to Table 4.5.

Table 4.3 Vector Tables (1/3)

Default priority	Interrupt source		Internal/ external	Vector address
	Name	Trigger		
0	INTWDTI	Watchdog timer interval (75% of overflow time + 1/2 fIL)	Internal	0004H
1	INTLVI	Voltage detected		0006H
2	INTP0	Pin input edge detected	External	0008H
3	INTP1			000AH
4	INTP2			000CH
5	INTP3			000EH
6	INTP4			0010H
7	INTP5			0012H
8	INTST2/ INTCSI20/ INTIIC20	UART2 transmission transfer end or buffer empty interrupt/ CSI20 transfer end or buffer empty interrupt/ IIC20 transfer end	Internal	0014H
9	INTSR2/ INTCSI21/ INTIIC21	UART2 reception transfer end/ CSI21 transfer end or buffer empty interrupt/ IIC21 transfer end		0016H
10	INTSRE2	UART2 reception communication error occurred		0018H
	INTTM11H	End of timer channel 11 count or capture (when the higher 8-bit timer is operating)		
11	INTST0/ INTCSI00/ INTIIC00	UART0 transmission transfer end/ CSI00 transfer end or buffer empty interrupt/ IIC00 transfer end		001EH
12	INTSR0/ INTCSI01/ INTIIC01	UART0 reception transfer end/ CSI01 transfer end or buffer empty interrupt/ IIC01 transfer end		0020H
13	INTSRE0	UART0 reception communication error occurred		0022H
	INTTM01H	End of timer channel 01 count or capture (when the higher 8-bit timer is operating)		
14	INTST1/ INTCSI10/ INTIIC10	UART1 transmission transfer end or buffer empty interrupt/CSI10 transfer end or buffer empty interrupt/IIC10 transfer end		0024H
15	INTSR1/ INTCSI11/ INTIIC11	UART1 reception transfer end/CSI11 transfer end or buffer empty interrupt/IIC11 transfer end		0026H
16	INTSRE1	UART1 reception communication error occurred		0028H
	INTTM03H	End of timer channel 03 count or capture (when the higher 8-bit timer is operating)		

Table 4.4 Vector Tables (2/3)

Default priority	Interrupt source		Internal/ external	Vector address
	Name	Trigger		
17	INTIICA0	End of IICA0 communication	Internal	002AH
18	INTTM00	End of timer channel 00 count or capture		002CH
19	INTTM01	End of timer channel 01 count or capture		002EH
20	INTTM02	End of timer channel 02 count or capture		0030H
21	INTTM03	End of timer channel 03 count or capture		0032H
22	INTAD	End of A/D conversion		0034H
23	INTRTC	Fixed-cycle signal of real-time clock/alarm match detected		0036H
24	INTIT	Interval signal detected		0038H
25	INTKR	Key return signal detected	External	003AH
26	INTST3/ INTCSI30/ INTIIC30	UART3 transmission transfer end or buffer empty interrupt/CSI30 transfer end or buffer empty interrupt/IIC30 transfer end	Internal	003CH
27	INTSR3/ INTCSI31/ INTIIC31	UART3 reception transfer end/ CSI31 transfer end or buffer empty interrupt/ IIC31 transfer end		003EH
28	INTTRJ0	Timer RJ interrupt		0040H
29	INTTM10	End of timer channel 10 count or capture		0042H
30	INTTM11	End of timer channel 11 count or capture		0044H
31	INTTM12	End of timer channel 12 count or capture		0046H
32	INTTM13	End of timer channel 13 count or capture		0048H
33	INTP6	Pin input edge detected	External	004AH
34	INTP7			004CH
35	INTP8			004EH
36	INTP9			0050H
37	INTP10	Pin input edge detected	External	0052H
	INTCMP0	Comparator detection 0	Internal	
38	INTP11	Pin input edge detected	External	0054H
	INTCMP1	Comparator detection 1	Internal	
39	INTTRD0	Timer RD0 input capture, compare match, overflow, underflow interrupt	Internal	0056H
40	INTTRD1	Timer RD1 input capture, compare match, overflow, underflow interrupt		0058H

Table 4.5 Vector Tables (3/3)

Default priority	Interrupt source		Internal/ external	Vector address
	Name	Trigger		
41	INTTRG	Timer RG input capture, compare match, overflow, underflow interrupt	Internal	005AH
42	INTSRE3	UART3 reception communication error occurred		005CH
	INTTM13H	End of timer channel 13 count or capture (when the higher 8-bit timer is operating)		
43	INTIICA1	End of IICA1 communication		0060H
44	INTFL	Reserved		0062H
–	BRK	BRK instruction executed	–	007EH
	RESET	$\overline{\text{RESET}}$ pin input		0000H
	POR	Power-on-reset		
	LVD	Voltage detected		
	WDT	Overflow of watchdog timer		
	TRAP	Illegal instruction executed		
	IAW	Illegal-memory access		
	RAMTOP	RAM parity error		

5. Reference Documents

RL78/G14 User's Manual: Hardware Rev. 2.00

M16C/62P Group (M16C/62P, M16C/62PT) Hardware Manual Rev.2.41

The latest versions can be downloaded from the Renesas Electronics website.

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REVISION HISTORY

Rev.	Date	Description	
		Page	Summary
1.00	Mar.3,2014		First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 LanGao Rd., Putuo District, Shanghai, China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 3.0