RL78/G13

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Voltage Detector (Reset Mode) for Cubesuite+ and IAR Toolchain

Introduction

This application note describes the reset mode of the voltage detector (LVD) on the RL78/G13. When the supply voltage (V_{DD}) becomes lower than the LVD detection voltage (V_{LVI}), the voltage detector generates an internal reset. Using LEDs, the internal reset can be distinguished from a power-on-reset (POR).

Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

This application note has been updated for the RSKRL78/G13 hardware platform.

Contents

1. Installation

This application note and associated code has been written to work with both Cubesuite+ and IAR IDEs and compilers.

Decompress (if zipped) the files.

For Cubesuite+: Open the .mtpj project in the \CS+ Code directory in Cubesuite+

For IAR: Open the .eww workspace in the \IAR directory in IAR Workbench.

2. Specifications

This application note describes the operation (reset mode) of the voltage detector.

When the supply voltage (V_{DD}) becomes lower than the LVD detection voltage (V_{LVI}), the voltage detector generates an internal reset. The three LEDs permit a visual distinction between this internal reset and a power-on-reset. The indications provided by these LEDs are changed according to the switch SW1 input count.

When $V_{DD} < V_{LVI}$, the voltage detector generates an internal reset. Later, when $V_{DD} \geq V_{LVI}$, this reset is ended. At this time, the system restarts from the state it was in when the LEDs provided the last indications.

When $V_{DD} < V_{PDR}$, an internal reset occurs due to a power-on-reset. Later, when $V_{DD} \geq V_{LVI}$, this internal reset is ended and the system restarts while all the LEDs are off.

Table 2.1 shows the required peripheral functions and their uses. Figure 2.2 presents an overview of the operation (reset mode) of the voltage detector.

Table 2.1 Required Peripheral Functions and Their Uses

Peripheral Function	Use
LVD	Supply voltage (VDD) monitoring
P50/INTP1	Switch SW1 Input
P53, P62, P63	LED lighting control (for LED1 to LED3)

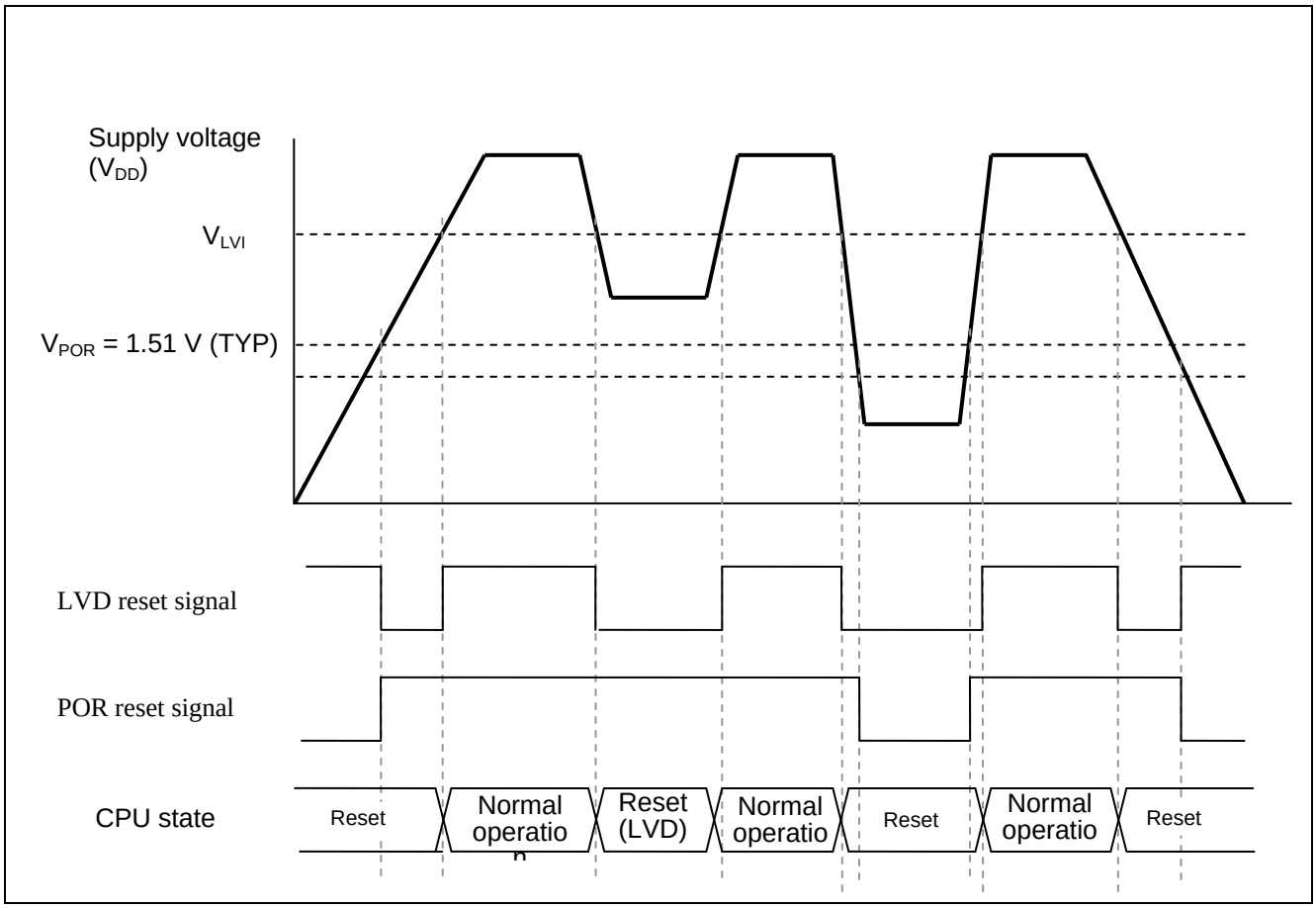


Figure 2.2 Overview of LVD Operation (Reset Mode)

3. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 3.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G13 (R5F100LEA)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 32 MHz • CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0 V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVI}): Reset mode • Rising edge voltage: 2.81 V (2.76 V to 2.87 V) • Falling edge voltage: 2.75 V (2.70 V to 2.81V)
Integrated development environments	CubeSuite+ V1.00.01 from Renesas Electronics Corp. IAR Embedded Workbench for Renesas RL78 version 1.10.4
C compiler	CA78K0R V1.20 from Renesas Electronics Corp. ICCRL78 V1.10.4 C/C++ Compiler for Renesas RL78 From IAR

4. Related Application Notes

The application note related to this application note is listed below for reference.

- RL78/G13 Initialization (R01AN1083EG0100) Application Note

5. Description of the Hardware

5.1 Hardware Configuration Example

Figure 5.1 shows an example of the hardware configuration used for this application note.

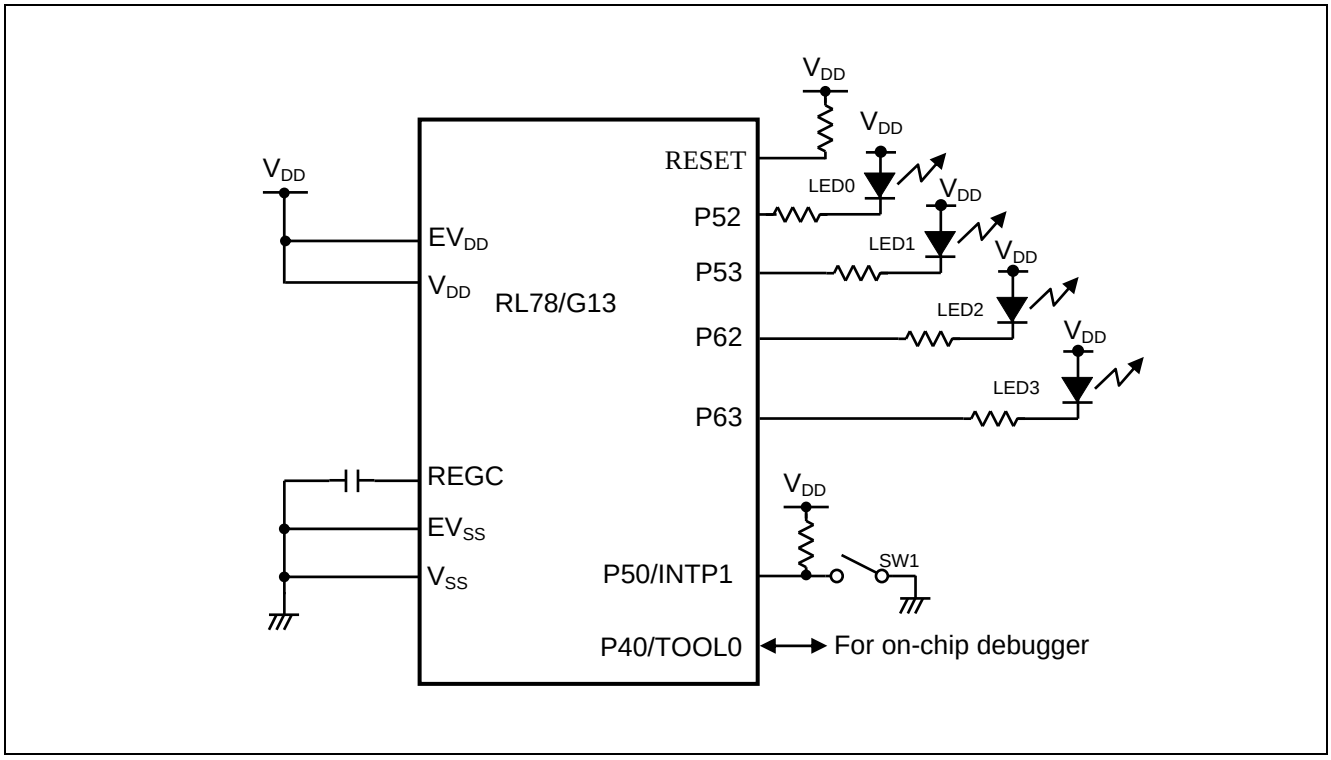


Figure 5.1 Hardware Configuration

Cautions 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.

5.2 List of Pins to be Used

Table 5.1 lists the pins to be used and their functions.

Table 5.1 Pins to be Used and Their Functions

Pin Name	I/O	Description
P52	Output	LED on (LED0) control port
P53	Output	LED on (LED1) control port
P62	Output	LED on (LED2) control port
P63	Output	LED on (LED3) control port
P50/INTP1	Input	Switch SW1 input port

6. Description of the Software

6.1 Operation Outline

The sample program described in this application note monitors the supply voltage using the voltage detector (reset mode).

When $V_{DD} < V_{LVI}$, the voltage detector generates an internal reset (LVD reset). At this time, various registers are initialized. If, however, V_{DD} is equal to or greater than the power-on-reset detection voltage (V_{PDR} = 1.50 V ± 0.03 V), the on-chip RAM's state remains unchanged since before the reset generation. Because the on-chip RAM holds the switch input count which was obtained before the reset generation, the system can restart from the state it was in when the LED indications were provided before the reset generation.

The switch input count is initialized when a reset other than the LVD reset occurs.

(1) Initializing the voltage detector

<Conditions for setting>

- When the power is turned on or after the reset is ended, the option byte should be referenced automatically and the voltage detector should be set to reset mode.
- The rising edge detection voltage should be set to 2.81 V. The falling edge detection voltage should be set to 2.75 V.

Caution: When reset mode is selected, the voltage detection level register (LVIS) is write-prohibited. The initial value for the LVIS register is set to 81H (low-voltage detection level: V_{LVI} for reset mode) automatically.

(2) Setting the input and output ports

- LED lighting control (for LED1 to LED3): Configure P52, P62 and P63 as the output ports.
- Switch SW1 input: Configure P50/INTP1 for detecting INTP1 falling edges (via an external pull-up resistor)

(3) LED indications depending on the switch SW1 input count

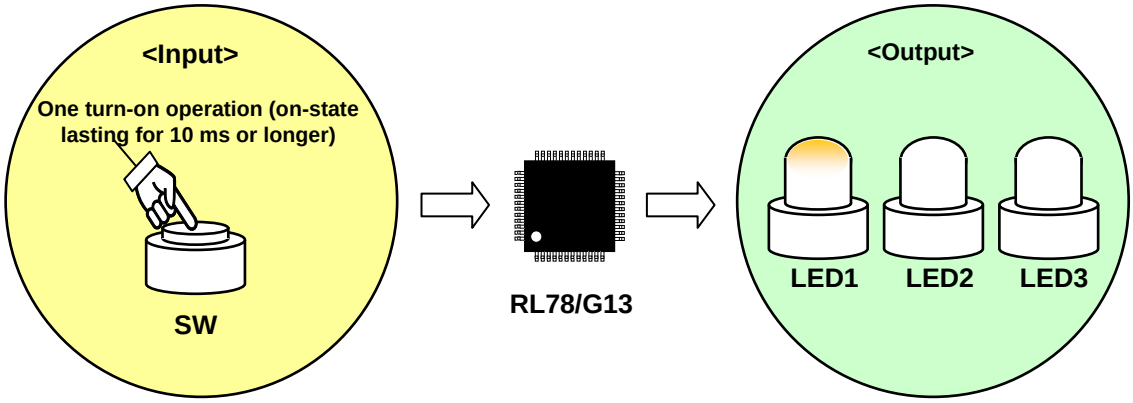
- Interrupt processing is started upon detection of a P50/INTP1 falling edge. Chattering is detected and, if the on state of the input lasts about 10 ms, it is recognized as a switch input and the LED indications are changed. When $V_{DD} < V_{LVI}$, an LVD reset is generated; however the on-chip RAM's state remains unchanged since before the reset generation (see Note).

(4') When $V_{DD} < V_{PDR}$, a POR internal reset occurs, deleting the LED indication data.

Caution: If the standard startup routine is used for programs written in C, data in the on-chip RAM is initialized before the main function is executed. To prevent it from being initialized, a startup routine which has its initialization code commented out is adopted.

Caution: Usage Precautions: For information about the precautions in using the device, refer to RL78/G13 User's Manual: Hardware.

Figure 5.1 presents an overview of the sample code operation.



Switch (SW1) input count Note	LED indications		
	LED1	LED2	LED3
0	OFF	OFF	OFF
1	ON	OFF	OFF
2	OFF	ON	OFF
3	ON	ON	OFF
4	OFF	OFF	ON
5	ON	OFF	ON
6	OFF	ON	ON
7	ON	ON	ON

Note: For the eighth and subsequent operations, the LED indications above are repeated.

Figure 6.1 Overview of Sample Code Operation

6.2 List of Option Byte Settings

Table 6.1 summarizes the settings of the option bytes.

Table 6.1 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode Rising edge voltage: 2.81 V (2.76 V to 2.87 V) Falling edge voltage: 2.75 V (2.70 V to 2.81 V)
000C2H/010C2H	11101000B	HS mode HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

6.3 List of Variables

Table 6.2 lists the global variables.

Table 6.2 Global Variables

Type	Variable Name	Contents	Function Used
uint8_t	g_ResetFactor	RESF register save area	main() R_CGC_Get_ResetSource()
uint8_t	g_SwCount	SW depress count	main() R_INTC1_Interrupt()

6.4 List of Functions

Table 6.3 gives a list of functions that are used by this sample program.

Table 6.3 Functions

Function Name	Outline
R_PORT_Create	Initializes the input and output ports.
R_INTC_Create	Initializes the external-interrupt settings.
R_INTC1_Start	Enables INTP1 interrupts.
R_INTC1_Interrupt	Processes INTP1 interrupts.

6.5 Function Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name] R_PORT_Create

Synopsis	Initializes the input and output ports.
Header	r_cg_port.h
Declaration	void R_PORT_Create(void)
Explanation	• LED lighting control (for LED 1 to LED3): This function configures P53, P62 and P63 as the output ports.
Arguments	• None
Return value	• None
Remarks	None

[Function Name] R_INTC_Create

Synopsis	Initializes the external-interrupt settings.
Header	r_cg_intc.h
Declaration	void R_INTC_Create(void)
Explanation	This function initializes the external-interrupt settings. This function clears the interrupt request.
Arguments	• None
Return value	• None
Remarks	None

[Function Name] R_INTC1_Start

Synopsis	Enables INTP1 interrupts.
Header	r_cg_intc.h
Declaration	void R_INTC1_Start(void)
Explanation	This function clears the interrupt request flag. This function enables INTP1 interrupts and starts taking in the switch input.
Arguments	• None
Return value	• None
Remarks	None

[Function Name] R_INTC1_Interrupt

Synopsis	Processes INTP1 interrupts.
Header	r_cg_intc.h
Declaration	__interrupt void R_INTC1_Interrupt(void)
Explanation	This function processes the INTP1 interrupt when it occurs. This function waits 10 ms and then scans the P50 (SW1 input pin). When the switch is depressed, this function causes the LED indication counter to count up.
Arguments	• None
Return value	• None
Remarks	None

6.6 Flowcharts

Figure 6.2 shows the overall flow of the sample program described in this application note.

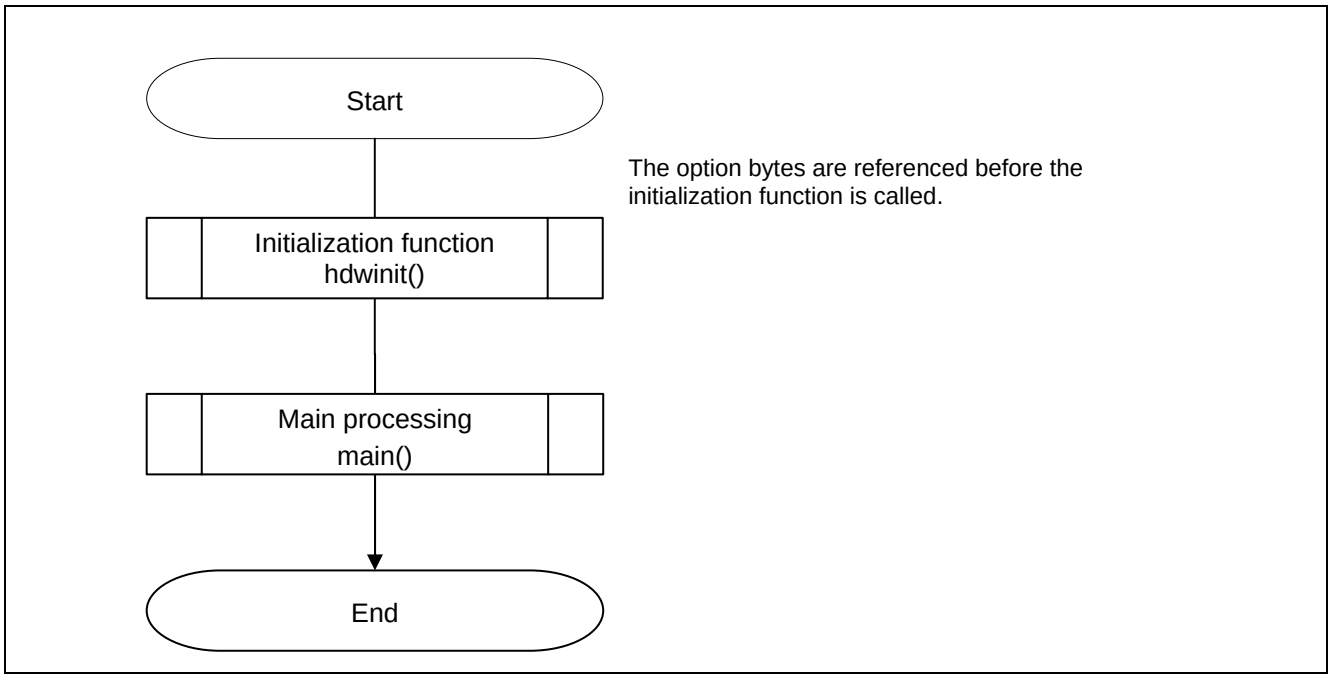


Figure 6.2 Overall Flow

6.6.1 Initialization Function

Figure 6.3 shows the flowchart for the initialization function.

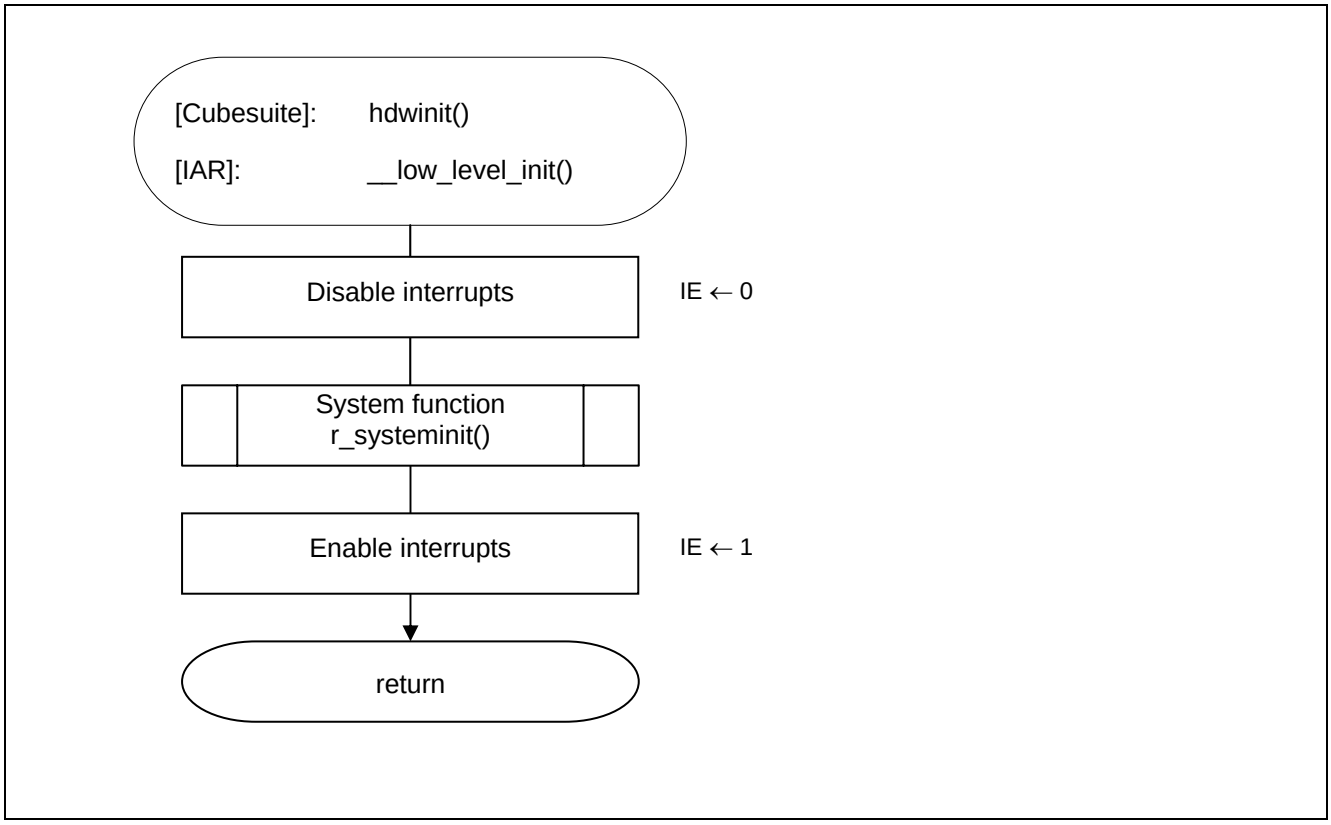


Figure 6.3 Initialization Function

6.6.2 System Function

Figure 6.4 shows the flowchart for the system function.

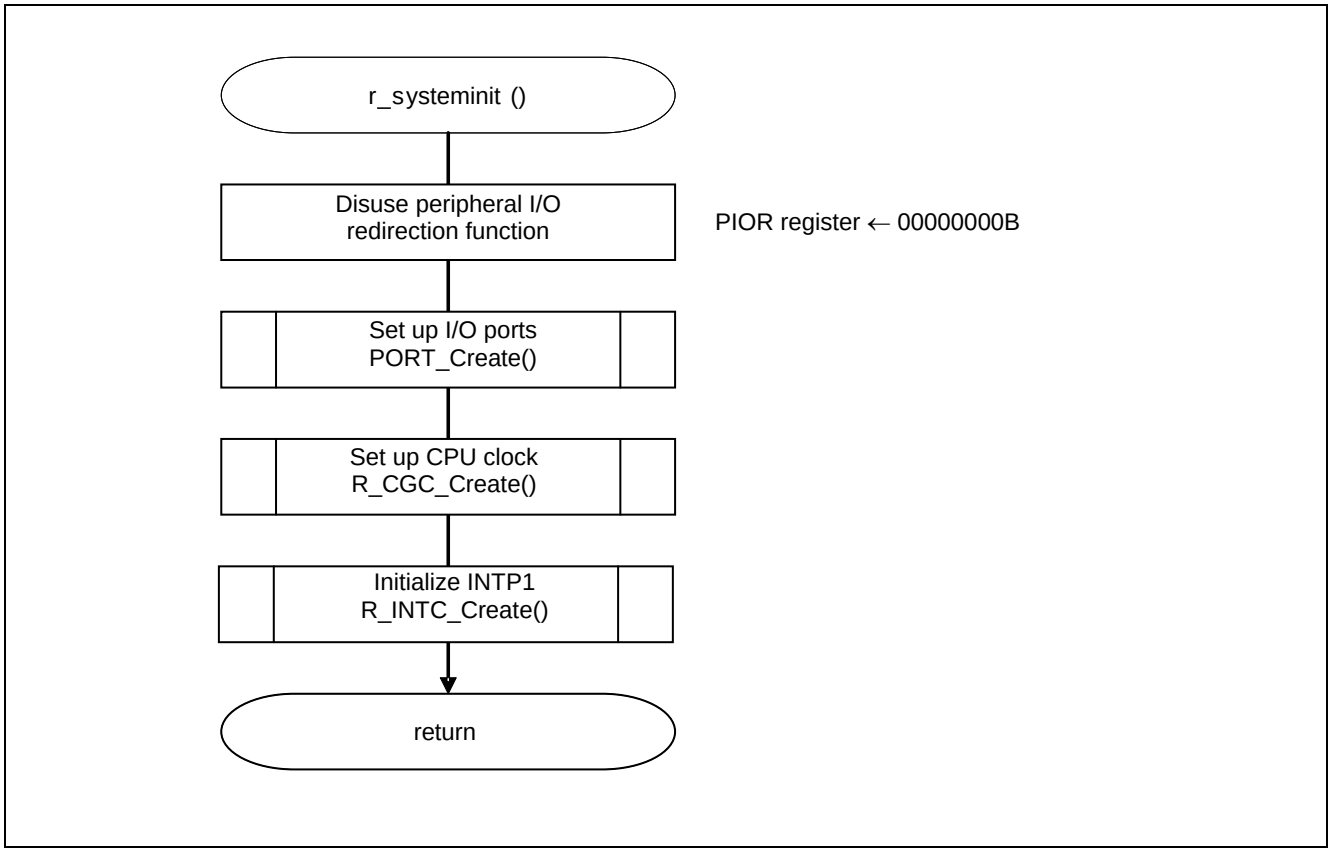


Figure 6.4 System Function

6.6.3 Setting up the I/O Ports

Figure 6.5 shows the flowchart for setting up the I/O ports.

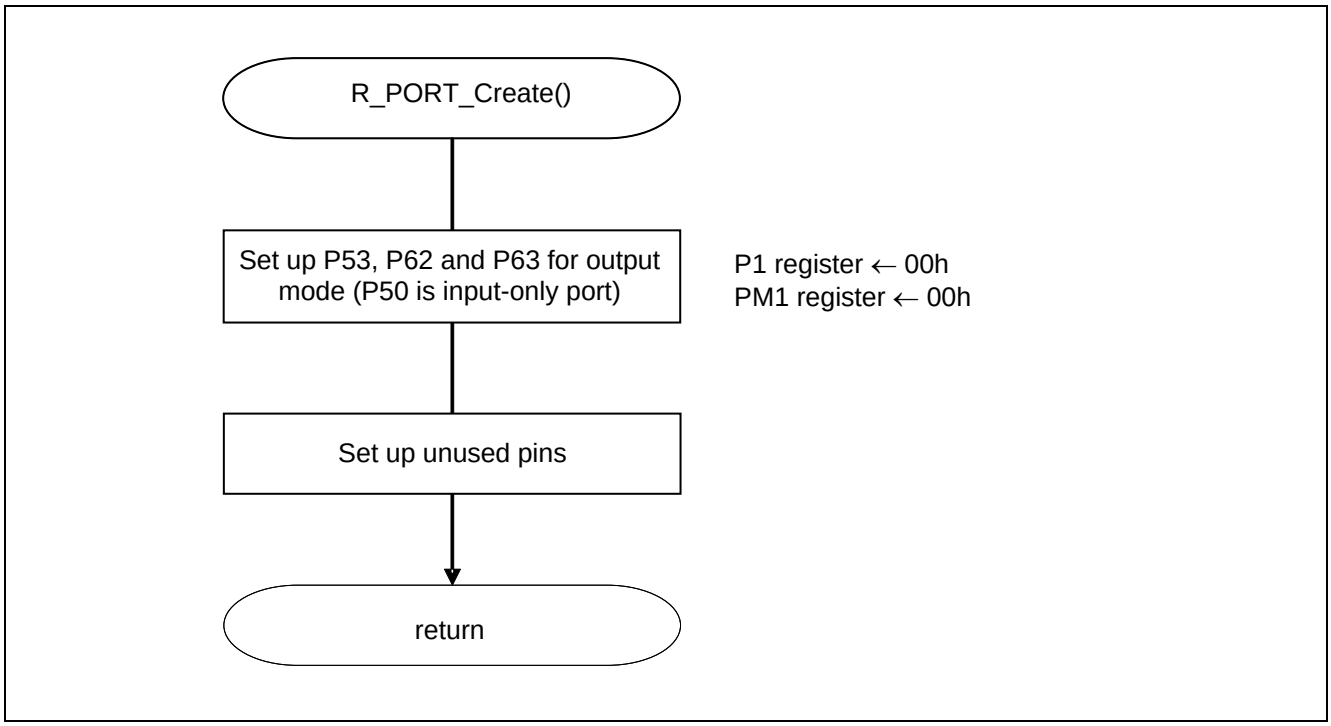


Figure 6.5 I/O Port Setup

Caution: Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN0451EJ0100) for the configuration of the unused ports.

Caution: Provide proper treatment for unused ports so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a resistor.

6.6.4 CPU Clock Setup

Figure 6.6 shows the flowchart for setting up the CPU clock.

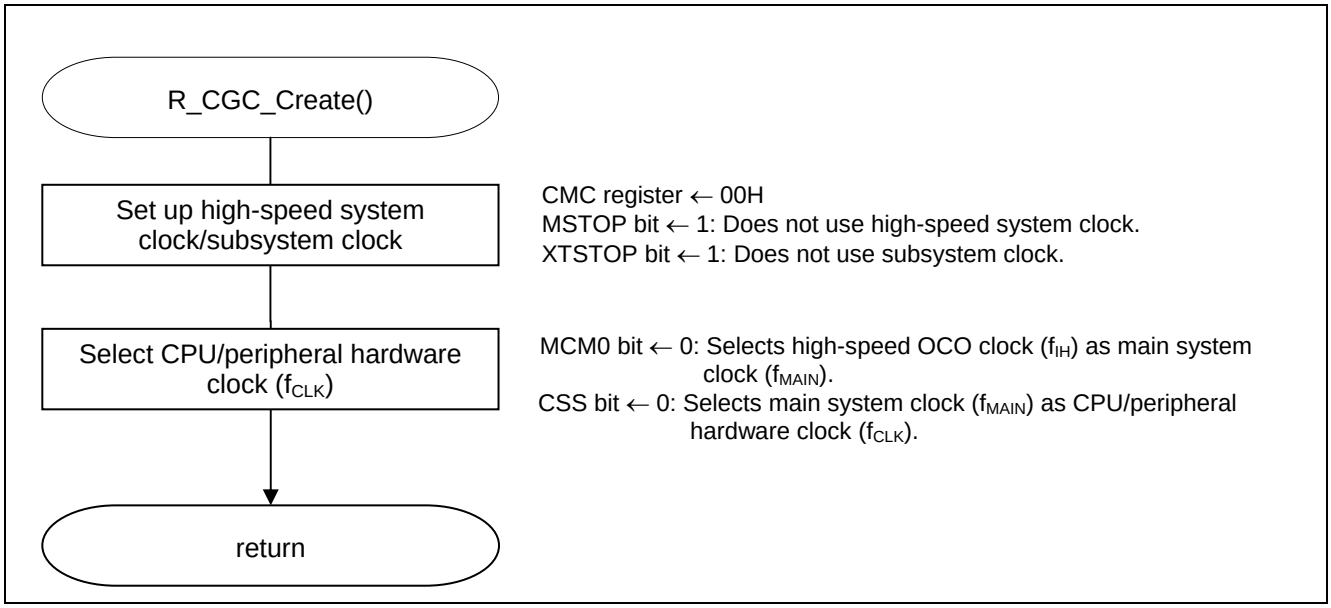


Figure 6.6 CPU Clock Setup

Caution: For details on the procedure for setting up the CPU clock (R_CGC_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN0451EJ0100).

6.6.5 INTP1 Initialization

Figure 6.7 shows the flowchart for INTP1 initialization.

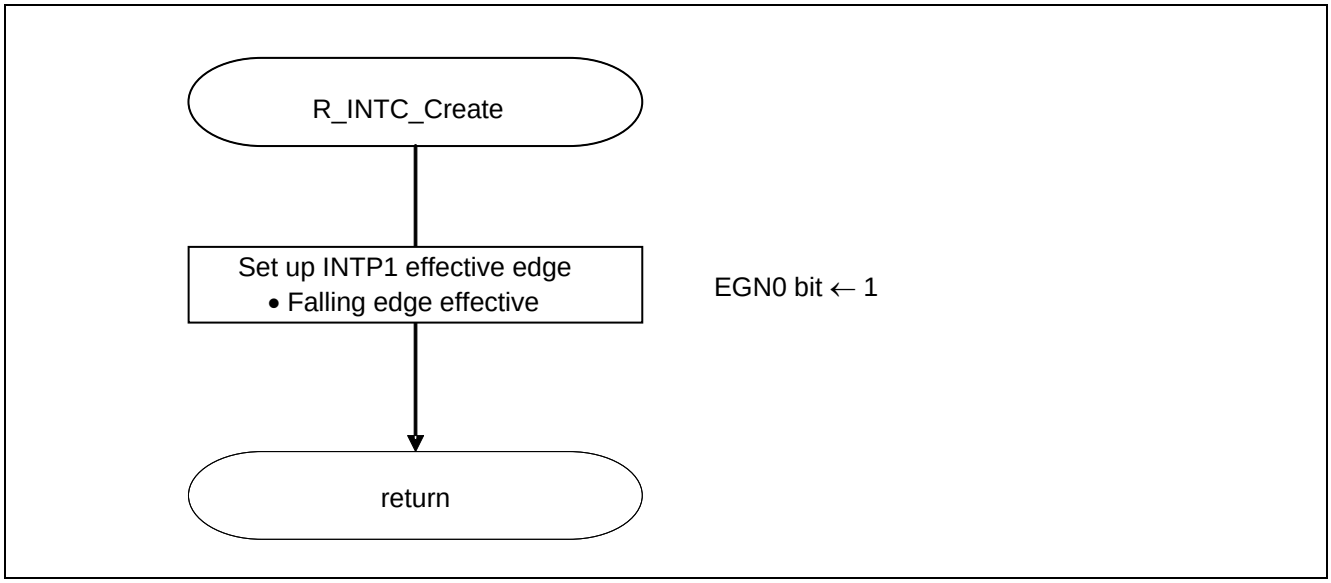


Figure 6.7 INTP1 Initialization

Setup for INTP1 pin edge detection

- External interrupt rising edge enable registers (EGP0, EGP1)
- External interrupt falling edge enable registers (EGN0, EGN1)

These registers are used to set up effective edges for INTP1 to INTP11

Symbol: EGP0

7	6	5	4	3	2	1	0
EGP7	EGP6	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0
x	x	x	x	x	x	x	**0**

Symbol: EGN0

7	6	5	4	3	2	1	0
EGN7	EGN6	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0
x	x	x	x	x	x	x	**1**

Bit 0

EGP0	EGN0	INTP1 pin valid edge selection
0	0	Edge detection disabled
0	**1**	**Falling edge**
1	0	Rising edge
1	1	Both rising and falling edges

Caution: For detailed information about setting the registers, refer to RL78/G13 User's Manual: Hardware.

6.6.6 Main Processing

Figure 6.8 shows the flowchart for main processing.

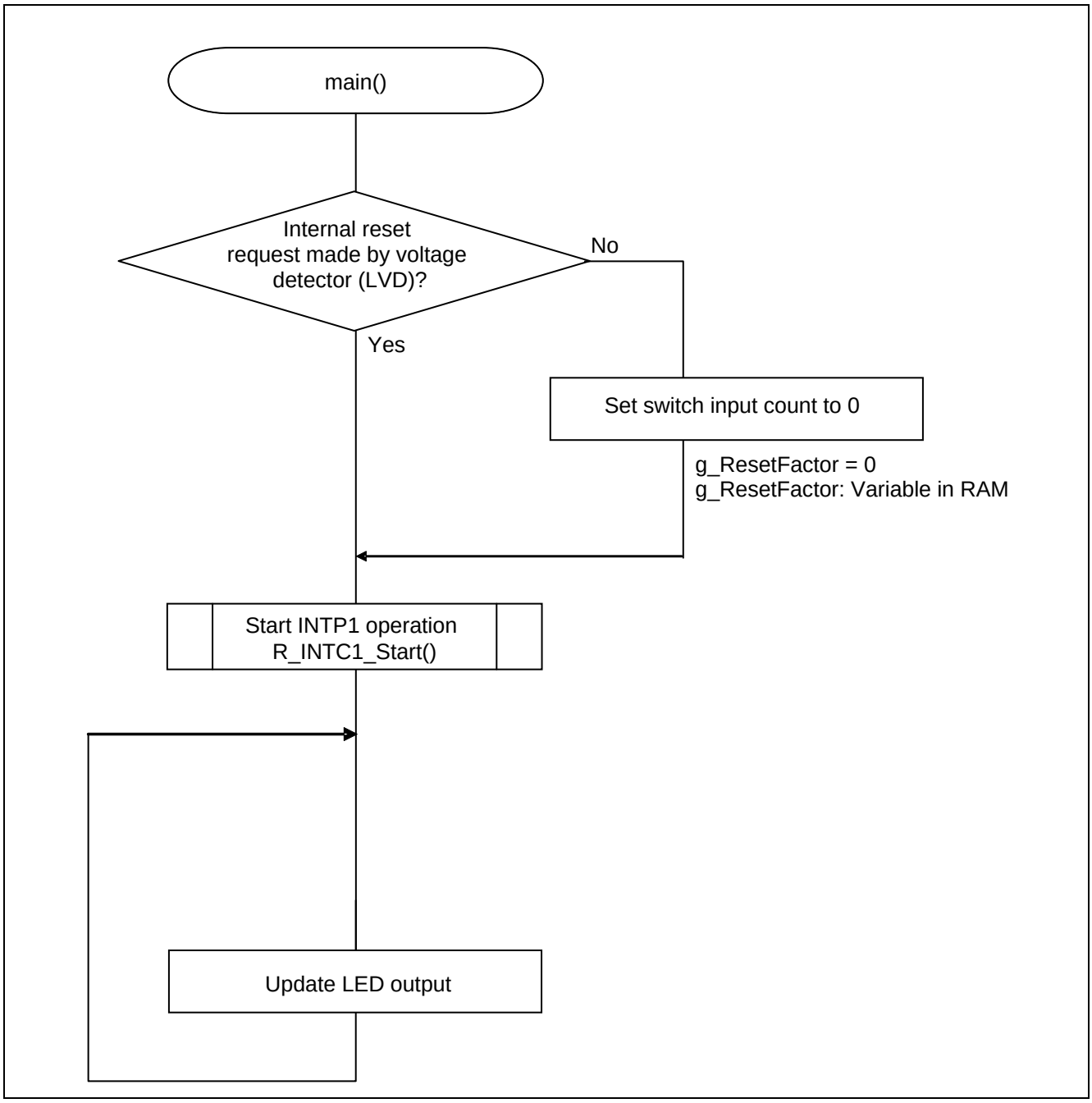


Figure 6.8 Main Processing

6.6.7 INTP1 Operation Start

Figure 6.9 shows the flowchart for starting INTP1 operation.

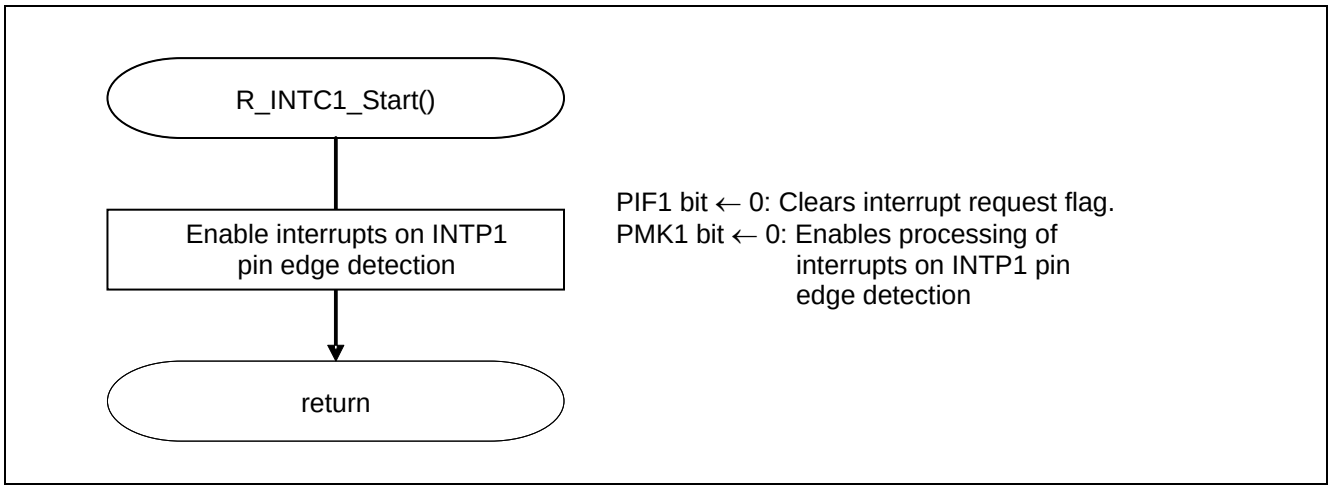


Figure 6.9 INTP1 Operation Start

Setup for INTP1 Interrupts

- Interrupt request flag register (IF1L)
  Clears interrupt request flag.
- Interrupt mask flag register (MK1L)
  Clears interrupt mask.

Symbol: IF0L

7	6	5	4	3	2	1	0
PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF	WDTIIF
x	x	x	x	**0**	x	x	x

Bit 2

PIF1	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request signal is generated, interrupt request status

Symbol: MK0L

7	6	5	4	3	2	1	0
PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK	WDTIMK
x	x	x	x	**0**	x	x	x

Bit 2

PMK1	Interrupt processing control
0	**Interrupt processing enabled**
1	Interrupt processing disabled

Caution: For detailed information about setting the registers, see RL78/G13 User's Manual: Hardware.

6.6.8 INTP1 Interrupt Processing

Figure 6.10 shows the flowchart for INTP1 interrupt processing.

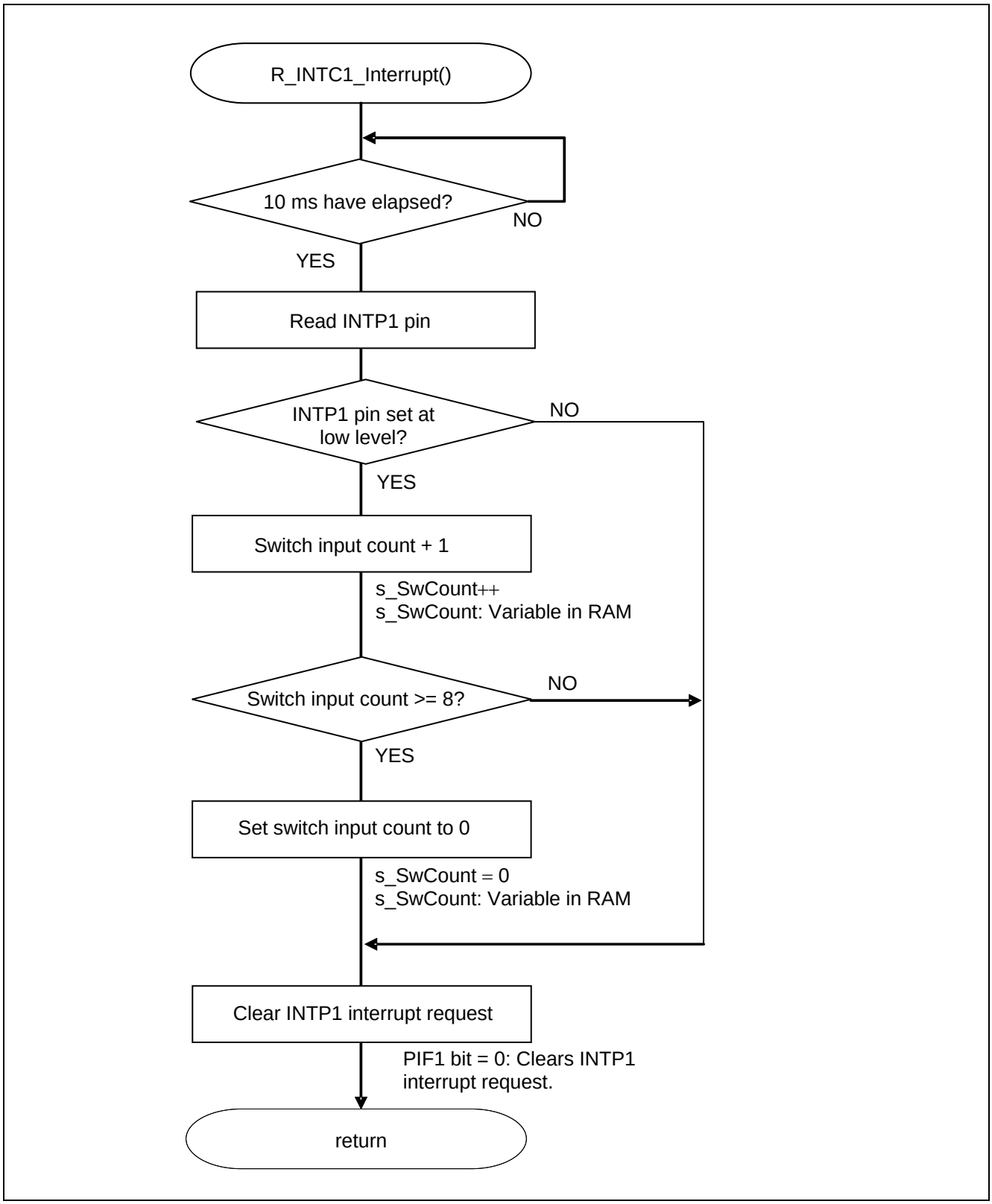


Figure 6.10 INTP1 Interrupt Processing

7. Sample Code

The sample code is available on the Renesas Electronics Website.

8. Documents for Reference

RL78/G13 User's Manual: Hardware Rev.1.00 (R01UH0146EJ0100)

RL78 Family User's Manual: Software Rev.1.00 (R01US0015EJ0100)

RL78/G13 Renesas Starter Kit Users’s Manual Rev.1.00 (R20UT0459EG0100)

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.13.2012		Ported from r01an0453ej0100 First edition issued Ported to RSKRL78/G13 hardware Added support for IAR Updated Document template

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The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
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