

RL78/G10

Timer Array Unit (PWM Output) CC-RL ---

Introduction

This application note describes the PWM output function of the timer array unit (TAU). This unit changes the PWM output duty ratio and inverts the LED indication at 500 ms intervals.

Target Device

RL78/G10

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications	3
2. Operation Check Conditions	5
3. Related Application Note.....	5
4. Description of the Hardware.....	6
4.1 Hardware Configuration Example	6
4.2 List of Pins to be Used	6
5. Description of the Software	7
5.1 Operation Outline	7
5.2 List of Option Byte Settings.....	8
5.3 List of Constant	8
5.4 List of Variables	8
5.5 List of Functions (Subroutines)	8
5.6 Function (Subroutine) Specifications	9
5.7 Flowcharts	10
5.7.1 CPU Initialization Function.....	11
5.7.2 I/O Port Setup	12
5.7.3 Clock Generation Circuit Setup.....	13
5.7.4 Timer Array Unit Setup	14
5.7.5 Main Processing	29
5.7.6 Timer Array Unit Startup	30
5.7.7 INTTM0 Interrupt Processing.....	33
6. Sample Code.....	34
7. Documents for Reference	34

1. Specifications

This application note describes the PWM output function which is realized using channel 0 as the master and channel 1 as the slave in simultaneous channel operation mode. The brightness of the LEDs is controlled by connecting the PWM output to LED2 (for PWM output). Timing signals with fixed cycle time (500 ms) are created by counting the number of timer interrupts (INTTM00) generated by channel 0. Using these timing signals, the duty ratio of the PWM output is changed and the output of LED1 (for updating) is inverted.

Table 1.1 shows the required peripheral function and its use. Figure 1.1 presents an overview of the PWM output operation. Table 1.2 shows the relation between PWM output duty ratios and LED brightnesses. Figure 1.2 is a simplified timing chart which summarizes the PWM output operation.

Table 1.1 Required Peripheral Function and Its Use

Peripheral function	Use
Timer array unit 0	This unit is used to realize the PWM function by operating channel 0 and channel 1 together and deliver a PWM output from the TO01 pin.

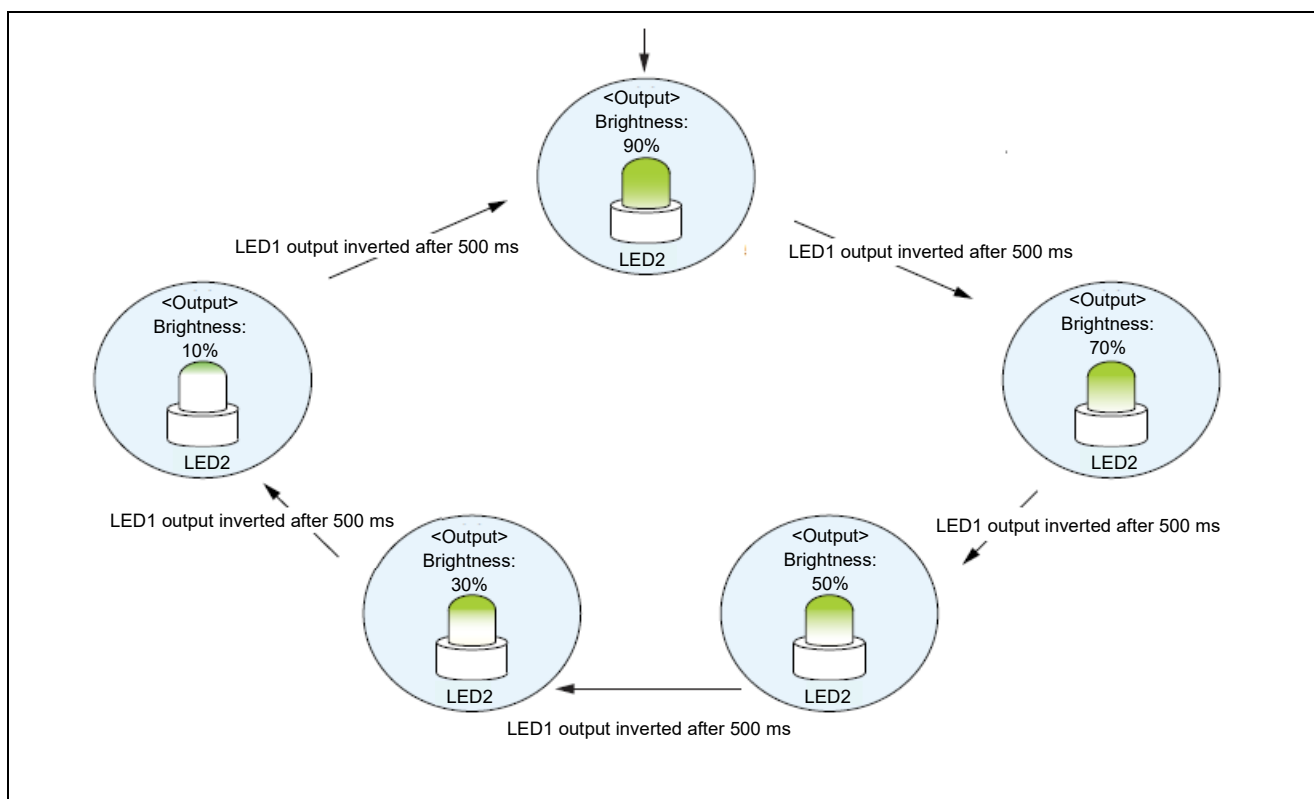


Figure 1.1 Overview of PWM Output Operation

Table 1.2 Relation between PWM Output Duty Ratios and LED Brightnesses

Duty ratio	LED2 brightness
10%	90%
30%	70%
50%	50%
70%	30%
90%	10%

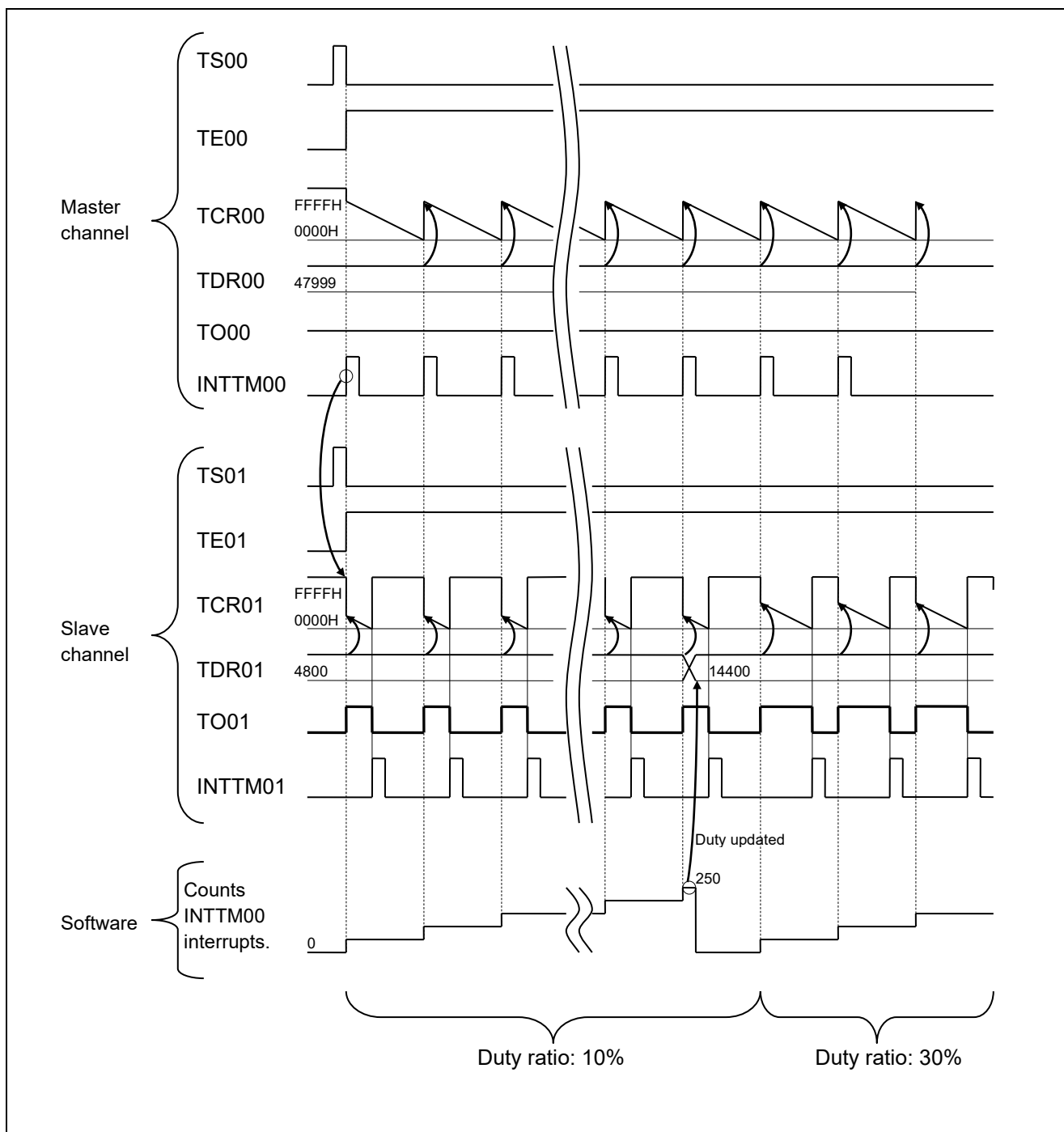


Figure 1.2 Simplified Timing Chart for PWM Output Operation

2. Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G10 (R5F10Y16ASP)
Operating frequency	<ul style="list-style-type: none"> High-speed on-chip oscillator (HOCO) clock: 20 MHz CPU/peripheral hardware clock: 20 MHz
Operating voltage	5.0 V (Operation is possible over a voltage range of 2.9 V to 5.5 V.) SPOR operation: VSPDR=2.82V, VSPOR=2.88V (Reset Occurrence: VDD<2.82V, Reset Release: 2.88V)
Integrated development environment (CS+)	CS+ for CC V3.01.00 from Renesas Electronics Corp.
Assembler (CS+)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (e ² studio)	e ² studio V4.0.2.008 from Renesas Electronics Corp.
Assembler (e ² studio)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.3 from IAR Systems.
Assembler (IAR)	IAR Assembler for Renesas RL78 V4.21.2.2420 from IAR Systems.
Board to be used	RL78/G10 target board (QB-R5F10Y16-TB)

3. Related Application Note

The application notes that are related to this application note are listed below for reference.

RL78/G10 Initialization (R01AN2668E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration used for this application note.

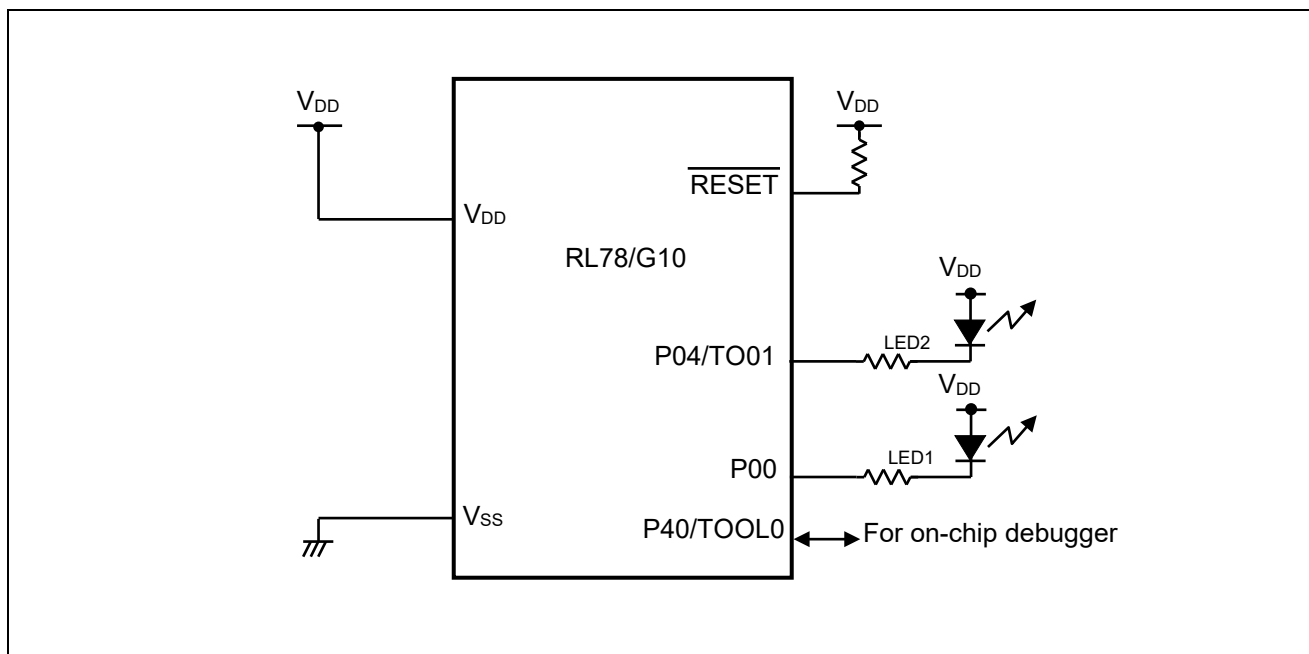


Figure 4.1 Hardware Configuration

- Cautions:
1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).
 2. V_{DD} must supply not lower than the reset release voltage (V_{SPOR}) that is specified as SPOR..

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their functions.

Table 4.1 Pins to be Used and Their Functions

Pin Name	I/O	Description
P04/TO01	Output	PWM outputport
P00	Output	Output port for LED1 indications

5. Description of the Software

5.1 Operation Outline

The sample program covered in this application note implements PWM by operating channel 0 and channel 1 together, and delivers a PWM output from P04/TO01.

Also, this program detects 250 timer interrupts (INTTM00) with 2-ms cycle time which are generated by channel 0. Then, it changes the PWM output duty ratio and inverts the LED indication at 500 ms intervals.

(1) Initialize the TAU.

<Conditions for setting>

- Set the P04/TO01 pin to a PWM output.
- Set TAU0 channel 0 to 2-ms cycle interval timer mode. ^{Note 1}
- Set TAU0 channel 1 to one-count mode.
- Initialize the duty ratio of the PWM output to 10 %. ^{Note 2}
- Use timer interrupts (INTTM00) from timer channel 0.

(2) Operation starts when both the operation enable trigger bits for TAU0 channel 0 and channel 1 are set to 1 simultaneously. The sample program executes a HALT instruction to wait for a timer interrupt (INTTM00) from channel 0.

(3) After the start of timer operation, channel 0 generates a timer interrupt (INTTM00) at 2 ms intervals.

(4) When the HALT mode is canceled by a timer interrupt (INTTM00) from channel 0, the sample program starts counting the number of INTTM00 interrupts generated. After channel 0 has generated 250 timer interrupts (i.e., after 500 ms), the sample program updates the channel 1 count value and changes the duty ratio. This duty ratio is increased from 10% to 90% (10% → 30% → 50% → 70% → 90%). It is incremented by 20% each time the number of channel 0 timer interrupts (INTTM00) generated reaches 250 ^{Note 3}. (Thus, it is incremented at 500 ms intervals) It is reset to 10% after the duty ratio to be set next exceeds 100%. ^{Note 2}

(5) After processing timer interrupts (INTTM00) from channel 0, the sample program executes another HALT instruction and waits for the next timer interrupt (INTTM00) from channel 0.

Notes. 1: Constant INTERVAL is defined as 2 (ms) at initial setting (r_init.asm).

2. Constant INITIAL is defined as 10 (%) at initial setting (r_init.asm).

3. Constant INCREMENT is defined as 20 (%) at initial setting (r_init.asm).

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H	01111111B	SPOR detection voltage When reset occurs: $V_{DD} < 2.82\text{ V}$ When reset is released: $V_{DD} \geq 2.88\text{ V}$
000C2H	11100000B	HS mode, HOCO: 20 MHz
000C3H	10000101B	Enables the on-chip debugger.

5.3 List of Constant

Table 5.2 lists the constants that are used in this sample program.

Table 5.2 Constant for the Sample Program

Constant	Setting	Description
INTERVAL	2	Cycle of PWM output in units of ms
INITIAL	10	Duty ratio of PWM in units of percent
INCREMENT	20	Increment in duty ratio of PWM in units of percent
PERIOD	$24000 * \text{INTERVAL}$	Number of clocks corresponding to duty ratio of PWM
INCDATA	$(\text{PERIOD} / 100) * \text{INCREMENT}$	Number of clocks corresponding to increment in duty ratio of PWM
INITDATA	$(\text{PERIOD} / 100) * \text{INITIAL}$	TDR01 setting for a 10% duty ratio

5.4 List of Variables

Table 5.3 lists the variables that are used in this sample program.

Table 5.3 Variables for the Sample Program

Variable Name	Outline
RTMCNT	Used to detect an elapse of 500 ms by counting occurrence of INTTM00 at an interval of 2 ms

5.5 List of Functions (Subroutines)

Table 5.4 lists the functions (subroutines) that are used in this sample program.

Table 5.4 Functions (Subroutines)

Function	Outline
SSTARTPWM	Timer array unit start processing
INTTM00	TAU0 channel 0 timer interrupt processing

5.6 Function (Subroutine) Specifications

This section describes the specifications for the functions that are used in this sample program.

[Function Name] SSTARTPWM

Synopsis	TAU0 channel 0 start processing
Explanation	This function starts count operation of channels 0 and 1 and unmask TAU0 channel 0 interrupts.
Arguments	None
Return value	None
Remarks	None

[Function Name] INTTM00

Synopsis	Channel 0 timer interrupt processing
Explanation	This function counts the number of INTTM00 interrupts generated. Each time the count reaches 250, it updates the duty ratio of a PWM output. (Thus, it updates the duty ratio at 500-ms intervals)
Arguments	None
Return value	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

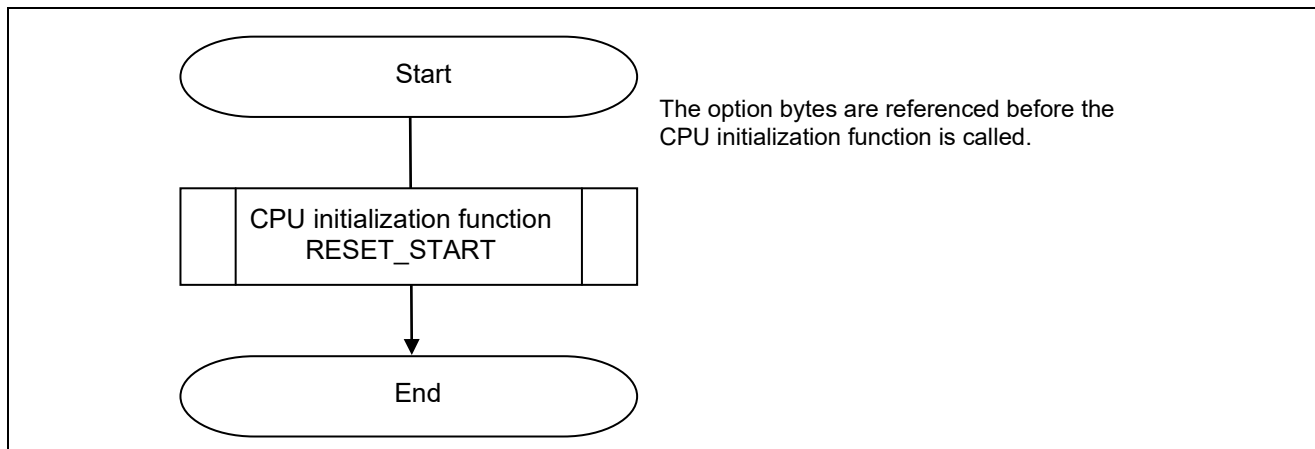


Figure 5.1 Overall Flow

5.7.1 CPU Initialization Function

Figure 5.2 shows the flowchart for the CPU initialization function.

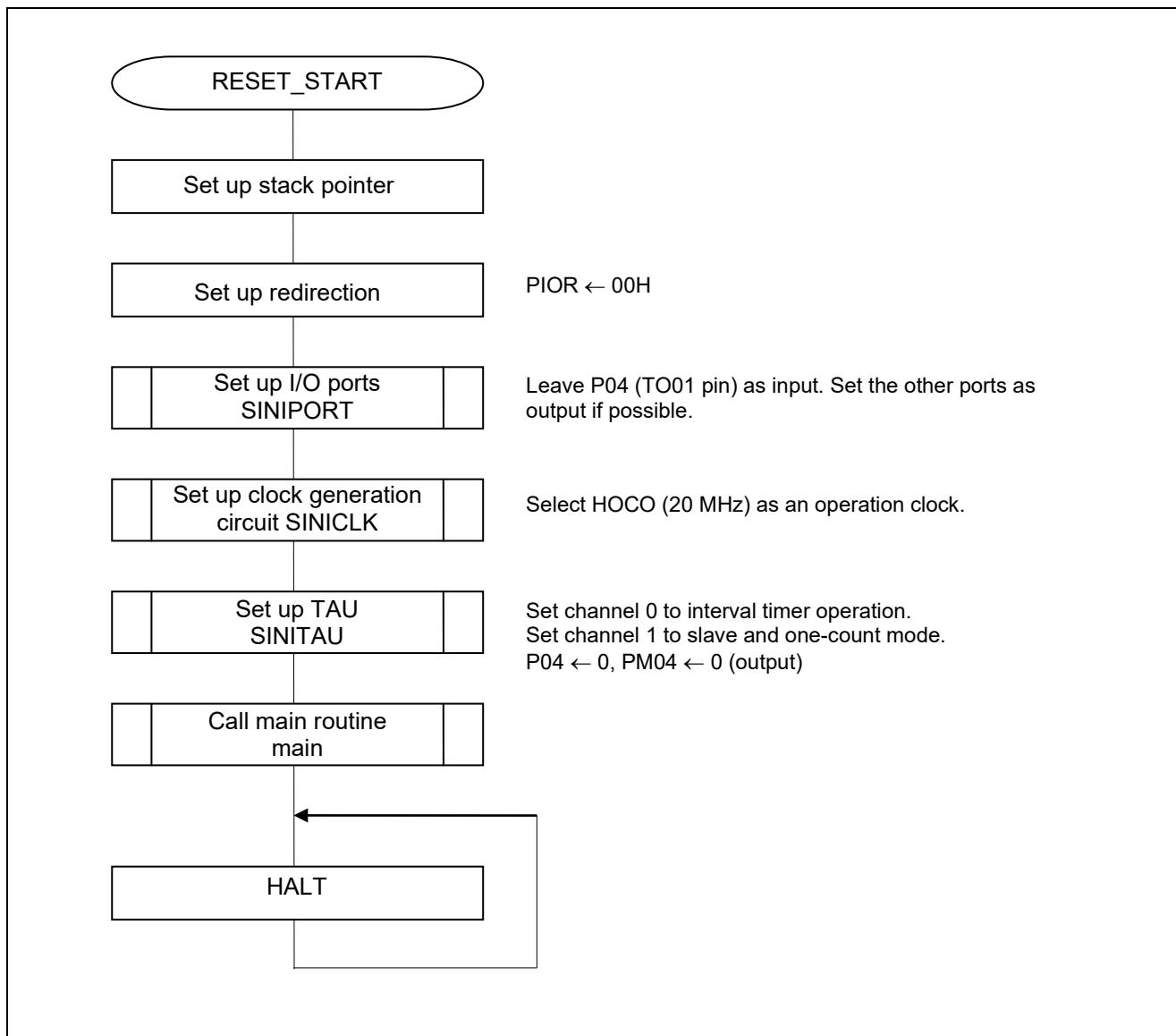


Figure 5.2 CPU Initialization Function

5.7.2 I/O Port Setup

Figure 5.3 shows the flowchart for setting up the I/O ports.

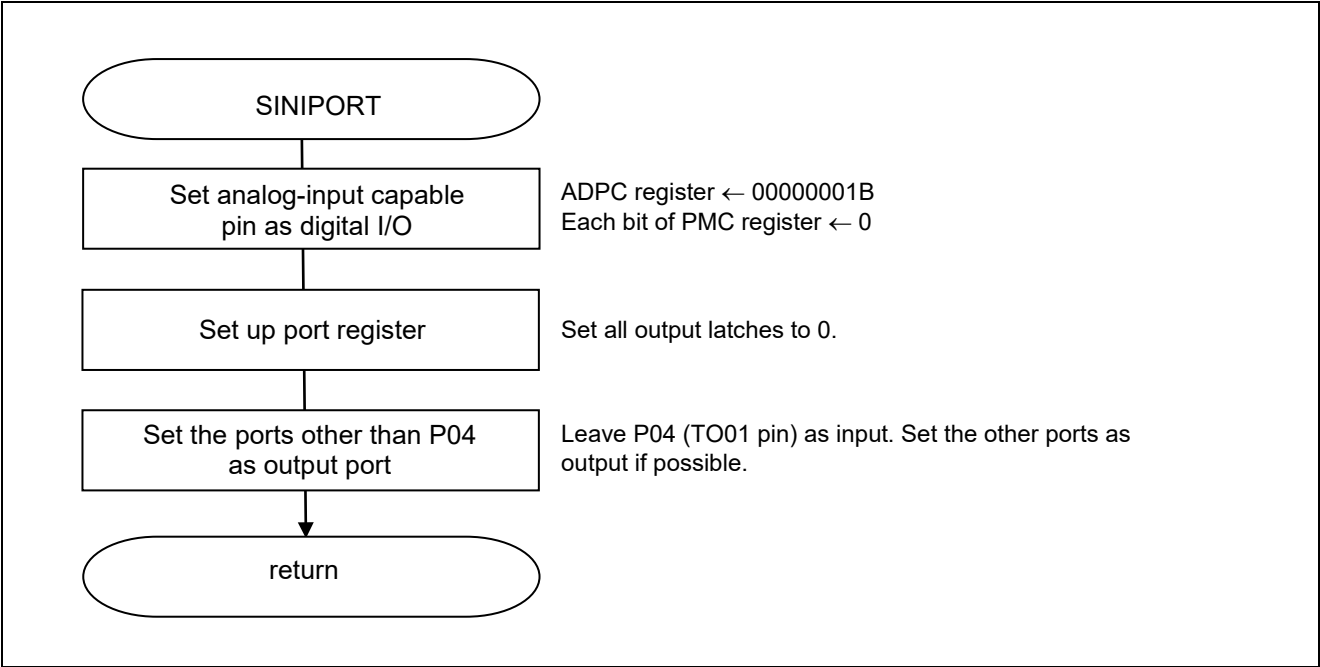


Figure 5.3 I/O Port Setup

Note: Refer to the section entitled "Flowcharts" in RL78/G10 Initialization Application Note (R01AN1454E) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

Setting up the LED pin to indicate updating of the duty ratio

- Port mode register (PM0)

Select I/O mode for PM00.

Symbol: PM0

7	6	5	4	3	2	1	0
1	PM06 ^{Note}	PM05 ^{Note}	PM04 ^{Note}	PM03 ^{Note}	PM02 ^{Note}	PM01 ^{Note}	PM00 ^{Note}
x	x	x	x	x	x	x	0

Bit 0

PM10	PM10 I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Note: 16-pin products only

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

5.7.3 Clock Generation Circuit Setup

Figure 5.4 shows the flowchart for clock generation circuit setup.

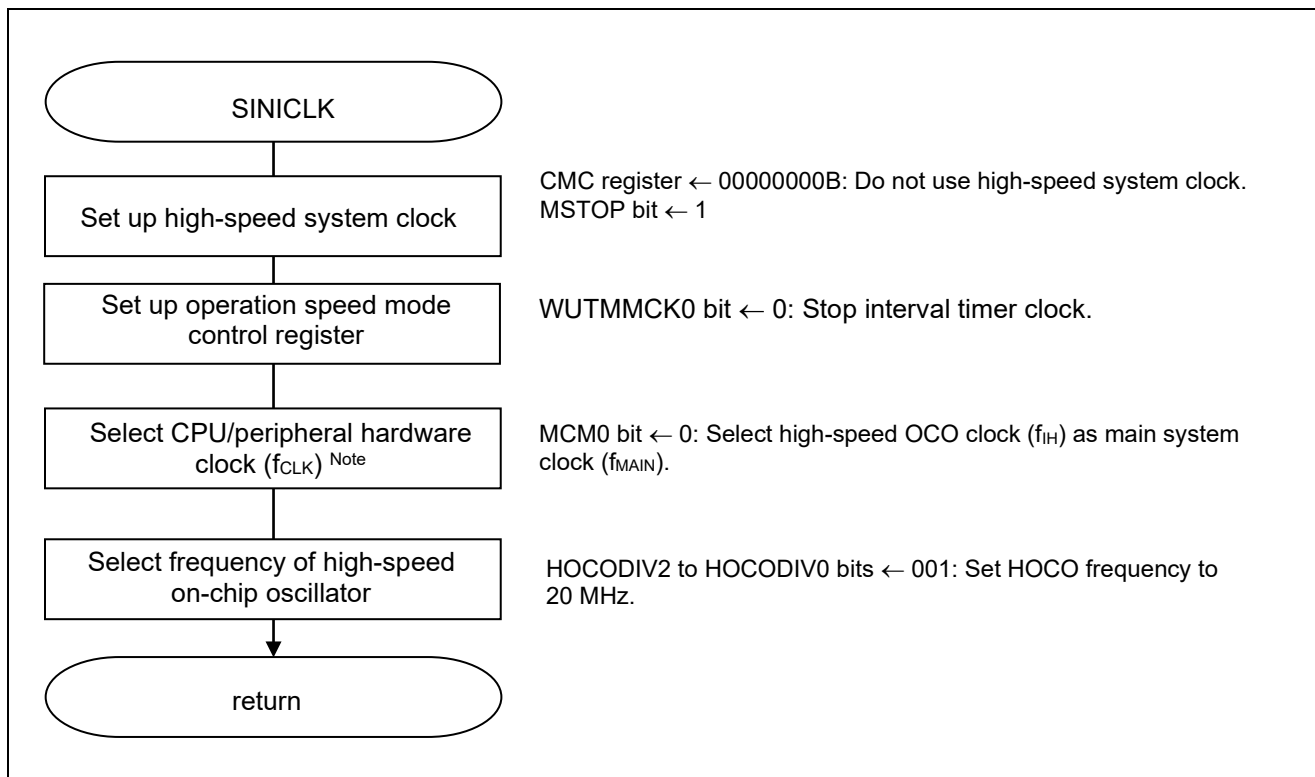


Figure 5.4 Clock Generation Circuit Setup

Note: 16-pin products only

Caution: For details on the procedure for setting up the clock generation circuit (SINICK), refer to the section entitled "Flowcharts" in RL78/G10 Initialization Application Note (R01AN2668E).

5.7.4 Timer Array Unit Setup

Figure 5.5 shows the flowcharts for setting up the timer array unit.

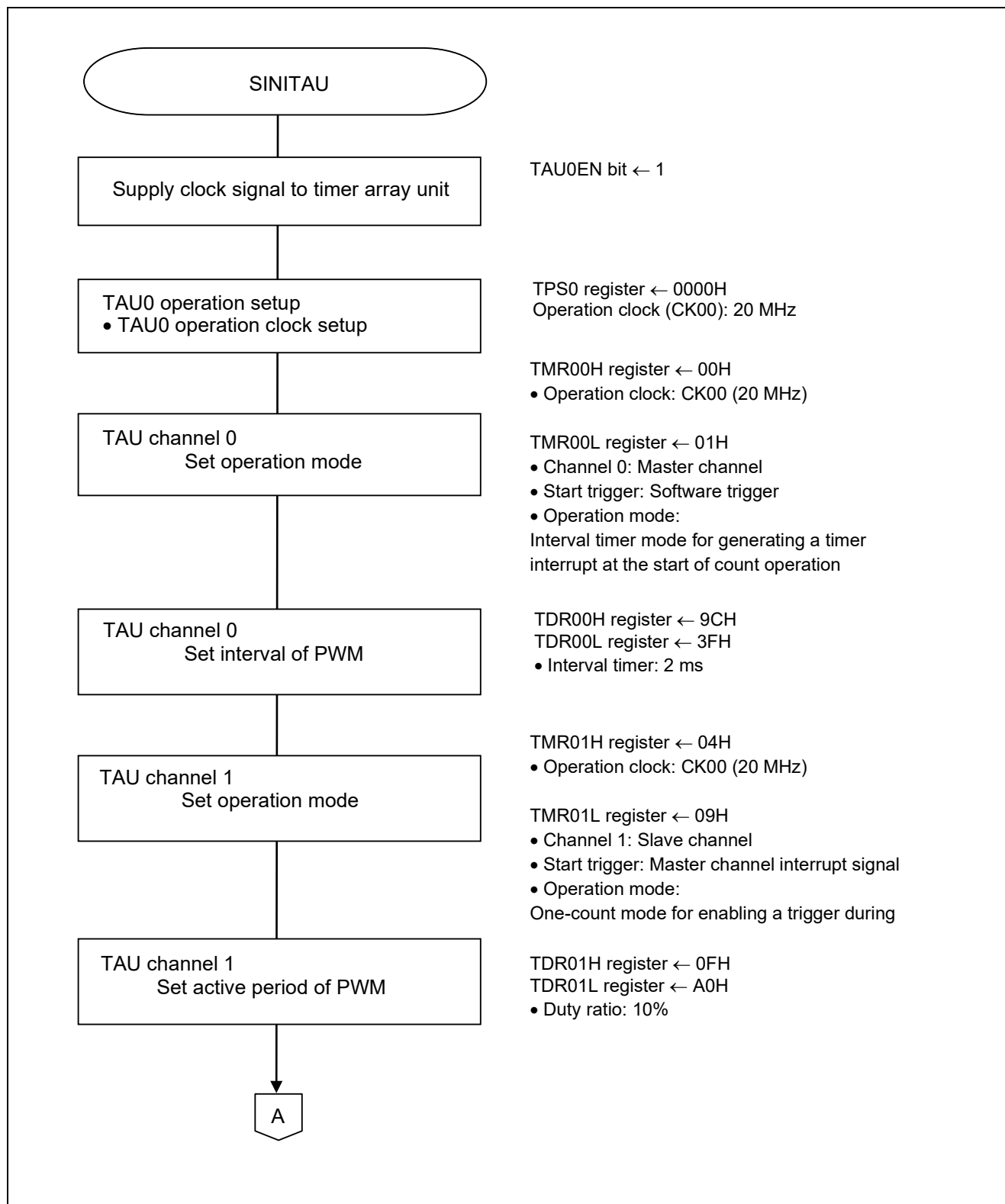


Figure 5.5 Timer Array Unit Setup (1/2)

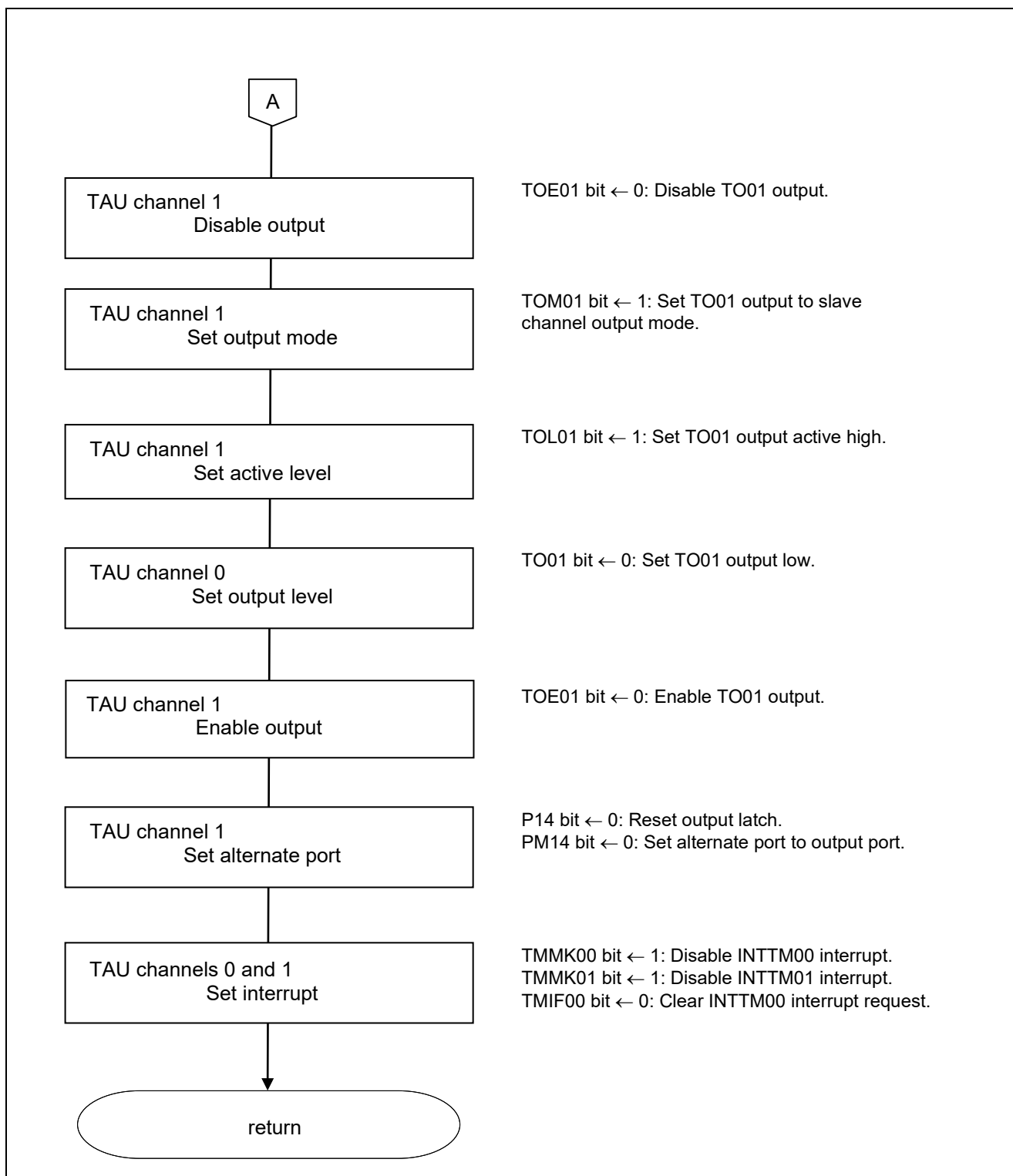


Figure 5.5 Timer Array Unit Setup (2/2)

Starting clock signal supply to the timer array unit 0

- Peripheral enable register 0 (PER0)
Start clock signal supply to the timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAE ^{Note}	0	ADCEN	IICA0EN ^{Note}	0	SAU0EN	0	TAU0EN
x	0	x	X	0	x	0	1

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply.
1	Enables input clock supply.

Note: 16-pin products only

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Setting up the timer clock frequency

- Timer clock select register 0 (TPS0)
Select the operation clock of the Time Array Unit 0.

Symbol: TPS0

7	6	5	4	3	2	1	0
PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
0	0	0	0	0	0	1	0

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000	Selection of operation clock (CK00)					
					f_{CLK} = 1.25MHz	f_{CLK} = 2.5MHz	f_{CLK} = 5MHz	f_{CLK} = 10MHz	f_{CLK} = 20MHz
0	0	0	0	f_{CLK}	1.25MHz	2.5MHz	5MHz	10MHz	20MHz
0	0	0	1	$f_{CLK}/2$	625kHz	1.25MHz	2.5MHz	5MHz	10MHz
0	0	1	0	$f_{CLK}/2^2$	313kHz	625kHz	1.25MHz	2.5MHz	5MHz
0	0	1	1	$f_{CLK}/2^3$	156kHz	313kHz	625kHz	1.25MHz	2.5MHz
0	1	0	0	$f_{CLK}/2^4$	78kHz	156kHz	313kHz	625kHz	1.25MHz
0	1	0	1	$f_{CLK}/2^5$	39kHz	78kHz	156kHz	313kHz	625kHz
0	1	1	0	$f_{CLK}/2^6$	19.5kHz	39kHz	78kHz	156kHz	313kHz
0	1	1	1	$f_{CLK}/2^7$	9.8kHz	19.5kHz	39kHz	78kHz	156kHz
1	0	0	0	$f_{CLK}/2^8$	4.9kHz	9.8kHz	19.5kHz	39kHz	78kHz
1	0	0	1	$f_{CLK}/2^9$	2.5kHz	4.9kHz	9.8kHz	19.5kHz	39kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.22kHz	2.5kHz	4.9kHz	9.8kHz	19.5kHz
1	0	1	1	$f_{CLK}/2^{11}$	625Hz	1.22kHz	2.5kHz	4.9kHz	9.8kHz
1	1	0	0	$f_{CLK}/2^{12}$	313Hz	625Hz	1.22kHz	2.5kHz	4.9kHz
1	1	0	1	$f_{CLK}/2^{13}$	152Hz	313Hz	625Hz	1.22kHz	2.5kHz
1	1	1	0	$f_{CLK}/2^{14}$	78Hz	152Hz	313Hz	625Hz	1.22kHz
1	1	1	1	$f_{CLK}/2^{15}$	39Hz	78Hz	152Hz	313Hz	625Hz

Note: 16-pin products only

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Setting up the channel 0 operation mode

- Timer mode register 00 (TMR00H, TMR00L)

Select an operation clock (f_{MCK}).

Select a count clock.

Select a start trigger and capture trigger.

Select a valid edge for timer input.

Set up the operation mode.

Symbol: TMR00H

7	6	5	4	3	2	1	0
CKS001	0	0	CCS00	0	STS002	STS001	STS000
0	0	0	0	0	0	0	0

Bits 7

CKS001	Selection of operation clock (f_{MCK}) of channel 0
0	Operation clock CK00 set by timer clock select register 0 (TPS0)
1	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	Operation clock CK01 set by timer clock select register 0 (TPS0)

Bit 4

CCS00	Selection of count clock (f_{CLK}) of channel 0
0	Operation clock (f_{MCK}) specified by the CKSmn0 and CKSmn1 bits
1	Valid edge of input signal input from the TI00 pin

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Bit 2-0

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Symbol: TMR00L

7	6	5	4	3	2	1	0
CIS001	CIS000	0	0	MD003	MD002	MD001	MD000
0	0	0	0	0	0	0	1

Bits 3-0

MD 003	MD 002	MD 001	MD 000	Operation mode of channel 0	Related function	TCR counting operation
0	0	0	1/0	Interval timer mode	Interval timer / Square wave output / Divider function / PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The MD000 bit operation varies depending on the operation mode (see the table below)

Operation mode (Value set by the MD003 to MD001 bits) (see table above)	MD000	TCR counting operation
<ul style="list-style-type: none"> Interval timer mode (0, 0, 0) Capture mode (0, 1, 0) 	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated, either.
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Setting up the PWM output pulse cycle time

- Timer data register 00 (TDR00)
Configure the PWM output pulse cycle time.

Symbol: TDR00H, TDR00L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Pulse cycle time = (TDR00 setting + 1) x Count clock cycle time
2 [ms] = (1/20[MHz]) x (TDR00 setting + 1)

⇒ TDR00 setting = 39999

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Setting up the channel 1 operation mode

- Timer mode register 01 (TMR01H, TMR01L)
 Select an operation clock (f_{MCK}).
 Select a count clock.
 Select the 16/8-bit timer.
 Select a start trigger and capture trigger.
 Select a valid edge for timer input.
 Set up the operation mode.

Symbol: TMR01H, TMR01L

7	6	5	4	3	2	1	0
CKS011	0	0	CCS01	SPLIT01	STS012	STS011	STS010
0	0	0	0	0	1	0	0

Bits 7

CKS011	Channel 1 operation clock (f_{MCK}) selection
0	Operation clock CK00 set by timer clock select register 0 (TPS0)
1	Operation clock CK01 set by timer clock select register 0 (TPS0)

Bit 4

CCS01	Selection of count clock (f_{CLK}) of channel 1
0	Operation clock (f_{MCK}) specified with the CKS011 bit
1	Valid edge of the input signal from the TI01 pin

Bit 3

SPLIT01	Selection of 8 or 16-bit timer operation for channel 1
0	Operates as 16-bit timer (Operates in independent channel operation function or as slave channel in simultaneous channel operation function.)
1	Operates as 8-bit timer.

Bits 2-0

STS012	STS011	STS010	Setting of start trigger or capture trigger of channel 1
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TI01 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI01 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Others than above			Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Symbol: TMR01L

7	6	5	4	3	2	1	0
CIS011	CIS010	0	0	MD013	MD012	MD011	MD010
0	0	0	0	1	0	0	1

Bits 3 to 0

MD013	MD012	MD011	MD010	Operation mode of channel 1	Related function	TCR counting operation
0	0	0	1/0	Interval timer mode	Interval timer / Square wave output / Divider function / PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The MD010 bit operation varies depending on the operation mode (see the table below)

Operation mode (Value set by the MD013 to MD011 bits) (see table above)	MD010	TCR counting operation
<ul style="list-style-type: none"> Interval timer mode (0, 0, 0) Capture mode (0, 1, 0) 	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
<ul style="list-style-type: none"> Event counter mode (0, 1, 1) 	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
<ul style="list-style-type: none"> One-count mode (1, 0, 0) 	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
<ul style="list-style-type: none"> Capture & one-count mode (1, 1, 0) 	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated, either.
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Configuring the PWM output duty ratio

- Timer data register 01 (TDR01H, TDR01L)
Configure the PWM output duty ratio.

Symbol: TDR01H, TDR01L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Duty ratio = (TDR01 setting)/(TDR00 setting + 1) x 100
10 [%] = (TDR01 setting)/(63999 + 1) x 100

⇒ TDR01 setting = 4000

Setting up the timer output mode

- Timer output mode register 0 (TOM0)
Set up the timer output mode for each channel.

Symbol: TOM0

7	6	5	4	3	2	1	0
0	0	0	0	TOM 03Note	TOM 02Note	TOM 01	0
0	0	0	0	x	x	1	0

Bit 1

TOM01	Channel 1 timer output mode control
0	Master channel output mode. (Output is toggled with the timer interrupt request signal (INTTM01).)
1	Slave channel output mode. (Output is set with the master channel's timer interrupt request signal (INTTM01) and reset with the slave channel's timer interrupt request signal (INTTM0p).)

Note: 16-pin products only

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Configuring the output level for the timer output pin

- Timer output level register 0 (TOL0)
Configure the output level for the timer output pin for each channel.

Symbol: TOL0

7	6	5	4	3	2	1	0
0	0	0	0	TO ₀₃ ^{Note}	TO ₀₂ ^{Note}	TO ₀₁	TO ₀₀
0	0	0	0	x	x	0	x

Bit 1

TOL01	Channel 1 timer output level control
0	Positive logic output (active-high)
1	Negative logic output (active-low)

Note: 16-pin products only

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Configuring the output value for the timer output pin

- Timer output register 0 (TO0)

Configure the output value for the timer output pin for each channel.

Symbol: TO0

7	6	5	4	3	2	1	0
0	0	0	0	TO 03 <small>Note</small>	TO 02 <small>Note</small>	TO 01	TO 00
0	0	0	0	x	x	0	x

Bit 1

TO01	Channel 1 timer output
0	Timer output value is 0
1	Timer output value is 1

Note: 16-pin products only

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Enabling the timer output

- Timer output enable register 0 (TOE0)

Enable/disable the timer output for each channel.

Symbol: TOE0

7	6	5	4	3	2	1	0
0	0	0	0	TOE0 ₃ Note	TOE0 ₂ Note	TOE0 ₁	TOE0 ₀
0	0	0	0	x	x	1	0

Bit 1

TOE01	Timer output enable/disable of channel 1
0	The TO01 operation stopped by count operation (timer channel output bit). Writing to the TO01 bit is enabled. The TO01 pin functions as data output, and it outputs the level set to the TO01 bit. The output level of the TO01 pin can be manipulated be software.
1	The TO01 operation enabled by count operation (timer channel output bit). Writing to the TO01 bit is disabled (writing is ignored). The TO01 pin functions as timer output, and the TOE01 bit is set or reset depending on the timer operation. The TO01 pin outputs the square-wave or PWM depending on the timer operation.

Bit 0

TOE00	Timer output enable/disable of channel 0
0	The TO00 operation stopped by count operation (timer channel output bit). Writing to the TO00 bit is enabled. The TO00 pin functions as data output, and it outputs the level set to the TO00 bit. The output level of the TO00 pin can be manipulated be software.
1	The TO00 operation enabled by count operation (timer channel output bit). Writing to the TO00 bit is disabled (writing is ignored). The TO00 pin functions as timer output, and the TOE00 bit is set or reset depending on the timer operation. The TO00 pin outputs the square-wave or PWM depending on the timer operation.

Note: 16-pin products only

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Setting up the PWM output pin

- Port mode register (P0)
Select the PM04 output latch.
- Port mode register (PM0)
Select the PM04 I/O mode.

Symbol: P0

7	6	5	4	3	2	1	0
1	P06 ^{Note}	P05 ^{Note}	P04	P03	P02	P01	P00
1	x	x	0	x	x	x	x

Bit 4

P04	P14 I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Symbol: PM0

7	6	5	4	3	2	1	0
1	PM06 ^{Note}	PM05 ^{Note}	PM04	PM03	PM02	PM01	PM00
1	x	x	0	x	x	x	x

Bit 4

PM14 ^{Note 2}	PM14 I/O mode selection ^{Note 2}
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Note: 16-pin products only

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Configuring the timer count end interrupts

- Interrupt request flag register (IF0L)
Clear the interrupt request flag.
- Interrupt mask flag register (MK0L)
Mask interrupts.

Symbol: IF0L

7	6	5	4	3	2	1	0
TMIF00	TMIF01H	SREIF0	SRIF0	STIF0 CSIF00 IICIF00	PIF1	PIF0	WDTIIF
0	x	x	x	x	x	x	x

Bit 7

TMIF00	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Symbol: MK0L

7	6	5	4	3	2	1	0
TMMK00	TMMK01H	SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	PMK1	PMK0	WDTIMK
0	x	x	x	x	x	x	x

Bits 7 and 6

TMMK00	Interrupt processing control
0	Enables interrupt processing.
1	Disables interrupt processing.

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

5.7.5 Main Processing

Figure 5.6 shows the flowchart for main processing.

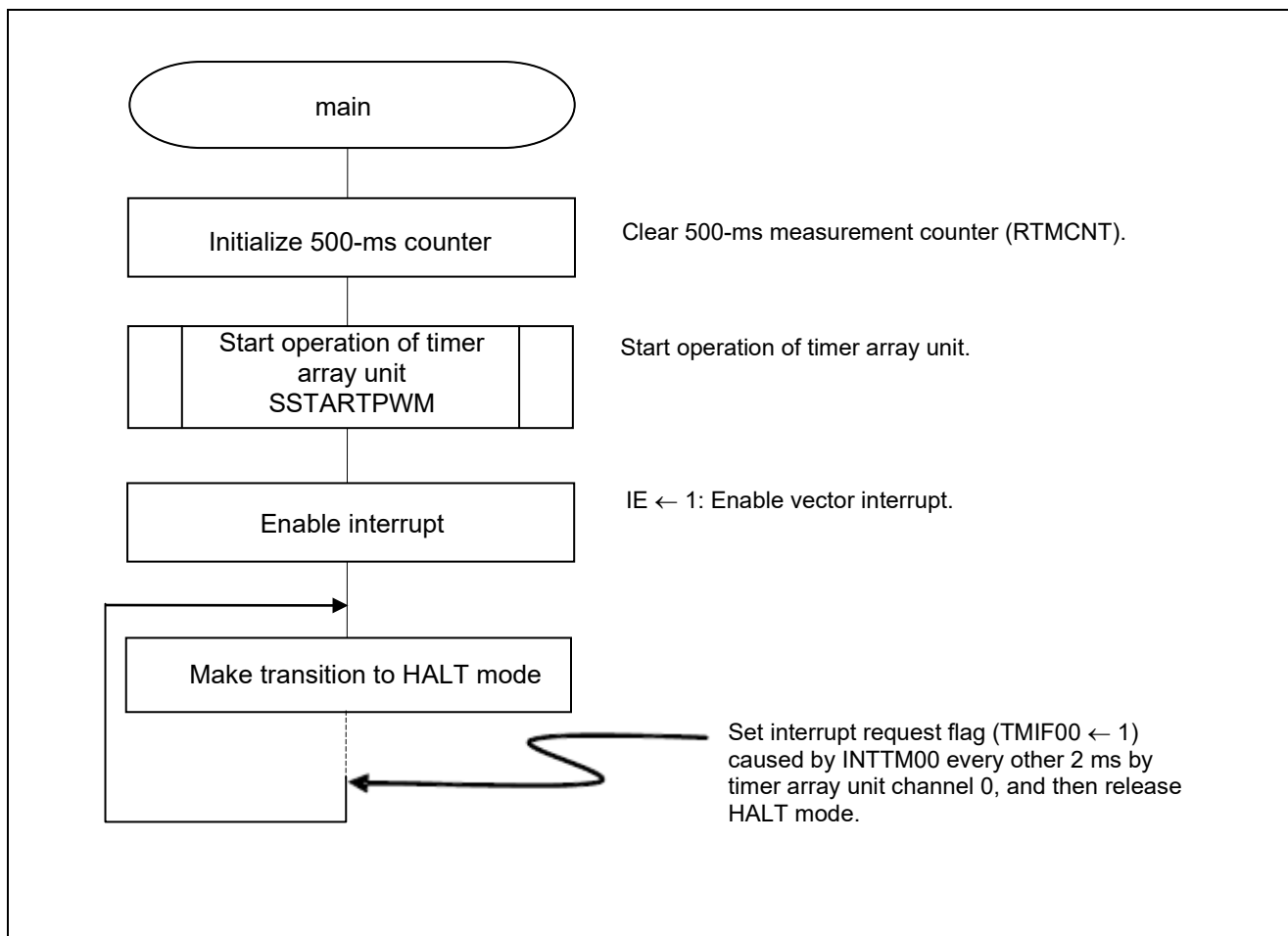


Figure 5.6 Main Processing

5.7.6 Timer Array Unit Startup

Figure 5.7 shows the flowchart for starting the operation of the timer array unit.

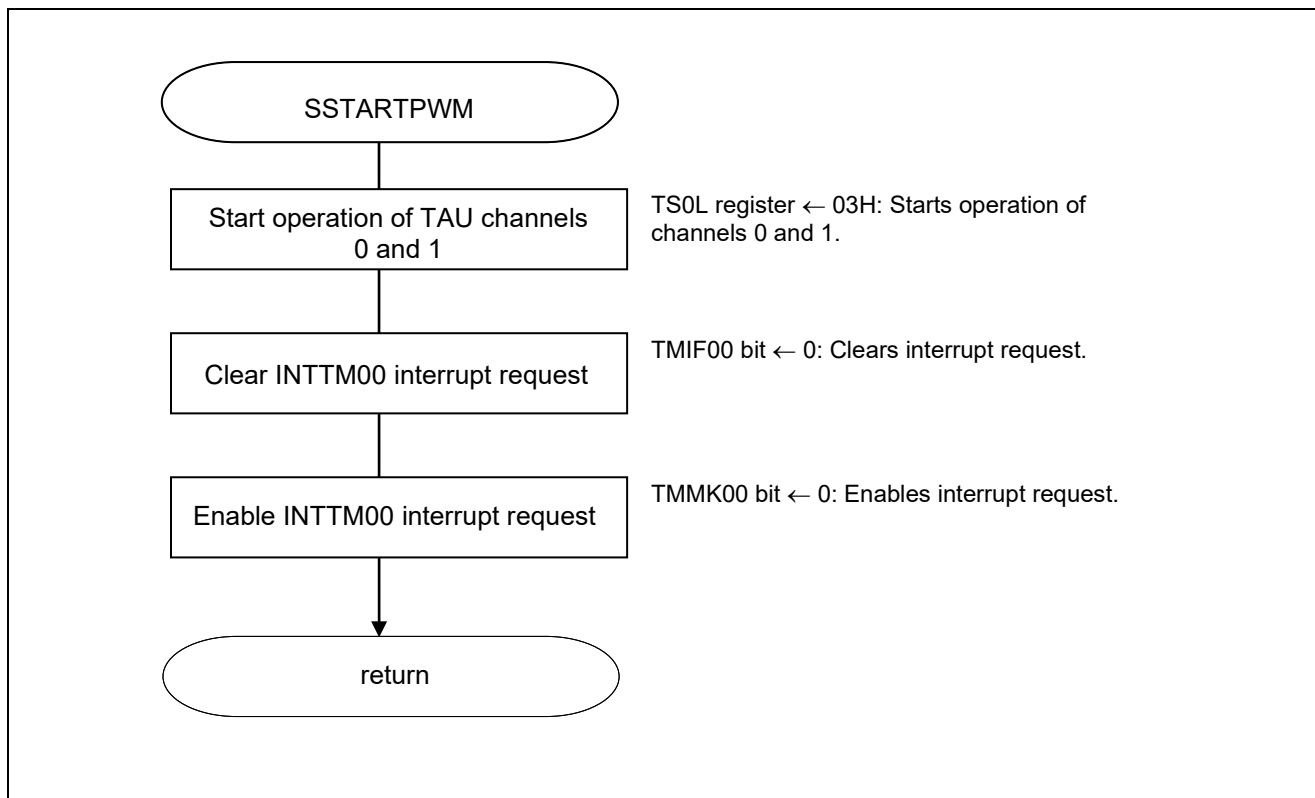


Figure 5.7 Timer Array Unit Startup

Configuring the timer startup

- Timer channel start register 0 (TS0)
Enable count operation of channel 0 and channel 1.

Symbol: TS0

7	6	5	4	3	2	1	0
0	0	0	0	TS 03 ^{Note}	TS 02 ^{Note}	TS 01	TS 00
0	0	0	0	x	x	1	1

Bit 1

TS01	Operation enable (start) trigger of channel 1
0	No trigger operation
1	The TE01 bit is set to 1 and the count operation becomes enabled. The TCR01 register count operation start in the count operation enabled state varies depending on each operation mode.

Bit 0

TS00	Operation enable (start) trigger of channel 0
0	No trigger operation
1	The TE00 bit is set to 1 and the count operation becomes enabled. The TCR00 register count operation start in the count operation enabled state varies depending on each operation mode.

Note: 16-pin products only

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Configuring the timer count end interrupts

- Interrupt request flag register (IF0L)
Clear the interrupt request flag.
- Interrupt mask flag register (MK0L)
Mask interrupts.

Symbol: IF0L

7	6	5	4	3	2	1	0
TMIF00	TMIF01H	SREIF0	SRIF0	STIF0 CSIF00 IICIF00	PIF1	PIF0	WDTIIF
0	x	x	x	x	x	x	x

Bit 7

TMIF00	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Symbol: MK0L

7	6	5	4	3	2	1	0
TMMK00	TMMK01H	SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	PMK1	PMK0	WDTIMK
0	x	x	x	x	x	x	x

Bit 7

TMMK00	Interrupt processing control
0	Enables interrupt processing.
1	Disables interrupt processing.

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

5.7.7 INTTM0 Interrupt Processing

Figure 5.8 shows the flowchart for INTTM0 interrupt processing.

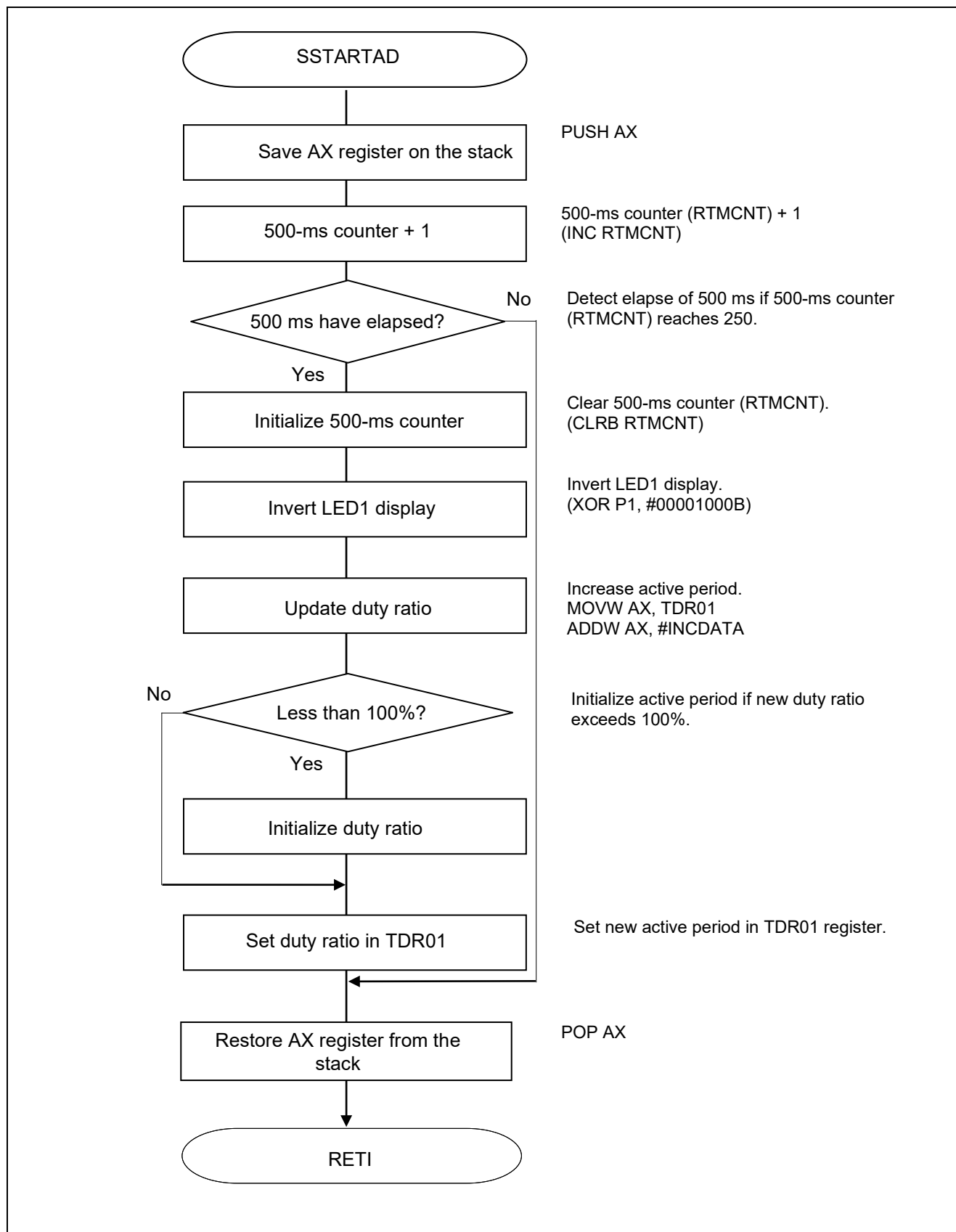


Figure 5.8 INTTM0 Interrupt Service Routine

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G10 User's Manual: Hardware (R01UH0384E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

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Revision Record	RL78/G10 Timer Array Unit (PWM Output) CC-RL
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Rev.	Date	Description	
		Page	Summary
1.00	Sep. 30. 2013	—	First edition issued
2.00	Nov. 11, 2015	5	Table 2.1: Added e2studio
		5	Table 2.1:Change the version information of CS+
		6	Changed the description of Cautions 2
		14	MCM0 bit was fixed of set value
2.10	June. 24, 2022	5	Operation check condition is updated.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
 - A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
 - The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
 - Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
 - Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
 - After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
 - Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
 - Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
 - Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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