RL78/G10

R01AN2550EJ0100
Rev.1.00
2016.1.28

EEPROM Control via Microwire Communications CC-RL

Introduction

This application note explains how to achieve microwire communications using the RL78/G10 serial array unit (SAU) 3-wire serial I/O.

Target Device

RL78/10 (R5F10Y16ASP)

When using this application note for other microcomputers, please modify it according to the corresponding specification and evaluate thoroughly before use.

Contents

1. Specifications

This application note explains how to achieve microwire communication using serial array unit (SAU) 3-wire serial I/O. The RL78/G10's CSI operates as the master while microwire communication is used to control ATMEL's EEPROM (AT93C46D) on the slave side. The application executes data write and read operations based on the AT93C46D instruction set, confirming that data is successfully read.

Table1.1 lists the application's peripheral functions and their usage; Figure 1.1 shows the microwire operating configuration.

Table 1.1 Peripheral Functions and Usage

Peripheral Function	Usage
Serial Array Unit (SAU)	CS100 master transmit/receive operations
Port output	Chip-select signal output

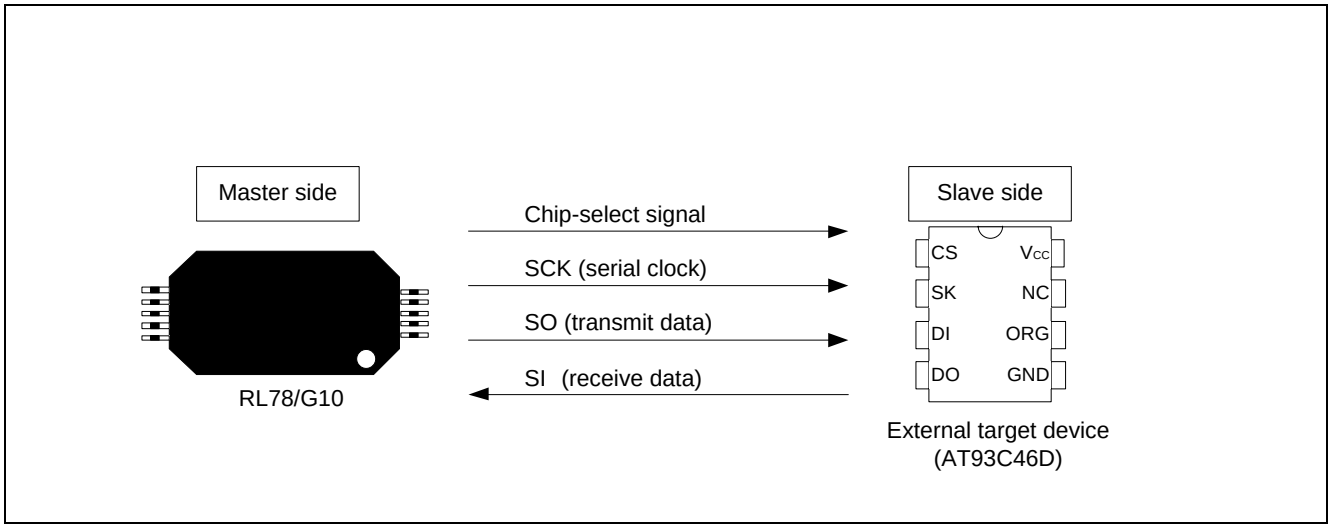


Figure 1.1 Microwire Operating Configuration

The external target device, ATMEL's AT93C46D, is an EEPROM device equipped with 8 pins used for microwire communication interface. AT93C46D provides 1,024 bits and supports two operating modes, as shown in Table 1.2, selected by ORG pin processing. The application described in this document uses the ORG pin connected to Vcc and the x16-bit organization (64 words of 16 bits). For the most current and accurate details, refer to the latest AT93C46D data sheet.

Table 1.2 AT93C46D Mode Switch

	Data Width per Address Unit	Address Area	Address Width
ORG pin: GND	8 bits	Addresses 0 to 127 (0 to 7FH)	7 bits
ORG pin: V_{cc}	16 bits	Addresses 0 to 63 (0 to 3FH)	6 bits

Table 1.3 lists the instructions in the AT93C46D instruction set that are used in this application. All numbers and characters are in binary values. The values in each row is bit row that from left SB to right Address (or data).For the most current and accurate details, refer to the latest AT93C46D data sheet.

Table 1.3 AT93C46D Control Instruction Set

Instruction	SB	OpC	Address						Data	Description
READ	1	10	A_5	A_4	A_3	A_2	A_1	A_0		The value (output string) read from the DO pin is preceded by the dummy bit's 0.
WRITE	1	01	A_5	A_4	A_3	A_2	A_1	A_0	D_{15}-D_0	Set the CS pin to Low with a 250ns wait after transmission to reflect the value in AT93C46D. Then reset the CS pin to High. The setting is successful when the DO pin goes to High.
ERAL	1	00	1	0	X	X	X	X		
EWEN	1	00	1	1	X	X	X	X		
EWDS	1	00	0	0	X	X	X	X		

SB: Start Bit

OpC: Operation Code

X: Don't Care

Figure 1.2 shows the timing chart for the AT93C46D CS pin. Microwave communication is enabled (selected) when the chip-select signal is High, and disabled (not selected) when Low. Note that this differs from SPI communication. The SK pin can receive a clock after 50ns or more elapse since the CS pin is set to High. The clock setting for this application requires at least one CPU clock (f_{CPU}). This required time differs according to the Vcc. For the most current and accurate details, refer to the latest AT93C46D data sheet.

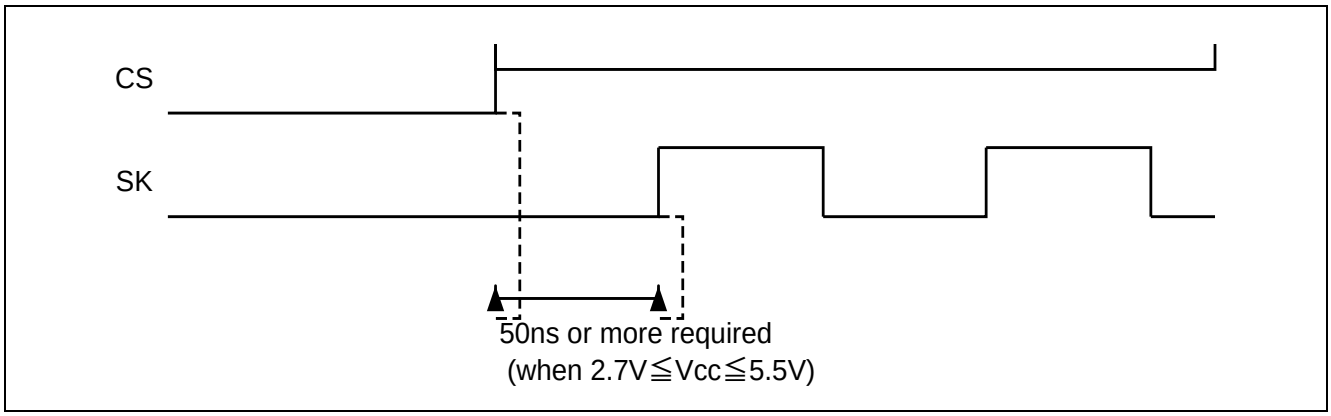


Figure 1.2 CS Pin Timing Chart

Figure 1.3 shows the setup timing for the AT93C46D DI pin (data input pin). The value set to the DI pin is obtained at the rising edge of the clock and received by AT93C46D. Therefore, as shown in Figure 1.3, DI pin data (data changes) should not set immediately before or after the rising edge of the clock. The required time shown in the figure differs according to the Vcc. For the most current and accurate details, refer to the latest AT93C46D data sheet.

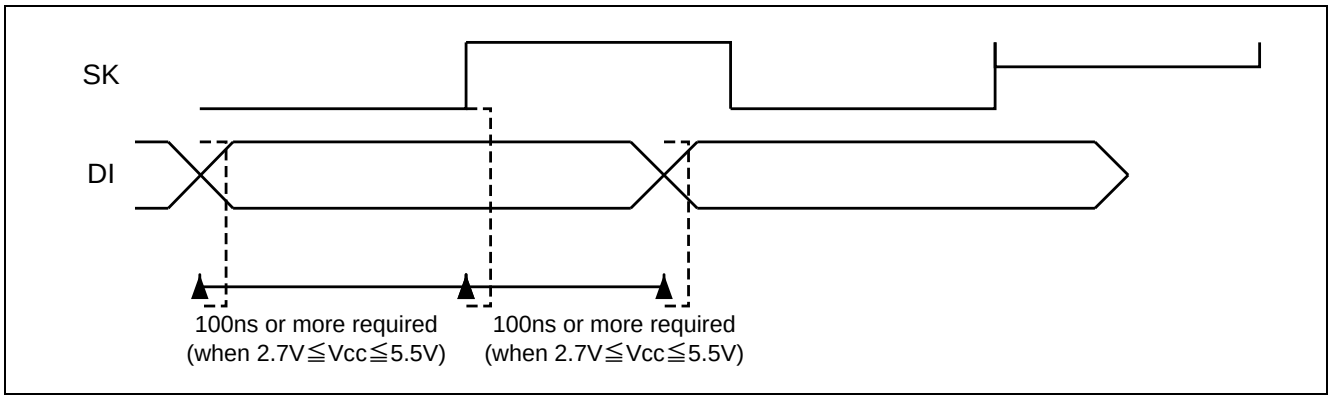


Figure 1.3 DI Pin Timing Chart

Figure 1.4 shows the timing for reading data from the DO pin (data output pin) with the AT93C46D READ instruction. This is an example of when the output value of the DO pin goes to 0. The rising edge of the SK pin clock becomes output and the rising edges of both DI and DO pins become triggers. Therefore, the phase setting must be set carefully when using the CSI function for communication; the required time differs according to the Vcc. For the most current and accurate details, refer to the latest AT93C46D data sheet.

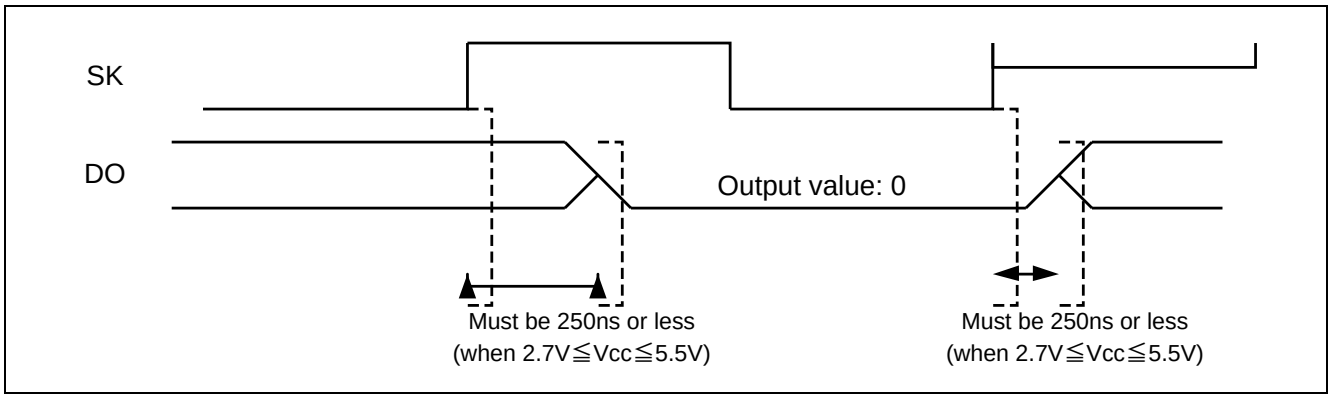


Figure 1.4 DO Pin Timing Chart

2. Operating Conditions

The sample code in this application note runs under the following operating conditions.

Table 2.1 Operating Conditions

Item	Description/Specification
MCU used	RL78/G10 (R5F10Y16ASP)
Operating frequency	・High-speed on-chip oscillator clock (HOCO): 20MHz ・CPU/peripheral hardware clock: 20MHz
Operating voltage	3.0V SPOR detection voltage When power supply falls: TYP. 2.84V (2.70V to 2.96V) When power supply rises: TYP. 2.90V (2.76V to 3.02V)
Integrated development environment	CS+ E3.01.00G (manufactured by Renesas Electronics)
Assembler	CC-RL V1.00.00.03 (manufactured by Renesas Electronics)
Ports used	RL78/G10 target board (QB-R5F10Y16-TB) + AT93C46D

3. Related Application Notes

Application notes related to this document are shown below. Please refer to these as needed.

・RL78/G10 Initialization (R01AN1454E) Application Note

4. Hardware Explanation

4.1 Hardware Configuration Example

Figure 4.1 shows an example Microwire connection between the RL78/G10 and EEPROM (AT93C46D).

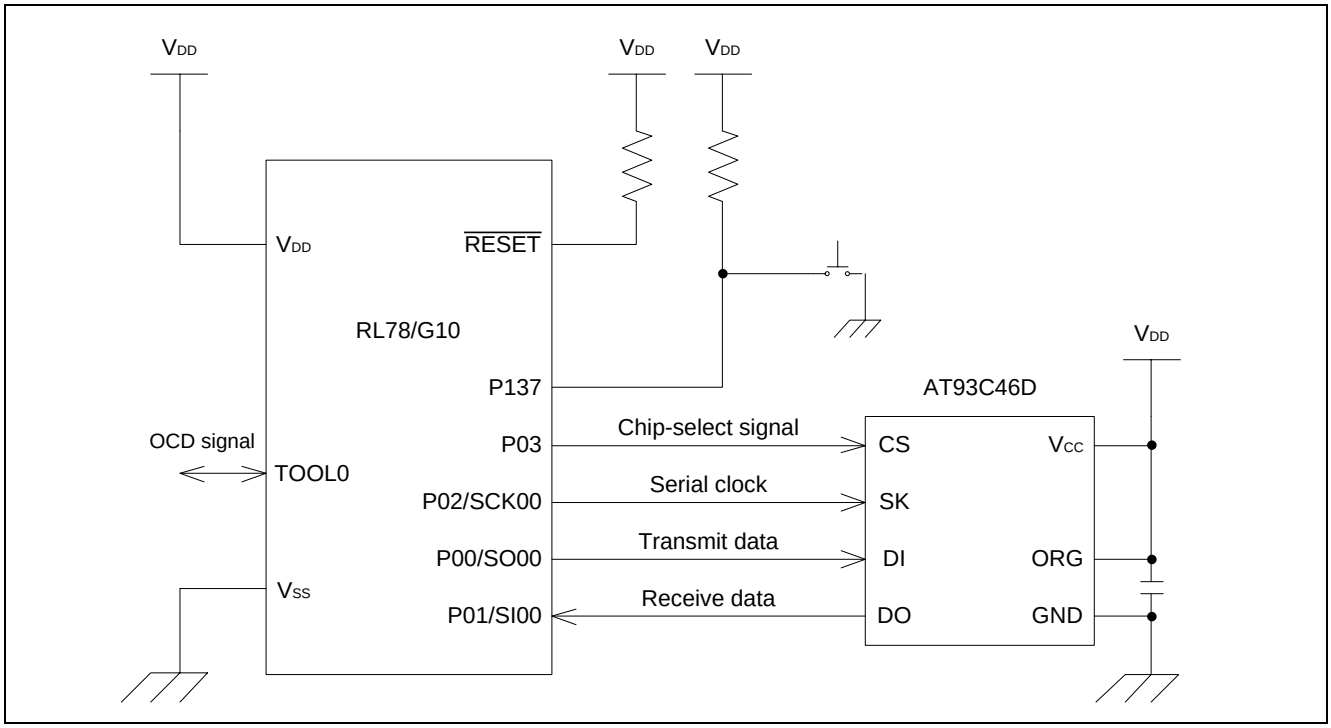


Figure 4.1 RL78/G10 and EEPROM (AT93C46D) Microwire Connection Example

Note: 1.This simplified circuit diagram was created to show an overview of connections only.
When designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements. (Connect each input-only port to V_{DD} or V_{SS} through a resistor.)
2. Make V_{DD} higher than the RESET release voltage (V_{SPOR}) set in SPOR.

4.2 Pin List

Table 4.1 provides a list of the pins used in this document and their functions.

Table 4.1 List of Pins and Functions

Pin Name	Input/Output	Function
P137	Input	Restart switch
P03	Output	Chip-select signal
P02/SCK00	Output	Serial clock
P01/SI00	Input	Data receive (MCU ← EEPROM)
P00/SO00	Output	Data transmit (MCU → EEPROM)

5. Software Explanation

5.1 Operation Outline

The application described in this document transmits and receives data to and from the external target device (slave side) using CSI (master transmission/reception). The master side supplies a clock to the slave side, and then transmits 128 bytes of data or receives 128 bytes of data from the slave side. Because the external target device (slave side) uses Microwire as the communication interface; this EEPROM control application uses half-duplex communication.

(1) SAU0 is initialized as follows:

<Settings>

・SAU0 channel 0: use as CSI

・Serial clock: 20MHz

・IINTCSI00 type: transfer complete interrupt (single transfer mode)

・Start trigger: software

・CSI communication mode: transmit/receive mode

・Clock and data phase : type 4

・MSB first transfer

・Baud rate: 500kbps (20MHz divided by 40)

・Data length: 8 bits

・SCK00 pin initial state: low level

・SO00 pin initial state: low level

（2） Execute the EWEN instruction (Write/Erase Enable) for the external target device (AT93C36D). This will enable use of the WRITE instruction and ERAL instruction (Erase All Areas).

（3） Execute the ERAL instruction (Erase All Areas) for the external target device. Then set the target device’s CS pin to Low (not selected state), wait the specified time, and confirm the DO pin (status). Repeat this process until the DO pin goes to High (all area erase complete status).

（4） Execute the WRITE instruction (Write data) for the external target device. Then set the target device’s CS pin to Low (not selected state), wait the specified time, and confirm the DO pin (status). Repeat this process until the DO pin goes to High (write complete). After write completion is confirmed, each write address and write data are updated, and the process is repeated 64 times, from target device address 0 to 63.

Two bytes of data are written to each address. In addition, a total of 25 bits (including 9 corresponding bits: start bit (1), PoC (2), and address (6)), are stored in LSB order in the 4-byte transmit buffer and transmitted prior to the write data. The following bytes are then sent in MSB first order: 1st byte 00000001B, 2nd byte $01A_5A_4A_3A_2A_1A_0$B, 3rd byte $D_{15}D_{14}D_{13}D_{12}D_{11}D_{10}D_9D_8$ and 4th byte $D_7D_6D_5D_4D_3D_2D_1D_0$. The external target device (AT93C36D) reads data from the DI pin at the clock’s rising edge, which the RL78/G10 CSI supports with phase type 4. Figure 5.1 shows the WRITE instruction execution timing.

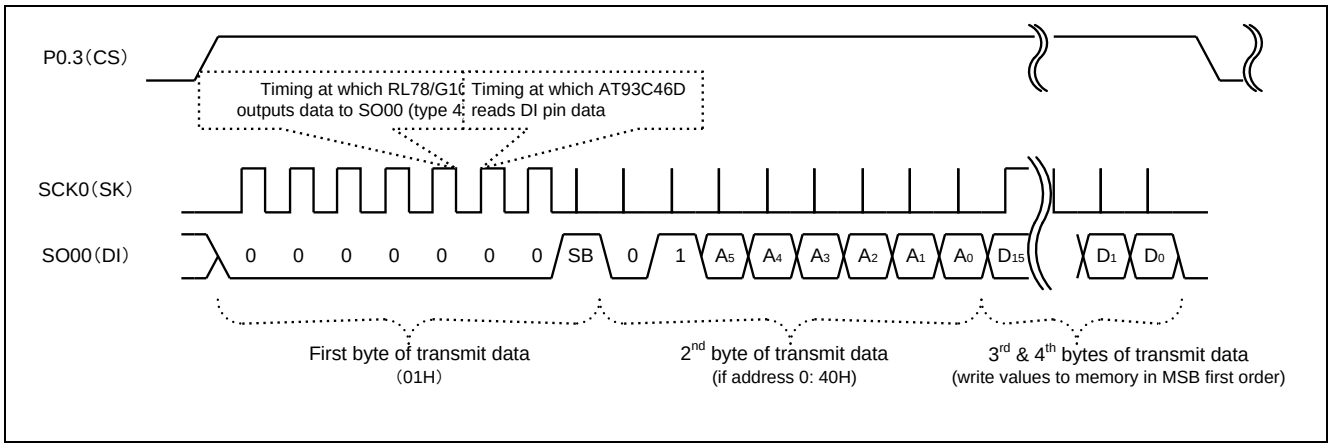


Figure 5.1 WRITE Instruction Execution Timing

(5) Execute the READ instruction (read data) for the external target device. The addresses are read from 0 to 63. Results are displayed on the debugger (CS+) screen to confirm that the written data and read data match. The read range is from addresses 0 to 63 of the external target device, so the READ instruction is executed 64 times. Figure 5.2 shows the READ instruction execution timing.

The read data consists of 2 bytes per address. The read instruction consists of a total 26 bits: start bit (1), OpC (2), addresses (6) dummy bit (value 0) for adjusting timing (1), and dummy bits (value FFFFH) for clock supply during data read operations (16) . The 26 bits are stored in the buffer in the 4-byte transmit buffer in LSB order and sent with the read data. In other words, the 1st bit is 00000010B, 2nd bit $1A_5A_4A_3A_2A_1A_0$B, 3rd bit FFH, and 4th bit FFH. These are sent in MSB first order. The external target device reads data from the DI pin at the rising edges of the clock, and the data is synchronously output to the DO pin at the rising edges of the clock. Normally, the application should switch from type 4 to type 2 at the 3rd byte of the instruction. In this case, however, because AT93C46D comes with a relatively long output delay time (250ns), more than enough time compared to the CSI00 hold time, the application continues to transmit and receive in phase type 4. Of course, this has only been confirmed experimentally and the user should confirm the corresponding data sheets of the external target device used for communication, making sure the design meets the specifications of the development project.

Figure 5.2 shows the READ instruction execution timing.

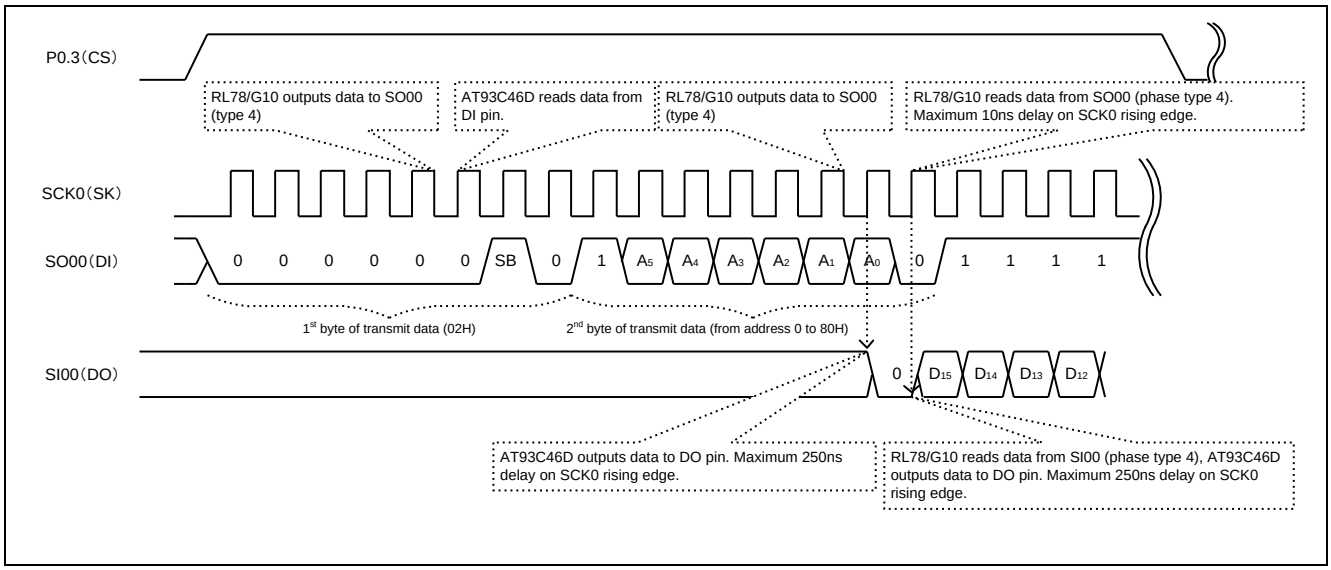


Figure 5.2 READ Instruction Execution Timing

5.2 Option Byte Settings

Table 5.1 shows the option byte settings. Set the optimal value for your system as required.

Table 5.1 Option Byte Settings

Address	Setting Value	Description
000C0H	11101110B	Watchdog timer operation stops (counting stopped after reset)
000C1H	11110111B	SPOR detection voltage When power supply falls: TYP. 2.84V (2.70V to 2.96V) When power supply rises: TYP. 2.90V (2.76V to 3.02V) Uses P125 as reset pin.
000C2H	11111001B	High-speed on-chip oscillator clock (HOCO): 20MHz
000C3H	10000101B	Enables on-chip debug operation

5.3 Constants

Table 5.2 lists the constants used in the sample code.

Table 5.2 Sample Code Constants

Constant Name	Setting Value	Description
TRGONn	00000001B	Stops communication operation.
SOEON	00000001B	Transitions to communication wait state.
CTRXMODEH	11110000B	SCR00H register setting value ・Execute transmission/reception ・Phase type 4 ・Error interrupt disabled ・No parity bit
CTRSMODEL	00000111B	SCR00L register setting value ・MSB first ・No stop bit ・Data length: 8 bits
CSMRDATAH	00000000B	SMR00H register setting value ・Selects CK00 as Operation clock f_{MCK} ・Selects division clock f_{MCK} as transfer clock ・Only software trigger enabled
CSMRDATAL	00100000B	SMR00L register setting value ・CSI mode ・Transfer complete interrupt
BUFFSIZE	32	Buffer size for all received data
ROMEND	01000000B	EEPROM end address

5.4 Variables

Table 5.3 lists the variables used in the sample code.

Table 5.3 Sample Code Variables

Function Name	Description
RCSISUBADDR	INTCSI00 interrupt processing address
DATACOUNT	Transmit data and receive data counter
DATAPOINT	Transmit data and receive data counter
RSNDBUF	Transmit data buffer
RRCVBUF	Receive data buffer
TESTBUFF	Data buffer

5.5 Functions (subroutines)

Table 5.4 lists the functions (subroutines) used in the sample code.

Table 5.4 Functions (subroutines)

Function Name	Description
main	EEPROM control via Microwire communication
__s_micro_read1	Reads data from specified addresses in EEPROM
__s_micro_write	Writes data to specified addresses in EEPROM
__s_micro_ewen	Puts EEPROM in write-enabled state
__s_micro_ewds	Puts EEPROM in write-disabled state
__s_micro_eral	Erases all areas of EEPROM chip
__s_waitend	Waits for completion of EEPROM data write/erase all areas.
__s_chekend	Reads completion status of EEPROM data write/erase all areas
IINTCSIp	INTCSI00 interrupt processing

5.6 Function (subroutine) Specifications

The following are the specifications of functions (subroutines) used in the sample code.

Function Name: main

Outline	Serial EEPROM control via Microwire communication
Description	Repeat data read processing to read data from all serial EEPROM addresses. If P13.7 is High level when the subroutine is started, data is written to the serial EEPROM after all areas are erased.
Argument	None
Return Value	None
Notes	None

Function Name: __s_micro_read1

Outline	Read data from specified addresses in serial EEPROM
Description	Transmits READ instruction to serial EEPROM, reads data from specified address.
Argument	AX register: EEPROM read address
Return Value	BC register: EEPROM address data was read from
Notes	None

Function Name: __s_micro_write

Outline	Data write trigger processing for specified addresses in serial EEPROM
Description	Transmits WRITE instruction to serial EEPROM, executes data write trigger for specified address. (A separate process is used to confirm write completion.)
Argument	AX register: EEPROM write address Stack pointer +4: data to be written to EEPROM
Return Value	None
Notes	None

Function Name: __s_micro_ewen

Outline	Put serial EEPROM in write enabled state.
Description	Transmits EWEN instruction to serial EEPROM, puts in write enabled state.
Argument	None

Return Value	None
Notes	None

Function Name: __s_micro_ewds

Outline	Put serial EEPROM in write disabled state.
Description	Transmits EWDS instruction to serial EEPROM, puts in write disabled state.
Argument	None
Return Value	None
Notes	None

Function Name: __s_micro_eral

Outline	Erase all areas on serial EEPROM chip.
Description	Transmits ERAL instruction to serial EEPROM, triggers the processing to start erasing all areas on the chip. (A separate process is used to confirm “erase all areas” completion.)
Argument	None
Return Value	None
Notes	None

Function Name: __s_waitend

Outline	Wait for completion of EEPROM data write/ erase all areas.
Description	Waits for completion of data write to the serial EEPROM or for all areas on chip to be erased.
Argument	None
Return Value	None
Notes	None

Function Name: __s_chekend

Outline	Read completion status of serial EEPROM data write/ erase all areas.
Description	Reads completion status of serial EEPROM data write/ erase all areas.
Argument	None
Return Value	CY register: completion status (0 = now processing, 1 = completed)
Notes	None

Function Name: IINTCSIp

Outline	INTCSI00 interrupt processing
Description	Executes contents of processing address set in RCSISUBADDR when the INTCSI00 interrupt is generated.
Argument	None
Return Value	None
Notes	None

5.7 Flowcharts

Figure 5.3 shows the entire flow of the sample code described in this application note.

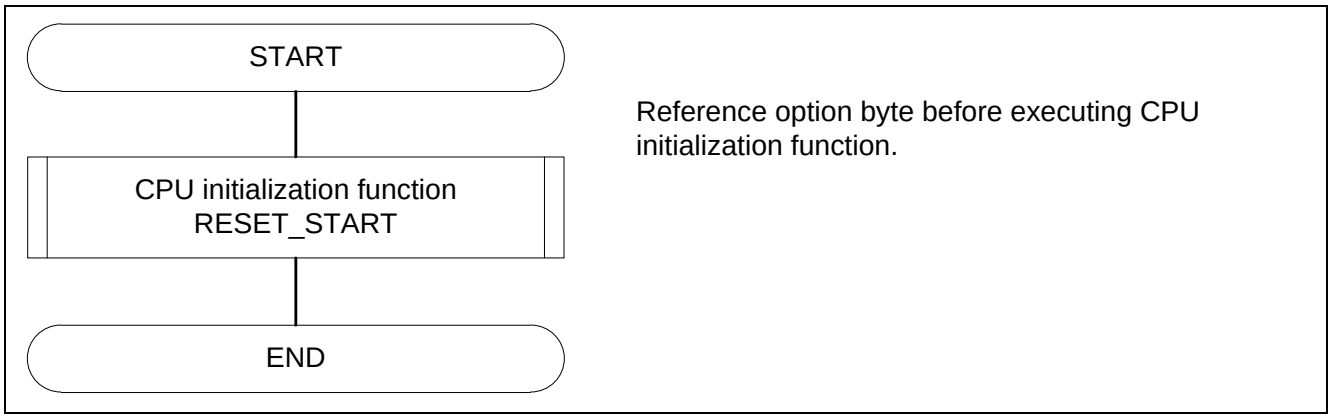


Figure 5.3 Entire Flow

5.7.1 CPU Initialization Function

Figure 5.4 shows the flowchart for the CPU initialization function.

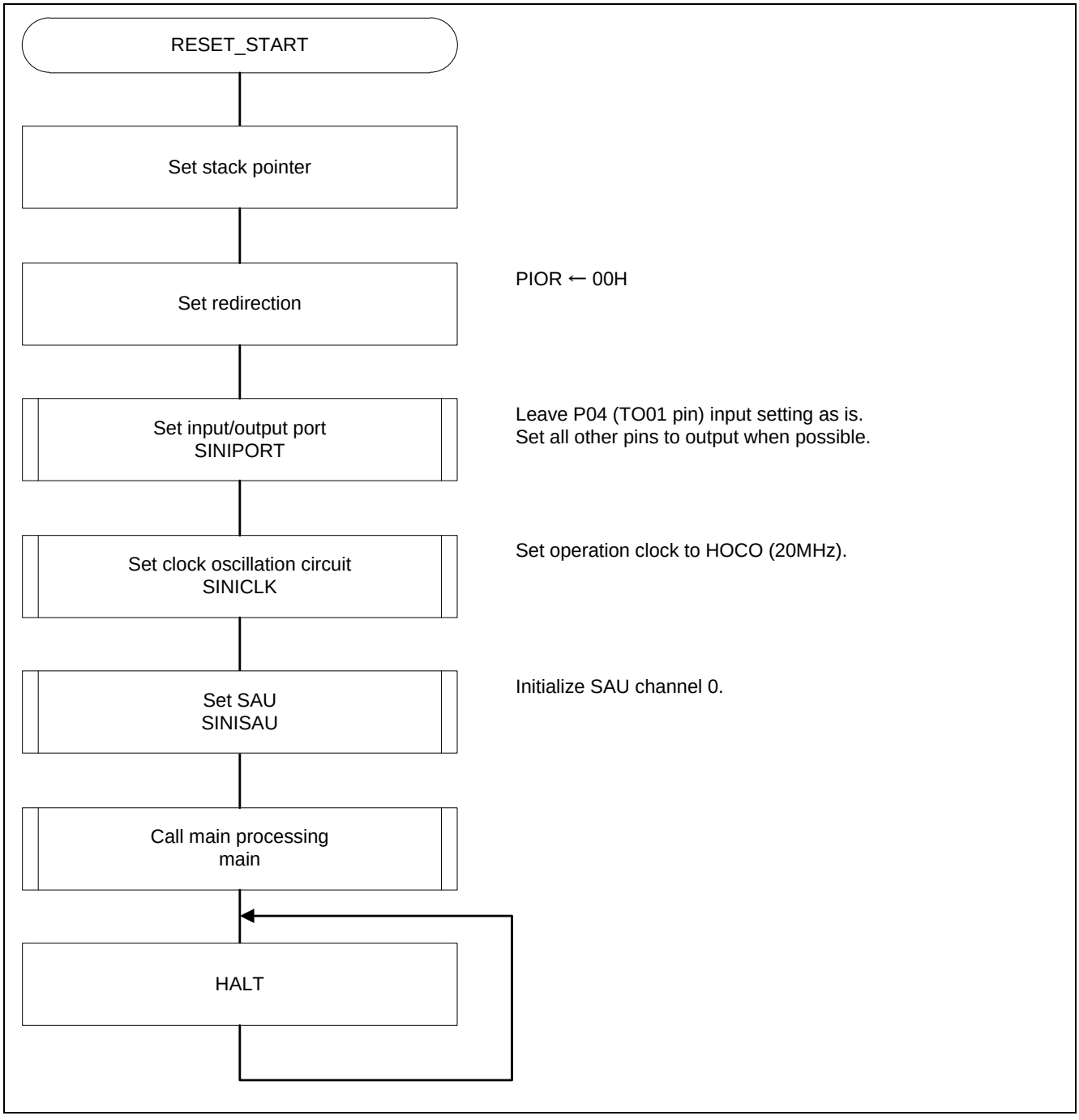


Figure 5.4 CPU Initialization Function

5.7.2 I/O Port Settings

Figure 5.5 shows the flowchart for setting the I/O ports.

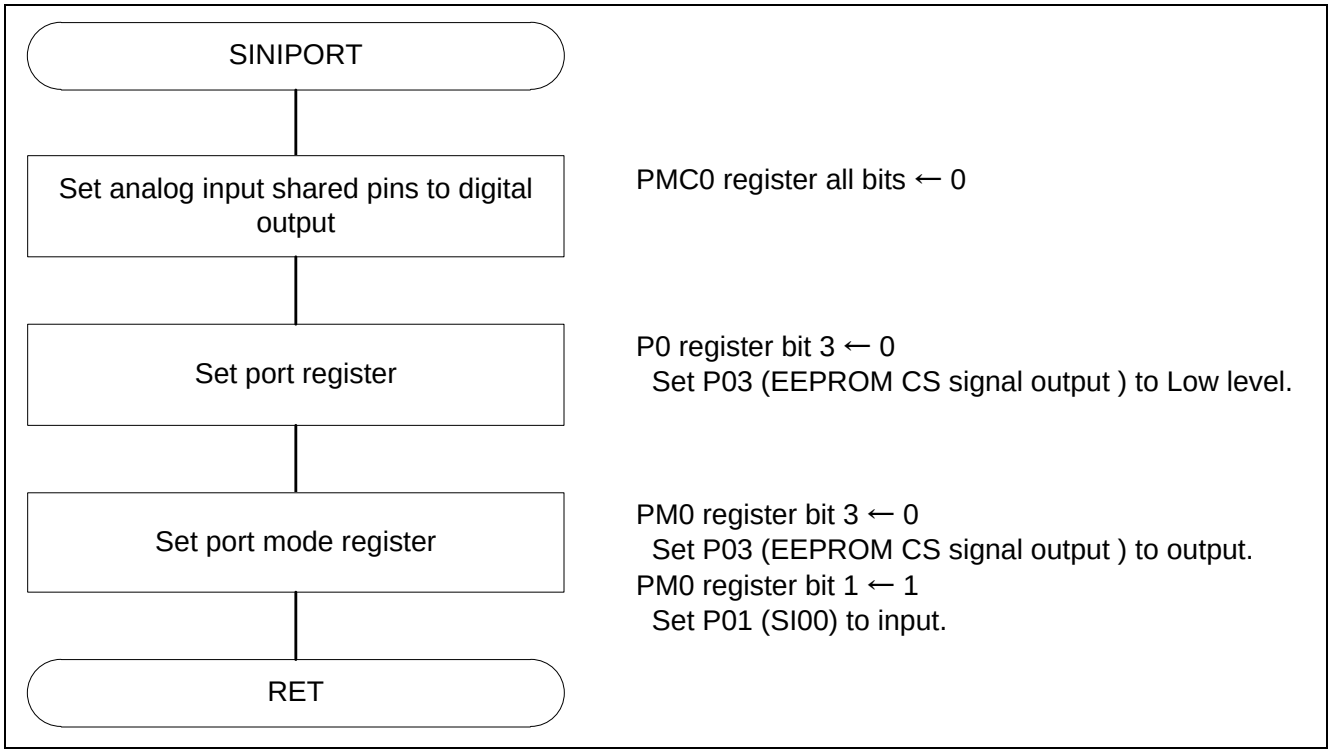


Figure 5.5 I/O Port Settings

Note: When designing circuits, always make sure unused ports are properly processed and all electrical characteristics are met. Also make sure each unused input-only port is connected to V_{DD} or V_{SS} through a resister.

Chip select signal output port, SI00 pin setting

- Port Register (P0)
- Port Mode Register (PM0)

  Select PM03 input/output.

  Select P01 (SI00) input/output.

Symbol: P0

7	6	5	4	3	2	1	0
0	0	0	P04	P03	P02	P01	P00
x	x	x	x	0	x	x	x

Bit 3

P03	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Symbol: PM0

7	6	5	4	3	2	1	0
1	1	1	PM04	PM03	PM02	PM01	PM00
x	x	x	x	0	x	1	x

Bit 3

PM03	PM03 input mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Bit 1

PM01	PM01 input mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Note: For detailed description on how to set registers, refer to RL78/G10 Users Manual (Hardware Version)

5.7.3 Clock Generation Circuit Setting

Figure 5.6 shows the flowchart for the clock oscillation circuit setting.

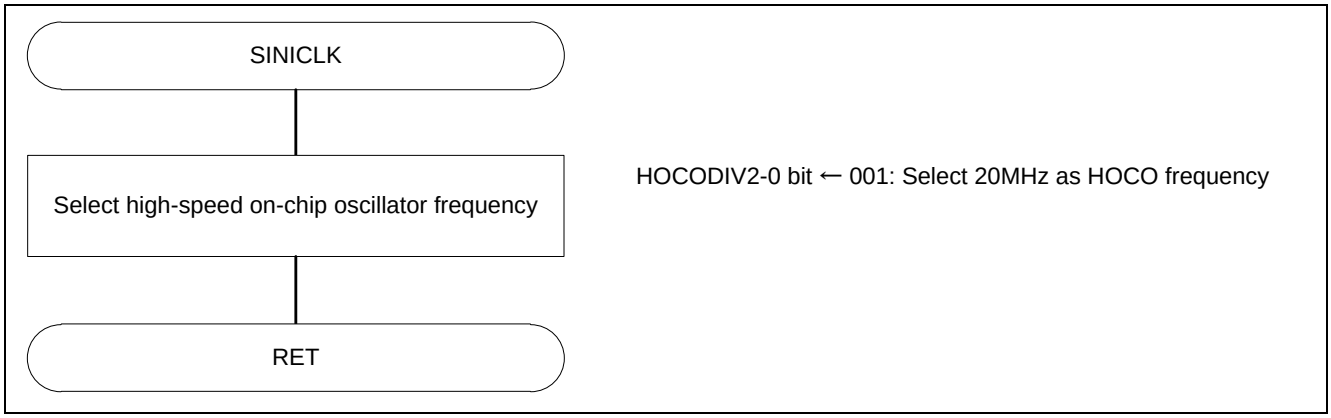


Figure 5.6 Clock Generation Circuit Settings

Note: For more details concerning CPU clock settings (SINICLK), refer to the flowchart in RL78/G10 Initialization (R01AN1454E) Application Note.

5.7.4 Serial Array Unit Setting

Figure 5.7 shows the flowchart for the serial array unit setting.

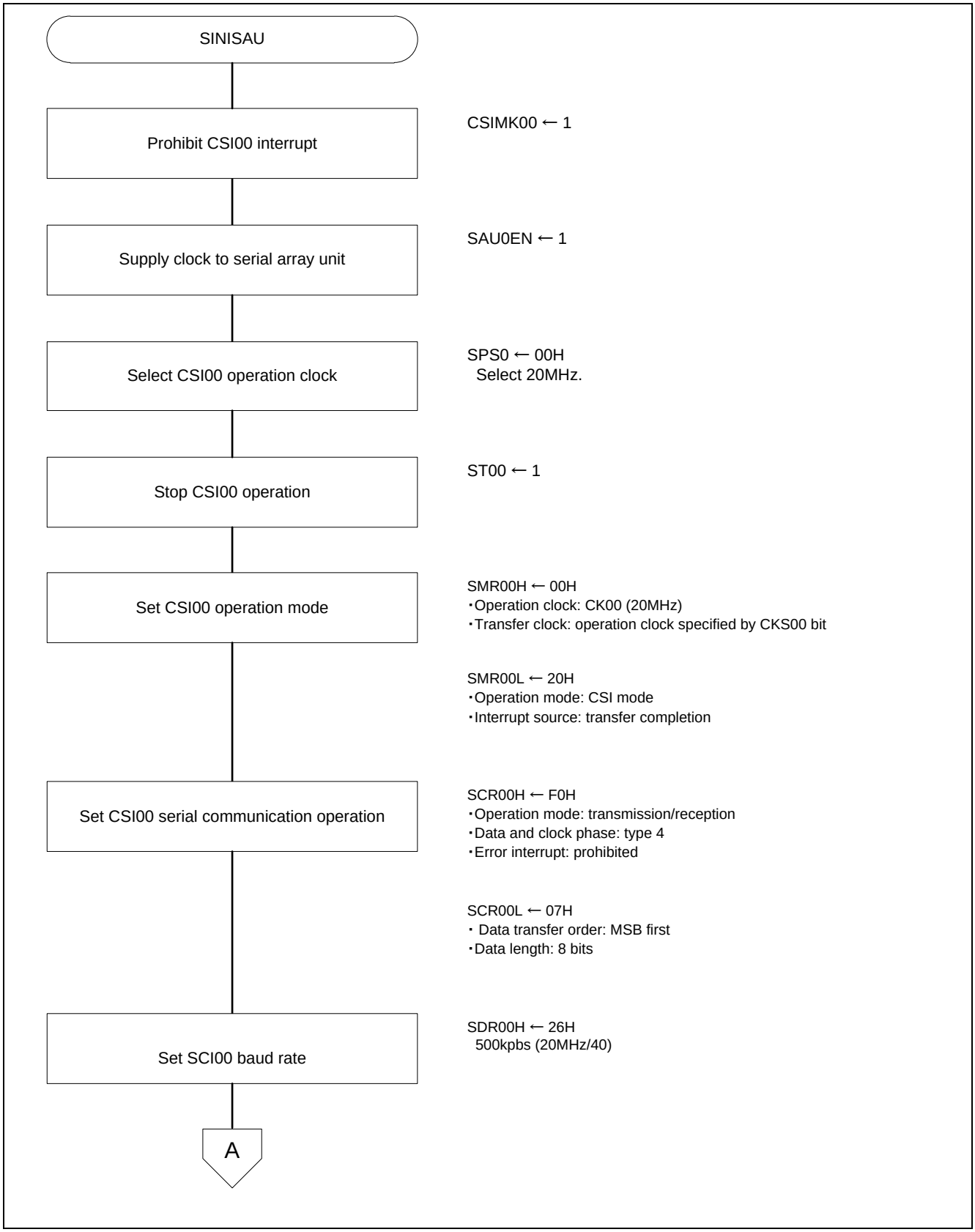


Figure 5.7 Serial Array Unit Setting (1/2)

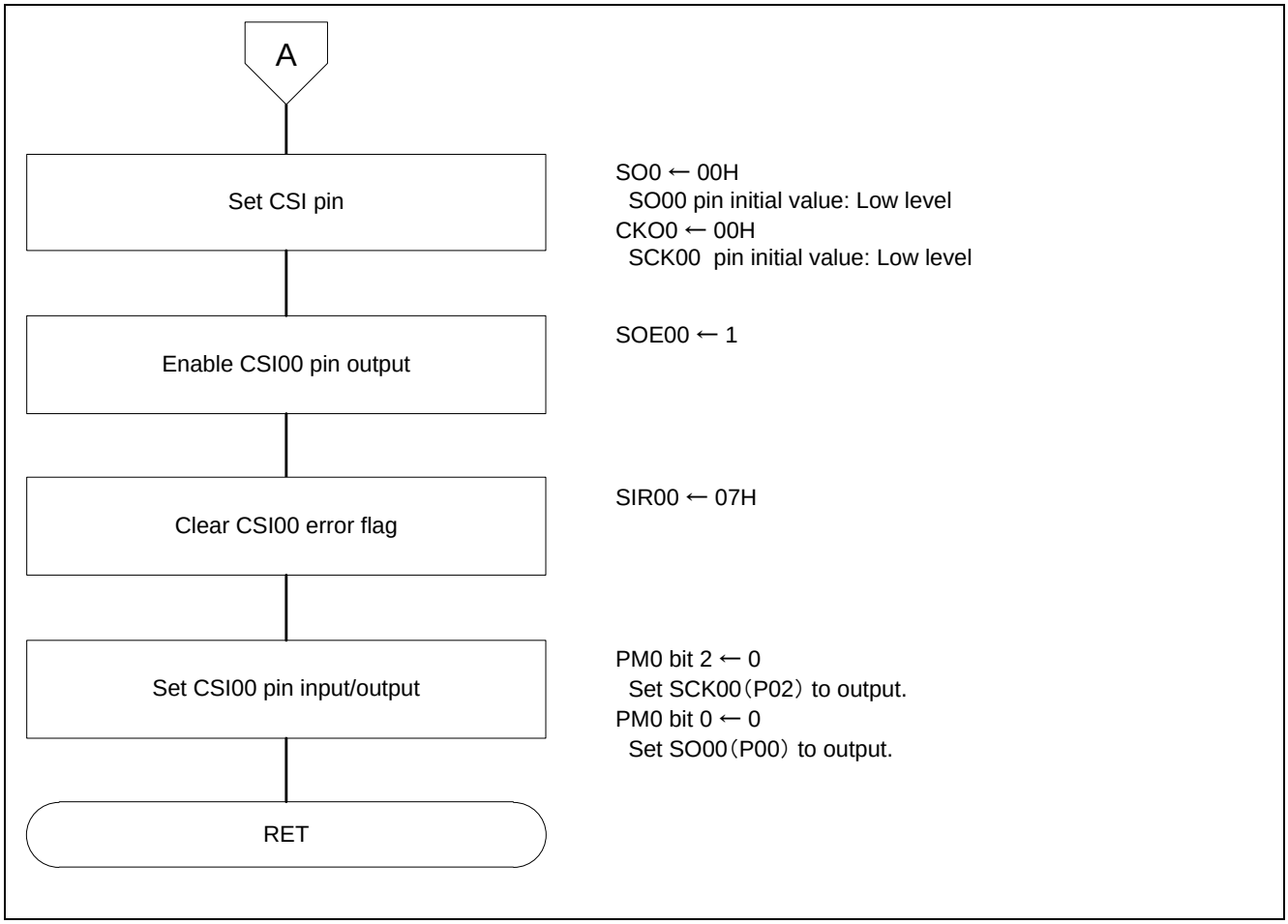


Figure 5.7 Serial Array Unit Setting (2/2)

SAU interrupt mask setting

・Interrupt mask flag register (MK0L)（MK0L）

Set interrupt mask.

Symbol: MK0L

7	6	5	4	3	2	1	0
TMMK00	TMMK01H	SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	PMK1	PMK0	WDTIMK
x	x	x	x	1	x	x	x

Bit 3

CSIMK00	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Note: For detailed description on how to set registers, refer to RL78/G10 Users Manual (Hardware Version).

Start clock supply to SAU

・Peripheral enable register 0 (PER0)

Set clock supply start/stop to serial array unit.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN Note	CPMEN Note	ADCEN	IICA0EN Note	0	SAU0EN	0	TAU0EN
x	x	x	x	0	1	0	x

Bit 2

SAU0EN	Control of serial array unit input clock supply
0	Stops input clock supply.
1	Enables input clock supply.

Note: 16-pin products only

Note: For detailed description on how to set registers, refer to RL78/G10 Users Manual (Hardware Version).

Serial clock selection

・Serial clock select register 0 (SPS0)

Select the serial array unit operation clock.

Symbol: SPS0

7	6	5	4	3	2	1	0
PRS013	PRS012	PRS011	PRS010	PRS003	PRS002	PRS001	PRS000
x	x	x	x	0	0	0	0

PRS 003	PRS 002	PRS 001	PRS 000		Selection of operation clock (CK00) Note				
					f_{CLK} = 1.25MHz	f_{CLK} = 2.5MHz	f_{CLK} = 5MHz	f_{CLK} = 10MHz	f_{CLK} = 20MHz
0	0	0	0	f_{CLK}	1.25MHz	2.5MHz	5MHz	10MHz	20MHz
0	0	0	1	$f_{CLK}/2$	625kHz	1.25MHz	2.5MHz	5MHz	10MHz
0	0	1	0	$f_{CLK}/2^2$	313kHz	625kHz	1.25MHz	2.5MHz	5MHz
0	0	1	1	$f_{CLK}/2^3$	156kHz	313kHz	625kHz	1.25MHz	2.5MHz
0	1	0	0	$f_{CLK}/2^4$	78.1kHz	156kHz	313kHz	625kHz	1.25MHz
0	1	0	1	$f_{CLK}/2^5$	39.1kHz	78.1kHz	156kHz	313kHz	625kHz
0	1	1	0	$f_{CLK}/2^6$	19.5kHz	39.1kHz	78.1kHz	156kHz	313kHz
0	1	1	1	$f_{CLK}/2^7$	9.77kHz	19.5kHz	39.1kHz	78.1kHz	156kHz
1	0	0	0	$f_{CLK}/2^8$	4.88kHz	9.77kHz	19.5kHz	39.1kHz	78.1kHz
1	0	0	1	$f_{CLK}/2^9$	2.44kHz	4.88kHz	9.77kHz	19.5kHz	39.1kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.22kHz	2.44kHz	4.88kHz	9.77kHz	19.5kHz
1	0	1	1	$f_{CLK}/2^{11}$	625Hz	1.22kHz	2.44kHz	4.88kHz	9.77kHz
1	1	0	0	$f_{CLK}/2^{12}$	313Hz	625Hz	1.22kHz	2.44kHz	4.88kHz
1	1	0	1	$f_{CLK}/2^{13}$	152Hz	313Hz	625Hz	1.22kHz	2.44kHz
1	1	1	0	$f_{CLK}/2^{14}$	78Hz	152Hz	313Hz	625Hz	1.22kHz
1	1	1	1	$f_{CLK}/2^{15}$	39Hz	78Hz	152Hz	313Hz	625Hz

Note: For detailed description on how to set registers, refer to RL78/G10 Users Manual (Hardware Version).

SAU operation Stop

・Serial channel stop register 0 (ST0)

Set the serial array unit channel to stop.

Symbol: ST0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ST01	ST00
0	0	0	0	0	0	x	1

Bit 0

ST00	Operation stop trigger of channel
0	No trigger operation
1	Clears the SE0n bit to 0 and stops the communication operation

Note: For detailed description on how to set registers, refer to RL78/G10 Users Manual (Hardware Version).

SAU0 channel operation mode setting

・Serial mod register 00 (SMR00H, SMR00L)

Select operation clock (f_{MCK}).

Select transfer clock (f_{TCLK}).

Set operation mode.

Set interrupt source.

Symbol: SMR00H

7	6	5	4	3	2	1	0
CKS00	CCS00	0	0	0	0	0	STS01 Note
0	0	0	0	0	0	0	0

Note: Provided in the SMR01H register only.

Bit 7

CKS00	Selection of channel 0 operation clock (f_{MCK})
0	Operation clock CK00 set by the SPS0 register
1	Operation clock CK01 set by the SPS0 register

Bit 6

CCS00	Selection of channel 0 count clock (f_{TCLK})
0	Divided operation clock f_{MCK} specified by the CKS00 bit
1	Clock input from the SCKp pin (slave transfer in CSI mode)

Bit 0

STS01 Note	Selection of Start trigger source
0	Only software trigger is valid (selected for CSI, UART transmission, and simplified I^2C).
1	Valid edge of the RxD0 pin (selected for UART reception)

Note: Provided in the SMR01H register only.

Symbol: SMR00L

7	6	5	4	3	2	1	0
0	0	1	0	0	MD002	MD001	MD000
0	0	1	0	0	0	0	0

Bits 2, 1

MD002	MD001	Setting of operation mode of channel 0
0	0	CSI mode
0	1	UART mode
1	0	Simplified I^2C mode
1	1	Setting prohibited

Bit 0

MD000	チ Selection of interrupt source of channel 0
0	Transfer end interrupt
1	Buffer empty interrupt (Occurs when data is transferred from the SDR00L register to the shift register.)

Note: For detailed description on how to set registers, refer to RL78/G10 Users Manual (Hardware Version).

SAU0 channel 0 serial communication operation setting

・Serial communication operation setting register 00 (SCR00H, SCR00L)

Set operation mode.

Set data and clock phase.

Select masked/unmasked error interrupt.

Set data transfer order.

Set data length.

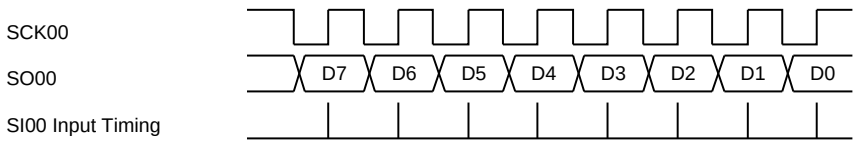
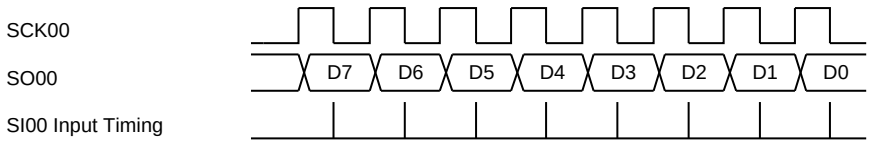
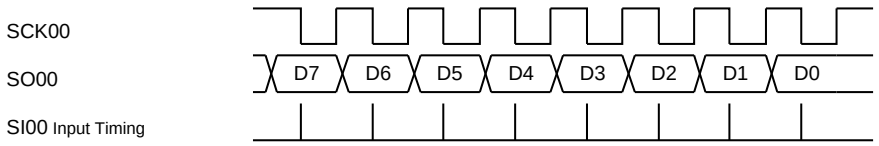
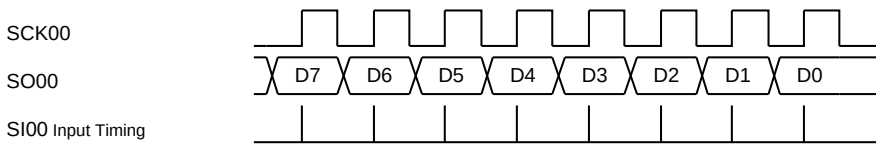
Symbol: SCR00H

7	6	5	4	3	2	1	0
TXE00	RXE00	DAP00	CKP00	0	ECC00	PTC001	PTC000
1	1	1	1	0	0	0	0

Bits 7, 6

TXE00	RXE00	Setting of operation mode of channel 0
0	0	Disable communication
0	1	Reception only
1	0	Transmission only
1	1	Transmission/reception

Bits 5, 4

DAP00	CKP00	Selection of data and clock phase in CSI mode	Type
0	0		1
0	1		2
1	0		3
1	1		4

Symbol: SCR00H

7	6	5	4	3	2	1	0
TXE00	RXE00	DAP00	CKP00	0	ECC00	PTC001	PTC000
1	1	1	1	0	0	0	0

Bit 2

ECC00	Selection of masking error interrupt signal (INSTRE0)
0	Disables generation of error interrupt (INTSRE0 is generated).
1	Enables generation of error interrupt (INTSRE0). (INTSRE0 is not generated if an error occurs).

Bits 1, 0

PTC001	PTC000	Setting of parity bit in UART mode	
		Transmission	Reception
0	0	Does not output the parity bit.	Receives without parity
0	1	Outputs parity 0.	No parity judgment.
1	0	Outputs even parity.	Judged as even parity.
1	1	Outputs odd parity.	Judged as odd parity.

Symbol: SCR00L

7	6	5	4	3	2	1	0
DIR00	0	SLC001	SLC000	0	1	1	DLS000
0	0	0	0	0	1	1	1

Bit 7

DIR00	Selection of data transfer sequence in CSI and UART modes
0	Inputs/outputs data with MSB first.
1	Inputs/outputs data with LSB first.

Bits 5, 4

SLC001	SLC000	Setting of stop bit in UART mode
0	0	No stop bit
0	1	Stop bit length = 1 bit
1	0	Stop bit length = 2 bits
1	1	Setting prohibited

Bit 0

DLS000	Setting of data length in CSI and UART modes
0	7-bit data length (stored in bits 0 to 6 of the SDR00L register)
1	8-bit data length (stored in bits 0 to 7 of the SDR00L register)

Note: For detailed description on how to set registers, refer to RL78/G10 Users Manual (Hardware Version).

Operation clock division setting

・Serial data register 00 (SDR00H)

Set the operation clock (f_{MCK}).

Symbol: SDR00H

7	6	5	4	3	2	1	0
							0

Bits 7-1

SDR00H[7:1]							Transfer clock setting by dividing the operation clock (f_{MCK})
0	0	0	0	0	0	0	$f_{MCK}/2$
0	0	0	0	0	0	1	$f_{MCK}/4$
0	0	0	0	0	1	0	$f_{MCK}/6$
0	0	0	0	0	1	1	$f_{MCK}/8$
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
0	0	1	0	0	1	1	$f_{MCK}/40$
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	1	0	$f_{MCK}/254$
1	1	1	1	1	1	1	$f_{MCK}/256$

Note: For detailed description on how to set registers, refer to RL78/G10 Users Manual (Hardware Version).

SCK00, SO00 pins output settings

- Serial clock output register 0 (CKO0)

  Set serial clock output pin output value.

- Serial output register 0 (SO0)

  Set serial output pin output value.

Symbol: CKO0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	CKO00
0	0	0	0	0	0	0	0

Bit 0

CKO00	Serial clock output of channel 0
0	Serial clock output value is “0”.
1	Serial clock output value is “1”.

Symbol: SO0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SO00
0	0	0	0	0	0	0	0

Bit 0

SO00	Serial data output of channel 0
0	Serial data output value is “0”.
1	Serial data output value is “1”.

Note: For detailed description on how to set registers, refer to RL78/G10 Users Manual (Hardware Version).

Output enable setting for serial communication operation

・Serial output enable register 0 (SOE0)

Enable/disable output by serial communication operation.

Symbol: SOE0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SOE00
0	0	0	0	0	0	0	1

Bit 0

SOE00	Serial output enable/disable of channel 0
0	Disables output by serial communication operation.
1	Enables output by serial communication operation.

Note: For detailed description on how to set registers, refer to RL78/G10 Users Manual (Hardware Version).

SAU0 channel 0 error flag clear

・Serial flag clear trigger register 00 (SIR00)

Clear parity error flag.

Clear overrun error flag.

Symbol: SIR00

7	6	5	4	3	2	1	0
0	0	0	0	0	0	PECT00	OVCT00
0	0	0	0	0	0	1	1

Bit 1

PECT00	Clear trigger of parity error flag of channel 0
0	Not cleared
1	Clears the PEF00 bit of the SSR00 register to 0.

Bit 0

OVCT00	Clear trigger of overrun error flag of channel 0
0	Not cleared
1	Clears the OVF00 bit of the SSR00 register to 0.

Note: For detailed description on how to set registers, refer to RL78/G10 Users Manual (Hardware Version).

SCK00, SO00 pins port settings

・Port mode register (PM0)

Select input/output of P02 (SCK00).

Select input/output of P00 (SO00).

Symbol: PM0

7	6	5	4	3	2	1	0
1	1	1	PM04	PM03	PM02	PM01	PM00
1	1	1	x	x	0	x	0

Bits 2, 0

PM02,PM01	PM03 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Note: For detailed description on how to set registers, refer to RL78/G10 Users Manual (Hardware Version).

5.7.5 Main processing

Figure 5.7 shows the flowchart for main processing.

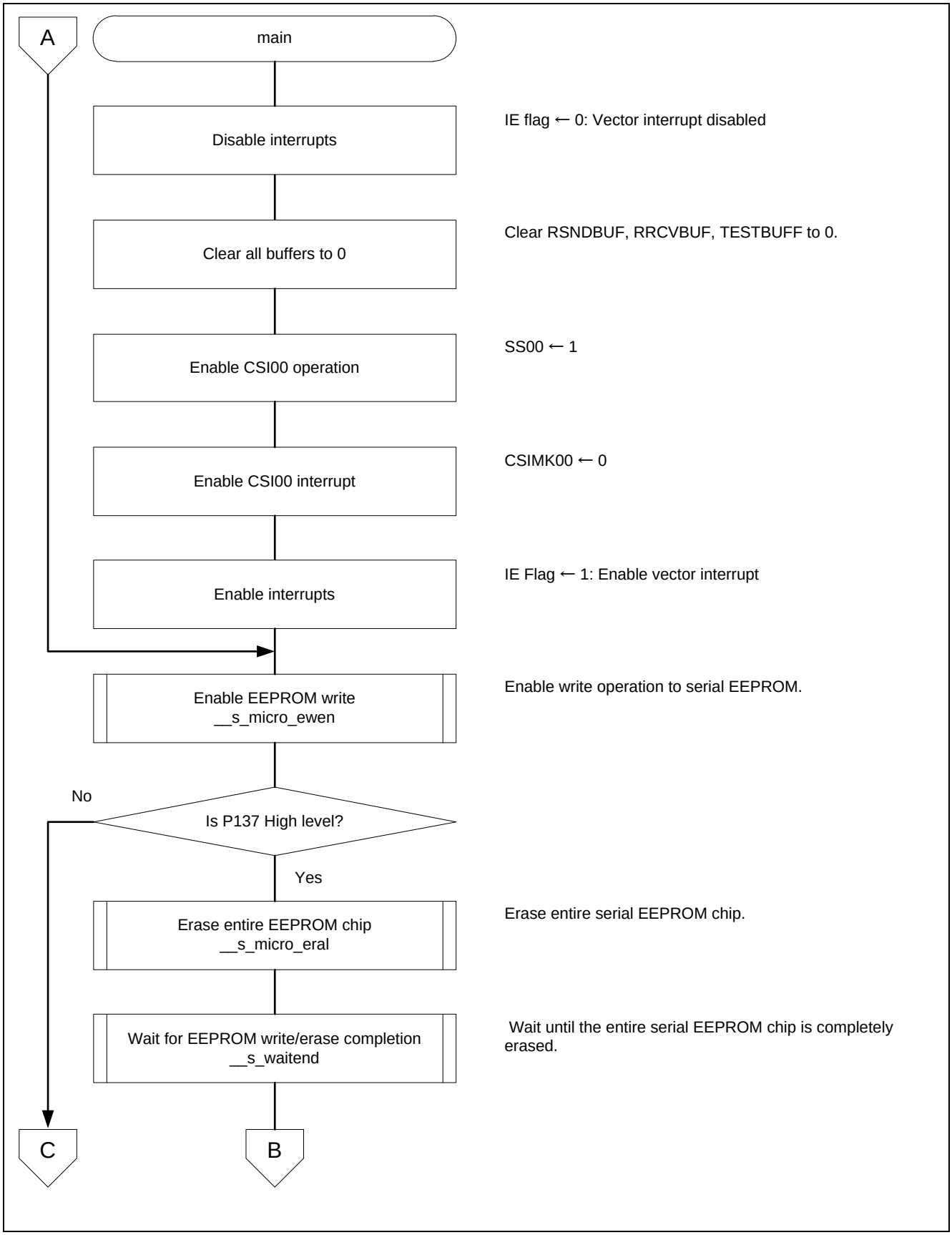


Figure 5.8 Main Processing (1/3)

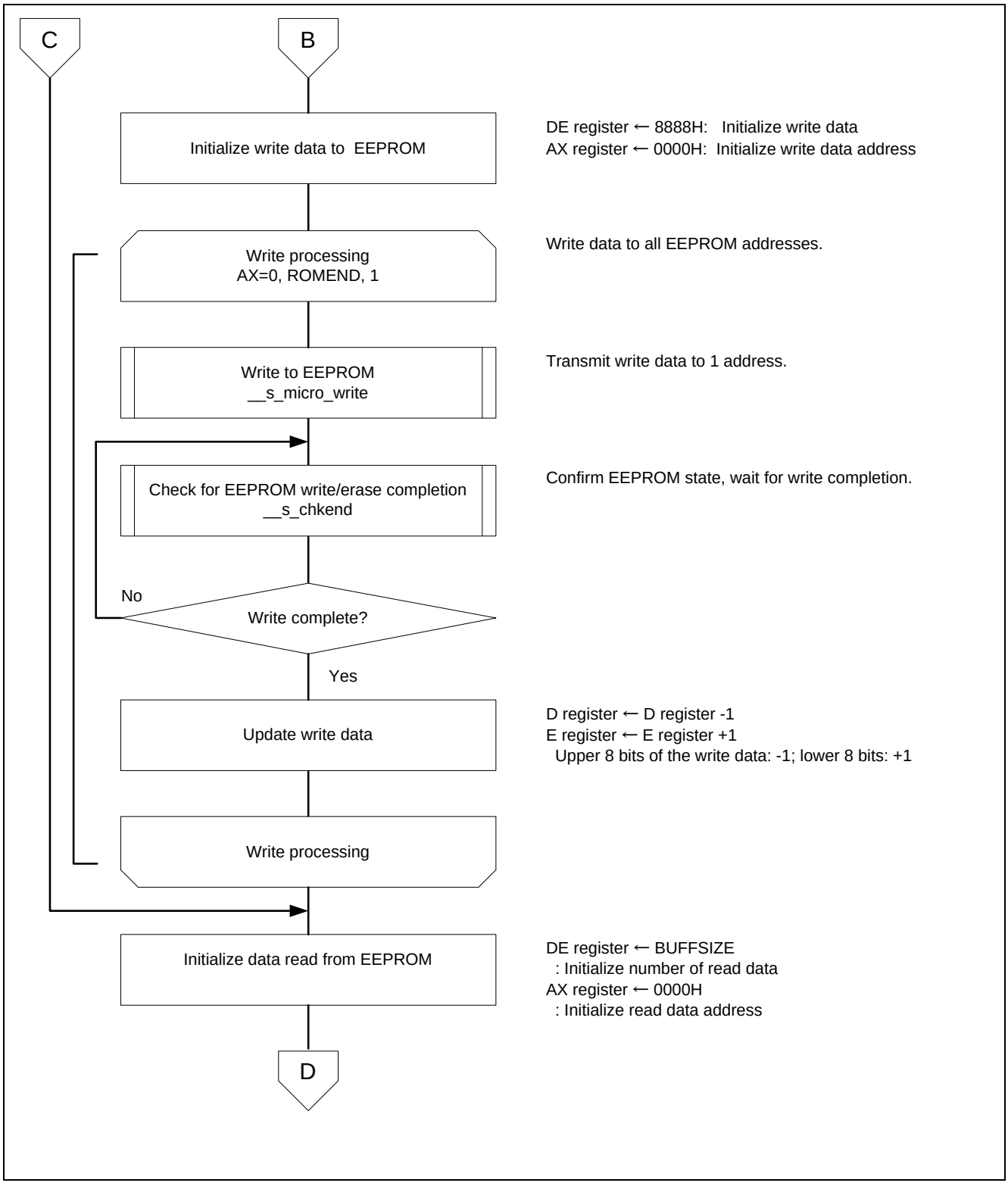


Figure 5.8 Main Processing (2/3)

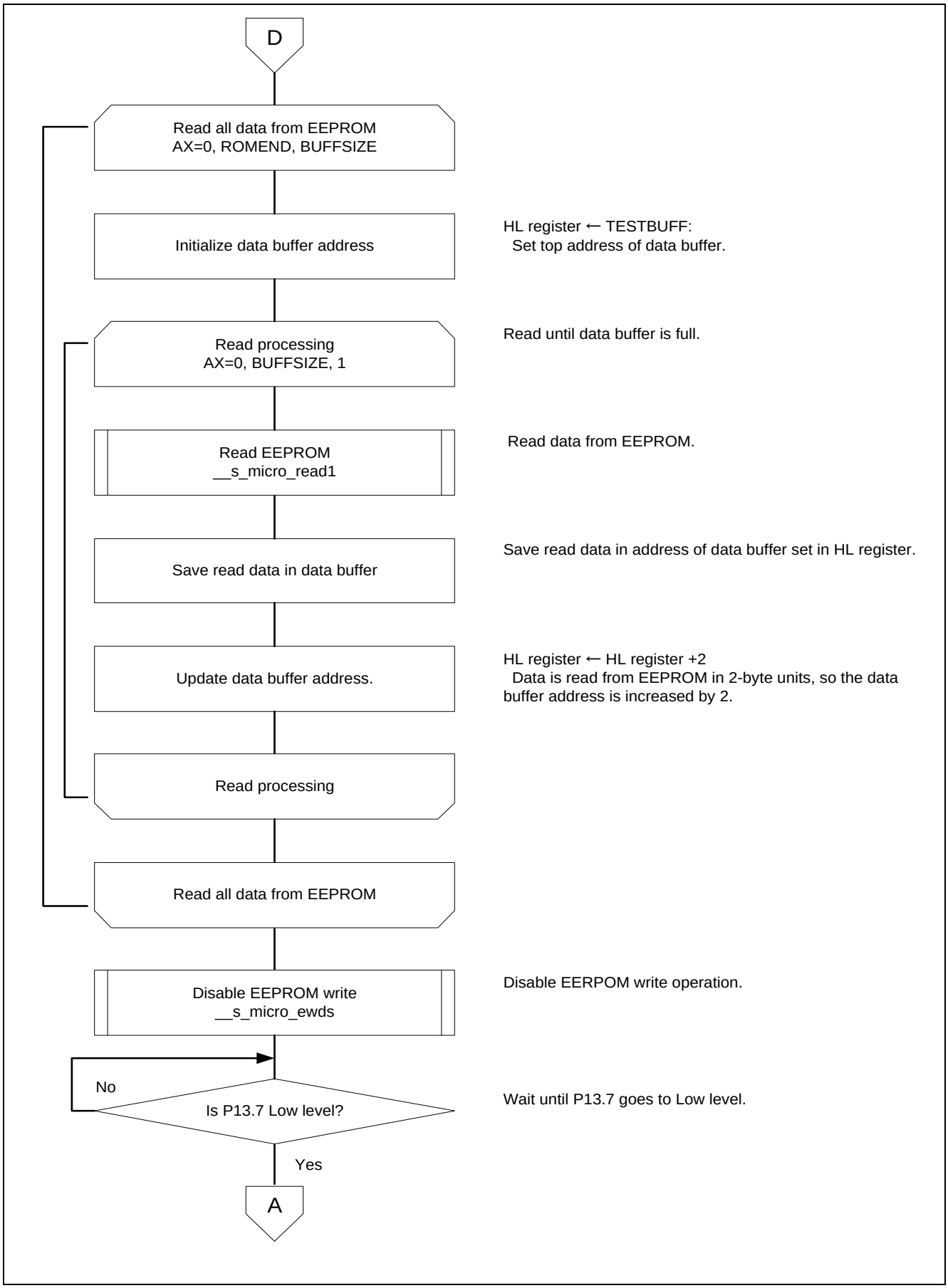


Figure 5.8 Main Processing (3/3)

SAU operation enable

・Serial channel start register 0 (SS0)

Enable serial array unit channel operation.

Symbol: SS0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SS01	SS00
0	0	0	0	0	0	0	1

Bit 0

SS00	Operation start trigger of channel
0	No trigger operation
1	Sets the SE0n bit to 1 and starts communication operation.

Note: For detailed description on how to set registers, refer to RL78/G10 Users Manual (Hardware Version).

SAU interrupt mask setting

・Interrupt mask flag register (MK0L)

Set interrupt mask.

Symbol: MK0L

7	6	5	4	3	2	1	0
TMMK00	TMMK01H	SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	PMK1	PMK0	WDTIMK
x	x	x	x	0	x	x	x

Bit 3

CSIMK00	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Note: For detailed description on how to set registers, refer to RL78/G10 Users Manual (Hardware Version).

5.7.6 Data Read Process from Specified EEPROM Address

Figure 5.9 shows the flowchart for the read process that reads data from a specified EEPROM address.

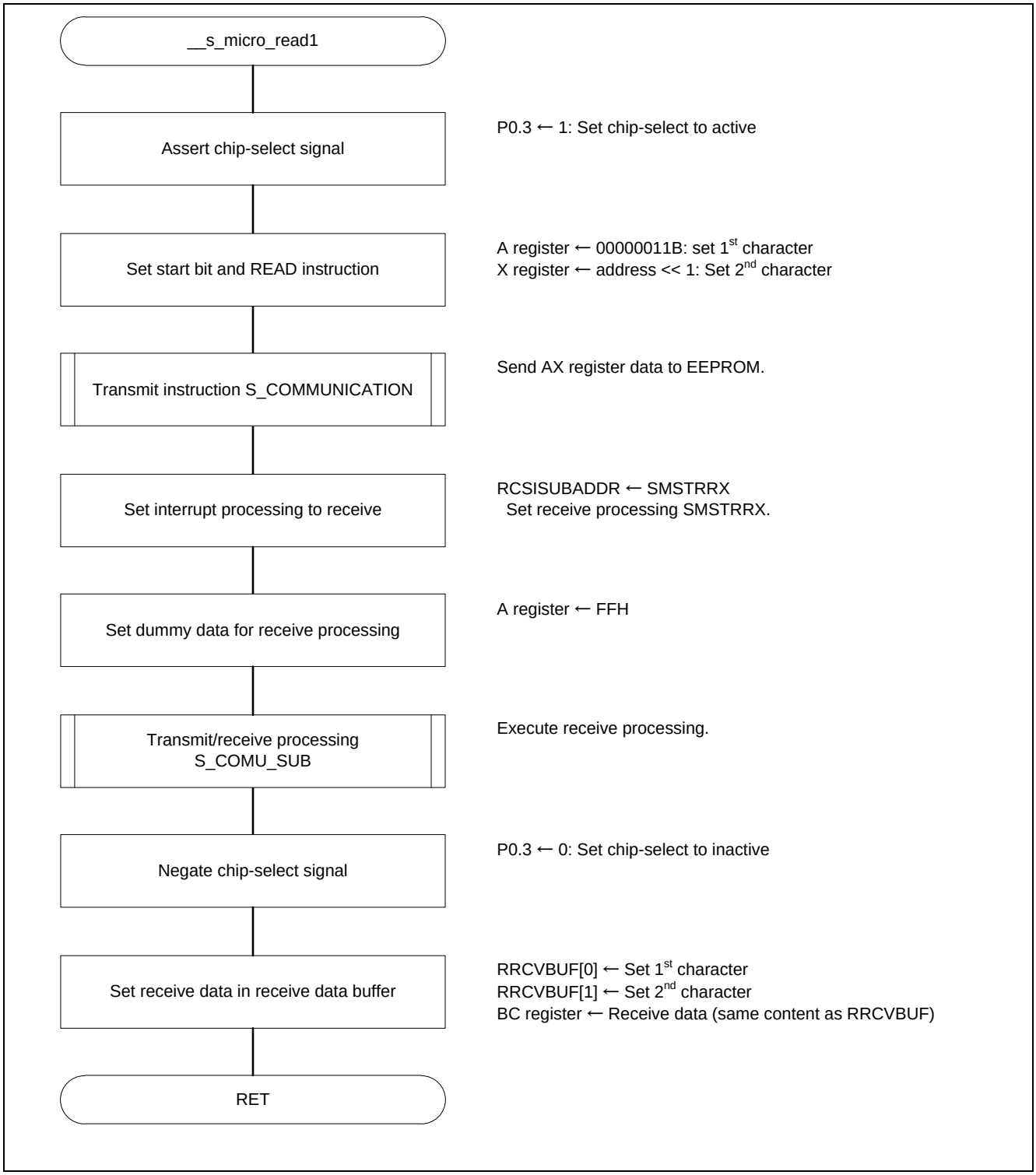


Figure 5.9 Data Read Process from Specified EEPROM Address

5.7.7 Data Write Process to Specified EEPROM Address

Figure 5.10 shows the flowchart for the write process that writes data from a specified EEPROM address.

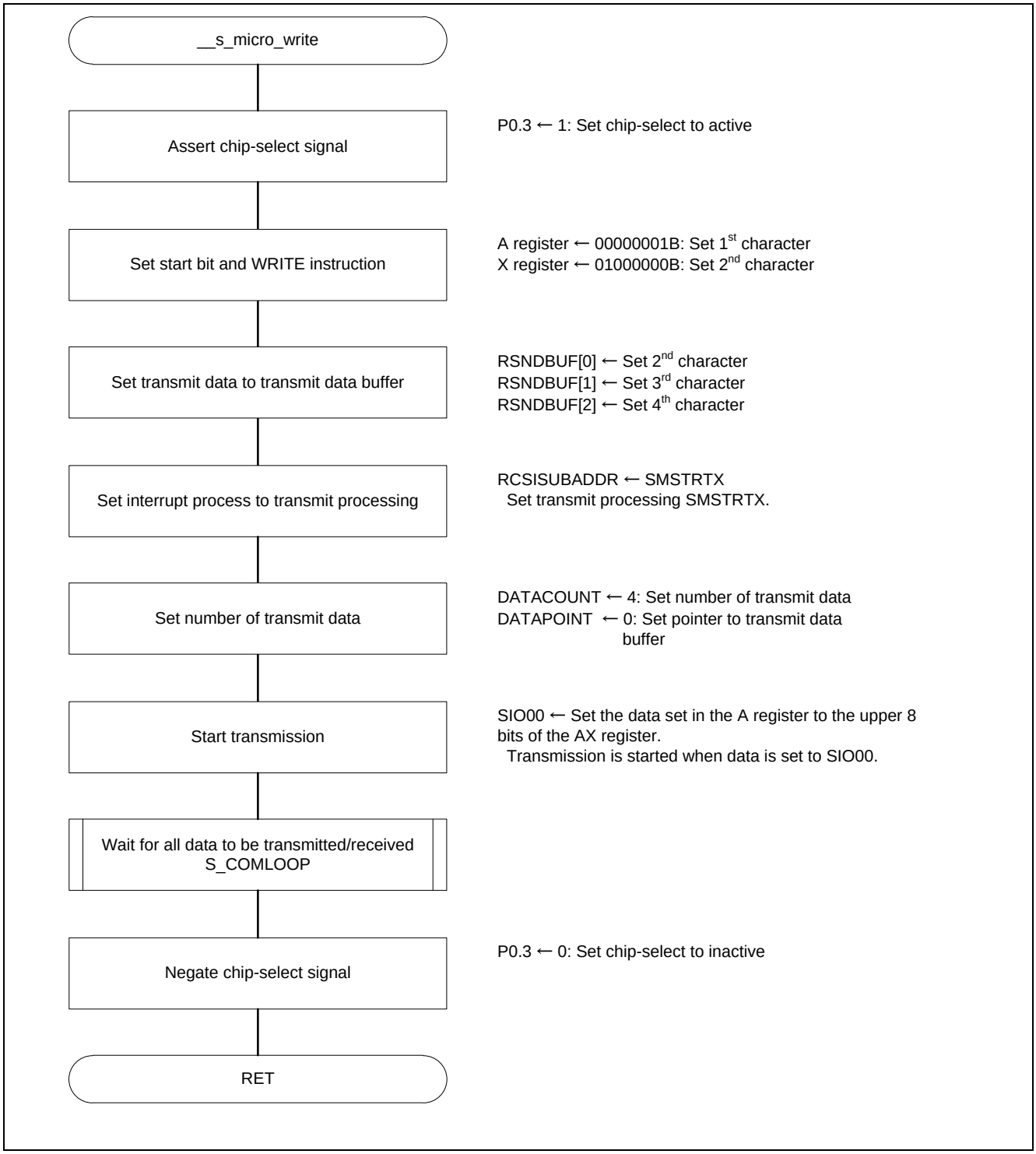


Figure 5.10 Data Write Process to Specified EEPROM Address

SAU0 channel 0 transmit data setting

・Serial data register 0 (SDR00L (SIO00))

Set transmit data.

Symbol: SDR00H (SIO00)

7	6	5	4	3	2	1	0

Note: For detailed description on how to set registers, refer to RL78/G10 Users Manual (Hardware Version).

5.7.8 EEPROM Write Enabled Status Processing

Figure 5.11 shows the flowchart for the processing which puts the EEPROM in the write enabled state.

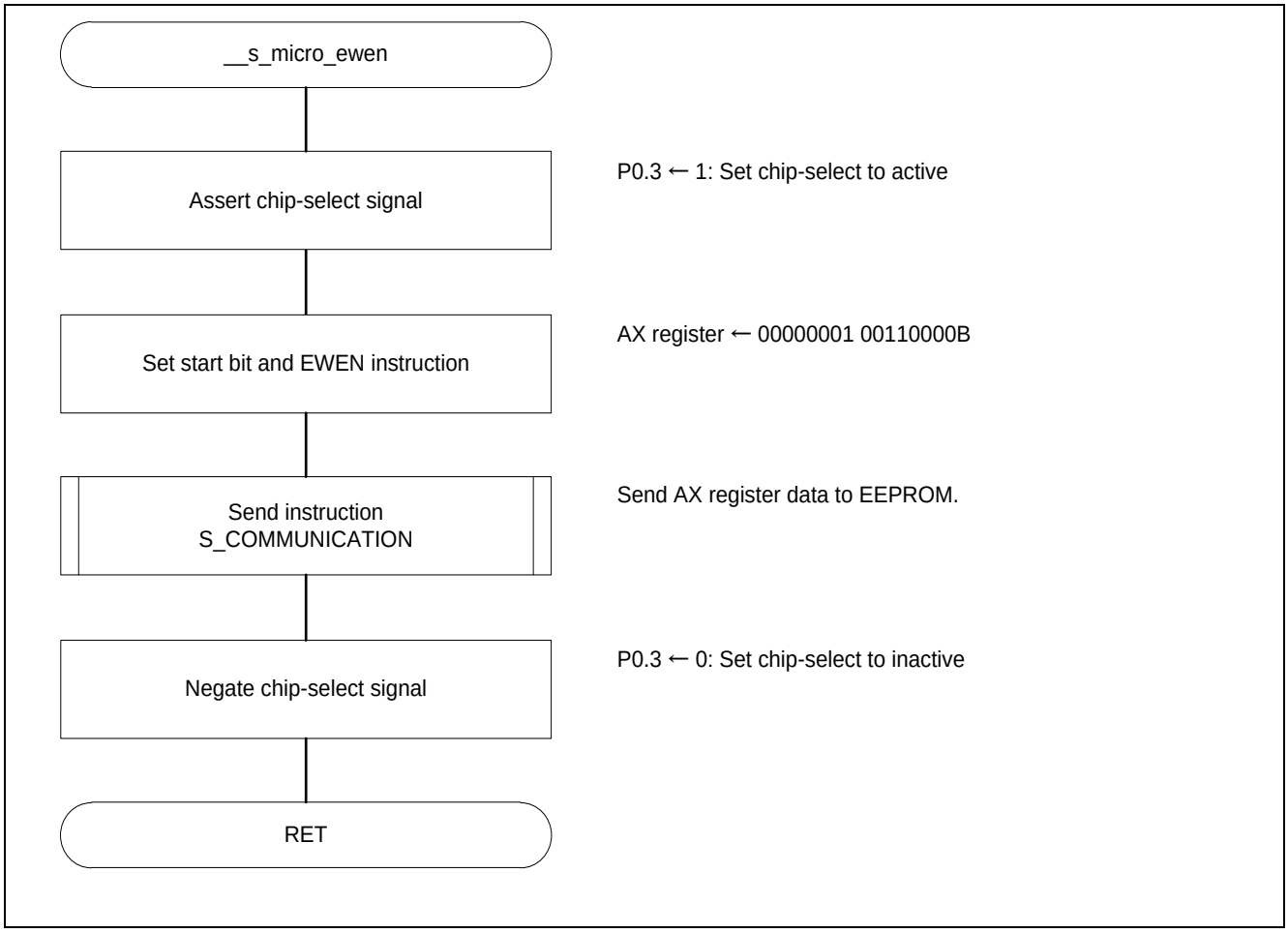


Figure 5.11 EEPROM Write Enabled Status Processing

5.7.9 EEPROM Write Disabled Status Processing

Figure 5.12 shows the flowchart for the processing which puts the EEPROM in the write disabled state.

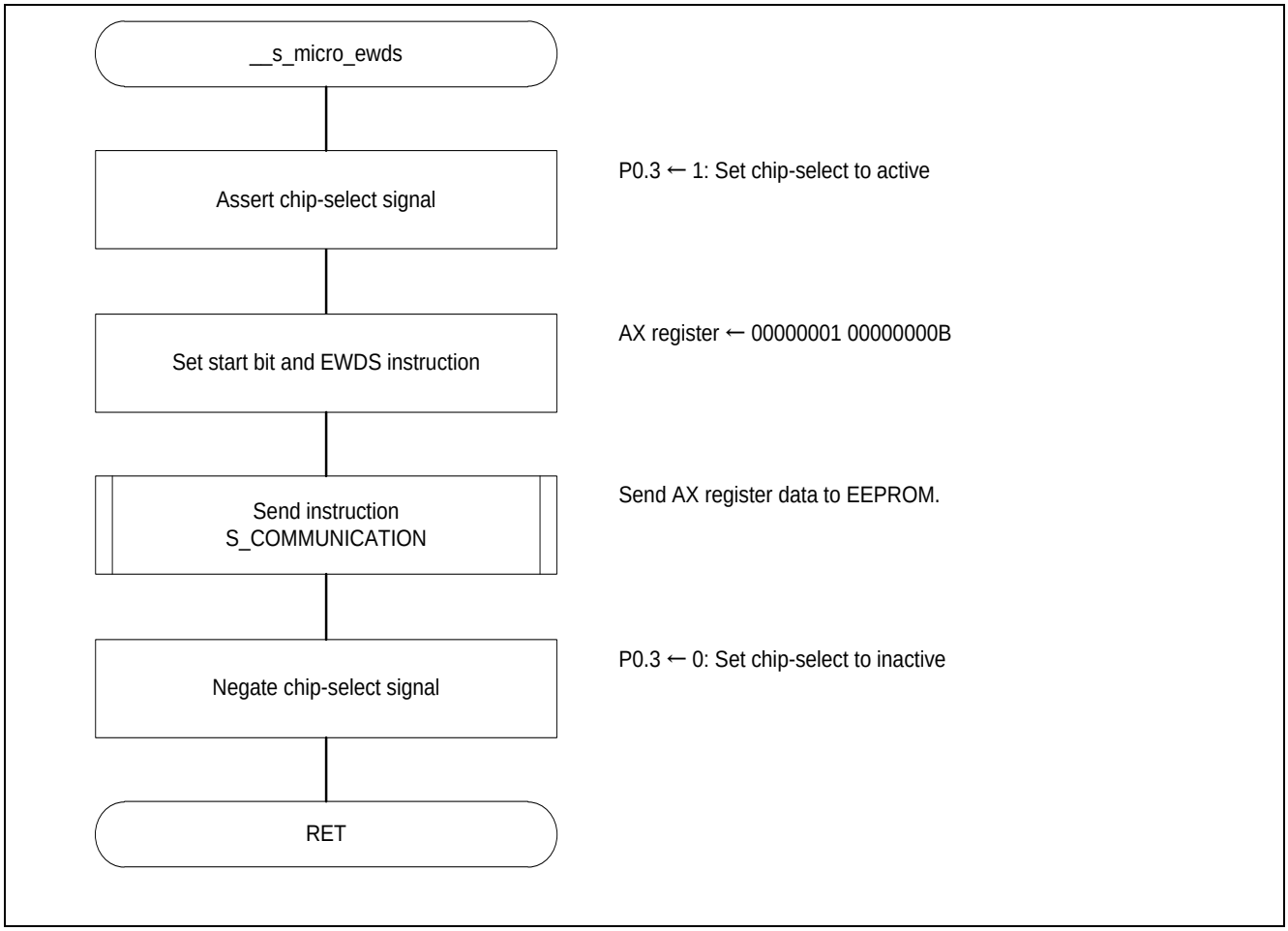


Figure 5.12 EEPROM Write Disabled Status Processing

5.7.10 EEPROM Erase All Areas Processing

Figure 5.13 shows the flowchart for the processing to erase all areas on the EEPROM chip.

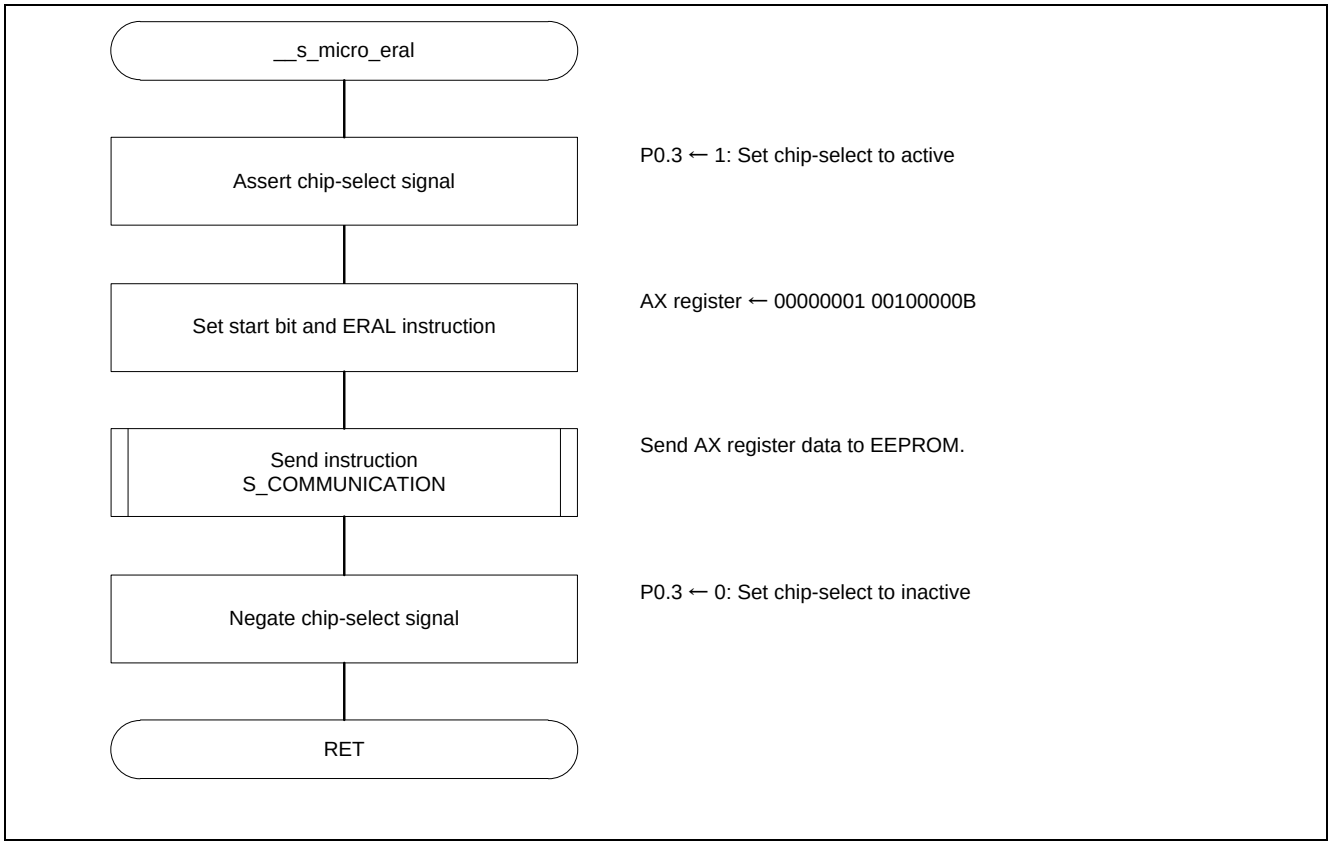


Figure 5.13 EEPROM Erase All Areas Processing

5.7.11 EEPROM Data Write/Erase All Areas Completion Wait Processing

Figure 5.14 shows the flowchart for the wait process of EEPROM data write/ erase all areas completion.

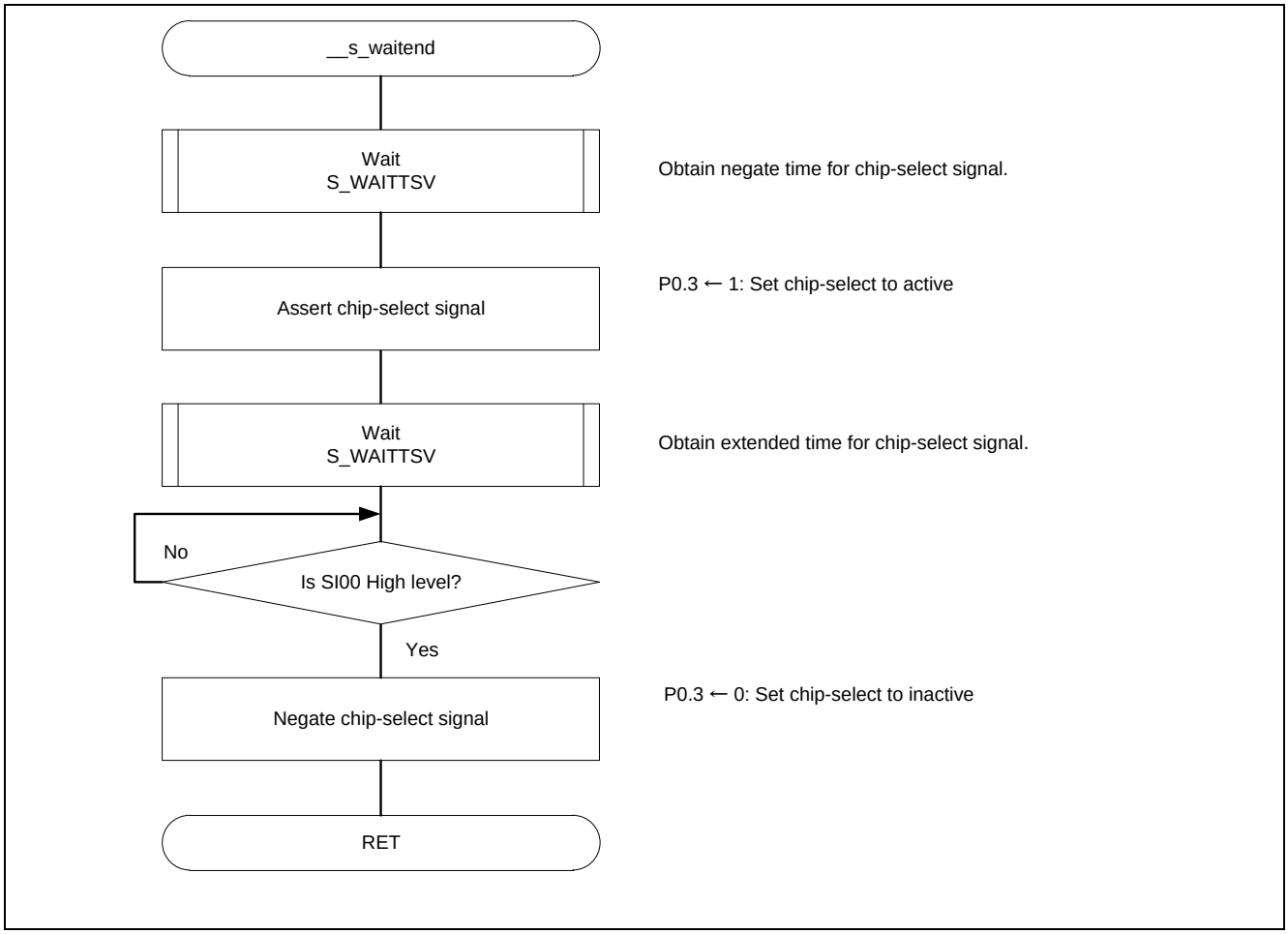


Figure 5.14 EEPROM Data Write/Erase All Areas Completion Wait Processing

5.7.12 EEPROM Data Write/Erase All Areas Completion Status Read Processing

Figure 5.15 shows the flowchart for the complete status read process of EEPROM data write/erase all areas.

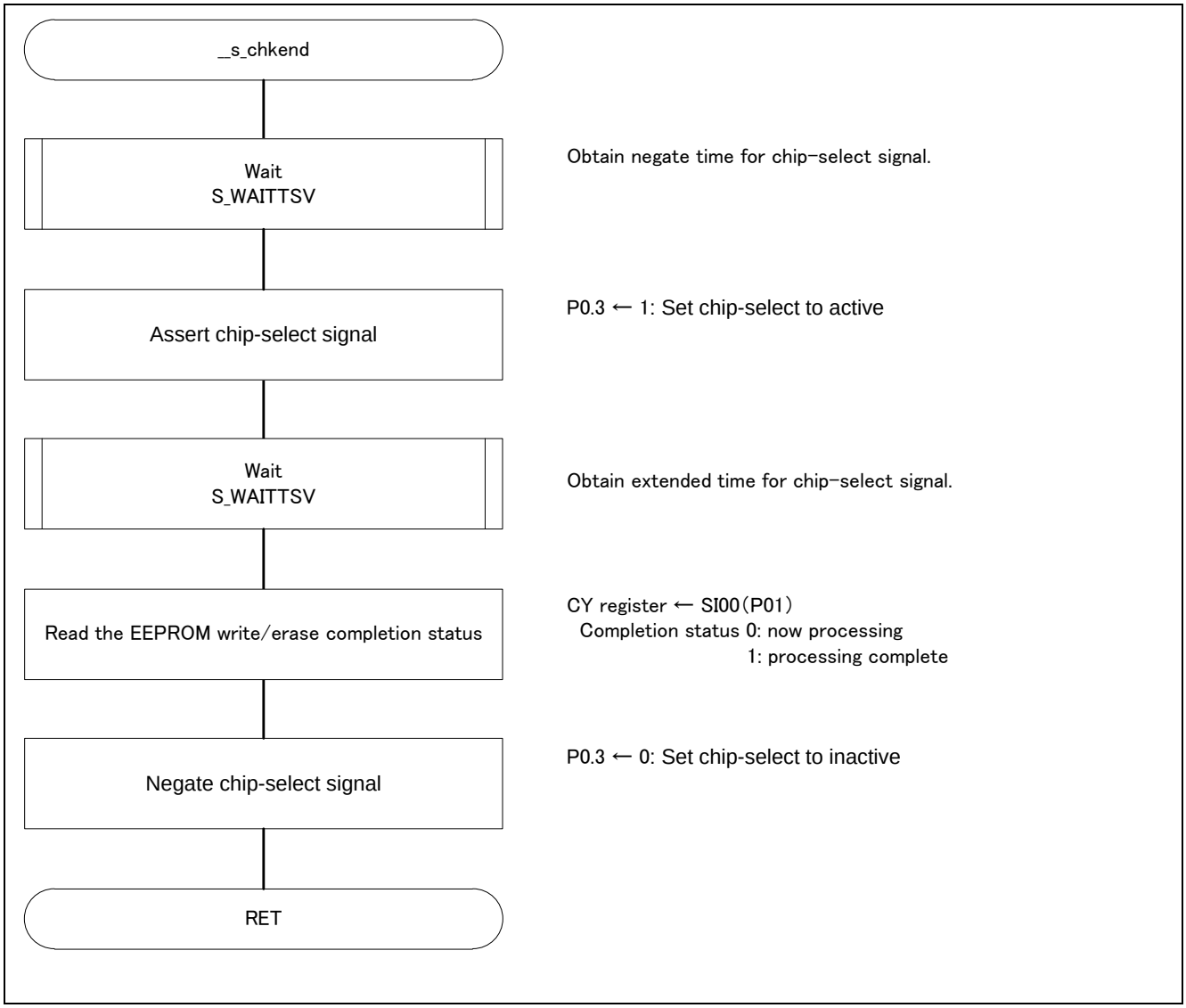


Figure 5.15 EEPROM Data Write/Erase All Completion Status Read Processing

5.7.13 INTCSI00 Interrupt Processing

Figure 5.16 shows the flowchart for INTCSI00 interrupt processing.

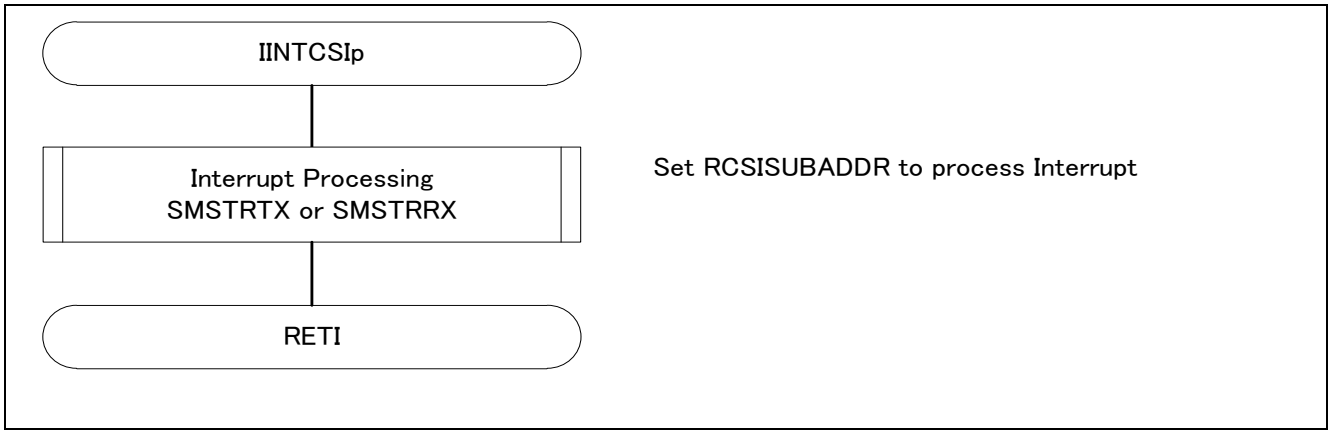


Figure 5.16 INTCSI00 Interrupt Processing

5.7.14 Transmit Processing

Figure 5.17 shows the flowchart for transmit processing.

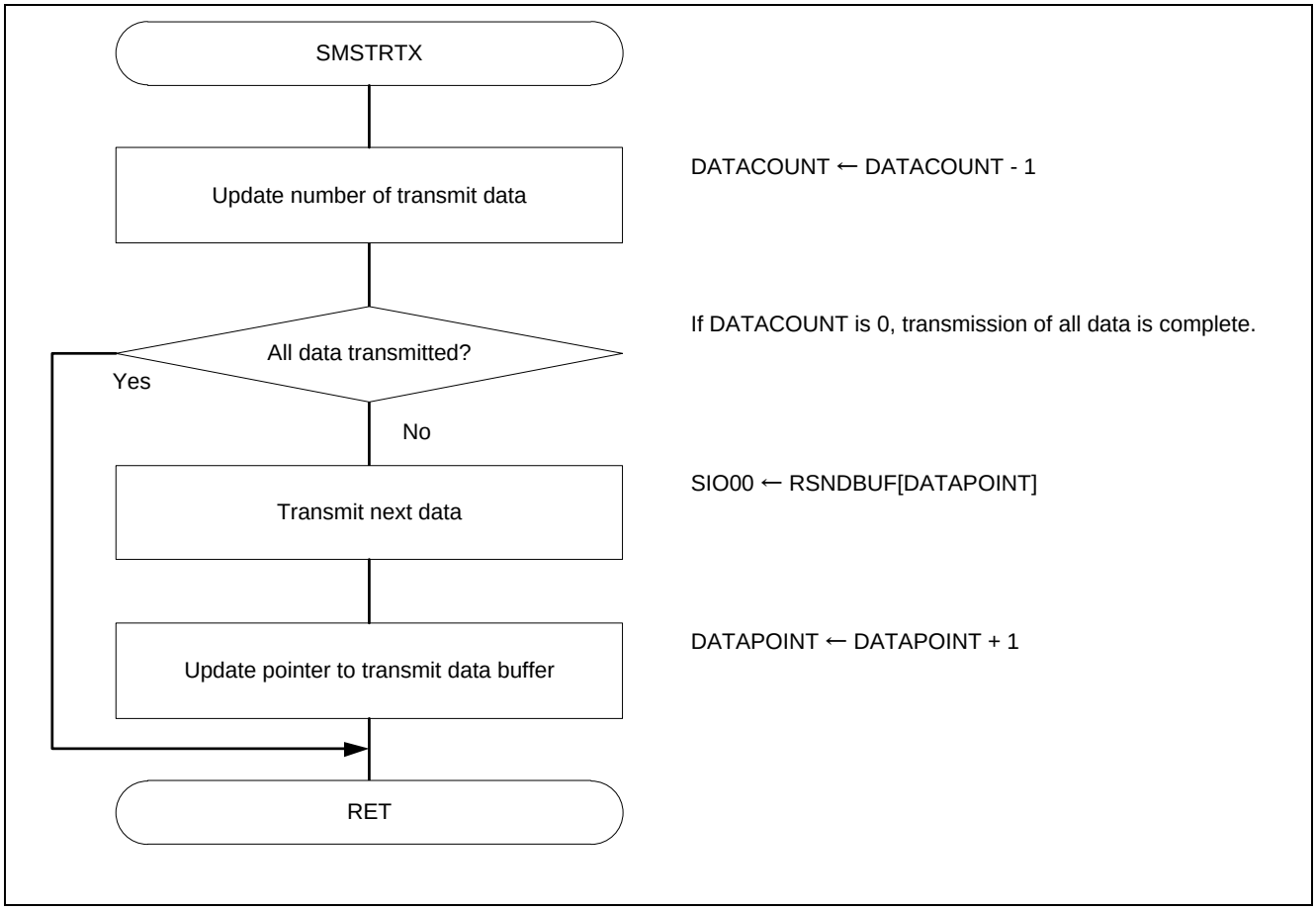


Figure 5.17 Transmit Processing

5.7.15 Receive Processing

Figure 5.17 shows the flowchart for receive processing.

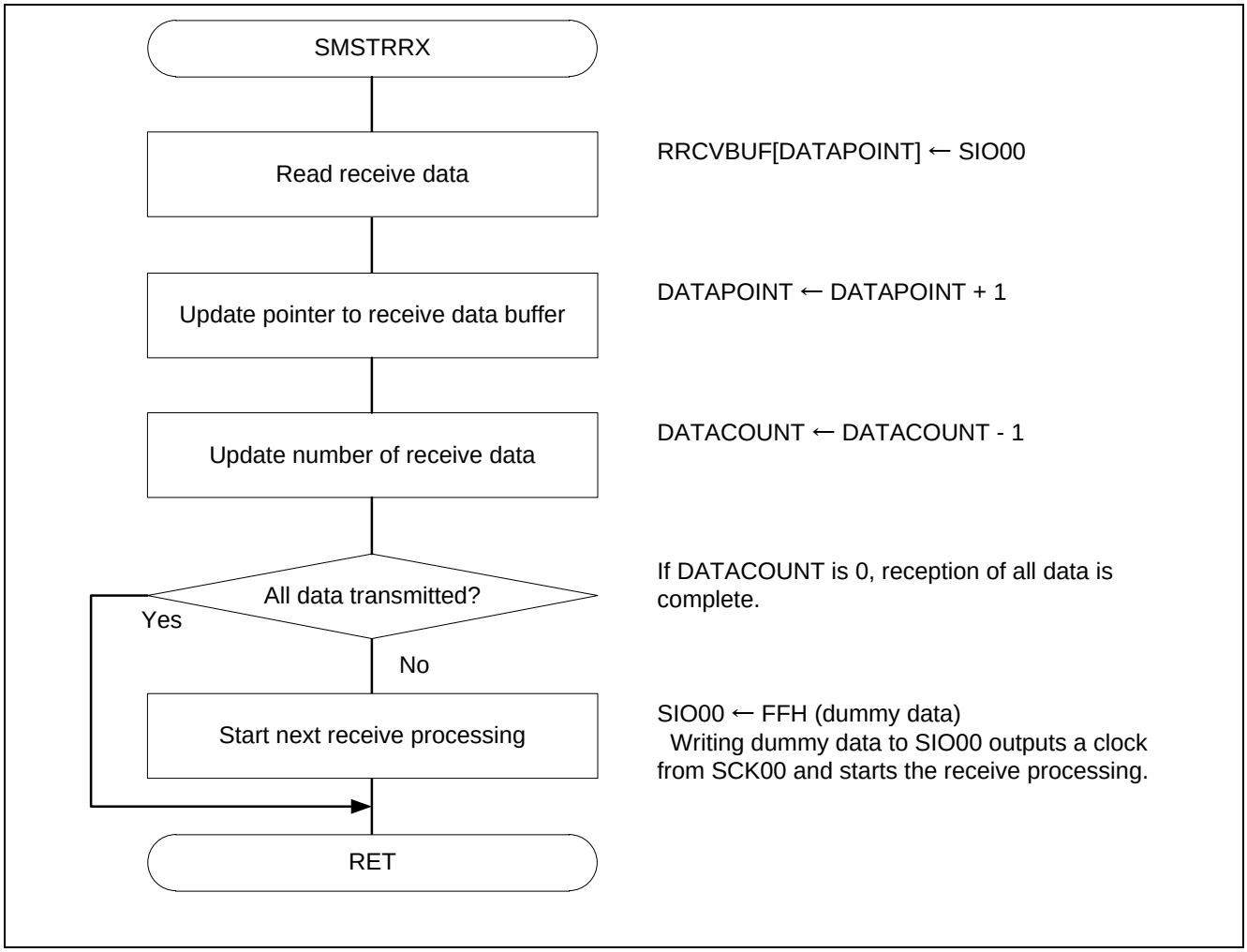


Figure 5.18 Receive Processing

Obtain SAU0 channel 0 receive data

・Serial data register 0 (SDR00L(SIO00))

Obtain receive data.

Symbol: SDR00H(SIO00)

7	6	5	4	3	2	1	0

Note: For detailed description on how to set registers, refer to RL78/G10 Users Manual (Hardware Version).

5.7.16 EEPROM Instruction Transmit Processing

Figure 5.19 shows the flowchart for EEPROM instruction transmit processing.

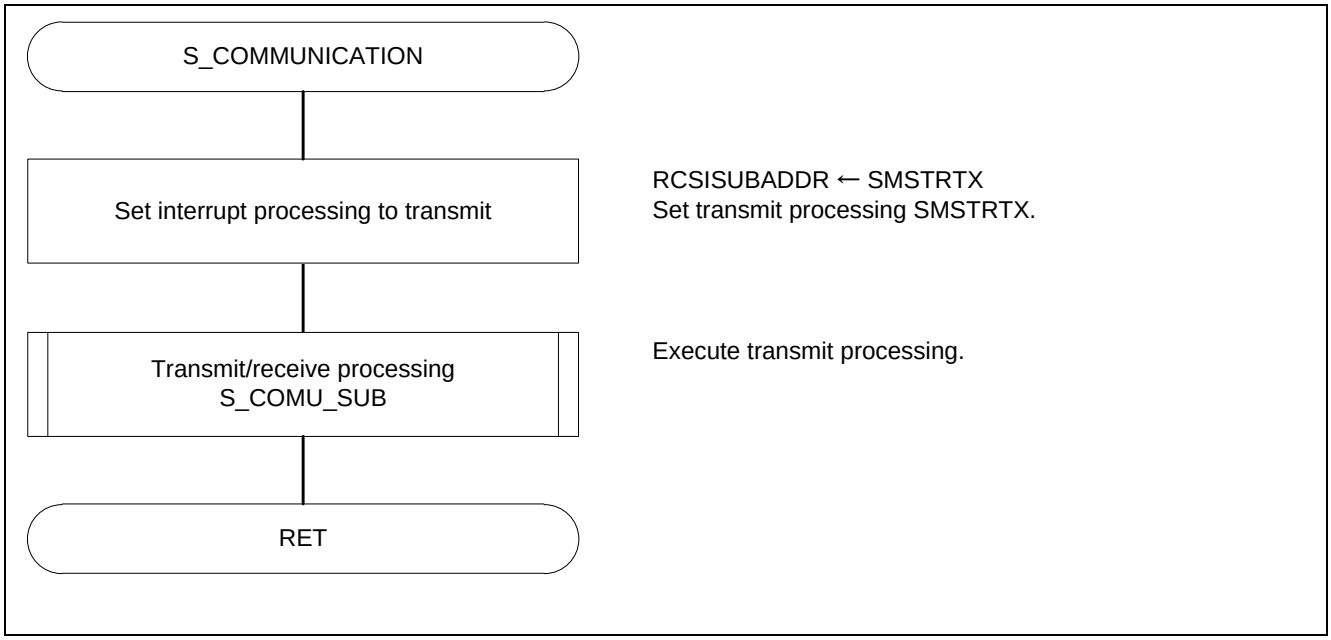


Figure 5.19 EEPROM Instruction Transmit Processing

5.7.17 EEPROM Transmit/Receive Processing

Figure 5.20 shows the flowchart for the EEPROM transmit/receive processing.

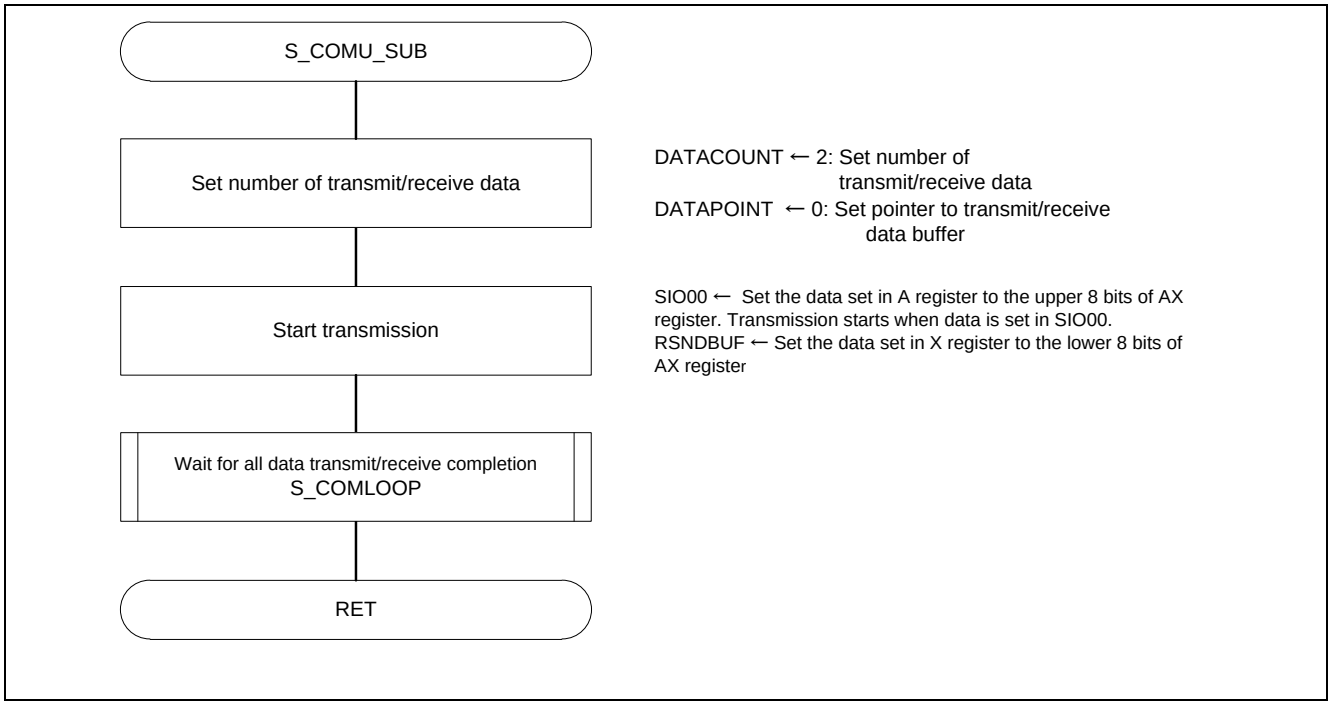


Figure 5.20 EEPROM Transmit/Receive Processing

5.7.18 All Data Transmit/Receive Complete Wait Processing

Figure 5.21 shows the flowchart for the all data transmit/receive complete wait processing.

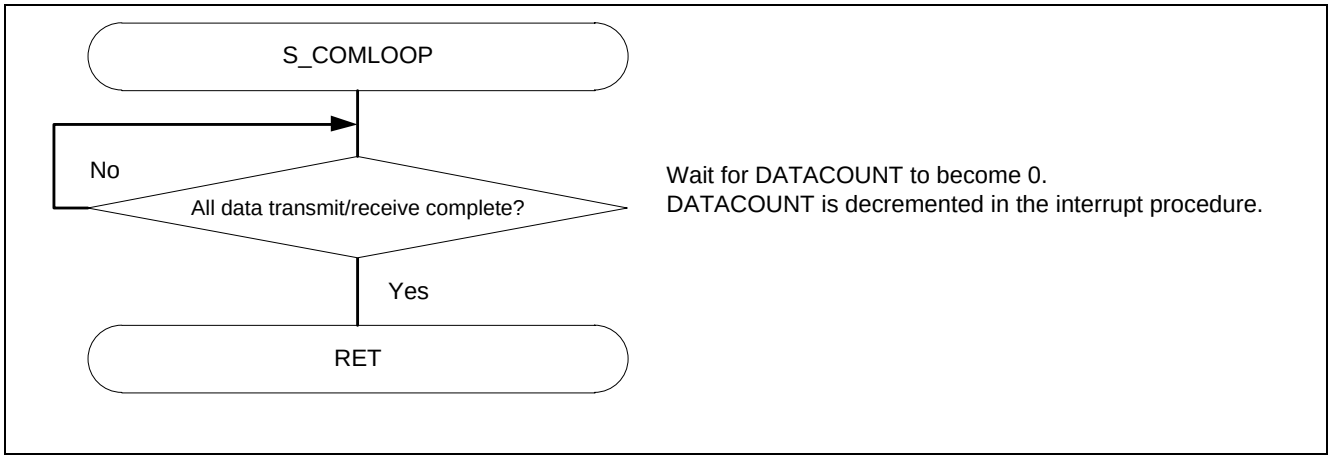


Figure 5.21 All Data Transmit/Receive Complete Wait Processing

5.7.19 Wait Time Processing

Figure 5.22 shows the flowchart for the wait time processing.

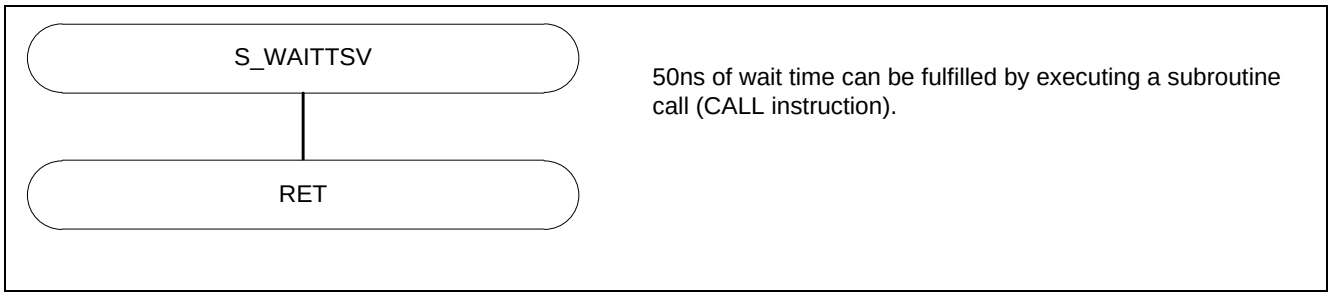


Figure 5.22 Wait Time Processing

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G10 User's Manual: Hardware Rev.3.00 (R01UH0384E)

RL78 Family User's Manual: Software Rev.2.20 (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

Website and Support

Renesas Electronics Website

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Inquiries

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Revision Record	RL78/G10 EEPROM Control via Microwire Communications

Rev.	Date	Description	
		Page	Summary
1.00	2016.1.28	—	First edition issued

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

- Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
  - The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

- The state of the product is undefined at the moment when power is supplied.
  - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
    In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
    In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

- Access to reserved addresses is prohibited.
  - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

- After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
  - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

- Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
  - The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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