RL78/G10

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Air-Conditioned Clothing with Automatic Airflow Adjustment Function

Introduction

This application note explains how to realize air-conditioned clothing in which the airflow is automatically adjusted according to the temperature within the air-conditioned clothing.

Target Device

RL78/G10

When applying the sample program covered in this application note to another microcontroller, modify the program according to the specifications of the microcontroller and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

The RL78/G10 acquires temperature data from a temperature sensor every 3 minutes when power is input, and controls a fan according to the temperature.

Temperature	Fan	PWM Output Duty Ratio
Lower than 20°C	Stopped	0%
20°C to 28°C	Low-speed rotation	20%
28°C to 35°C	Medium-speed rotation	50%
35°C or higher	High-speed rotation	100%

Figure 1.1 shows the system configuration outline.

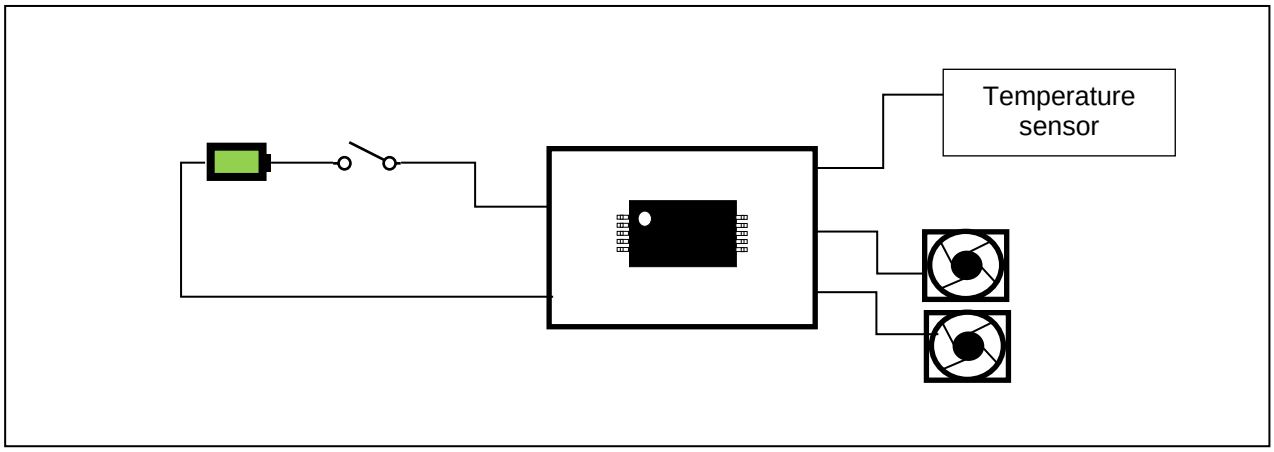


Figure 1.1 the system configuration

1.1 Temperature Sensor

In this application note, a temperature sensor is used having an output that changes in proportion to the change in temperature. When actually designing the circuit, be sure to satisfy the electrical characteristics.

Temperature sensor used:
Measurement temperature range: -40°C to +125°C
Relationship between voltage and temperature: Vout = 10mV/°C × (Temperature°C) + 500mV
For example, 100 mV at -40°C, 500 mV at 0°C, 750 mV at +25°C.

1.2 DC Fan Motor

In this application note, the rotation speed of the fan motor is controlled by changing the duty ratio of the PWM output. In order to suppress power losses in fan driving, a power MOSFET capable of fast switching and with a low ON-resistance is used. When actually building a circuit, the design should satisfy the electrical characteristics of the model used.

2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G10 (R5F10Y47ASP)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 5 MHz • CPU/peripheral hardware clock: 5 MHz
Operating voltage	5.0 V (can run on a voltage range of 2.2 V to 5.5 V.) SPOR operation: Min 2.70 V at fall, Max 3.02 V at rise
Integrated development environment (CS+)	CS+ for CC V6.01.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.06.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V5.1.0.022 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.06.00 from Renesas Electronics Corp.

3. Related Application Note

An application note related to this application note is indicated below.

The following application note employs assembler language, but the initial setting method should be referenced.

RL78/G10 Initialization CC-RL (R01AN2668E) Application Note

4. Hardware Descriptions

4.1 Hardware Configuration

Figure 4.1 shows an example of the hardware configuration for the system described in this application note.

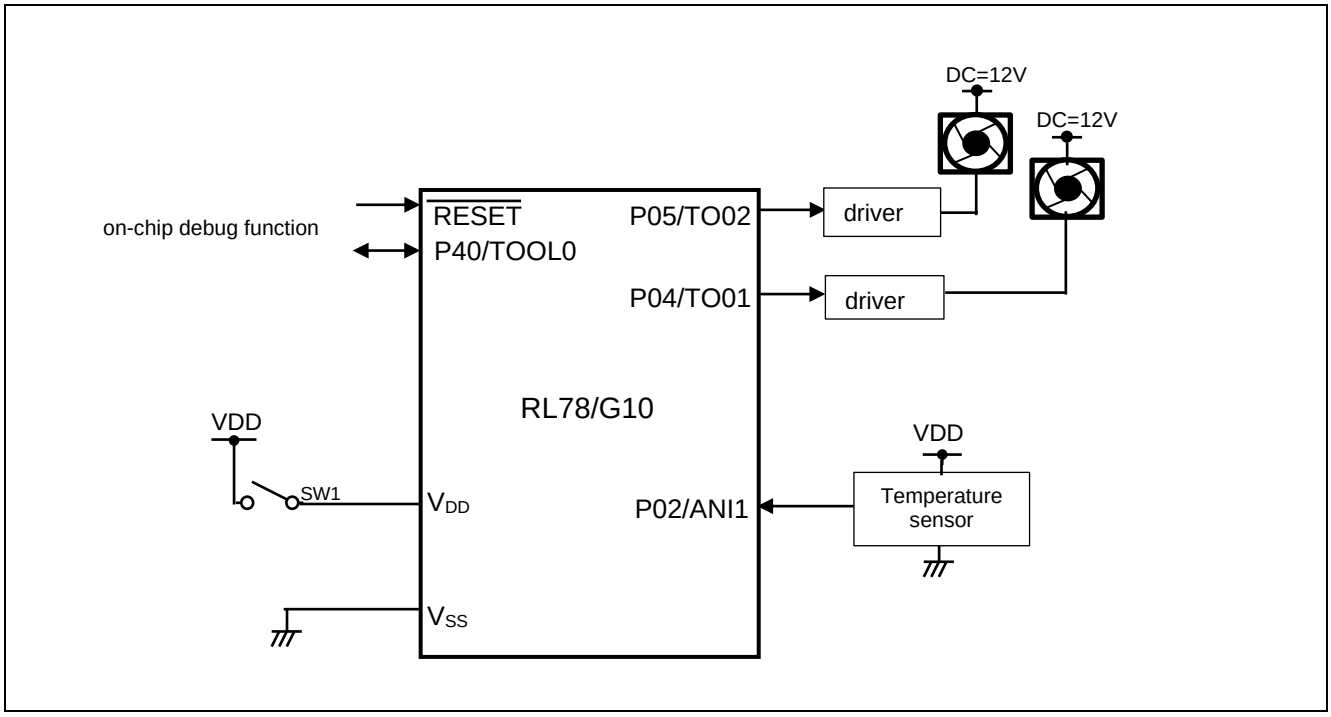


Figure 4.1 the hardware configuration used for this application

Notes: 1. The above figure is a simplified circuit image for showing the outline of the connections. The actual circuit should be designed so that the pins are handled appropriately and that the electrical characteristics are satisfied (input-only ports should be each connected to V_{DD} or V_{SS} via a resistor).

2. VDD must be equal to or greater than the reset release voltage (V_{SPOR}) specified with SPOR.

4.2 List of Pins Used

Table 4.1 lists the pins used and their functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Description
P05/TO02	Output	Fan drive port (PWM output)
P04/TO01	Output	Fan drive port (PWM output)
P02/ANI1	Input	Analog input port for temperature sensor
P40/TOOL0	I/O	For on-chip debugging
P125/RESET	Input	For on-chip debugging

5. Software Descriptions

5.1 Operation Summary

In this application note, channels 0, 1, and 2 of the timer array unit are made to operate in concert, and PWM signals are output from P04 and P05. The analog voltage output from the temperature sensor every 3 minutes is A/D converted, the PWM output duty ratio is calculated, and the fan rotation speed is controlled.

5.2 List of Option Byte Settings

Table 5.1 shows the option byte settings.

Table 5.1 Option Byte Settings

Address	Setting	Description
000C0H	11101111B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H	11110111B	SPOR detection voltage: 2.90 V at fall; 2.84 V at rise
000C2H	11111011B	HOCO: 5 MHz
000C3H	10000101B	Enables the on-chip debugger.

5.3 List of Variables

Table 5.2 lists the global variables.

Table 5.2 Global Variables

Type	Variable Name	Contents	Function Used
int16_t	vout_value1	Temperature data1	main()
int16_t	vout_value2	Temperature data2	main()
int16_t	vout_value3	Temperature data3	main()
uint16_t	g_adc_ResultT	A/D converter data	main()
int16_t	temperature_value	Temperature data	main()

5.4 List of Functions (Subroutines)

Table 5.3 lists the functions (subroutines).

Table 5.3 List of Functions (Subroutines)

Function (Subroutine) Name	Outline
fan_speed_zero()	Control to stop fan rotation
fan_speed_slow()	Control to set fan rotation speed to low
fan_speed_mid()	Control to set fan rotation speed to medium
fan_speed_high()	Control to set fan rotation speed to high
R_TAU0_Channel3_Start()	Start count for timer array unit channel 3
R_TAU0_Channel0_Start()	Start count for timer array unit channels 0, 1, 2

5.5 Function Specifications

This section gives the specifications of the functions used in the sample program.

[Function Name] R_TAU0_Channel0_Start		
Synopsis	Starts operation of the timer array unit channel 0,1,2.	
Header	r_cg_tau.h	
Declaration	void R_TAU0_Channel0_Start(void)	
Explanation	Starts operation of the timer array unit channel 0,1,2.	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] R_TAU0_Channel3_Start		
Synopsis	Start operation of the timer array unit channel 3.	
Header	r_cg_tau.h	
Declaration	void R_TAU0_Channel3_Start(void)	
Explanation	Start operation of the timer array unit channel 3.	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] fan_speed_zero		
Synopsis	Stop to fan driving.	
Header	-	
Declaration	void fan_speed_zero(void)	
Explanation	-	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] fan_speed_low		
Synopsis	Fan driving for low speed	
Header	-	
Declaration	void fan_speed_low(void)	
Explanation		
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] fan_speed_mid		
Synopsis	Fan driving for middle speed	
Header		
Declaration	void fan_speed_mid(void)	
Explanation		
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] fan_speed_high		
Synopsis	Fan driving for high speed	
Header		
Declaration	void fan_speed_high(void)	
Explanation		
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] main		
Synopsis	Main function	
Declaration	—	
Explanation	Main processing function of the sample program.	
Arguments	None	
Return value	None	
Remarks	None	

5.6 Flowcharts

Figure 5.1 shows an overall flow of the sample program described in this application note.

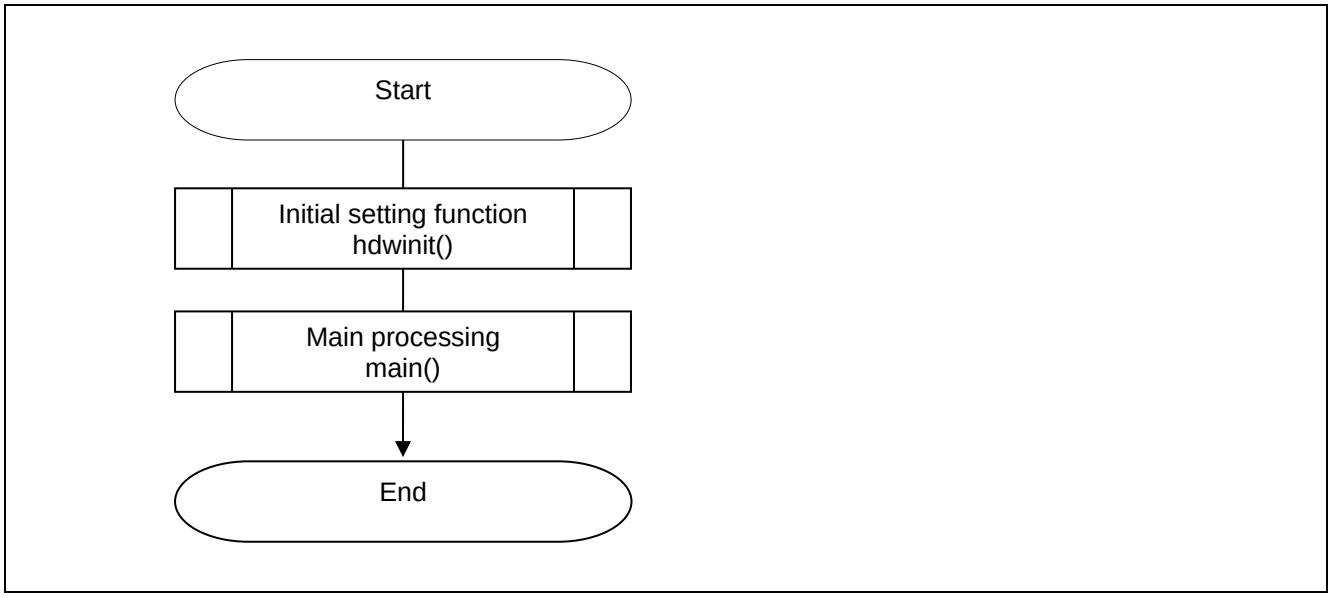


Figure 5.1 the overall flow

5.6.1 Initial Setting Function

Figure 5.2 shows the flowchart of the initial setting function.

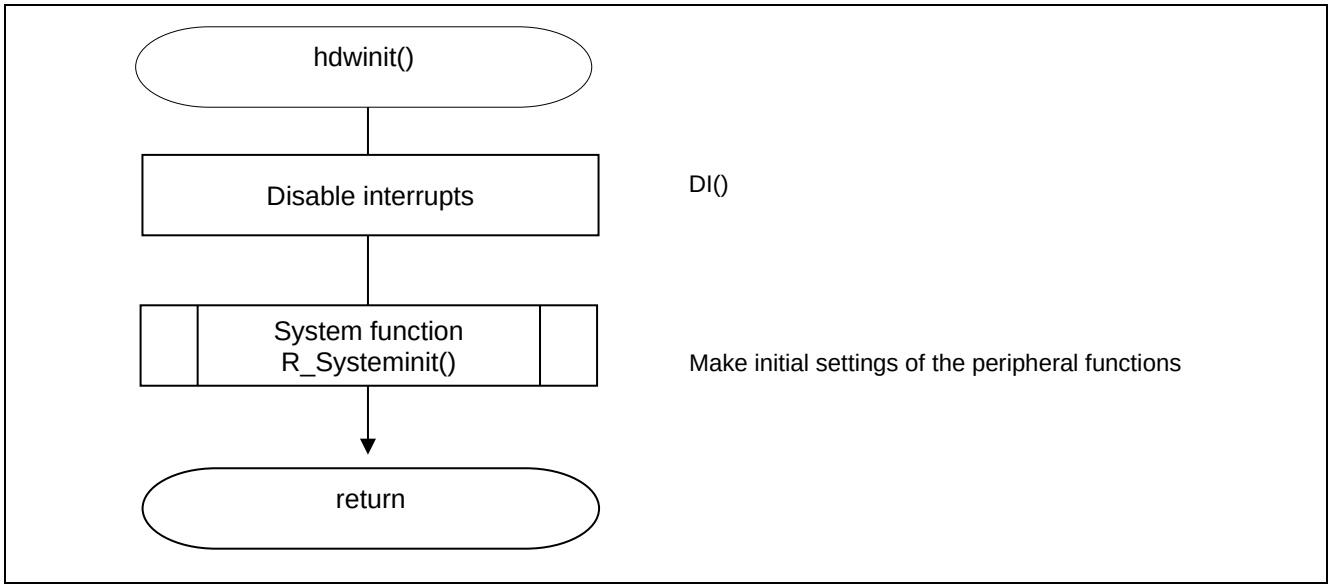


Figure 5.2 Initial Setting Function

5.6.2 System Function

Figure 5.3 shows the flowchart of the system function.

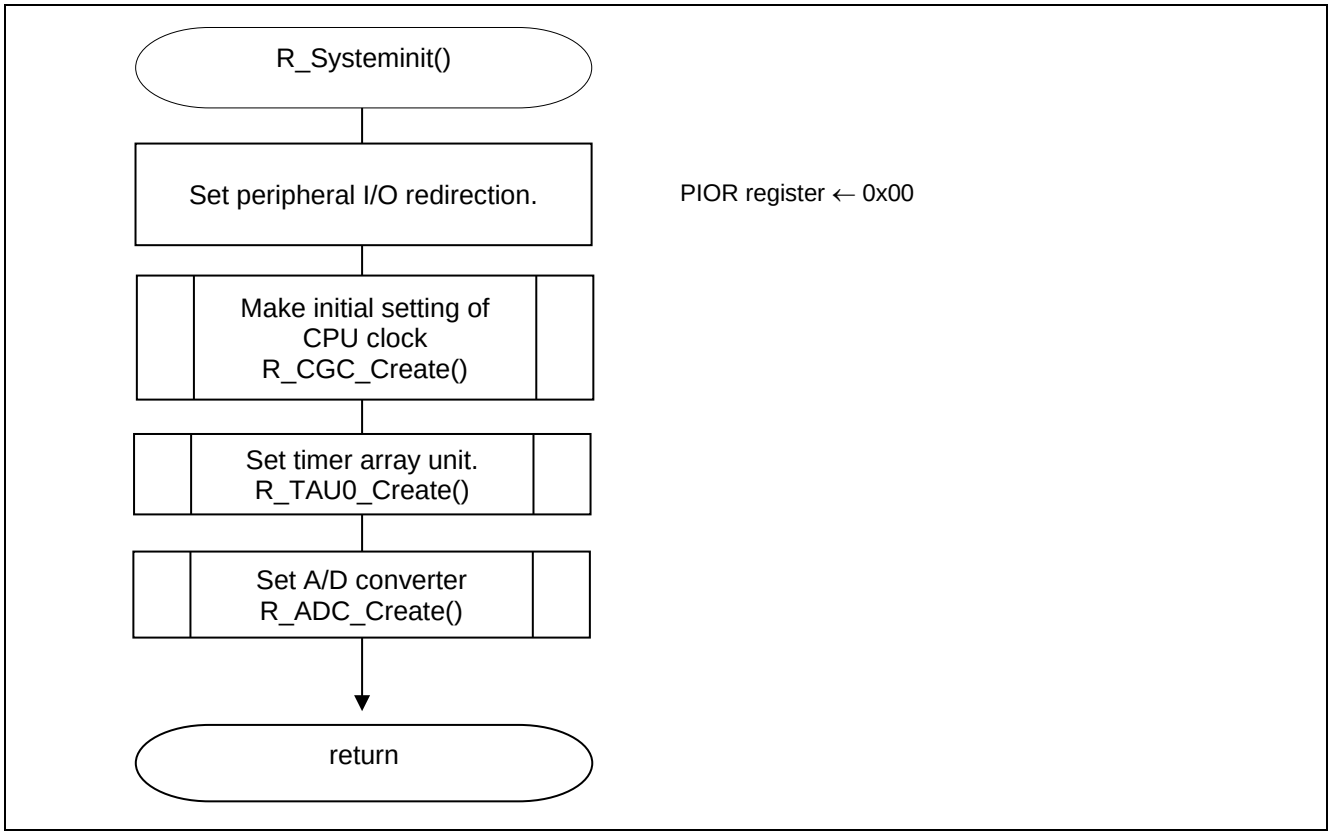


Figure 5.3 System Function

5.6.3 CPU Clock Setup

Figure 5.4 shows the flowchart for setting up the CPU clock.

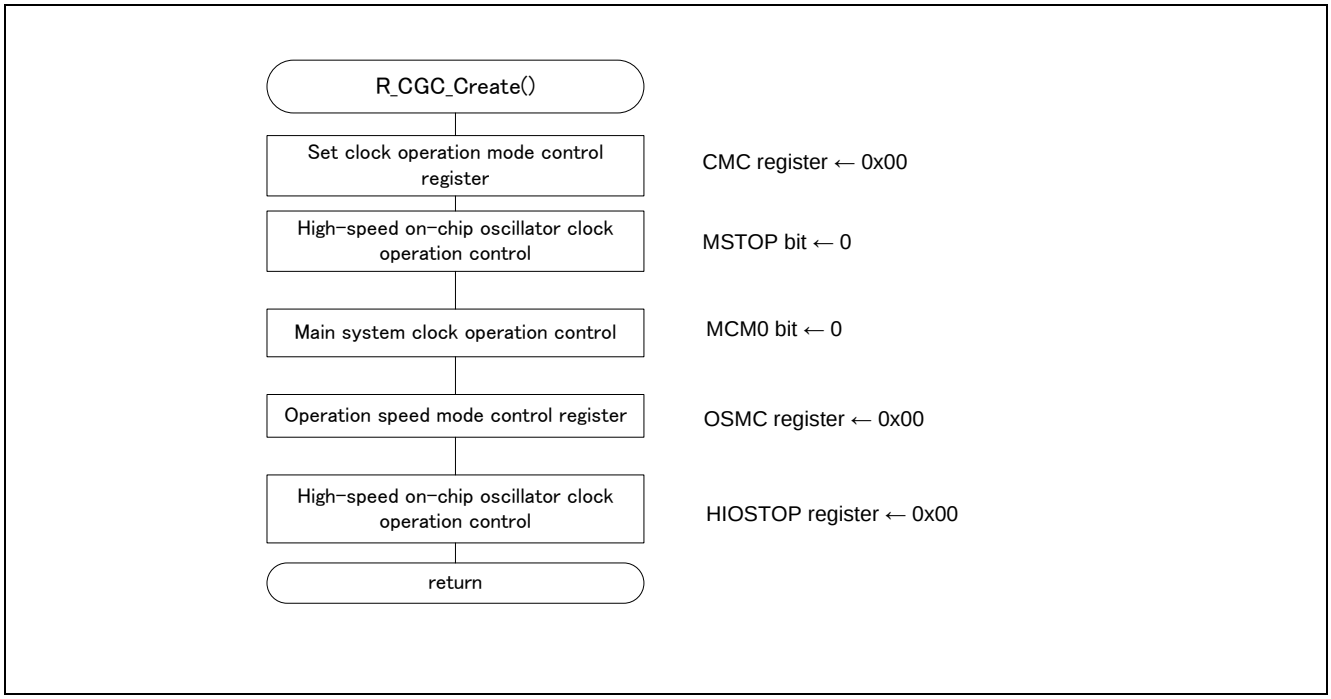


Figure 5.4 CPU Clock Setup

5.6.4 A/D converter Setup

Figure 5.5 shows the flowchart for setting up the A/D converter.

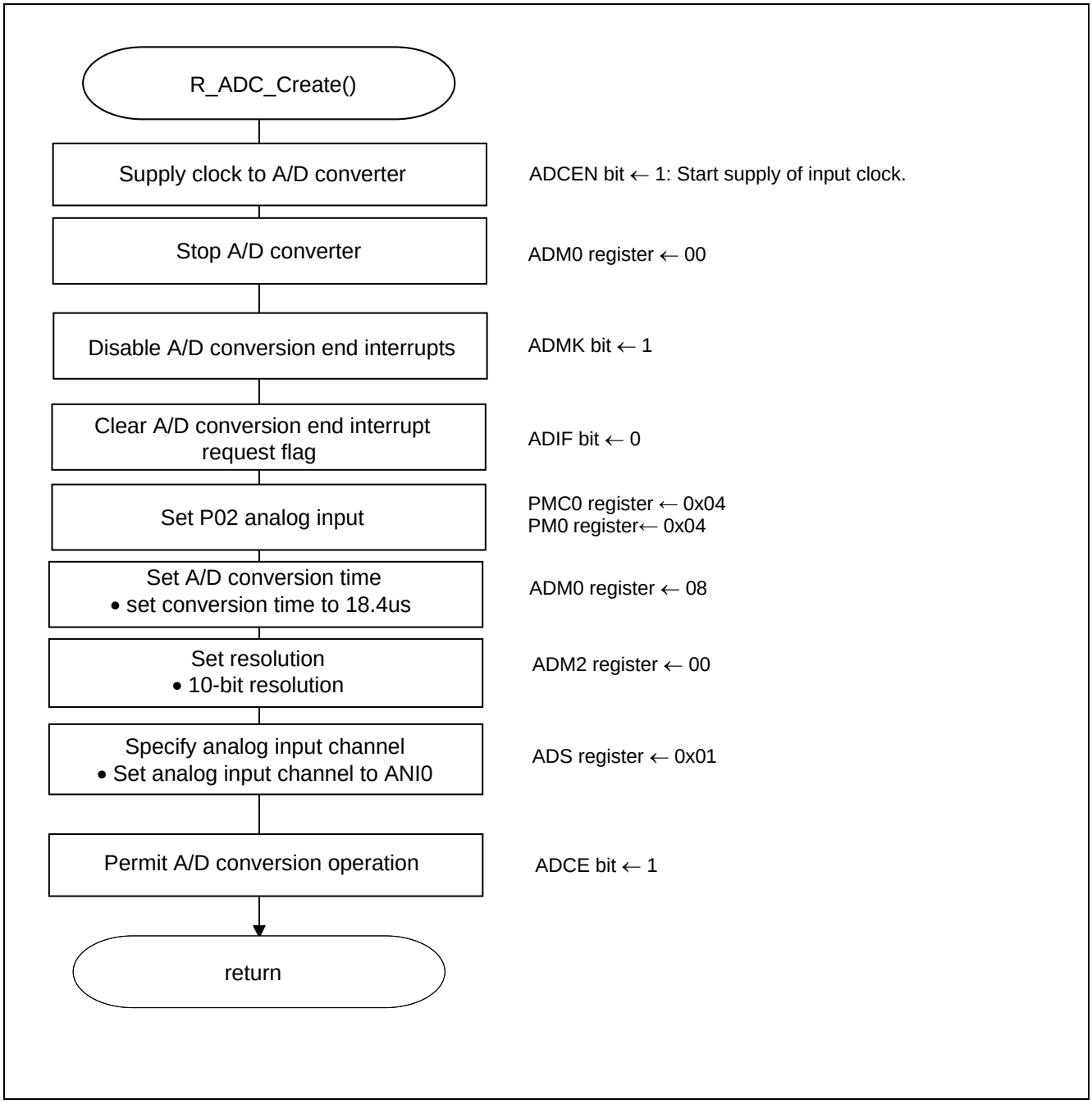


Figure 5.5 A/D Converter Setup

Starting the supply of clock to the A/D converter

- Peripheral enable register 0 (PER0)
  Starts the supply of the clock to the A/D converter.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN Note	0	ADCEN	IICA0EN Note	0	SAU0EN	0	TAU0EN
x	0	**1**	x	x	x	0	x

Bit 5

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Note 16-pin products only.

Caution For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.

Setting up the A/D conversion time and operation mode

- A/D converter mode register 0 (ADM0)
  Controls the A/D conversion operation.
  Specifies the A/D conversion channel selection mode.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	0	0	FR1	FR0	0	LV0	ADCE
x	0	0	**0**	**1**	0	**0**	**1**

Bits 4, 3, and 1

(1) 10-Bit Resolution A/D Conversion Time Selection

ADM0			Conversion Clock	Number of Conversion Clock	Conversion Time	Conversion Time Selection [µs]				
FR1	FR0	LV0				f_{CLK} = 1.25 MHz	f_{CLK} = 5 MHz	f_{CLK} = **5 MHz**	f_{CLK} = 10 MHz	**f_{CLK} =** 20 MHz
0	0	**0**	$f_{CLK}/8$	23 f_{AD} (Number of sampling clock: 9 f_{AD})	$184/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	18.4	9.2
0	**1**		**$f_{CLK}/4$**		**$92/f_{CLK}$**			**18.4**	9.2	4.6
1	0		$f_{CLK}/2$		$46/f_{CLK}$		18.4	9.2	4.6	Setting prohibited
1	1		f_{CLK}		$23/f_{CLK}$	18.4	9.2	4.6	Setting prohibited	
0	0	1	$f_{CLK}/8$	17 f_{AD} (Number of sampling clock: 5 f_{AD})	$136/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	18.4	6.8
0	1		$f_{CLK}/4$		$68/f_{CLK}$			18.4	9.2	3.4
1	0		$f_{CLK}/2$		$34/f_{CLK}$		13.6	9.2	4.6	Setting prohibited
1	1		f_{CLK}		$17/f_{CLK}$	13.6	6.8	4.6	Setting prohibited	

(2) 8-Bit Resolution A/D Conversion Time Selection

ADM0			Conversion Clock	Number of Conversion Clock	Conversion Time	Conversion Time Selection [µs]				
FR1	FR0	LV0				f_{CLK} = 1.25 MHz	f_{CLK} = 5 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz
0	0	0	$f_{CLK}/8$	21 f_{AD} (Number of sampling clock: 9 f_{AD})	$168/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	16.8	8.4
0	1		$f_{CLK}/4$		$84/f_{CLK}$			16.8	8.4	4.2
1	0		$f_{CLK}/2$		$43/f_{CLK}$		16.8	8.4	4.2	Setting prohibited
1	1		f_{CLK}		$21/f_{CLK}$	16.8	8.4	4.2	Setting prohibited	
0	0	1	$f_{CLK}/8$	15 f_{AD} (Number of sampling clock: 3 f_{AD})	$120/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	12.0	6.0
0	1		$f_{CLK}/4$		$60/f_{CLK}$			12.0	6.0	3.0
1	0		$f_{CLK}/2$		$30/f_{CLK}$		12.0	6.0	3.0	Setting prohibited
1	1		f_{CLK}		$15/f_{CLK}$	12.0	6.0	3.0	Setting prohibited	

bit 0

ADCE	**Control of A/D converter input clock supply**
0	Stops input clock supply
1	**Enables input clock supply**

Caution For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.

Setting up the resolution

- A/D converter mode register 2 (ADM2)
  Sets the resolution.

Symbol: ADM2

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	ADTYP
0	0	0	0	0	0	0	**0**

Bit 0

ADTYP	Resolution of A/D conversion
0	**10-bit resolution**
1	8-bit resolution

Caution For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.

5.6.5 Timer array unit Setup

Figure 5.6,5.7 shows the flowchart for setting up the timer array unit.

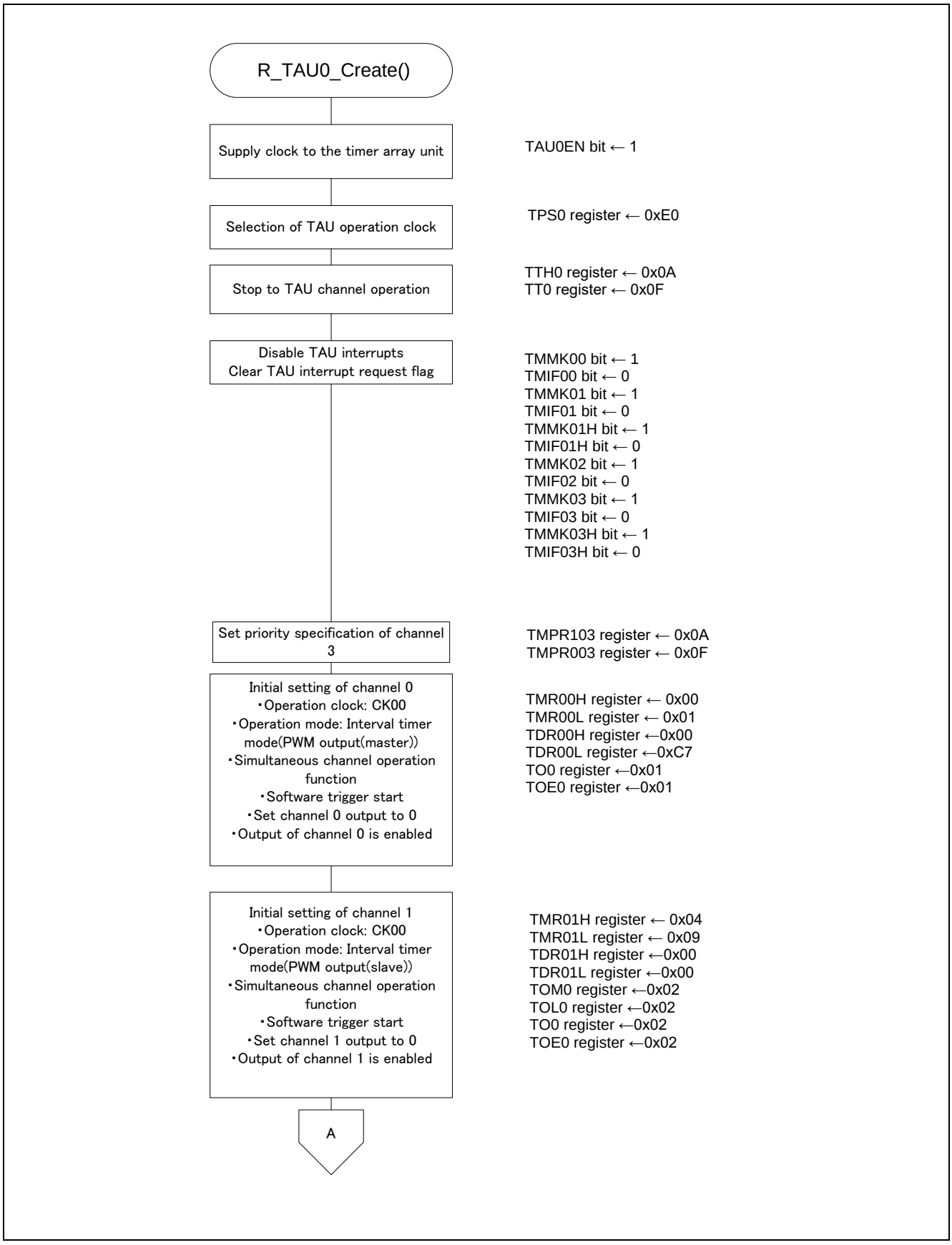


Figure 5.6 Timer Array Unit Setup (1/2)

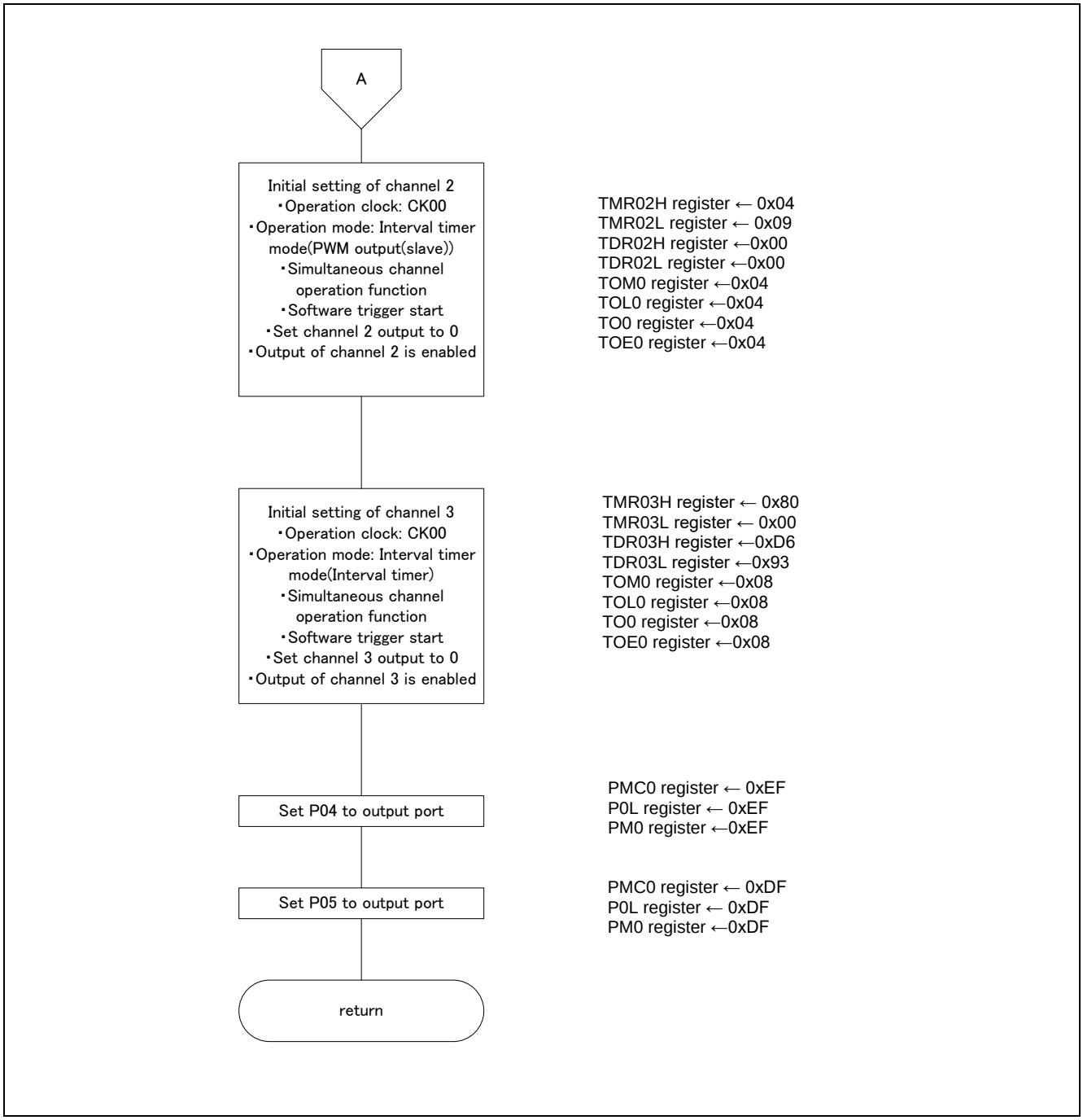


Figure 5.7 Timer Array Unit Setup (2/2)

Starting clock supply to the timer array unit 0

Peripheral enable register 0 (PER0)
Start supplying clock to the timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN[Note]	CMPEN[Note]	ADCEN	IICA0EN[Note]	0	SAU0EN	0	TAU0EN
0	0	x	0	0	x	0	**1**

bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops supply of input clock.
1	**Supplies input clock.**

Note: 16-pin products only.
Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Stop timer channel

Timer channel stop register 0 (TT0, TTH0(8-bit mode))
Select timer channel to stop operation.

Symbol：TTH0、TT0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TTH03	0	TTH01	0	0	0	0	0	TT03	TT02	TT01	TT00
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	**1**

bit n

TT0n	Operation stop trigger of channel n (n=0 to 3)
0	No trigger operation
1	**TE0n is cleared to 0, and counting operation is stopped**

Configuring the timer clock frequency

Timer clock select register 0 (TPS0)

Select an operation clock for timer array unit 0.

Symbol: TPS0

7	6	5	4	3	2	1	0
PRS013	PRS012	PRS011	PRS010	PRS003	PRS002	PRS001	PRS000
1	**1**	**1**	**0**	**0**	**0**	**0**	**0**

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000		Selection of operation clock (CK00)				
					f_{CLK}= 1.25MHz	f_{CLK}= 2.5MHz	f_{CLK}= 5MHz	f_{CLK}= 10MHz	**f_{CLK}=** 20MHz
0	0	0	0	f_{CLK}	1.25 MHz	2.5MHz	5 MHz	10MHz	**20 MHz**
0	**0**	**0**	**1**	**$f_{CLK}/2$**	625kHz	1.25 MHz	2.5MHz	5 MHz	**10MHz**
0	0	1	0	$f_{CLK}/2^2$	313 kHz	625kHz	1.25 MHz	2.5MHz	5 MHz
0	0	1	1	$f_{CLK}/2^3$	156 kHz	313 kHz	625kHz	1.25 MHz	2.5MHz
0	1	0	0	$f_{CLK}/2^4$	78.1 kHz	156 kHz	313 kHz	625kHz	1.25 MHz
0	1	0	1	$f_{CLK}/2^5$	39.1 kHz	78.1 kHz	156 kHz	313 kHz	625kHz
0	1	1	0	$f_{CLK}/2^6$	19.5 kHz	39.1 kHz	78.1 kHz	156 kHz	313 kHz
0	1	1	1	$f_{CLK}/2^7$	9.77 kHz	19.5 kHz	39.1 kHz	78.1 kHz	156 kHz
1	0	0	0	$f_{CLK}/2^8$	4.88 kHz	9.77 kHz	19.5 kHz	39.1 kHz	78.1 kHz
1	0	0	1	$f_{CLK}/2^9$	2.44 kHz	4.88 kHz	9.77 kHz	19.5 kHz	39.1 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.22 kHz	2.44 kHz	4.88 kHz	9.77 kHz	19.5 kHz
1	0	1	1	$f_{CLK}/2^{11}$	610 Hz	1.22 kHz	2.44 kHz	4.88 kHz	9.77 kHz
1	1	0	0	$f_{CLK}/2^{12}$	305 Hz	610 Hz	1.22 kHz	2.44 kHz	4.88 kHz
1	1	0	1	$f_{CLK}/2^{13}$	153 Hz	305 Hz	610 Hz	1.22 kHz	2.44 kHz
1	**1**	**1**	**0**	$f_{CLK}/2^{14}$	76.3 Hz	153 Hz	**305 Hz**	610 Hz	1.22 kHz
1	**1**	**1**	**1**	$f_{CLK}/2^{15}$	38.1Hz	76.3 Hz	**153 Hz**	305 Hz	610 Hz

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Timer interrupt
- Interrupt mask flag registers（MK0L）
  Interrupt mask selection
- Interrupt request flag registers（IF0L）
  clear interrupt request

Symbol：MK0L

bit 7,6

××MK××	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Symbol：IF0L

bit 7,6

××IF××	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Setting up the operation mode of channel 0

Timer mode register 00 (TMR00H, TMR00L)
Select an operation clock (fMCK).
Select a count clock.
Set up the start trigger and capture trigger
Select the valid edge of TI00 pin.
Set up the operation mode.

Symbol：TMR00H、TMR00L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 0n1	0	0	CCS 0n	SPLIT 0n	STS 0n2	STS 0n1	STS 0n0	CIS 0n1	CIS 0n0	0	0	MD 0n3	MD 0n2	MD 0n1	MD 0n0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**1**

CKS0n1	CKS000	Selection of operation clock (f_{MCK}) of channel 0
0	**0**	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)

CCS0n	Selection of count clock (f_{TCLK}) of channel 0
0	**Operation clock (f_{MCK}) specified by the CKS000 and CKS001 bits**
1	Valid edge of the input signal from the TI00 pin

SPLIT0n	Selection of count clock (f_{TCLK}) of channel 0
0	**16bit timer operation**
1	8bit timer operation

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected).**
0	0	1	**Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.**
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Bit 7-6

CIS 001	CIS 000	Selection of TI00 pin input valid edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured)
1	1	Both edges (when high-level width is measured)

Bit 3-0

MD 003	MD 002	MD 001	MD 000	Operation mode of channel 0	Corresponding function	Counting operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer/Square wave output/Divider function /PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter/One-shot pulse output/PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

Operation mode (Value set by the MD003 to MD001 bits) (See the above table)	MD000	Setting of starting count and interrupt
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• Capture/one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
Other than above		Setting prohibited

Setting the interval timer cycle time

Timer data register 01 (TDR00H, TDR00L)

Setting delay time

Symbol：TDR00H、TDR00L

TDR00H TDR00L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**1**

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Enabling the timer output

timer putout register 0 (TO0)

setting putout 0

Timer output enable register 0 (TOE0)

Enable/disable the timer output for each channel.

Symbol：TO0

7	6	5	4	3	2	1	0
0	0	0	0	TO03	TO02	TO01	TO00
0	0	0	0	**0**	**0**	0	**1**

bit 1

TO00	**Timer output of channel n**
0	Timer output value is “0”
1	**Timer output value is “1”**

Symbol：TOE0

7	6	5	4	3	2	1	0
0	0	0	0	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	**1**

bit 0

TOE01	**Timer output enable/disable of channel 0**
0	**Disables the timer output.** **Timer operation is not reflected in the TO00 bit, and the output is fixed.** **Writing to the TO00 bit is allowed.**
1	**Enables the timer output.** **Timer operation is reflected in the TO00 bit, and output waveform is generated.** **Writing to the TO00 bit is ignored.**

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Setting up the operation mode of channel 1

Timer mode register 01 (TMR01H, TMR01L)
Select an operation clock (fMCK).
Select a count clock.
Set up the start trigger and capture trigger
Select the valid edge of TI00 pin.
Set up the operation mode.

Symbol：TMR01H、TMR01L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 0n1	0	0	CCS 0n	SPLIT 0n	STS 0n2	STS 0n1	STS 0n0	CIS 0n1	CIS 0n0	0	0	MD 0n3	MD 0n2	MD 0n1	MD 0n0
0	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	0	0	**1**	**0**	**0**	**1**

CKS0n1	CKS000	Selection of operation clock (f_{MCK}) of channel 0
0	**0**	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)

CCS0n	Selection of count clock (f_{TCLK}) of channel 0
0	**Operation clock (f_{MCK}) specified by the CKS000 and CKS001 bits**
1	Valid edge of the input signal from the TI00 pin

SPLIT0n	Selection of count clock (f_{TCLK}) of channel 0
0	**16bit timer operation**
1	8bit timer operation

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected).**
0	**0**	**1**	**Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.**
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Bit 7-6

CIS 001	CIS 000	Selection of TI00 pin input valid edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured)
1	1	Both edges (when high-level width is measured)

Bit 3-0

MD 003	MD 002	MD 001	MD 000	Operation mode of channel 0	Corresponding function	Counting operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer/Square wave output/Divider function /PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter/One-shot pulse output/PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

Operation mode (Value set by the MD003 to MD001 bits) (See the above table)	MD000	Setting of starting count and interrupt
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• Capture/one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
Other than above		Setting prohibited

Setting the interval timer cycle time

Timer data register 01 (TDR01H, TDR01L)

Setting delay time

Symbol：TDR01H、TDR01L

TDR01H								TDR01L							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Setting up the timer output mode

- Timer output mode register 0 (TOM0)
  Set up the timer output mode for each channel.

Symbol: TOM0

7	6	5	4	3	2	1	0
0	0	0	0	TOM03Note	TOM02Note	TOM01	0
0	0	0	0	x	x	**1**	0

Bit 1

TOM01	Channel 1 timer output mode control
0	Master channel output mode. (Output is toggled with the timer interrupt request signal (INTTM01).)
1	**Slave channel output mode. (Output is set with the master channel's timer interrupt request signal (INTTM01) and reset with the slave channel's timer interrupt request signal (INTTM0p).)**

Note: 16-pin products only

Configuring the output level for the timer output pin

- Timer output level register 0 (TOL0)
  Configure the output level for the timer output pin for each channel.

Symbol: TOL0

7	6	5	4	3	2	1	0
0	0	0	0	TO03Note	TO02Note	TO01	TO00
0	0	0	0	x	x	**0**	x

Bit 1

TOL01	Channel 1 timer output level control
0	**Positive logic output (active-high)**
1	Negative logic output (active-low)

Note: 16-pin products only

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Enabling the timer output

timer putout register 0 (TO0)
setting putout 0
Timer output enable register 0 (TOE0)
Enable/disable the timer output for each channel.

Symbol：TO0

7	6	5	4	3	2	1	0
0	0	0	0	TO03	TO02	TO01	TO00
0	0	0	0	**0**	**0**	**1**	0

bit 1

TO00	Timer output of channel n
0	Timer output value is “0”
1	**Timer output value is “1”**

Symbol：TOE0

7	6	5	4	3	2	1	0
0	0	0	0	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	**1**	0

bit 0

TOE01	Timer output enable/disable of channel 0
0	**Disables the timer output.** **Timer operation is not reflected in the TO00 bit, and the output is fixed.** **Writing to the TO00 bit is allowed.**
1	**Enables the timer output.** **Timer operation is reflected in the TO00 bit, and output waveform is generated.** **Writing to the TO00 bit is ignored.**

bit1

TOE01	Timer output enable/disable of channel 1
0	**Disables the timer output.** **Timer operation is not reflected in the TO00 bit, and the output is fixed.** **Writing to the TO00 bit is allowed.**
1	**Enables the timer output.** **Timer operation is reflected in the TO00 bit, and output waveform is generated.** **Writing to the TO00 bit is ignored.**

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Setting up the operation mode of channel 2

Timer mode register 01 (TMR02H, TMR02L)
Select an operation clock (fMCK).
Select a count clock.
Set up the start trigger and capture trigger
Select the valid edge of TI00 pin.
Set up the operation mode.

Symbol：TMR02H、TMR02L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 0n1	0	0	CCS 0n	SPLIT 0n	STS 0n2	STS 0n1	STS 0n0	CIS 0n1	CIS 0n0	0	0	MD 0n3	MD 0n2	MD 0n1	MD 0n0
0	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	0	0	**1**	**0**	**0**	**1**

CKS0n1	CKS000	Selection of operation clock (f_{MCK}) of channel 0
0	**0**	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)

CCS0n	Selection of count clock (f_{TCLK}) of channel 0
0	**Operation clock (f_{MCK}) specified by the CKS000 and CKS001 bits**
1	Valid edge of the input signal from the TI00 pin

SPLIT0n	Selection of count clock (f_{TCLK}) of channel 0
0	**16bit timer operation**
1	8bit timer operation

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected).**
0	**0**	**1**	**Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.**
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Bit 7-6

CIS 001	CIS 000	Selection of TI00 pin input valid edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured)
1	1	Both edges (when high-level width is measured)

Bit 3-0

MD 003	MD 002	MD 001	MD 000	Operation mode of channel 0	Corresponding function	Counting operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer/Square wave output/Divider function /PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter/One-shot pulse output/PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

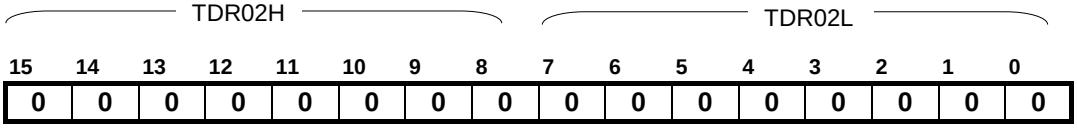
Operation mode (Value set by the MD003 to MD001 bits) (See the above table)	MD000	Setting of starting count and interrupt
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• Capture/one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
Other than above		Setting prohibited

Setting the interval timer cycle time

Timer data register 01 (TDR01H, TDR01L)

Setting delay time

Symbol：TDR02H、TDR02L



Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Setting up the operation mode of channel 3

Timer mode register 01 (TMR03H, TMR03L)
Select an operation clock (fMCK).
Select a count clock.
Set up the start trigger and capture trigger
Select the valid edge of TI00 pin.
Set up the operation mode.

Symbol：TMR03H、TMR03L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 0n1	0	0	CCS 0n	SPLIT 0n	STS 0n2	STS 0n1	STS 0n0	CIS 0n1	CIS 0n0	0	0	MD 0n3	MD 0n2	MD 0n1	MD 0n0
1	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

CKS0n1	CKS000	Selection of operation clock (f_{MCK}) of channel 0
0	0	Operation clock CK00 set by timer clock select register 0 (TPS0)
1	**0**	**Operation clock CK01 set by timer clock select register 0 (TPS0)**

CCS0n	Selection of count clock (f_{TCLK}) of channel 0
0	**Operation clock (f_{MCK}) specified by the CKS000 and CKS001 bits**
1	Valid edge of the input signal from the TI00 pin

SPLIT0n	Selection of count clock (f_{TCLK}) of channel 0
0	**16bit timer operation**
1	8bit timer operation

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected).**
0	0	1	**Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.**
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Bit 7-6

CIS 001	CIS 000	Selection of TI00 pin input valid edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured)
1	1	Both edges (when high-level width is measured)

Bit 3-0

MD 003	MD 002	MD 001	MD 000	Operation mode of channel 0	Corresponding function	Counting operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer/Square wave output/Divider function /PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter/One-shot pulse output/PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

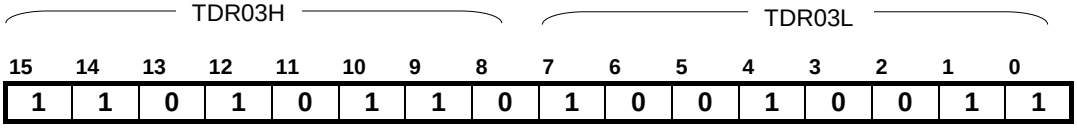
Operation mode (Value set by the MD003 to MD001 bits) (See the above table)	MD000	Setting of starting count and interrupt
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• Capture/one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
Other than above		Setting prohibited

Setting the interval timer cycle time

Timer data register 01 (TDR03H, TDR03L)

Setting delay time

Symbol：TDR03H、TDR03L



Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Setting up the PWM output pin

- Port mode register (PMC0)
  Select the PMC04 digital I/O latch.
- Port mode register (P0)
  Select the P04 output latch.
- Port mode register (PM0)
  Select the PM04 I/O mode.

Symbol：PMC0

7	6	5	4	3	2	1	0
PMC07	PMC06	PMC05	PMC04	PMC03	PMC03	PMC01	PMC00
1	1	1	**0**	1	1	1	1

bit4

PMC04	**PMC04 digital selection**
0	**Digital I/O（alternate function other than analog input）**
1	Analog input

Symbol: P0

7	6	5	4	3	2	1	0
1	P06 Note	P05 Note	P04	P03	P02	P01	P00
1	x	x	**0**	x	x	x	x

bit 4

P04	P04 I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Symbol: PM0

7	6	5	4	3	2	1	0
1	PM06 Note	PM05 Note	PM04	PM03	PM02	PM01	PM00
1	x	x	**0**	x	x	x	x

bit 4

PM04 Note 2	PM04 I/O mode selection Note 2
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Note: 16-pin products only

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

5.6.6 Main Processing

Figure 5.8 shows the flowchart of the main processing.

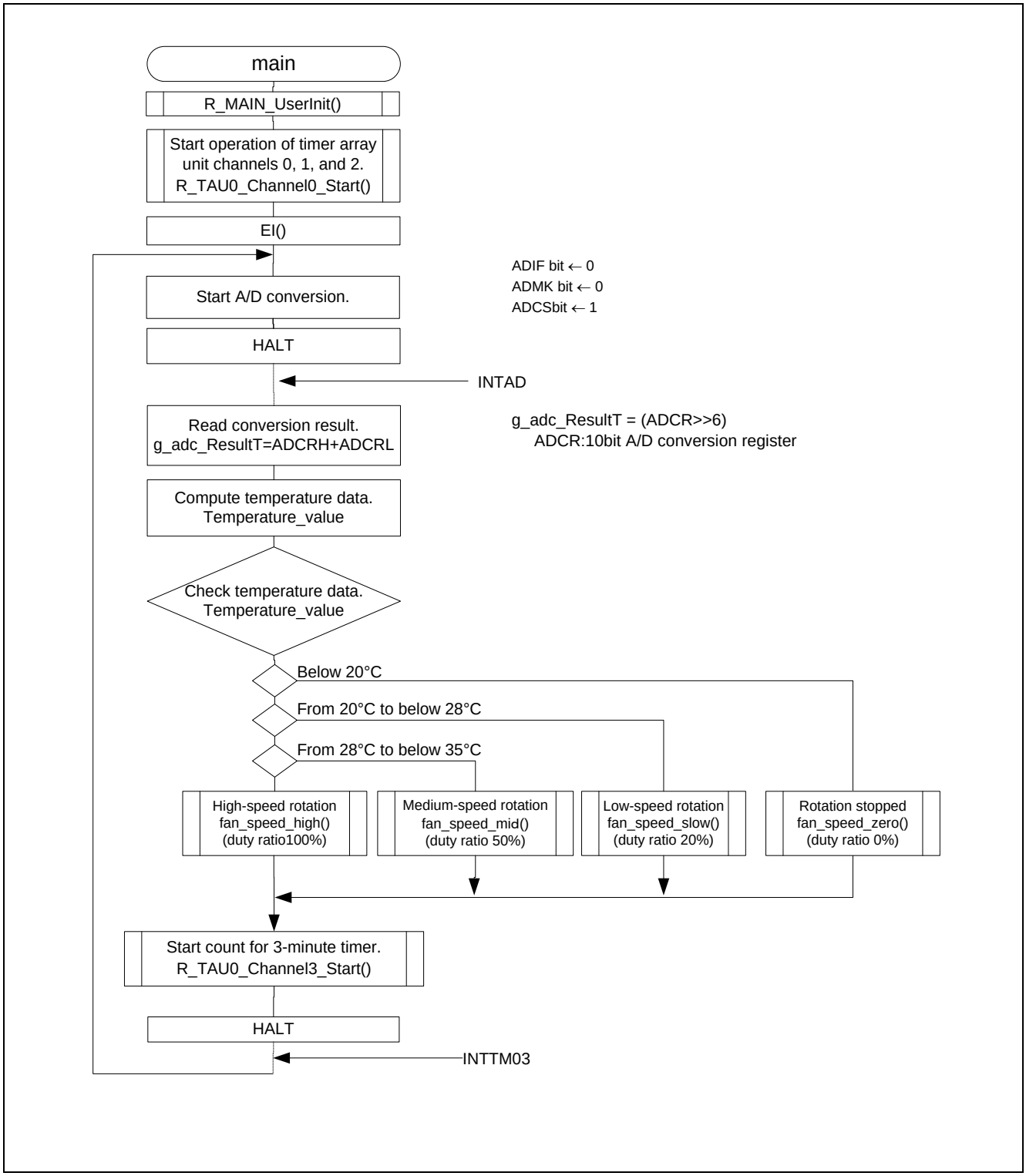


Figure 5.8 Main Processing Flowchart

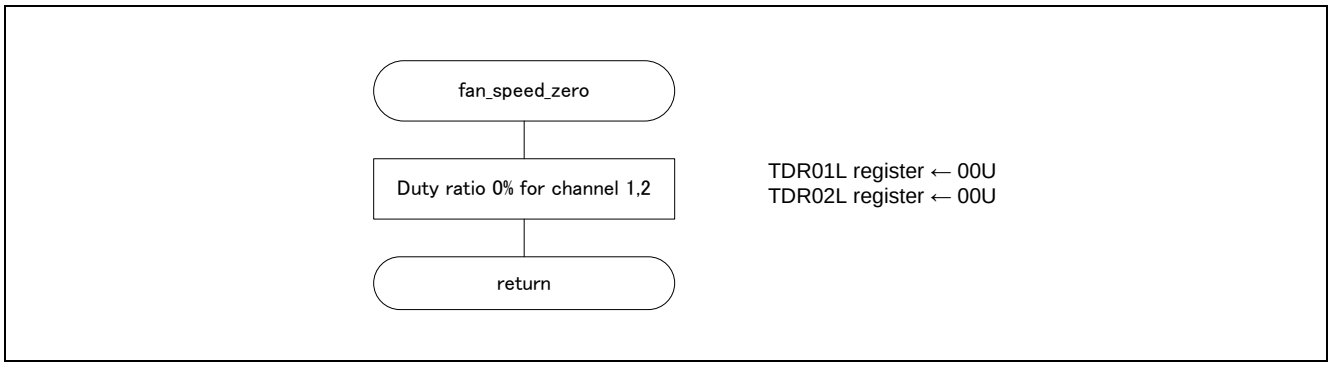


Figure 5.9 Flowchart of Interrupt Processing

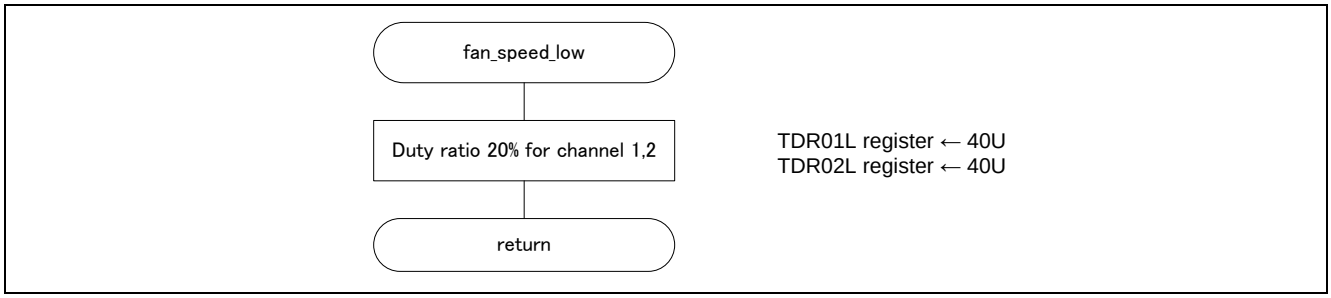


Figure 5.10 Flowchart of fan stopping

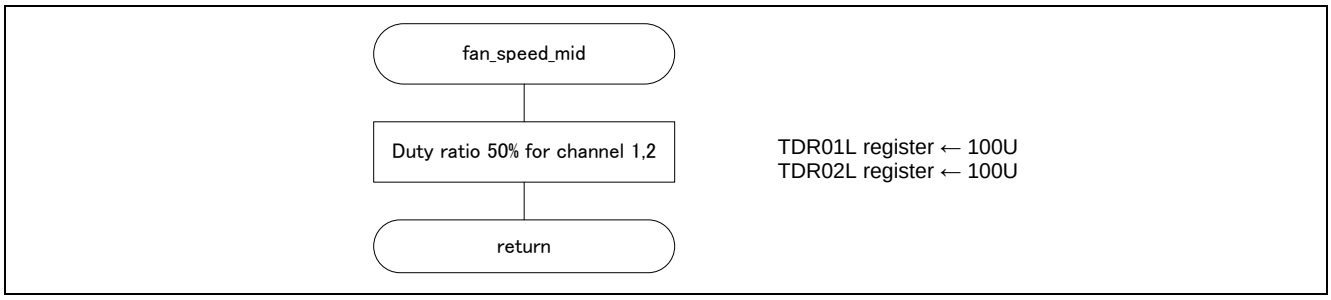


Figure 5.11 Flowchart of fan middle speed

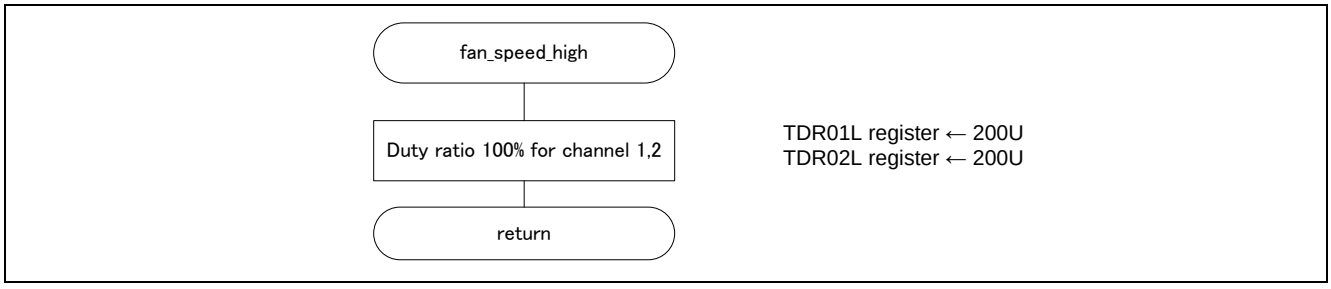


Figure 5.12 Flowchart of fan high speed

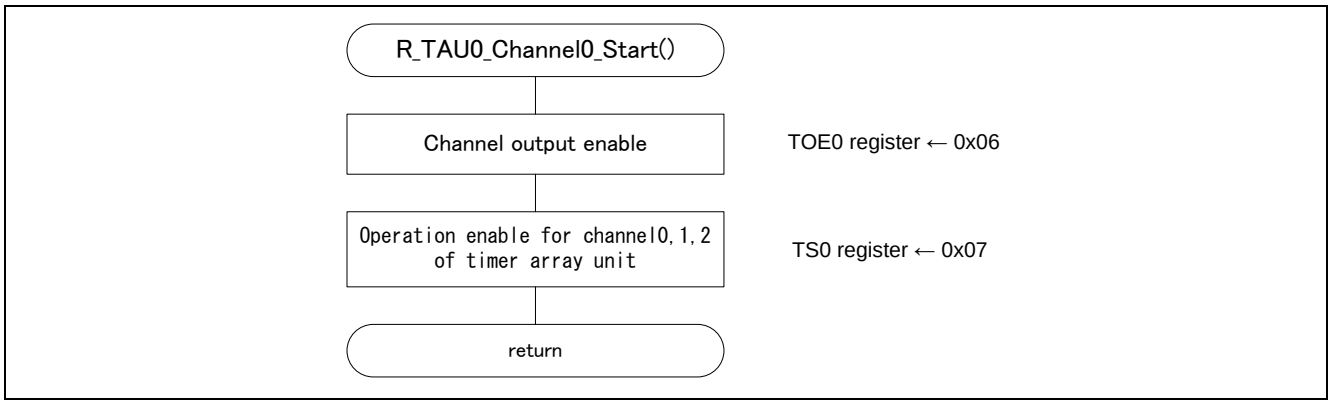


Figure 5.13 Flowchart of TAU channel0 start

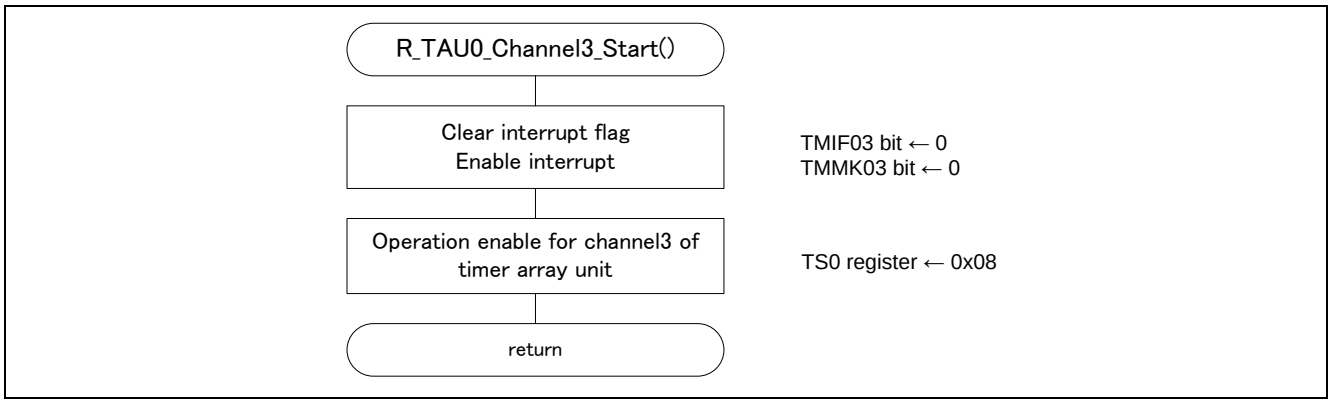


Figure 5.14 Flowchart of TAU channel3 start

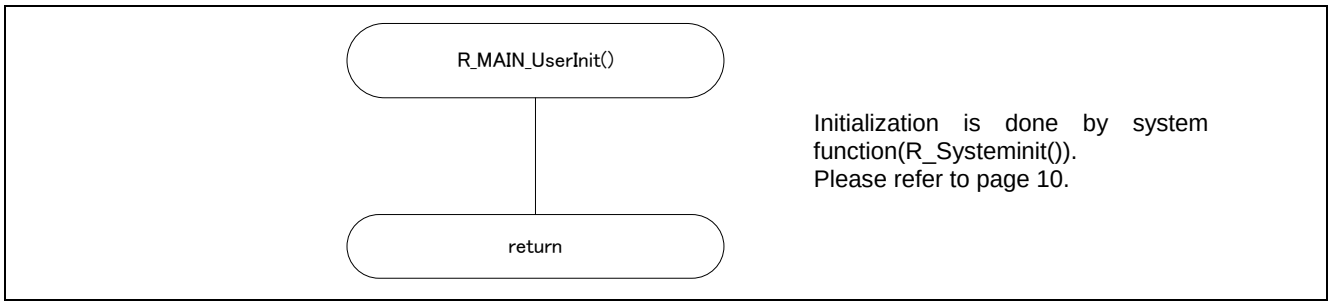


Figure 5.15 Flowchart of main function

Website and Support

Renesas Electronics Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/contact/

Revision History <revision history,rh>

Rev.	Date	Description	
		Page	Summary
1.00	2018.7.20	-	

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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