R8C/35A, R8C/35C, R8C/35D, R8C/35M Groups

Differences between R8C/35A, R8C/35C, R8C/35D, and R8C/35M Groups

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1. Abstract

This document is reference material for identifying differences between the R8C/35A Group, R8C/35C Group, R8C/35D Group, and R8C/35M Group.

2. Introduction

This document applies to the following microcomputers (MCUs):

- MCUs: R8C/35A Group, R8C/35C Group, R8C/35D Group, R8C/35M Group

3. Differences between Groups

3.1 Function and Specification Differences

Table 3.1 and Table 3.2 list differences in the functions and specifications. For more details and electrical characteristics, refer to the documents listed in 5. Reference Documents.

Table 3.1 Function and Specification Differences (1)

Item		R8C/35A Group	R8C/35C Group	R8C/35M Group	R8C/35D Group
Memory	ROM/RAM	• 16 KB/1.5 KB • 24 KB/2 KB • 32 KB/2.5 KB • 48 KB/4 KB • 64 KB/6 KB • 96 KB/8 KB • 128 KB/10 KB			• 16 KB/1 KB • 24 KB/1 KB • 32 KB/1 KB
Voltage Detection Circuit	Voltage detection 2	Detection voltage can be selected. (VCC or LVCMP2 pin)	Detection voltage cannot be selected.	Detection voltage can be selected. (VCC or LVCMP2 pin)	Detection voltage cannot be selected.
Bus Control		Registers DA0, DA1, RMAD0, AIER0, RMAD1, and AIER1 are connected to the CPU by an 16-bit bus.			Registers RMAD0, RMAD1, and AIER are connected to the CPU by an 8-bit bus.
Clock Generation Circuit	Peripheral function clock	fC2 is included in the peripheral function clock.			fC2 is not included in the peripheral function clock.
High-Speed On-Chip Oscillator		Not included [1]	Included [2]		
Power Control	• Select 10b for bits CM37 and CM36	Not available	Available	Not available	Available
	• Enter stop mode while bits CM37 and CM36 are 00b in high-speed on-chip oscillator mode	—	Available	Not available	Available
	• Select 11b for bits CM37 and CM36 in low-speed clock mode.	Available		Not available	Available
Interrupts		• Number of interrupt sources: 40 • External interrupt inputs: 9 ($\overline{INT}$ x 5 and key input x 4)	• Number of interrupt sources: 36 • External interrupt inputs: 9 ($\overline{INT}$ x 5 and key input x 4)	• Number of interrupt sources: 40 • External interrupt inputs: 9 ($\overline{INT}$ x 5 and key input x 4)	• Number of interrupt sources: 30 • External interrupt inputs: 9 ($\overline{INT}$ x 5 and key input x 4)
DTC		Included			Not included
Timer RD		Included			Not included

Notes:
1. Since the R8C/35A Group does not include a high-speed on-chip oscillator, it cannot be selected as the peripheral function count source.
2. Electrial characteristics for the high-speed on-chip oscillator in these groups differ. Refer to the documents of each group for details.

Table 3.2 Function and Specification Differences (2)

Item		R8C/35A Group	R8C/35C Group	R8C/35M Group	R8C/35D Group
Serial Interface	UART1	Included			Not included
	td(C-Q) TXDi output delay time	Maximum 70 ns (VCC = 5.0 V)	Maximum 50 ns (VCC = 5.0 V)	• When selecting external clock: Maximum 90 ns (VCC = 5.0 V) • When selecting internal clock: Maximum 10 ns (VCC = 5.0 V)	Maximum 50 ns (VCC = 5.0 V)
Synchronous Serial Communication Unit (SSU)		Included			Not included
I^2C-bus Interface		Included			Not included
Hardware LIN		Included			Not included
A/D Converter	Conversion rate per pin (ϕAD = fAD)	Minimum: 43 ϕAD cycles	Minimum: 44 ϕAD cycles		
	Sampling time	15 ϕAD (ϕAD = 20 MHz: 0.75 μs)	16 ϕAD (ϕAD = 20 MHz: 0.8 μs)		
	A/D conversion execution time	Open-circuit detection disabled: 40 ϕAD cycles Open-circuit detection enabled: 42 ϕAD cycles	Open-circuit detection disabled: 40 ϕAD cycles + 1 to 3 fAD cycles Open-circuit detection enabled: 42 ϕAD cycles + 1 to 3 fAD cycles		
D/A Converter		Included			Not included
Comparator A		Included	Not included	Included	Not included
Flash Memory	Program operation (programming to the flash memory) while auto-erasure is suspended for the suspend function.	Cannot be performed	Can be performed		
	Interval from erase start/restart until following suspend request	Minimum: 33 ms	Minimum: 0 ms		
	Suspend interval necessary for auto-erasure to be completed	Minimum: 33 ms	Minimum: 0 ms		
	Data flash (including BGO)	Included			Not included

3.2 Pin Function Differences

Table 3.3 lists differences in the I/O ports assigned to the peripheral function pins. For more details, refer to the documents listed in 5. Reference Documents.

Table 3.3 Pin Function Differences

Peripheral Function Pin	Assigned I/O Ports			
	R8C/35A Group	R8C/35C Group	R8C/35M Group	R8C/35D Group
LVCMP1	P1_0	—	P1_0	—
LVCMP2	P1_1	—	P1_1	—
LVREF	P1_2	—	P1_2	—
LVCOUT1	P1_3	—	P1_3	—
LVCOUT2	P1_6	—	P1_6	—
CLK1	P6_5, P6_2, P0_3			—
RXD1	P6_4, P0_2			—
TXD1	P6_3, P0_1			—
TRDIOA0	P2_0			—
TRDIOB0	P2_2			—
TRDIOC0	P2_1			—
TRDIOD0	P2_3			—
TRDIOA1	P2_4			—
TRDIOB1	P2_5			—
TRDIOC1	P2_6			—
TRDIOD1	P2_7			—
TRDCLK	P2_0			—
SCL	P3_5			—
SDA	P3_7			—
SSI	P3_4			—
SCS	P3_3			—
SSCK	P3_5			—
SSO	P3_7			—
DA0	P0_6			—
DA1	P0_7			—

The symbol "—" indicates there is no pin for the peripheral function.

3.3 Differences of SFRs

Table 3.4 to Table 3.6 list differences in the SFRs. For more details, refer to the documents listed in 5. Reference Documents.

Table 3.4 Differences of SFRs (1)

R8C/35A Group	R8C/35C Group	R8C/35M Group	R8C/35D Group	Differences to R8C/35A Group (1)		
				R8C/35C Group	R8C/35M Group	R8C/35D Group
CMPA	CMPA	CMPA	CMPA	Bits 0 to 3 deleted		Bits 0 to 3 deleted
VCA2	VCA2	VCA2	VCA2	• Bits 1 to 4 deleted • Functions changed in bits 6 and 7		• Bits 1 to 4 deleted • Functions changed in bits 6 and 7
VW2C	VW2C	VW2C	VW2C	Function changed in bit 7		Function changed in bit 7
TRDPSR0			—			—
TRDPSR1			—			—
U1SR			—			—
SSUIICSR			—			—
PINSR			PINSR			Bits 4 to 7 deleted
CM3	CM3	CM3	CM3	Functions changed in bits 6 and 7		Functions changed in bits 6 and 7
FRA0	FRA0			Functions added to bits 0, 1, and 3		
—	FRA1			Register added		
—	FRA2			Register added		
—	FRA3			Register added		
—	FRA4			Register added		
—	FRA5			Register added		
—	FRA6			Register added		
—	FRA7			Register added		
S1TIC			—			—
S1RIC			—			—
TRD0IC			—			—
TRD1IC			—			—
SSUIC/IICIC			—			—
AIER0			AIER			• Register name changed • Bit 1 added
AIER1			—			—
DTCTL			—			—
DTCEN0			—			—
DTCEN1			—			—
DTCEN2	DTCEN2	DTCEN2	—	Functions in bits 4 and 5 changed		—

The symbol "—" indicates there is no SFR.

Note:

1. Blank spaces indicate no difference with the R8C/35A Group.

Table 3.5 Differences of SFRs (2)

R8C/35A Group	R8C/35C Group	R8C/35M Group	R8C/35D Group	Differences to R8C/35A Group (1)		
				R8C/35C Group	R8C/35M Group	R8C/35D Group
DTCEN3			—			—
DTCEN4			—			—
DTCEN5			—			—
DTCEN6			—			—
DTCVCT0 to 63 (2)			—			—
DTCD0 to 23			—			—
TRAIOC			TRAIOC			Bit 3 deleted
MSTCR			MSTCR			Bits 3 and 4 deleted
TRCCR1	TRCCR1			Functions changed in bits 4 to 6		
TRDECR			—			—
TRDADCR			—			—
TRDSTR			—			—
TRDMR			—			—
TRDPMR			—			—
TRDFCR			—			—
TRDOER1			—			—
TRDOER2			—			—
TRDOCR			—			—
TRDDF0			—			—
TRDDF1			—			—
TRDCR0	TRDCR0		—	Functions changed in bits 0 to 2		—
TRDIORA0			—			—
TRDIORC0			—			—
TRDSR0			—			—
TRDIER0			—			—
TRDPOCR0			—			—
TRD0			—			—
TRDGRA0			—			—
TRDGRB0			—			—
TRDGRC0			—			—
TRDGRD0			—			—
TRDCR1	TRDCR1		—	Functions changed in bits 0 to 2		—
TRDIORA1			—			—

The symbol "—" indicates there is no SFR.

Note:

1. Blank spaces indicate no difference with the R8C/35A Group.
2. DTC transfer vector area (2C00h to 2C3Fh)

Table 3.6 Differences of SFRs (3)

R8C/35A Group	R8C/35C Group	R8C/35M Group	R8C/35D Group	Differences to R8C/35A Group (1)		
				R8C/35C Group	R8C/35M Group	R8C/35D Group
TRDIORC1			—			—
TRDSR1			—			—
TRDIER1			—			—
TRDPOCR1			—			—
TRD1			—			—
TRDGRA1			—			—
TRDGRB1			—			—
TRDGRC1			—			—
TRDGRD1			—			—
U1MR			—			—
U1BRG			—			—
U1TB			—			—
U1C0			—			—
U1C1			—			—
U1RB			—			—
LINCR2			—			—
LINCR			—			—
LINST			—			—
SSBR			—			—
SSTDR/ICDRT			—			—
SSTDRH			—			—
SSRDR/ICDRR			—			—
SSRDRH			—			—
SSCRH/ICCR1			—			—
SSCRL/ICCR2			—			—
SSMR/ICMR			—			—
SSER/ICIER			—			—
SSSR/ICSR			—			—
SSMR2/SAR			—			—
ADMOD	ADMOD		ADMOD	Function changed in bit 2		Functions changed in bits 2, 6, and 7
DA0			—			—
DA1			—			—
DACON			—			—
FMR1			FMR1			Bits 4 to 7 deleted

The symbol "—" indicates there is no SFR.

Note:

1. Blank spaces indicate no difference with the R8C/35A Group.

3.4 Interrupt Vector Differences

Table 3.7 lists differences in the fixed vector table and lists differences in the relocatable vector table. For more details, refer to the documents listed in 5. Reference Documents.

Table 3.7 Differences in Fixed Vector Table and Relocatable Vector Table

Differences in Fixed Vector Table

Vector addresses Addresses Low to High	Interrupt Source of R8C/35A Group	Interrupt Source of R8C/35C Group	Interrupt Source of R8C/35M Group	Interrupt Source of R8C/35D Group
0FFF0h to 0FFF3h	Watchdog timer Oscillation stop detection Voltage monitor 1/comparator A1 Voltage monitor 2/comparator A2	Watchdog timer Oscillation stop detection Voltage monitor 1 Voltage monitor 2	Watchdog timer Oscillation stop detection Voltage monitor 1/comparator A1 Voltage monitor 2/comparator A2	Watchdog timer Oscillation stop detection Voltage monitor 1 Voltage monitor 2

Differences in Relocatable Vector Table

Software Interrupt Number	Interrupt Source of R8C/35A Group	Interrupt Source of R8C/35C Group	Interrupt Source of R8C/35M Group	Interrupt Source of R8C/35D Group
8	Timer RD0			—
9	Timer RD1			—
15	Synchronous Serial Communication Unit/I2C-bus interface			—
19	UART1 transmit			—
20	UART1 receive			—
50	Volage monitor 1/comparator A1	Voltage monitor 1	Volage monitor 1/comparator A1	Voltage monitor 1
51	Volage monitor 2/comparator A2	Voltage monitor 2	Volage monitor 2/comparator A2	Voltage monitor 2

4. Notes

Each product has different oscillation circuit constants of XIN-XOUT, XCIN-XCOUT. Therefore, contact an oscillator manufacturer when selecting an oscillator and oscillation circuit constants so that a stable operation clock can be obtained on the user system and conditions for mass-production. Be careful especially when the voltage and temperature range is wide. The wiring pattern of the feedback resistor, damping resistor, and the load capacity should be considered in advance when designing a circuit.

In addition, although compatibility in characteristics is fully considered when designing each device, actual values such as operating margin, A/D conversion accuracy, noise immunity, noise radiation may be different within the range of electrical characteristics due to different manufacturing processes. Therefore, perform sufficient system evaluations for each individual product before starting mass production.

5. Reference Documents

R8C/35A Group User's Manual: Hardware Rev.0.40
R8C/35C Group User's Manual: Hardware Rev.1.00
R8C/35D Group User's Manual: Hardware Rev.1.00
R8C/35M Group User's Manual: Hardware Rev.0.10
The latest versions can be downloaded from the Renesas Electronics website.

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6. Website and Support

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Revision History	R8C/35A, R8C/35C, R8C/35D, R8C/35M Groups Differences between R8C/35A, R8C/35C, R8C/35D, and R8C/35M Groups

Rev.	Date	Description	
		Page	Summary
1.00	June 24, 2010	—	First edition issued
2.00	Jan 20, 2011	—	Document number changed (old number: REJ05B1375)
		Full page	Differences of R8C/35M Group added
		3	Table 3.1 Differeneces of A/D converter sampling time and A/D conversion execution time added
2.01	Feb. 3, 2011	Full page	Descriptions in tables reviewed and revised
		2	Table 3.1 Power Control revised
		5	Table 3.4 CM3 revised

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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