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April 1st, 2010
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H8/300H Tiny Series

Pulse Output of Arbitrary Phase Differences using Timer Z Output Compare Function

Introduction

The timer Z output-compare function is used to output two waveforms of 50% duty cycle pulses with a desired phase difference.

Target Device

H8/3687

Contents

1. Specifications

1. The timer Z output-compare function is used to output two waveforms of 50% duty cycle pulses with a desired phase difference.
2. The FTIOA0 and FTIOB0 pins output pulses with a desired phase difference.
3. The period of a pulse is specified by the general register A0 (GRA0).
4. The phase difference of pulses output from the FTIOA0 and FTIOB0 pins are specified by the general register B0 (GRB0).
5. In this sample task, two pulse waveforms of 16-ms period are output with a phase difference of 3 ms.

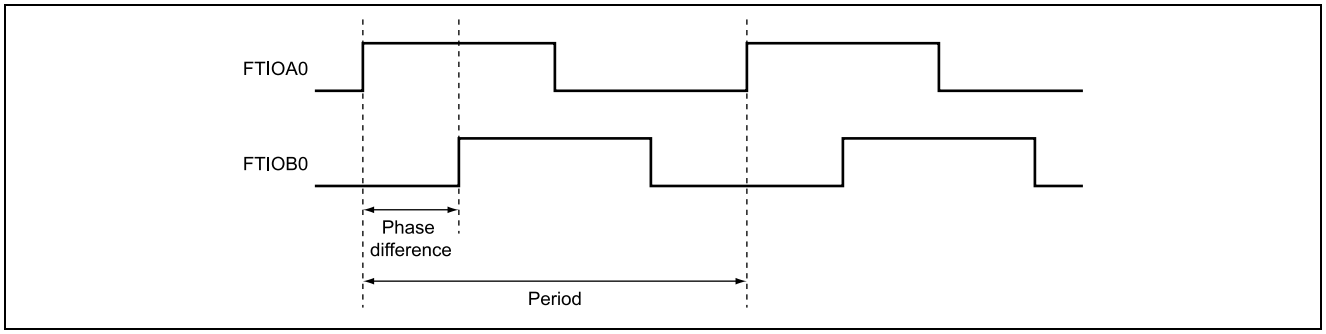


Figure 1.1 Outputting Pulses with a Desired Phase Difference

2. Description of Functions

1. In this sample task, timer Z compare-match function is used to output 50%-duty cycle pulses with a desired phase difference. Figure 2.1 is a block diagram of timer Z output-compare function. The elements of the block diagram are described below.

- The system clock (ϕ) is a 16-MHz clock that is used as a reference clock for operating the CPU and peripheral functions.
- Prescaler S (PSS) is a 13-bit counter with clock input of ϕ. PSS is incremented every cycle.
- Timer control register 0 (TCR0) selects TCNT0 input clock and clearing method. In this sample task, the TCNT0 counts the rising edge of ϕ/2 and the TCNT0 is specified to be cleared at GRA0 compare-match.
- Timer I/O control register A0 (TIORA0) controls GRA0 and GRB0. In this sample task, GRA0 and GRB0 are used an output-compare registers, and the TCNT0 is cleared on GRA0 compare-match.
- Timer status register 0 (TSR0) indicates the timer Z status. In this sample task, the input-capture/compare-match flags A and B (IMFA and IMFB) are set to one on GRA0 and GRB0 compare-matches, respectively.
- Timer interrupt enable register (TIER0) enables or disables each interrupt. In this sample task, interrupt requests by IMFA and IMFB flags of TSR0 are enabled and other interrupts are disabled.
- Timer counter 0 (TCNT0) is a 16-bit readable/writable upward counter that is incremented by the internal clock or external clock input. In this sample task, TCNT0 is counted at the rising edge of ϕ/2.
- General register A0 (GRA0) is a 16-bit readable/writable register. The value of GRA0 is always compared with that of TCNT0 and the IMFA flag of TSR0 is set to 1 when TNCT0 matches GRA0. If IMIEA of TEIR0 is set to 1 while IMFA of TSR0 is set to 1, an interrupt is requested to the CPU.
- General register B0 (GRB0) is a 16-bit readable/writable register. The value of GRB0 is always compared with that of TCNT0 and the IMFB flag of TSR0 is set to 1 when TNCT0 matches GRB0. If IMIEB of TEIR0 is set to 1 while IMFB of TSR0 is set to 1, an interrupt is requested to the CPU.
- Timer start register (TSTR) starts or stops the TCNT0 and TCNT1 operation. In this sample task, TCNT0 is specified to start counting and TCNT1 is specified to stop counting.
- Timer mode register (TMDR) selects synchronous or independent operation of TCNT0 and TCNT1. In this sample task, TCNT0 operates independently of TCNT1.
- Timer PWM mode register (TPMR) specifies the output pins for normal operation mode or PWM mode. In this sample task, all output pins are specified normal operation.

- Timer function control register (TFCR) specifies various operation modes and selects the output level. In this sample task, channels 0 and 1 are specified for normal operation.
- Timer output master enable register (TOER) enables or disables channels 0 and 1 outputs. In this sample task, the FTIOA0 and FTIOB0 outputs are enabled.
- Timer output control register (TOCR) specifies the initial value which is output until the first compare-match is generated. In this sample task, the initial values of FTIOA0 and FTIOB0 are specified as 0.

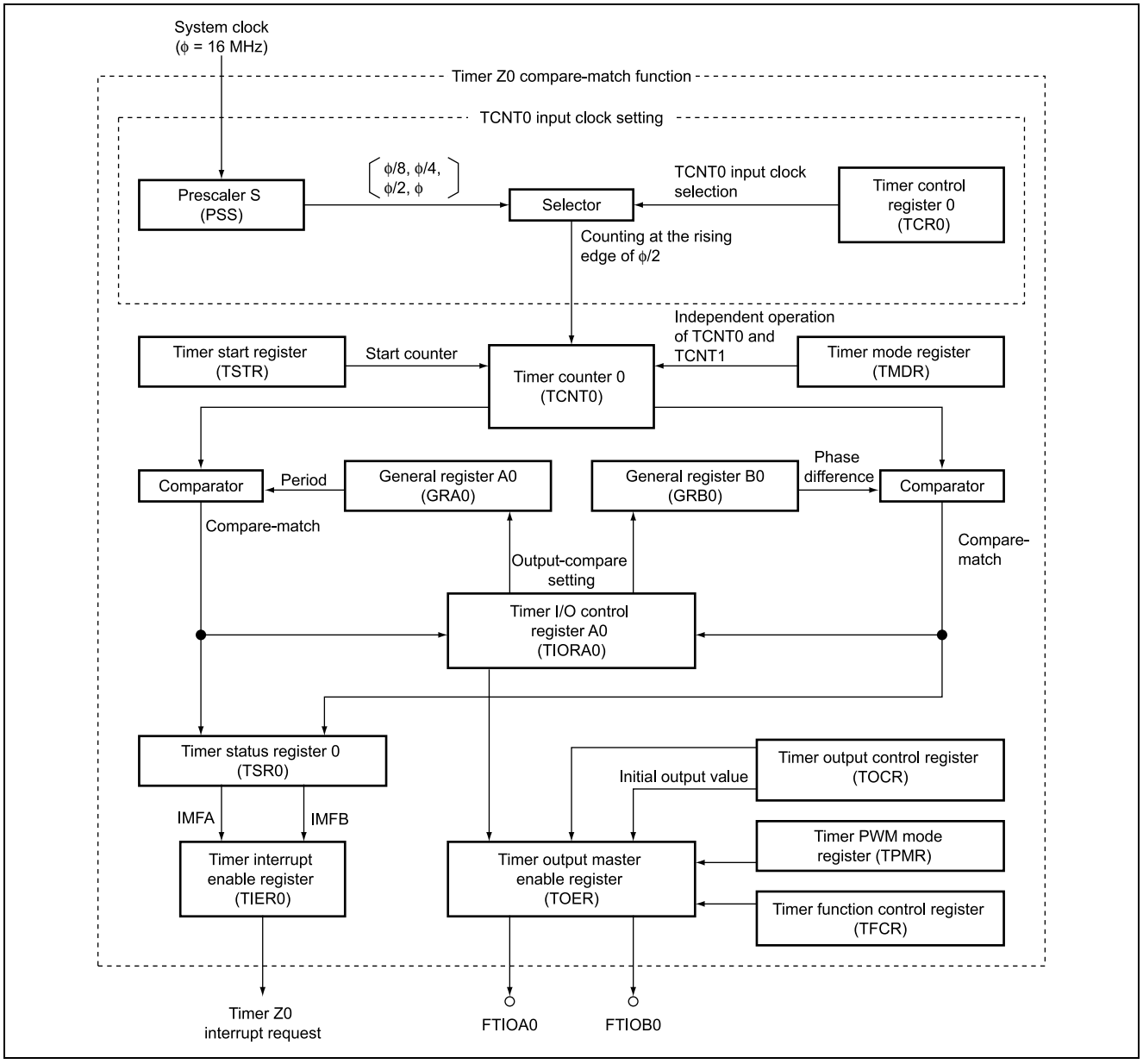


Figure 2.1 Block Diagram of Timer Z0

2. Figure 2.2 shows how the period and phase difference of the output pulses are set.

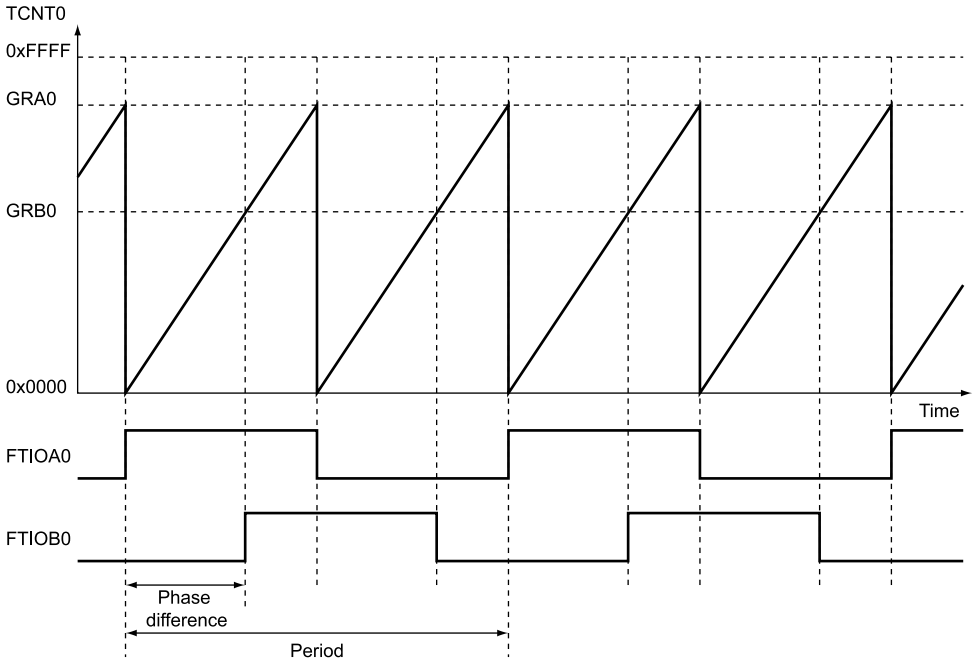


Figure 2.2 How the Period and Phase Difference of the Output Pulses are Set

3. Table 2.1 lists the function allocation for this sample task. The functions listed in this table are allocated so that two pulse waveforms are output with a desired phase difference.

Table 2.1 Function Allocation

Function	Description
TCR0	Specifies the TCNT0 input clock.
TIORA0	Specifies the GRA0 and GRB0 as output-compare registers
TSR0	Controls flags by GRA0 and GRB0 compare-matches .
TIER0	Enables interrupt requests by GRA0 and GRB0 compare-matches.
TCNT0	16-bit counter that counts at the rising edge of $\phi/2$.
GRA0	Specifies a pulse period.
GRB0	Specifies a phase difference of the pulse waveforms.
TSTR	Controls TCNT0 count start and stop.
TMDR	Specifies TCNT0 to operate independently of TCNT1.
TPMR	Specifies the FTIOB pin for normal operation.
TFCR	Specifies channels 0 and 1 for normal operation.
TOER	Enables the FTIOA0 and FTIOB0 pin outputs.
TOCR	Specifies the FTIOA0 and FTIOB0 pins' initial output values as 0.

3. Description of Operation

Operation of this sample task is described in figure 3.1. Hardware and software processing are applied in the way shown in figure 3.1 to output two pulse waveforms with a desired phase difference by using the timer Z0 compare-match function.

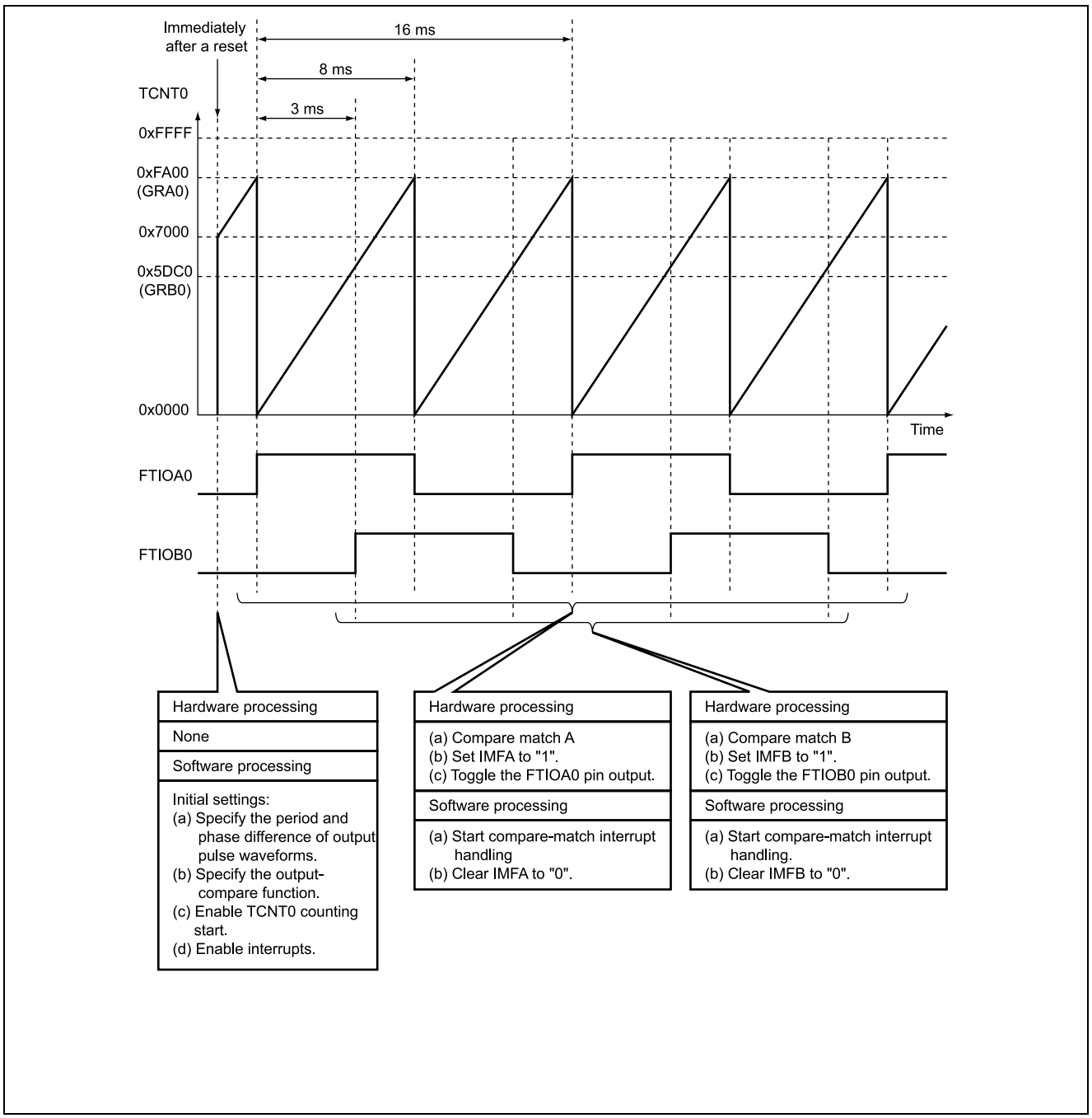


Figure 3.1 Principle of Operation

4. Description of Software

4.1 Modules

Table 4.1 describes the modules used in this sample task.

Table 4.1 Description of Modules

Module Name	Label Name	Function
Main routine	main	Specifies a period and a phase difference of pulses that is output using the timer Z0 output-compare function, starts the counter, and specifies interrupts.
Timer Z0 interrupt handling	tz0int	Timer Z0 interrupt handling. Clears the IMFA and IMFB flags.

4.2 Arguments

This sample task uses no arguments.

4.3 Internal Registers

The internal registers used in this sample task are described below.

- TCR0 Timer control register 0 Address: 0xF700

Bit	Bit Name	Setting	Function
7	CCLR2	CCLR2 = 0	Counter clear 2 to 0
6	CCLR1	CCLR1 = 0	CCLR2 = 0, CCLR1 = 0, CCLR0 = 1:
5	CCLR0	CCLR0 = 1	Clears TCNT0 on compare-match/input-capture with GRA0.
4	CKEG1	CKEG1 = 0	Clock edge 1 to 0
3	CKEG0	CKEG0 = 0	CKEG1 = 0, CKEG0 = 0: Counts at the rising edge of the clock.
2	TPSC2	TPSC2 = 0	Timer prescaler 2 to 0
1	TPSC1	TPSC1 = 0	TPSC2 = 0, TPSC1 = 0, TPSC0 = 1: Counts by ϕ/2.
0	TPSC0	TPSC0 = 1	

- TIORA0 Timer I/O control register A0 Address: 0xF701

Bit	Bit Name	Setting	Function
6	IOB2	IOB2 = 0	I/O control B2 to B0
5	IOB1	IOB1 = 1	IOB2 = 0, IOB1 = 1, IOB0 = 1:
4	IOB0	IOB0 = 1	Specifies the GRB0 as an output-compare register and specifies the FTIOB0 pin to toggle the output on a compare-match.
2	IOA2	IOA2 = 0	I/O control A2 to A0
1	IOA1	IOA1 = 1	IOA2 = 0, IOA1 = 0, IOA0 = 1:
0	IOA0	IOA0 = 1	Specifies the GRA0 as an output-compare register and specifies the FTIOA0 pin to toggle the output on a compare-match.

- TSR0 Timer status register 0 Address: 0xF703

Bit	Bit Name	Setting	Function
1	IMFB	0	Input capture/compare-match flag B IMFB = 0: Indicates that the TCNT0 value does not match GRB0. IMFB = 1: Indicates that the TCNT0 value matches GRB0.
0	IMFA	0	Input capture/compare-match flag A IMFA = 0: Indicates that the TCNT0 value does not match GRA0. IMFA = 1: Indicates that the TCNT0 value matches GRA0.

- TIER0 Timer interrupt enable register 0 Address: 0xF704

Bit	Bit Name	Setting	Function
1	IMIEB	1	Input-capture/compare-match interrupt enable B IMIEB = 0: Disables interrupts by IMFB of TSR0 when IOB2 of TIORB0 is 0 (output compare is selected). IMIEB = 1: Enables interrupts by IMFB of TSR0 when IOB2 of TIORB0 is 0 (output compare is selected).
0	IMIEA	1	Input-capture/compare-match interrupt enable A IMIEA = 0: Disables interrupts by IMFA of TSR0 when IOA2 of TIORA0 is 0 (output compare is selected). IMIEA = 1: Enables interrupts by IMFA of TSR0 when IOA2 of TIORA0 is 0 (output compare is selected).

- TCNT0 Timer counter 0 Address: 0xF706
  Function: A 16-bit upward counter that is incremented at the rising edge of $\phi/2$.
  Setting: 0x7000

- GRA0 General register A0 Address: 0xF708
  Function: A compare-match is generated if the GRA0 value matches TCNT0 counter value.
  Setting: 0xFA00

- GRB0 General register B0 Address: 0xF70A
  Function: A compare-match is generated if the GRB0 value matches TCNT0 counter value.
  Setting: 0x5DC0

- TSTR Timer start register Address: 0xF720

Bit	Bit Name	Setting	Function
0	STR0	0	Channel 0 counter start STR0 = 0: Stops counting by TCNT0. STR0 = 1: Starts counting by TCNT0

- TMDR Timer mode register Address: 0xF721

Bit	Bit Name	Setting	Function
0	SYNC	0	Timer synchronization SYNC = 0: TCNT0 operates independently of TCNT1. SYNC = 1: TCNT0 operates synchronously with TCNT1.

- TPMR Timer PWM mode register Address: 0xF722

Bit	Bit Name	Setting	Function
0	PWMB0	0	PWM mode B0 PWMB0 = 0: Specifies the FTIOB0 pin for normal operation mode. PWMB0 = 1: Specifies the FTIOB0 pin for PWM mode.

- TFCR Timer function control register Address: 0xF723

Bit	Bit Name	Setting	Function
1	CMD1	CMD1 = 0	Combination mode 1 to 0
0	CMD0	CMD0 = 0	CMD1 = 0, CMD0 = 0: Channels 0 and 1 operate in normal operation mode.

- TOER Timer output master enable register Address: 0xF724

Bit	Bit Name	Setting	Function
1	EB0	0	Master enable B0 EB0 = 0: Enables the FTIOB0 pin output. EB0 = 1: Disables the FTIOB0 pin output.
0	EA0	0	Master enable A0 EA0 = 0: Enables the FTIOA0 pin output. EA0 = 1: Disables the FTIOA0 pin output.

- TOCR Timer output control register Address: 0xF725

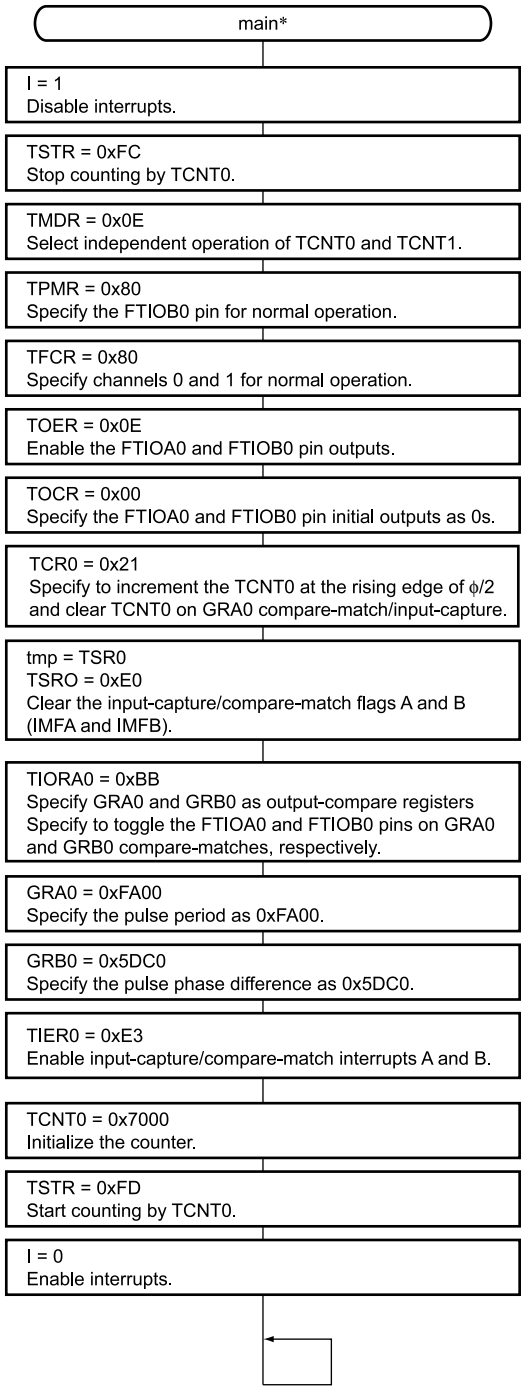
Bit	Bit Name	Setting	Function
1	TOB0	0	Output level select B0 TOB0 = 0: Specifies the FTIOB0 pin initial output as 0. TOB0 = 1: Specifies the FTIOB0 pin initial output as 1.
0	TOA0	0	Output level select A0 TOA0 = 0: Specifies the FTIOA0 pin initial output as 0. TOA0 = 1: Specifies the FTIOA0 pin initial output as 1.

4.4 Description of RAM

This sample task does not use RAM.

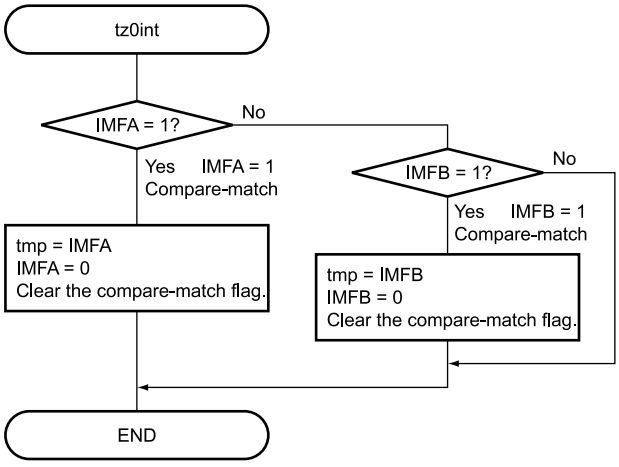
5. Flowcharts

1. Main routine



Note: * The stack pointer is specified by INIT.SRC (assembly language).

2. Timer Z0 interrupt handling



6. Program Listing

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*   H8/300HN Series -H8/3687-                                                                                          */
/*   Application Note                                                                                                   */
/*                                                                                                                      */
/*   'Pulse Output of Random Phase Difference by                                                                        */
/*   Output Compare Function'                                                                                           */
/*                                                                                                                      */
/*   Function                                                                                                           */
/*   : Timer Z Output Compare                                                                                           */
/*                                                                                                                      */
/*   External Clock :    16MHz                                                                                          */
/*   Internal Clock :    16MHz                                                                                          */
/*   Sub Clock :    32.768kHz                                                                                           */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*   Symbol Definition                                                                                                  */
/************************************************************************************************************************/
struct BIT {
     unsigned char   b7:1;         /* bit7 */
     unsigned char   b6:1;         /* bit6 */
     unsigned char   b5:1;         /* bit5 */
     unsigned char   b4:1;         /* bit4 */
     unsigned char   b3:1;         /* bit3 */
     unsigned char   b2:1;         /* bit2 */
     unsigned char   b1:1;         /* bit1 */
     unsigned char   b0:1;         /* bit0 */
};

#define        TCR0           *(volatile unsigned char *)0xF700                  /* Timer control register_0                */
#define        TIORA0         *(volatile unsigned char *)0xF701                  /* Timer I/O Control Register A_0          */
#define        TSR0           *(volatile unsigned char *)0xF703                  /* Timer status register_0                 */
#define        TSR0_BIT       (*(struct BIT *)0xF703)                            /* Timer status register_0                 */
#define        IMFB           TSR0_BIT.b1                                        /* Input Capture/Compare Match Flag B      */
#define        IMFA           TSR0_BIT.b0                                        /* Input Capture/Compare Match Flag A      */
#define        TIER0          *(volatile unsigned char *)0xF704                  /* Timer interrupt enable register0        */
#define        TIER0_BIT      (*(struct BIT *)0xF704)                            /* Timer interrupt enable register0        */
#define        IMIEA          TIER0_BIT.b0                                       /* Input Capture/Compare Match             */
                                                                                 /* Interrupt Enable A                      */
#define        TCNT0          *(volatile unsigned short *)0xF706                 /* Timer counter_0                         */
#define        GRA0           *(volatile unsigned short *)0xF708                 /* General register A_0                    */
#define        GRB0           *(volatile unsigned short *)0xF70A                 /* General register B_0                    */
#define        TSTR           *(volatile unsigned char *)0xF720                  /* Timer start register                    */
#define        TMDR           *(volatile unsigned char *)0xF721                  /* Timer mode register                     */
#define        TPMR           *(volatile unsigned char *)0xF722                  /* Timer PWM mode register                 */
#define        TFCR           *(volatile unsigned char *)0xF723                  /* Timer function control register         */
#define        TOER           *(volatile unsigned char *)0xF724                  /* Timer output master enable register     */
#define         TOCR          *(volatile unsigned char *)0xF725                  /* Timer output control register           */

#pragma interrupt   (tz0int)
```

```
/************************************************************************************************************************/
/*   Function define                                                                                                    */
/************************************************************************************************************************/
extern void INIT ( void )                                                   /* SP Set                                   */
void main ( void );
void tz0int ( void );

/************************************************************************************************************************/
/*   Vector Address                                                                                                     */
/************************************************************************************************************************/
#pragma section     V1                                                      /* VECTOR SECTOIN SET                       */
void (*const VEC_TBL1[])(void) = {                                          /* 0x00 - 0x0f                              */
     INIT                                                                   /* 00 Reset                                 */
};
#pragma section     V2                                                      /* VECTOR SECTOIN SET                       */
void (*const VEC_TBL2[])(void) = {
     tz0int                                                                 /* 34 Timer Z0 Interrupt                    */
};

#pragma section                                                             /* P                                        */
/************************************************************************************************************************/
/*   Main Program                                                                                                       */
/************************************************************************************************************************/
void main ( void )
{
     unsigned char tmp;

     set_imask_ccr(1);                                                      /* Interrupt Disable                        */

     TSTR = 0xFC;                                                           /* TCNT0 count stop                         */
     TMDR = 0x0E;                                                           /* TCNT0,TCNT1 Single Mode                  */
     TPMR = 0x88;                                                           /* FTIOB0 is Normal Mode                    */
     TFCR = 0x80;                                                           /* Chanel 0,1 is Normal Mode                */
     TOER = 0xFC;                                                           /* FTIOA0,B0 Output Enable                  */
     TOCR = 0x00;                                                           /* FTIOA0,B0 initial outputs is 0           */
     TCR0 = 0x21;                                                           /* Rising edge, phi/2 Clock count           */
     tmp = TSR0;
     TSR0 = 0xE0;                                                           /* Interrupt Flag Clear                     */
     TIORA0 = 0xBB;                                                         /* FTIOA0,B0 Toggle Output                  */
     GRA0 = 0xFA00;                                                         /* Set GRA0                                 */
     GRB0 = 0x5DC0;                                                         /* Set GRB0                                 */
     TIER0 = 0xE3;                                                          /* IMFA,IMFB Interrupt Enable               */
     TCNT0 = 0x7000;                                                        /* Set                                      */
     TSTR = 0xFD;                                                           /* TCNT0 count start                        */

     set_imask_ccr(0);                                                      /* Interrupt Enable                         */

     while(1);
}
```

```
/************************************************************************************************************************/
/*   Timer Z0 Interrupt                                                                                                 */
/************************************************************************************************************************/
void tz0int ( void )
{
     unsigned char tmp;

     if(IMFA == 1){                                                    /* Interrupt by IMFA flag                 */
          tmp = IMFA;
          IMFA = 0;                                                    /* Clear IMFA Flag                        */
     }
     else if(IMFB == 1){                                               /* Interrupt by IMFB flag                 */
          tmp = IMFB;
          IMFB = 0;                                                    /* Clear IMFB Flag                        */
     }
}
```

Link address specifications

Section Name	Address
CV1	0x0000
CV2	0x0034
P	0x0100
B	0xFB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.29.03	—	First edition issued

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