

1. Abstract

This document describes procedures to enter PLL operating mode (PLL clock divided by 1) from high-speed mode (main clock divided by 1), and high-speed mode (main clock divided by 1) from PLL operating mode (PLL clock divided by 1) in the M16C/64A Group.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU):

- MCU: M16C/64A Group

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the sample code described in this application note.

3. Clock Mode Transition Procedure

Figure 3.1 shows the Transition from High-Speed Mode to PLL Operating Mode, and Figure 3.2 shows the Transition from PLL Operating Mode to High-Speed Mode.

tsu(PLL): PLL frequency synthesizer stabilization wait time

Refer to the “Electrical Characteristics” in the User’s Manual: Hardware (Hardware Manual) for details on tsu(PLL).

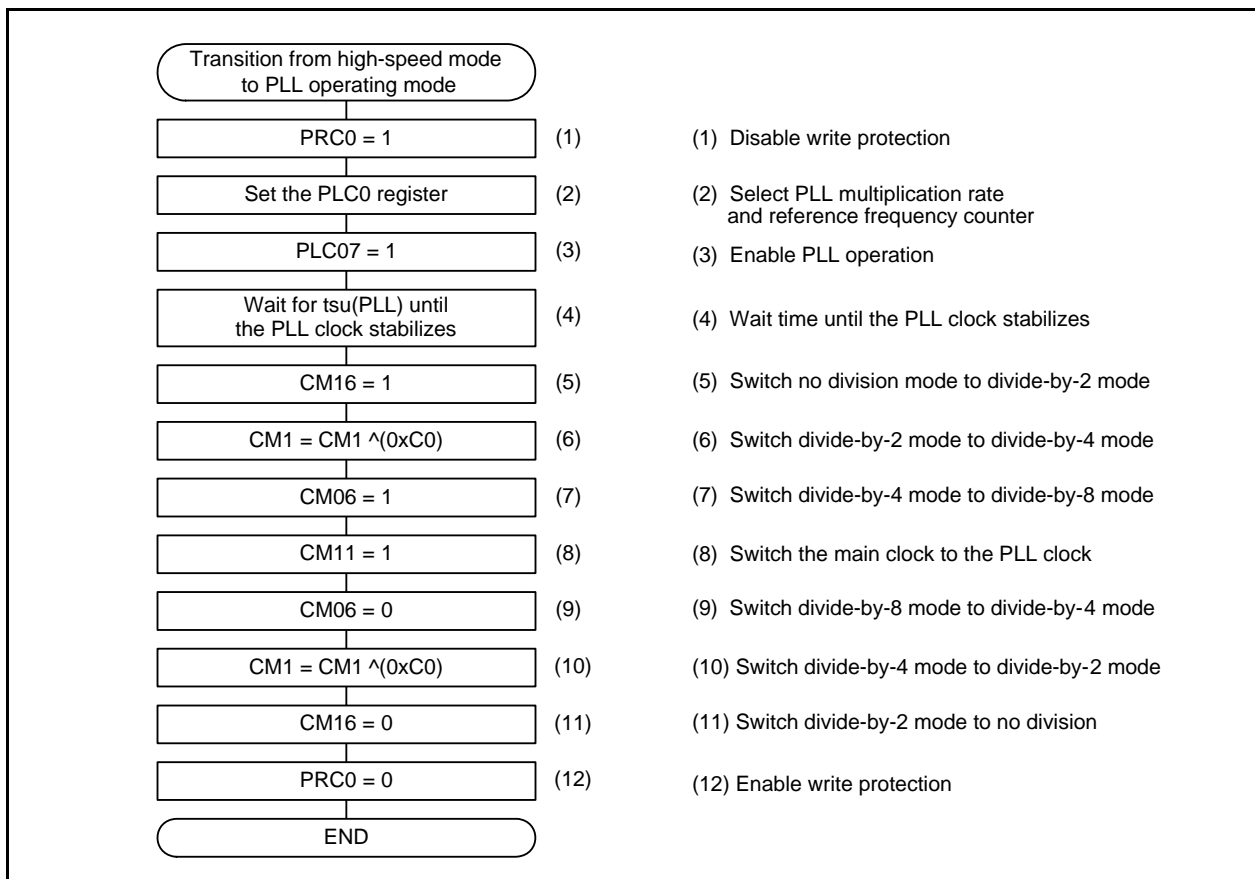


Figure 3.1 Transition from High-Speed Mode to PLL Operating Mode

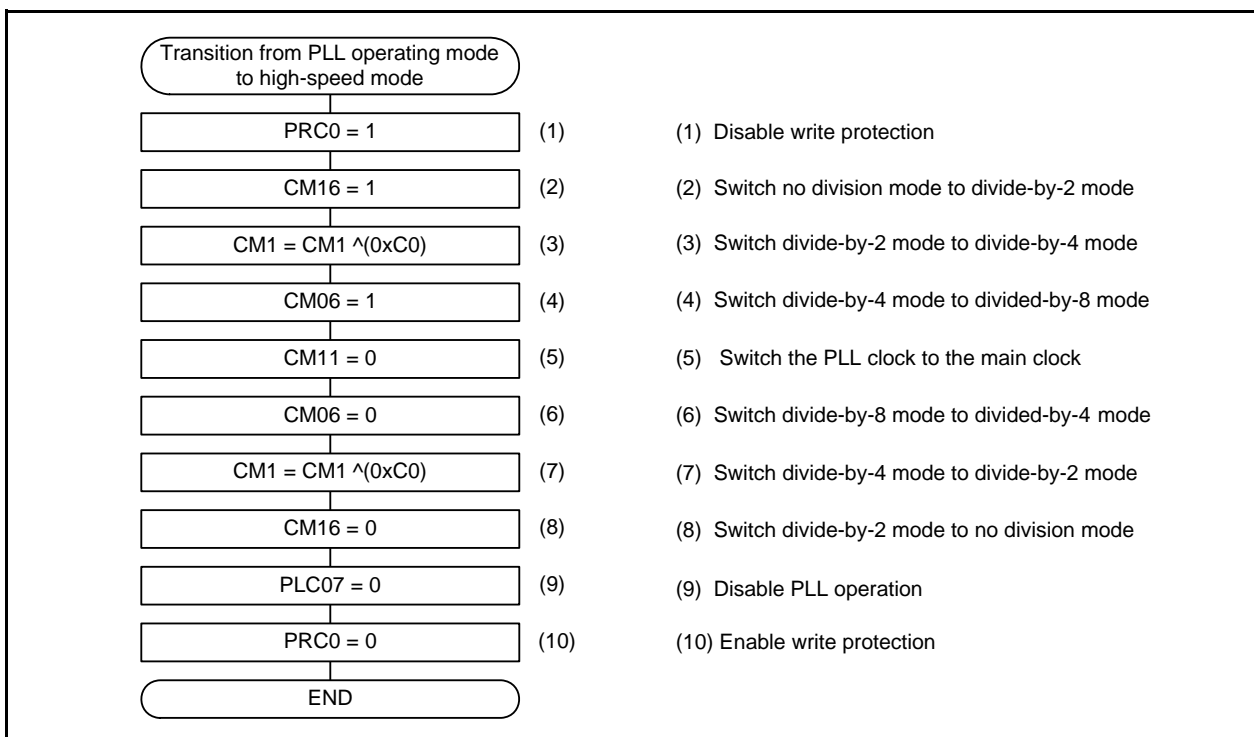


Figure 3.2 Transition from PLL Operating Mode to High-Speed Mode

4. Sample Code

A sample code can be downloaded from the Renesas Electronics website.
To download, click “Application Notes” in the left-hand side menu of the M16C Family page.

4.1 Sample Code Operation

Functions for transitions between high-speed mode and PLL operating mode are executed in the sample code. Refer to 4.2 Function Tables for details of each function.

The settings in the sample code are as follows: the PLL reference frequency counter is no division, the multiplication rate selected in the PLC0 register is multiply-by-6, and the PLL frequency synthesizer stabilization wait time is approximately 5 ms when the CPU clock is 4 MHz.

4.2 Function Tables

Function Tables for This Document

| | |
|----------------|-------------------------------------------------------------------------------------------|
| Declaration | void pll_from_highspeed(void) |
| Outline | Transition from high-speed mode to PLL operating mode |
| Argument | None |
| Variable | None |
| Returned value | None |
| Function | Switch the CPU clock from high-speed mode to PLL operating mode (PLL clock divided by 1). |

| | |
|----------------|-------------------------------------------------------------------------------------------|
| Declaration | void highspeed_from_pll(void) |
| Outline | Transition from PLL operating mode to high-speed mode |
| Argument | None |
| Variable | None |
| Returned value | None |
| Function | Switch the CPU clock from PLL operating mode (PLL clock divided by 1) to high-speed mode. |

Function Tables for the Sample Code

| | |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| Declaration | void mcu_init(void) |
| Outline | CPU initialization |
| Argument | None |
| Variable | None |
| Returned value | None |
| Function | Set to single-chip mode. Switch the CPU clock from 125 kHz on-chip oscillator mode divided-by-8 to 125 kHz on-chip oscillator mode divided-by-1. |

| | |
|----------------|-----------------------------------------------------------------------------------------------------|
| Declaration | void highspeed_from_foco125k(void) |
| Outline | Transition from 125 kHz on-chip oscillator mode to high-speed mode |
| Argument | None |
| Variable | None |
| Returned value | None |
| Function | Switch the CPU clock from 125 kHz on-chip oscillator mode (fOCO-S divided by 1) to high-speed mode. |

5. Reference Documents

M16C/64A Group User's Manual: Hardware (Hardware Manual) Rev.1.10

The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

M16C Series/R8C Family C Compiler Package V.5.45 C Compiler User Manual Rev.2.00

The latest version can be downloaded from the Renesas Electronics website.

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| | |
|------------------|-----------------------------------------------------------------------------|
| Revision History | M16C/64A Group Transition between High-Speed Mode and PLL Operating Mode |
|------------------|-----------------------------------------------------------------------------|

| Rev. | Date | Description | |
|------|------------|-------------|----------------------|
| | | Page | Summary |
| 1.00 | 2010.07.01 | — | First edition issued |
| | | | |

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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