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**M16C/63, 64A, 64C, 65, 65C, 6C, 5LD, 56D, 5L, 56, 5M,  
57 Groups**  
 ROM Verification Using CRC-CCITT During Self Test on MCU Start-Up
 

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 R01AN0706EJ0100  
 Rev. 1.00  
 July 31, 2011

## Abstract

To ensure safety, Europe requires that household appliances comply with the IEC 60730 safety standard. IEC 60730 Annex H provides three software classifications for automatic electronic controls.

Class A: Control functions, which are not intended to be relied upon for the safety of the equipment.

Examples: Timers, switches, and lighting controls.

Class B: Control functions, which are intended to prevent unsafe operation of the controlled equipment.

Examples: Washing machines, dishwashers, dryers, and refrigerator controls.

Class C: Control functions, which are intended to prevent special hazards.

Example: Burner controls.

Renesas recommends the following self-tests be performed for end products included in class B.

- Stack fault diagnostics for the MCU and program counter
- Anomaly diagnostics for interrupt periods
- Anomaly diagnostics for MCU clock frequencies
- Anomaly diagnostics for ROM/RAM
- Anomaly diagnostics for external interfaces (communication)

This application note describes a method for diagnosing anomalies in the ROM. When starting up the M16C/60 Series and M16C/50 Series MCUs, read the CRC calculation in the program ROM 1 area, and ascertain if an anomaly has occurred.

In this application note, the CRC calculation result is output using the CRC code generator. For details on using the CRC code generator, refer to chapter 6 Application Example. The CRC code generator can be downloaded from the following URL:

[http://www.renesas.com/support/downloads/download\\_results/C2012801-C2012900/crc\\_code.jsp](http://www.renesas.com/support/downloads/download_results/C2012801-C2012900/crc_code.jsp)

This URL is subject to change without prior notice.

## Products

MCUs: M16C/63 Group, M16C/64A Group, M16C/64C Group, M16C/65 Group, M16C/65C Group, M16C/6C Group, M16C/5LD Group, M16C/56D Group, M16C/5L Group, M16C/56 Group, M16C/5M Group, M16C/57 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

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# 1. Specifications

Use the CRC code generator to calculate the CRC code for comparison in advance, and write the result to a data flash area. When the MCU starts up, sequentially read the data in the program ROM 1 area in 1-byte units from the start address <sup>(1)</sup> to the end address (FFFFh). Then perform CRC calculation on the data read using the CRC-CCITT generator polynomial. Ascertain if the CRC calculation result in the program ROM 1 area and the CRC code for comparison prewritten to the data flash area match. If the values match, the program ROM 1 area is determined to be accurate. This document describes an example using the M16C/65 Group.

Note:

1. The start address varies with the ROM size.

Figure 1.1 shows the CRC address, and the address of the internal ROM (program ROM 1) checked when the MCU starts up.

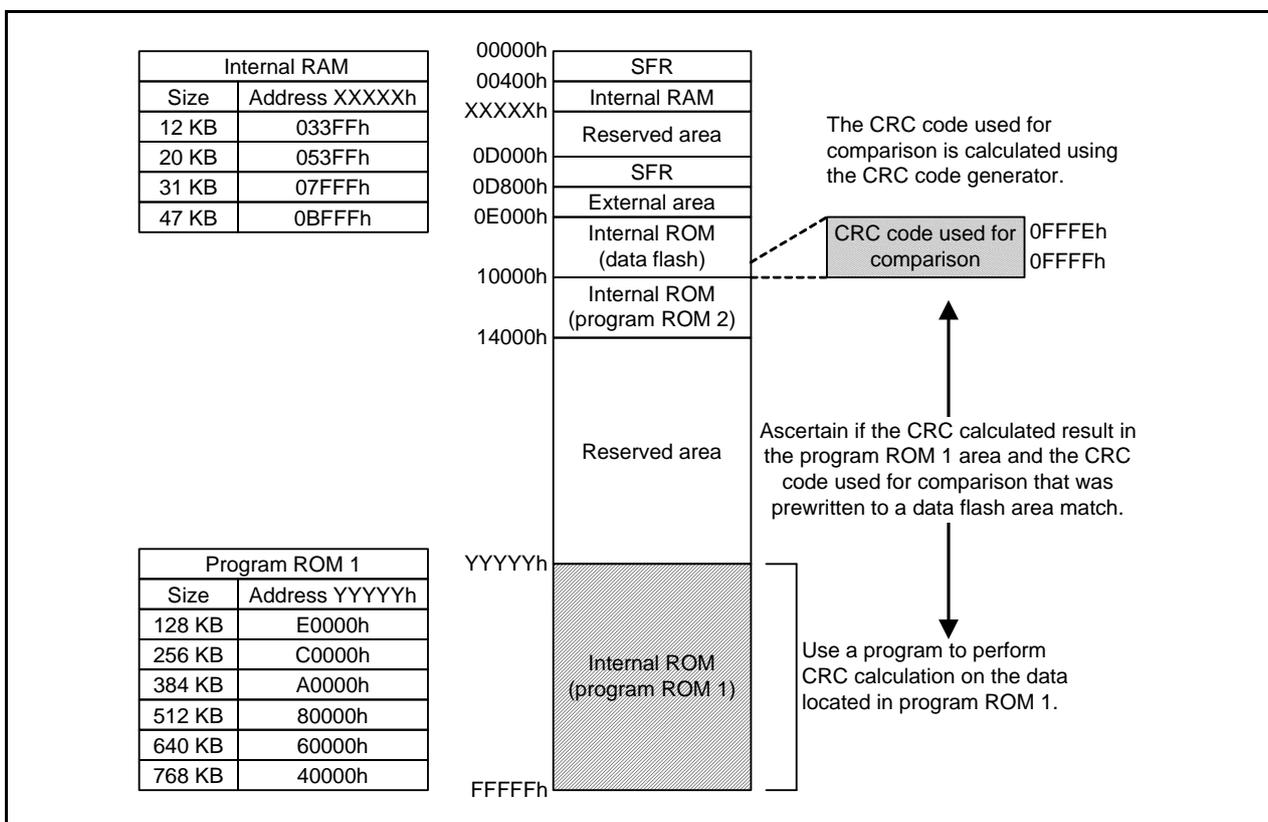


Figure 1.1 Sample Code Address Space in the M16C/65 Group

## 2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

**Table 2.1 Operation Confirmation Conditions**

Item	Contents
MCU used	M16C/65 Group
Operating frequencies	<ul style="list-style-type: none"><li>• XIN clock: 8 MHz</li><li>• CPU clock: 32 MHz (PLL clock is divided by 2, then multiplied by 8)</li></ul>
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.08
C compiler	Renesas Electronics Corporation M16C Series, R8C Family Compiler V.5.45 Release 01 Compile options -c -finfo -dir "\$(CONFIGDIR)" (Default setting is used in the integrated development environment.)
Operating mode	Single-chip mode
Sample code version	Version 1.00

## 3. Reference Application Note

The application note associated with this application note is listed below. Refer to this application note for additional information.

- M16C/63, 64A, 64C, 65, 65C, 6C, 5LD, 56D, 5L, 56, 5M, 57 Groups  
ROM Verification Using Checksum During Self-Test on MCU Start-Up (R01AN0705EJ)

## 4. Hardware

### 4.1 Pins Used

Table 4.1 lists the Pins Used and Their Functions.

**Table 4.1 Pins Used and Their Functions**

Pin Name	I/O	Function
P4_0	Output	High is output when the values match.
P4_1	Output	High is output when the values do not match.

## 5. Software

### 5.1 Operation Overview

In the sample code, steps (1) to (3) of the self-test are performed in order when the MCU starts up. Figure 5.1 shows Sample Code Operation.

- (1) Initialize the MCU after it starts up.
- (2) Verify the ROM area.
  - (2.1) Read the program ROM 1 area data in 1-byte units from the start address to the end address. Use the CRC-CCITT generator polynomial to CRC calculate the data that was read.
  - (2.2) Compare the CRC calculation results and the CRC code for comparison that was prewritten to the data flash area. If the values match, store the OK result in the variable. If the values do not match, store the NG result in the variable.
- (3) Perform processing for each match.
  - Output high from port P4\_0 when the values match.
  - Output high from port P4\_1 when the values do not match.

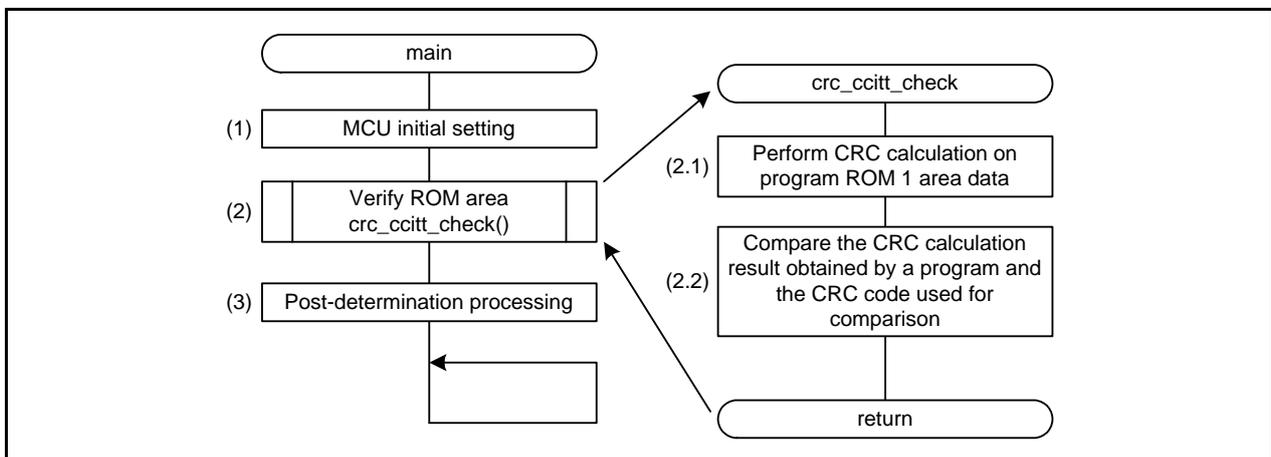


Figure 5.1 Sample Code Operation

## 5.2 Required Memory Size

Table 5.1 lists the Required Memory Size.

**Table 5.1 Required Memory Size**

Memory Used	Size	Remarks
ROM	270 bytes	In the r01an0706_src.c module
RAM	0 bytes	In the r01an0706_src.c module
Maximum user stack usage	18 bytes	
Maximum interrupt stack usage	0 bytes	

The required memory size varies depending on the C compiler version and compile options.

## 5.3 Constants

Table 5.2 lists the Constants Used in the Sample Code.

**Table 5.2 Constants Used in the Sample Code**

Constant Name	Setting Value	Contents
OK	0	The CRC codes match.
NG	FFh	The CRC codes do not match.
ROM_TOP	80000h	Start address of the program ROM 1 area (the sample code uses a starting address that assumes the ROM capacity to be 512 KB).
ROM_END	FFFFFFh	End address of the program ROM 1 area.
SUM_DF_ADR	0FFFCh	Address where the CRC code for comparison is saved (the sample code saves this to the data flash area last).

## 5.4 Functions

Table 5.3 lists the Functions.

**Table 5.3 Functions**

Function Name	Outline
mcu_init	CPU initial setting
crc_ccitt_check	ROM area determination

## 5.5 Function Specifications

The following tables list the sample code function specifications.

mcu_init	
Outline	CPU initial setting
Header	None
Declaration	void mcu_init(void)
Explanation	Set the PLL clock (divided by 2 and multiplied by 8) as the CPU clock.
Argument	None
Returned value	None
Remark	

crc_ccitt_check	
Outline	ROM area determination
Header	None
Declaration	unsigned char crc_ccitt_check(void)
Explanation	Use the CRC-CCITT generator polynomial to perform CRC calculation on the data in the program ROM 1 area, and ascertain if it matches the CRC code for comparison prewritten in the data flash area.
Argument	None
Returned value	<ul style="list-style-type: none"><li>• If the CRC codes match: OK (0)</li><li>• If the CRC codes do not match: NG (FFh)</li></ul>
Remark	

## 5.6 Flowcharts

### 5.6.1 Main Processing

Figure 5.2 shows the Main Processing.

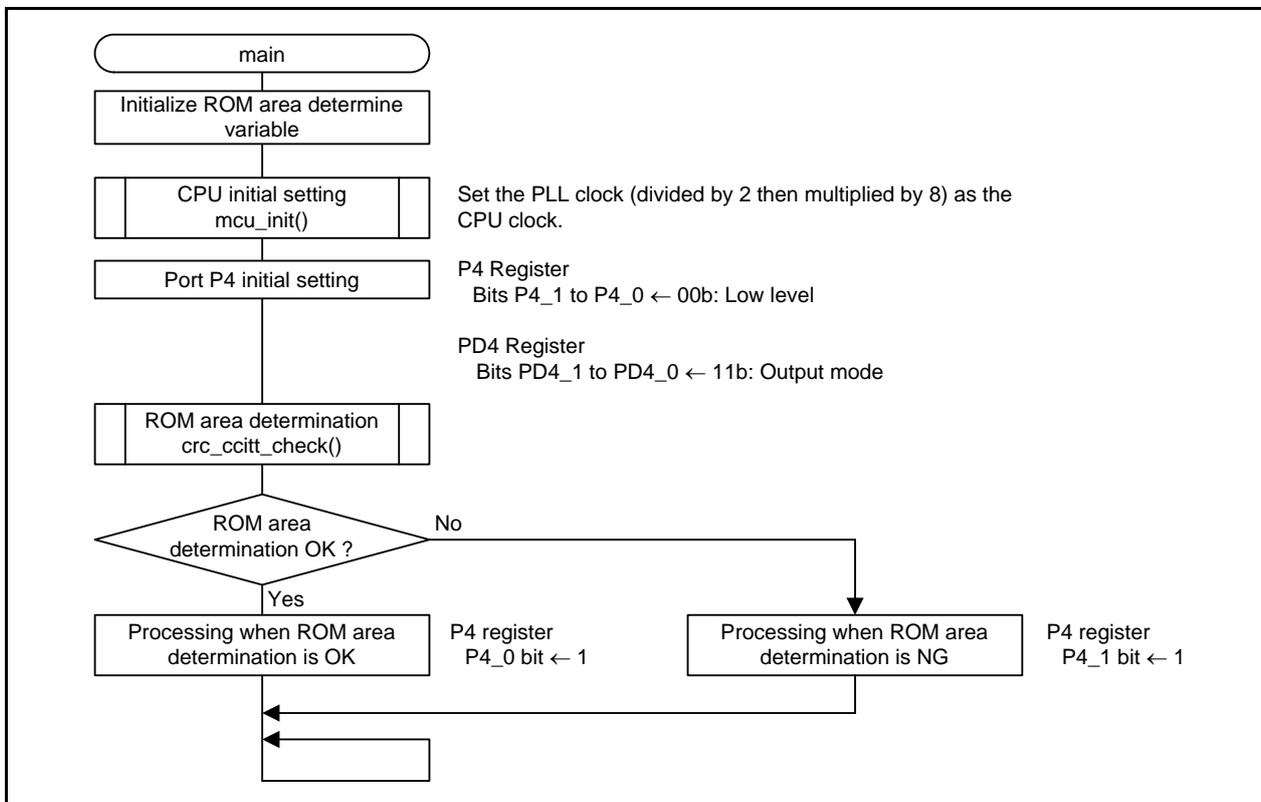


Figure 5.2 Main Processing

### 5.6.2 ROM Area Determination

Figure 5.3 shows the ROM Area Determination.

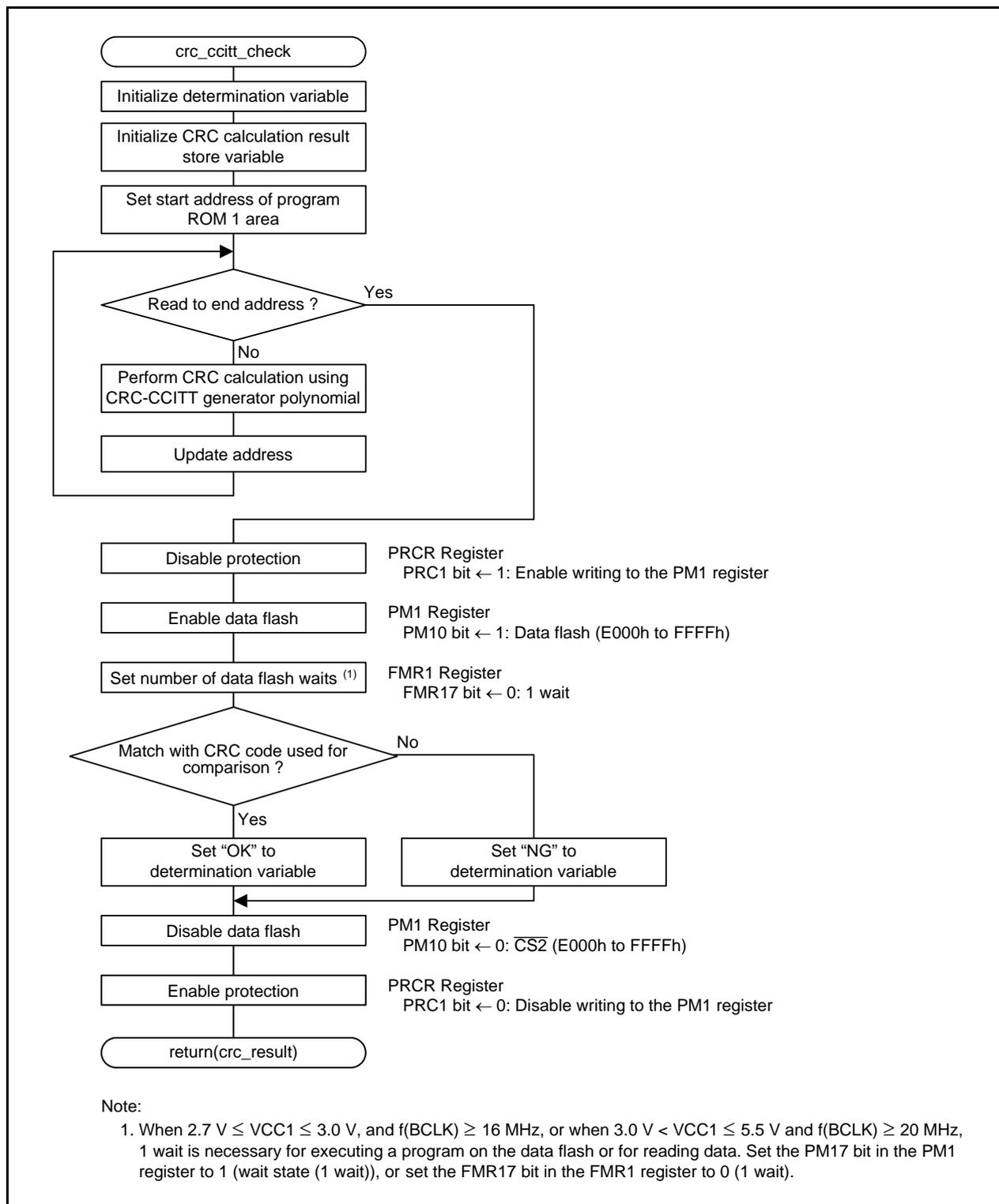


Figure 5.3 ROM Area Determination

## 6. Application Example

This application note uses the CRC code generator. For details on the CRC code generator, refer to the attached CRC code generator document.

### 6.1 CRC Code Generator Settings

This section describes how to set the CRC code generator to an integrated development environment using the custom build function in the High-performance Embedded Workshop. Figures 6.1 to 6.6 show an example of how to set the CRC code generator.

- (1) Register a build phase.

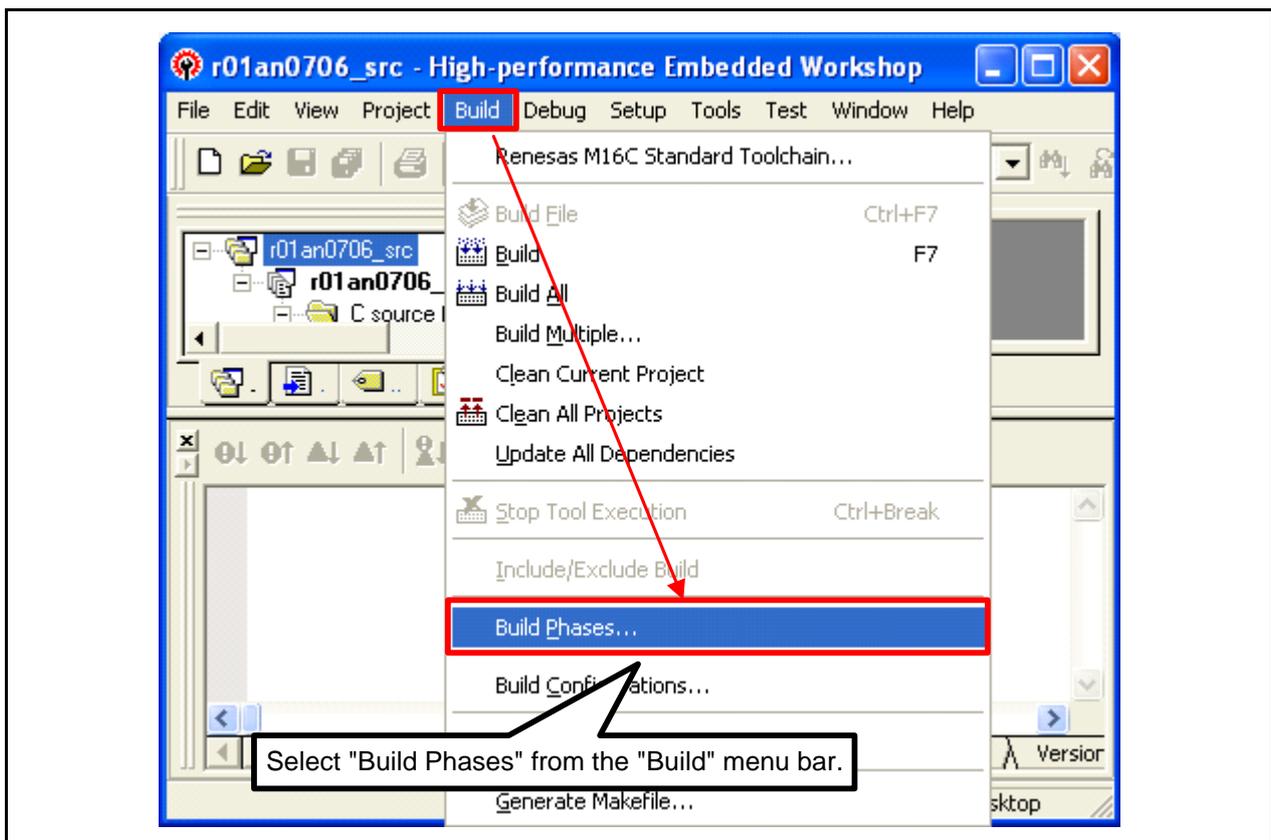


Figure 6.1 CRC Code Generator Setting (1/7)

(2) Add a build phase.

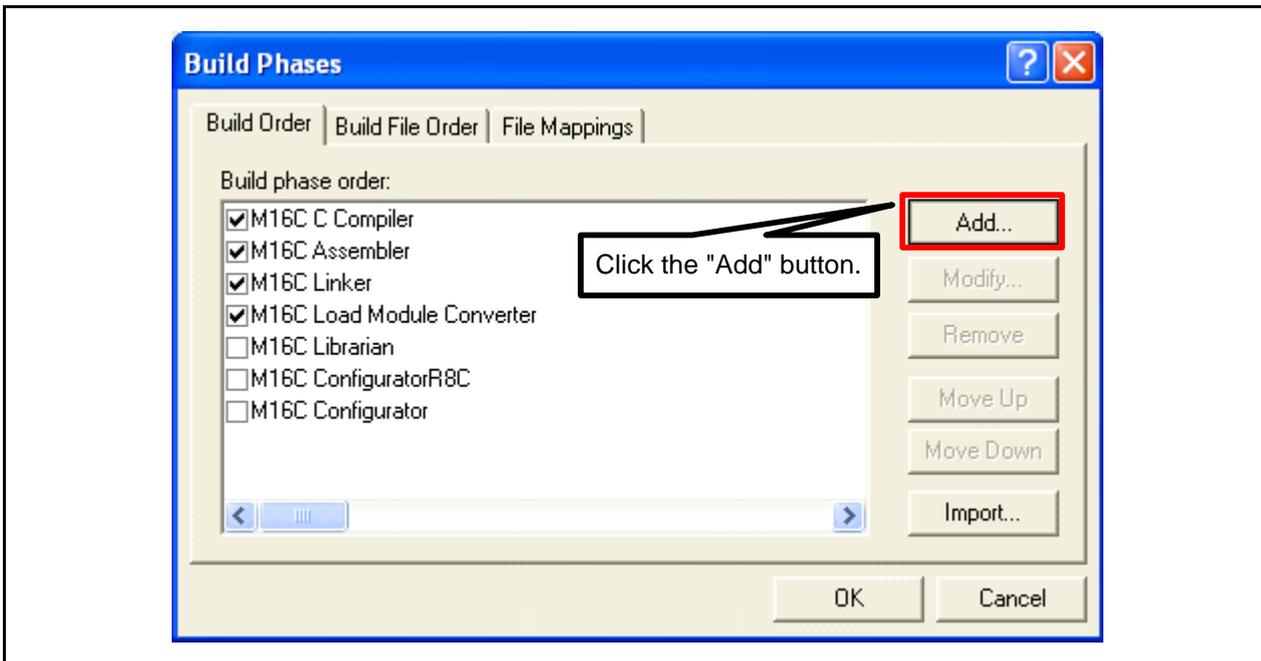


Figure 6.2 CRC Code Generator Setting (2/7)

(3) Create a new custom phase.

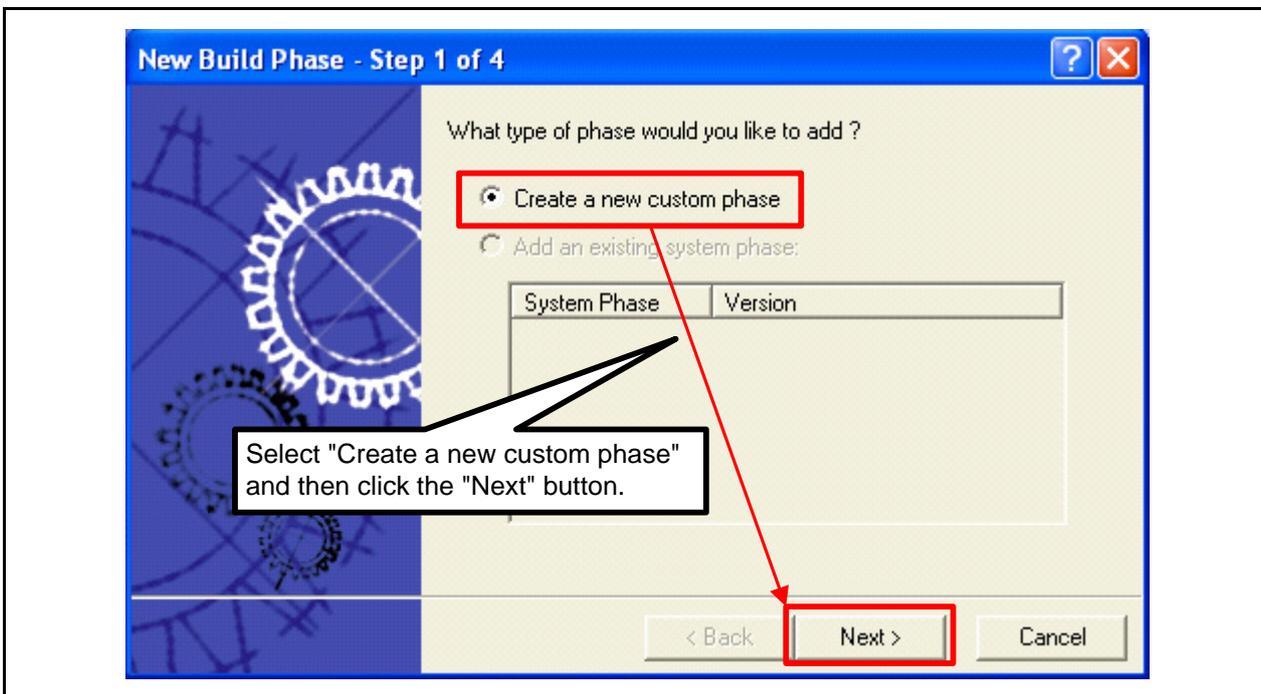


Figure 6.3 CRC Code Generator Setting (3/7)

(4) Select single phase.

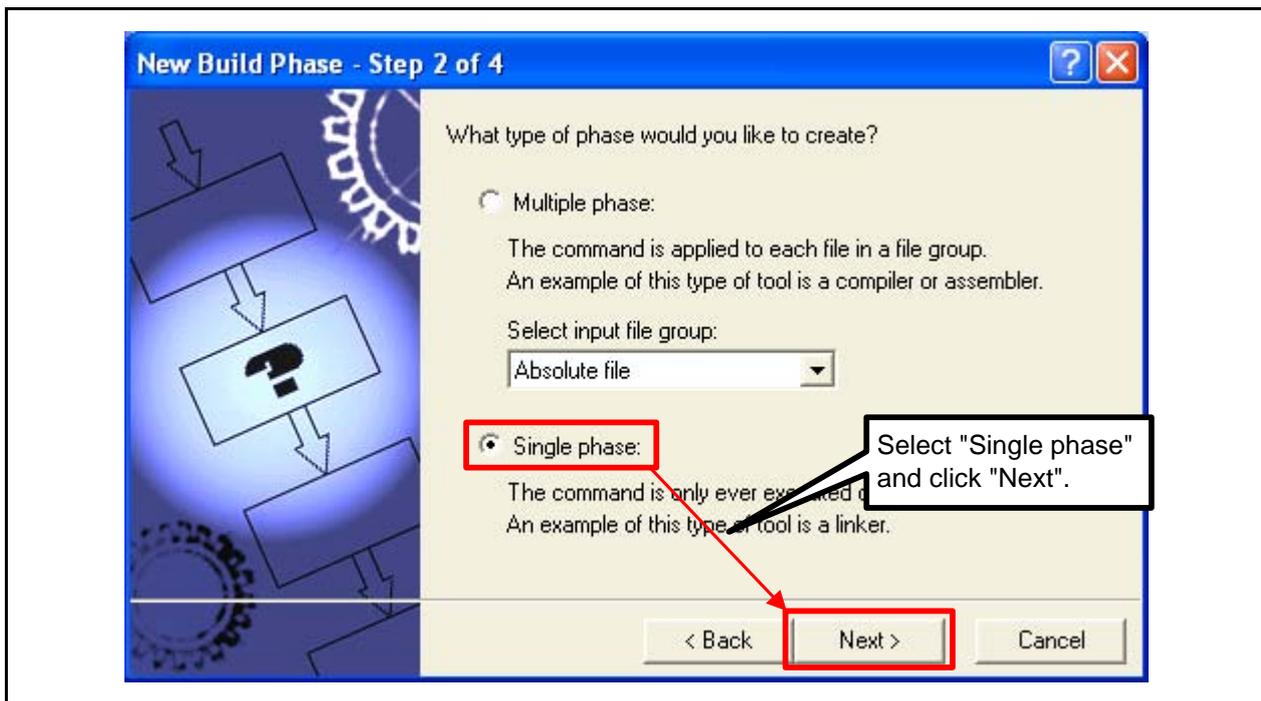


Figure 6.4 CRC Code Generator Setting (4/7)

(5) Input phase name and select the directory installed.

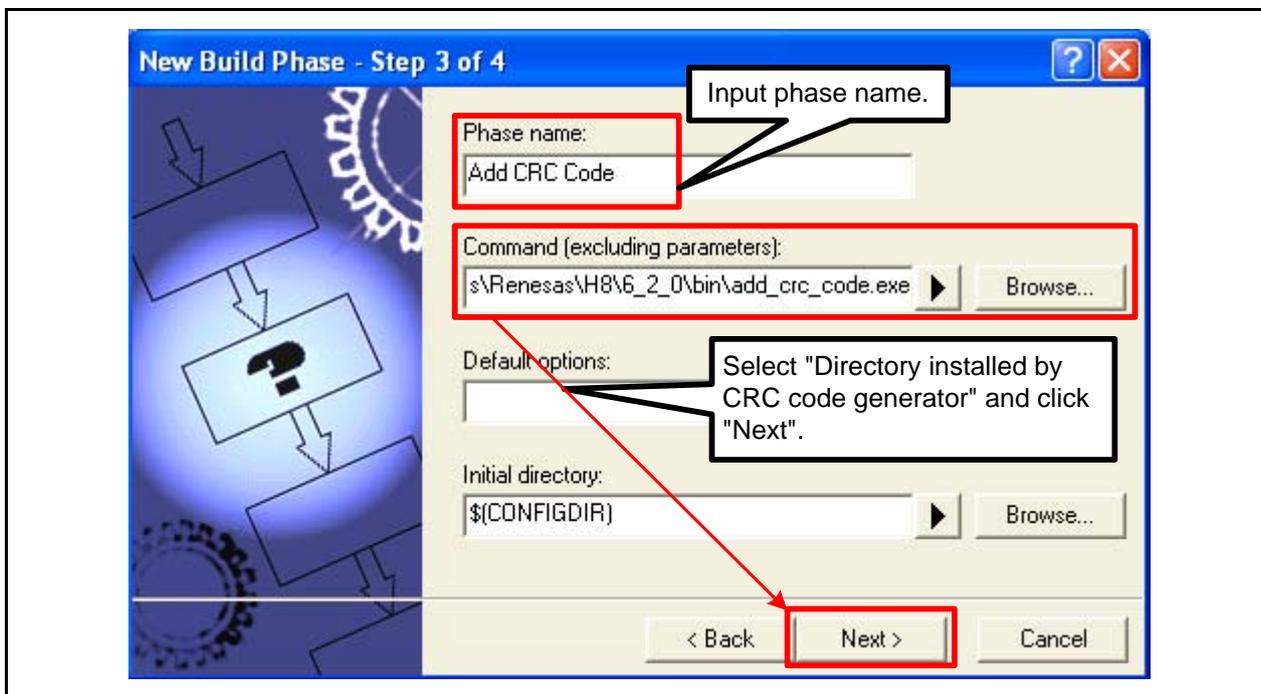


Figure 6.5 CRC Code Generator Setting (5/7)

(6) Set environment variables.

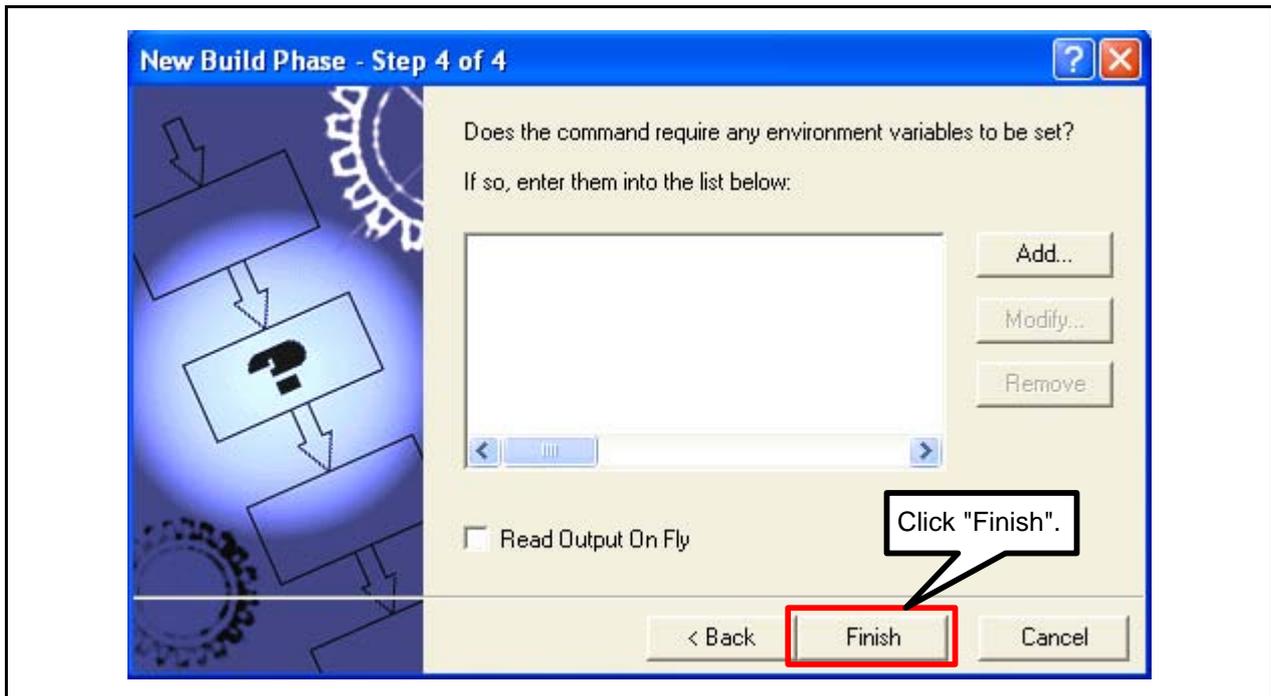


Figure 6.6 CRC Code Generator Setting (6/7)

(7) Complete build phase registration.

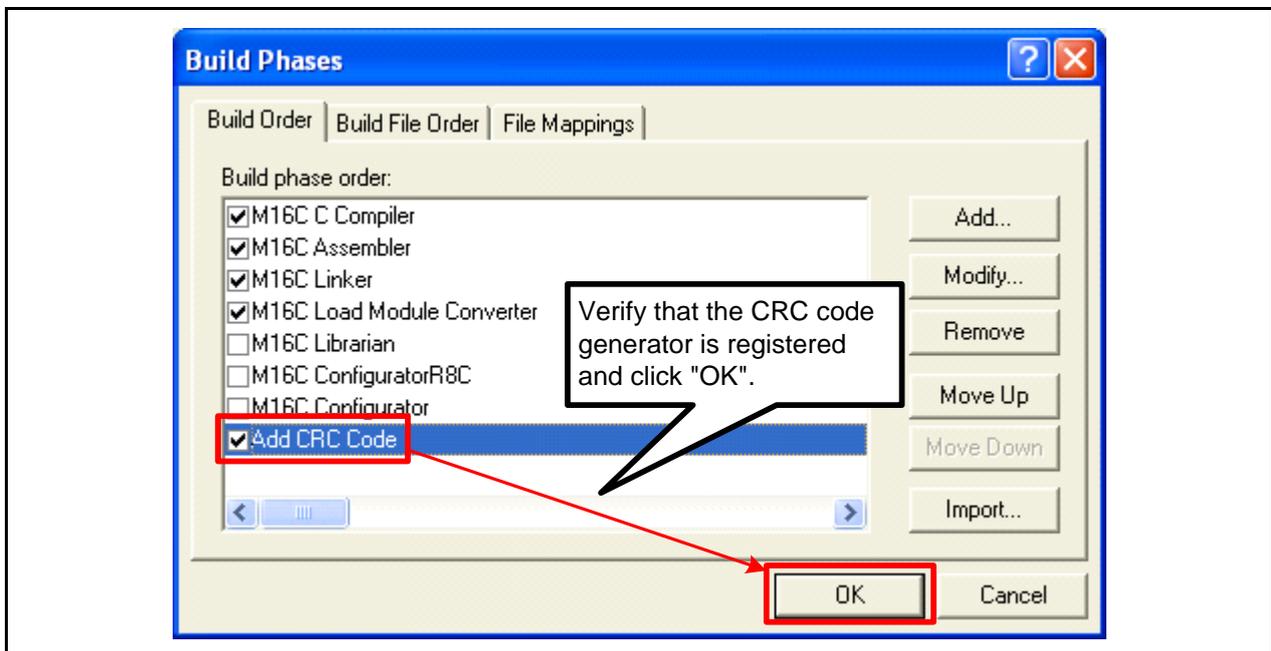


Figure 6.7 CRC Code Generator Setting (7/7)

## 6.2 CRC Code Generator Optional Settings

The CRC code generator has optional settings that can be used for creating a mot file that includes CRC code.

- (1) Select "Add CRC Code" from the "Build" menu.

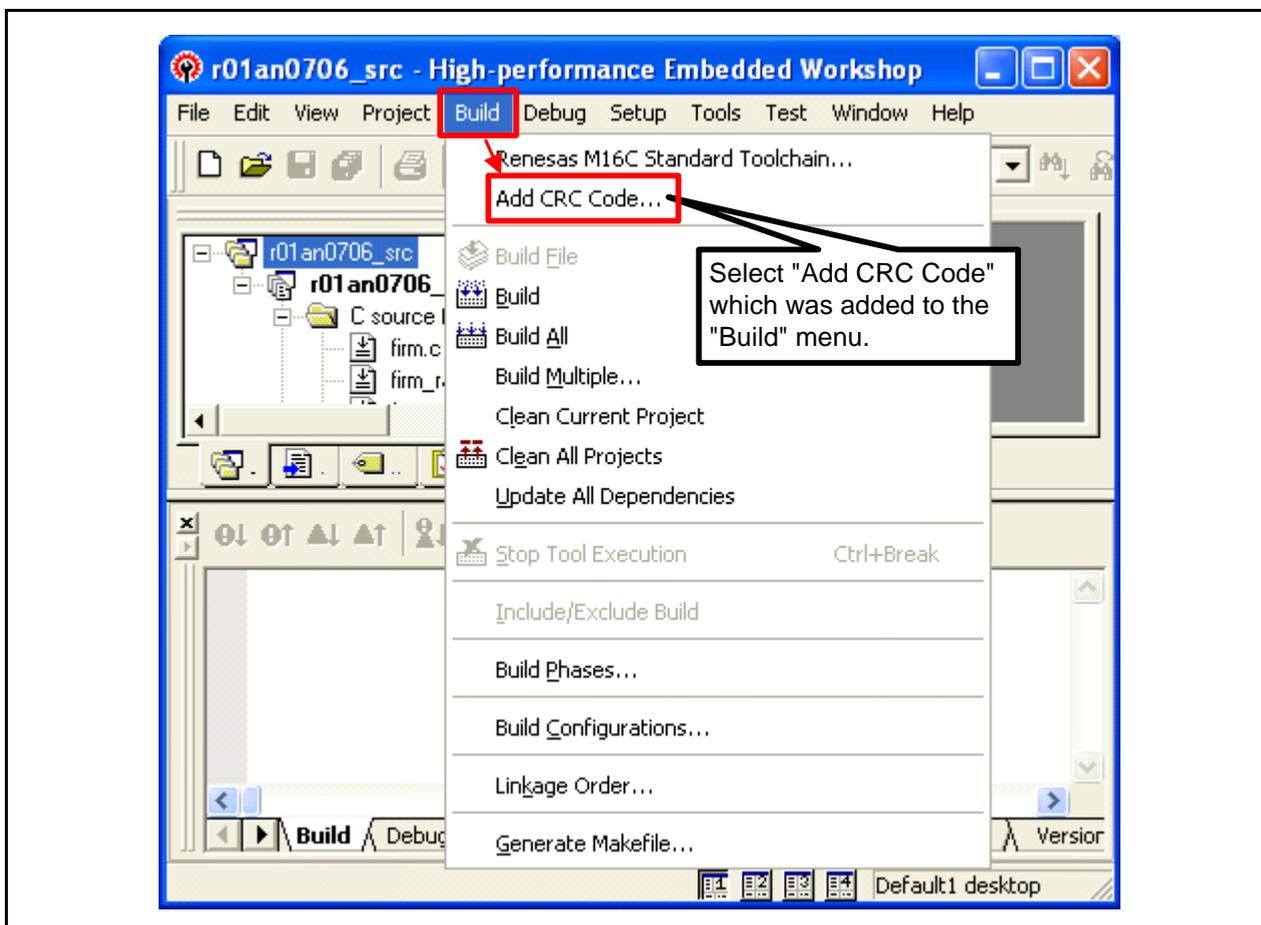


Figure 6.8 CRC Code Generator Optional Settings (1/4)

(2) Optional settings

Below are optional settings performed in this application note. For details on the optional settings, refer to the attached CRC code generator document.

- -crc=FFFE=80000-FFFFF  
CRC calculation result output: Address FFFEh  
Calculation range: Addresses 80000h to FFFFFh  
Polynomial: CRC-CCITT
- \${CONFIGDIR}\\${PROJECTNAME}.mot  
Input file: r01an0706\_src.mot
- -output=\${CONFIGDIR}\\${PROJECTNAME}\_crc.mot  
Output file: r01an0706\_src\_crc.mot
- -endian=little  
Endian: Little endian

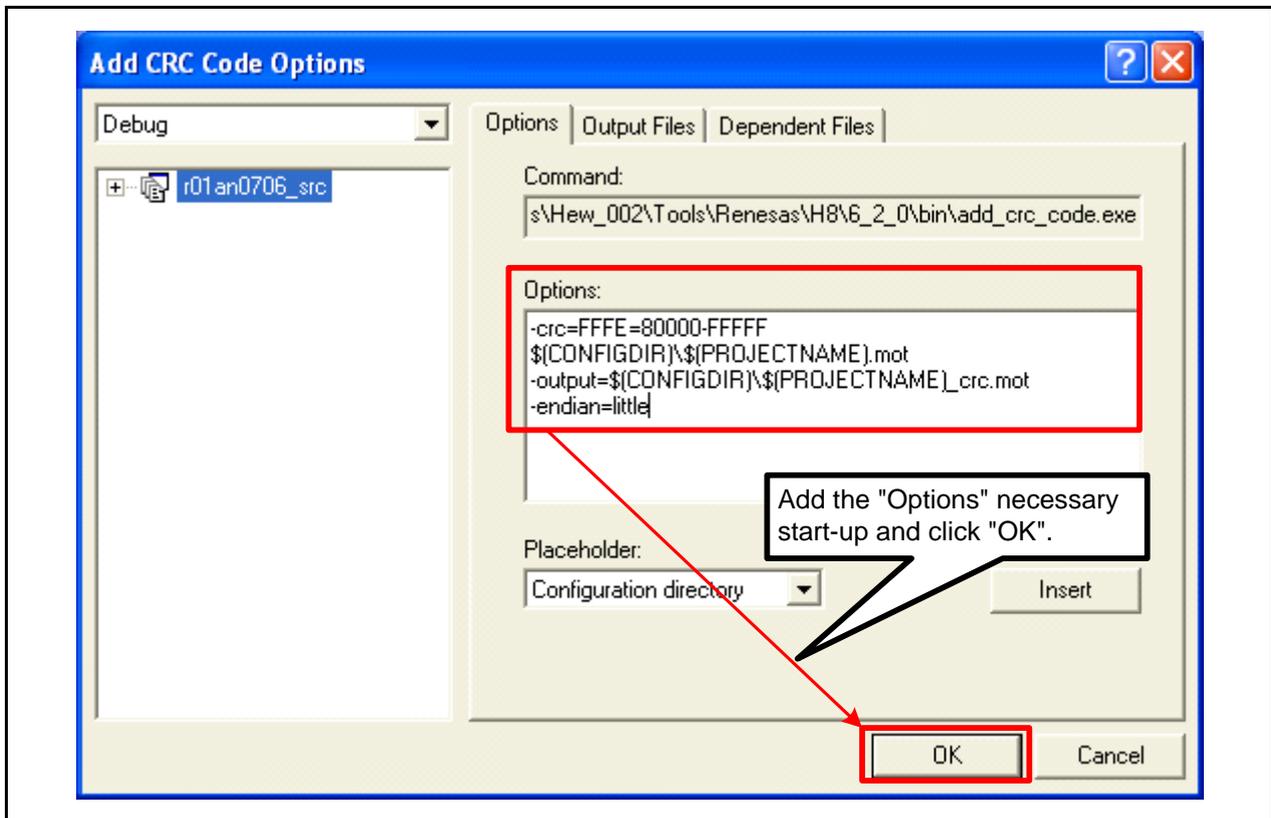


Figure 6.9 CRC Code Generator Optional Settings (2/4)

- (3) Perform a build.

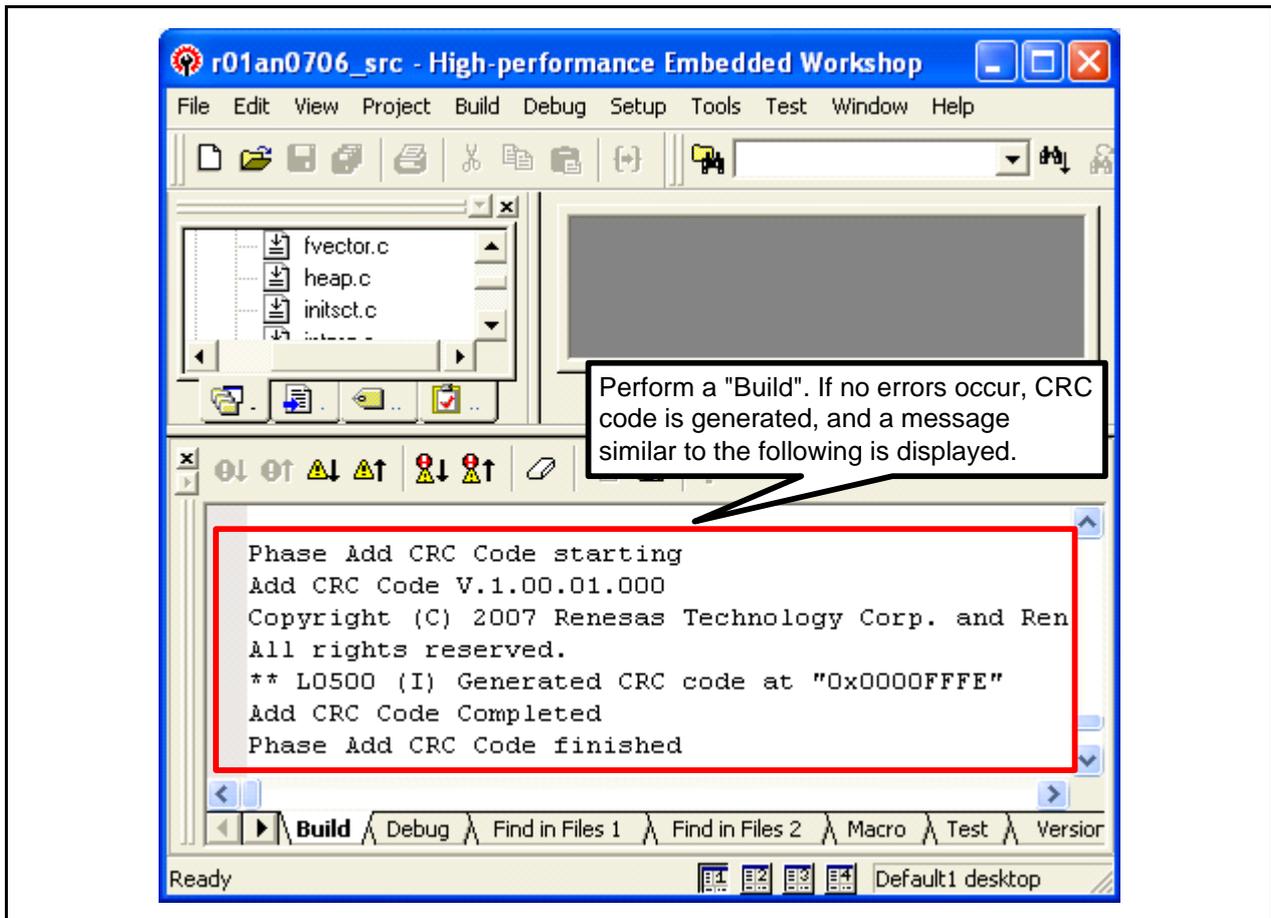


Figure 6.10 CRC Code Generator Optional Settings (3/4)

- (4) Create a mot file that includes CRC code.  
Download the generated mot file to the MCU.

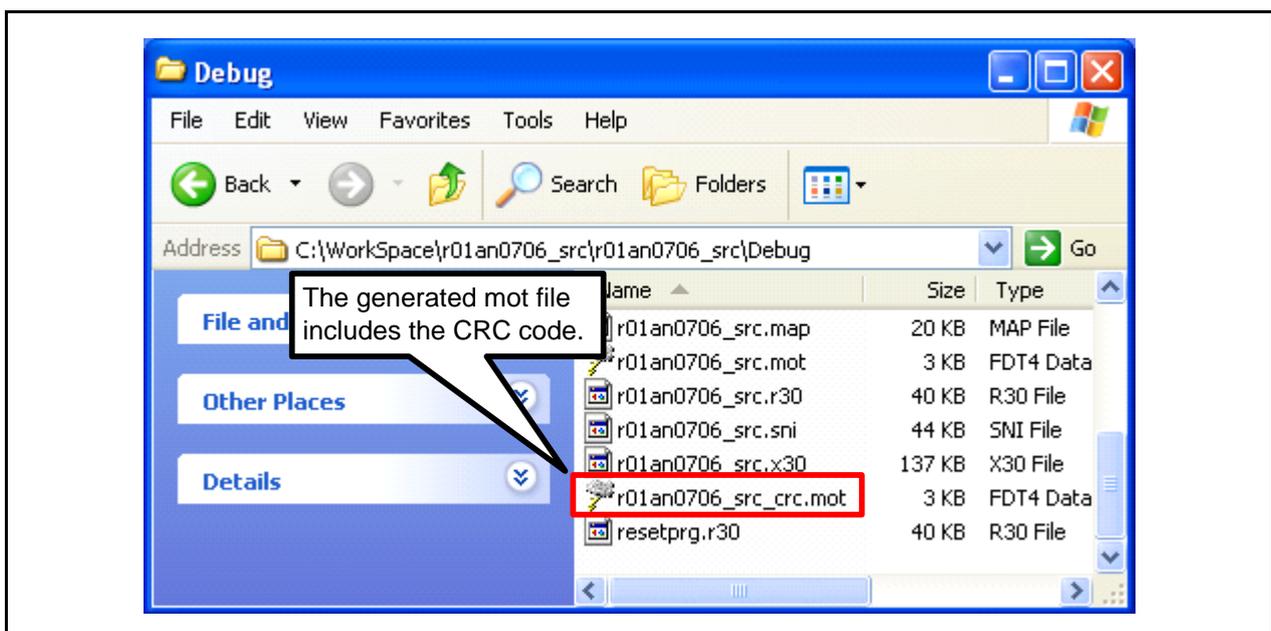


Figure 6.11 CRC Code Generator Optional Settings (4/4)

## 7. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

## 8. Reference Documents

M16C/63 Group User's Manual: Hardware Rev.2.00

M16C/64A Group User's Manual: Hardware Rev.2.00

M16C/64C Group User's Manual: Hardware Rev.1.00

M16C/65 Group User's Manual: Hardware Rev.2.00

M16C/65C Group User's Manual: Hardware Rev.1.00

M16C/6C Group User's Manual: Hardware Rev.2.00

M16C/5LD, M16C/56D Group User's Manual: Hardware Rev.1.10

M16C/5L, M16C/56 Group User's Manual: Hardware Rev.1.00

M16C/5M, M16C/57 Group User's Manual: Hardware Rev.1.01

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual

M16C Series, R8C Family C Compiler Package V.5.45

C Compiler User's Manual Rev.2.00

The latest version can be downloaded from the Renesas Electronics website.

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Revision History	M16C/63, 64A, 64C, 65, 65C, 6C, 5LD, 56D, 5L, 56, 5M, 57 Groups ROM Verification Using CRC-CCITT During Self Test on MCU Start-Up
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		Page	Summary
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## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

### 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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