
M16C/63,64A,64C,65,65C,6C,5LD,56D,5L,56,5M,57 Groups

R01AN0540EC0101

Rev.1.01

Operation of Serial I/O (Transmission in Clock-Synchronous Serial I/O Mode)Apr. 28, 2011

1. Abstract

In transmitting data in clock-synchronous serial I/O mode, choose functions from those listed in Table 3.1. Operations of the marked items are described below. The examples are explained below using the M16C/65 Group.

2. Introduction

This application note is applied to the following MCUs:

MCU(s): M16C/63, 64A, 64C, 65, 65C, 6C, 5LD, 56D, 5L, 56, 5M, 57 Groups

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above groups. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Chosen functions

Table 3.1 Chosen Functions

Item	Set-up	Item	Set-up
Clock prior to division select	✓ f1	Transfer format	✓ LSB first
	fOCO-F		MSB first
Peripheral clock	✓ f1SIO	Transmission interrupt factor	✓ Transmission buffer empty
	f2SIO		Transmission complete
Transfer clock source	✓ Internal clock (f1SIO/f2SIO/f8SIO/f32SIO)	Output transfer clock to multiple pins ⁽¹⁾	✓ Not selected
	External clock (CLKi pin)		Selected
$\overline{\text{CTS}}$ function	✓ $\overline{\text{CTS}}$ function enabled	Serial data logic	✓ No reverse
	$\overline{\text{CTS}}$ function disable		Reverse
CLK polarity	✓ Output transmission data at the falling edge of the transfer clock	Separate $\overline{\text{CTS}}$ / $\overline{\text{RTS}}$ pins ⁽²⁾	✓ Shared pin
	Output transmission data at the rising edge of the transfer clock		Separated

Notes:

1. This can be selected only when UART1 is used in combination with the internal clock.
2. This function separates $\overline{\text{CTS0}}$ / $\overline{\text{RTS0}}$, outputs $\overline{\text{RTS0}}$ from the P6_0 pin, and inputs $\overline{\text{CTS0}}$ from the P6_4 pin. When this function is selected, UART1 $\overline{\text{CTS}}$ / $\overline{\text{RTS}}$ function can not be utilized. Set the UART1 $\overline{\text{CTS}}$ / $\overline{\text{RTS}}$ disable bit to "1".

4. Operation

- (1) Setting the transmit enable bit to "1" and writing transmission data to the UARTi transmit buffer register makes data transmissible status ready.
- (2) When input to the $\overline{\text{CTS}}_i$ pin goes to "L" level, transmission starts (the $\overline{\text{CTS}}_i$ pin must be controlled on the reception side).
- (3) In synchronization with the first falling edge of the transfer clock, transmission data held in the UARTi transmit buffer register is transmitted to the UARTi transmit register. At this time, the UARTi transmit interrupt request bit goes to "1". Also, the first bit of the transmission data is transmitted from the TxDi pin. Then the data is transmitted bit by bit from the lower order in synchronization with the falling edges.
- (4) When transmission of 1-byte data is completed, the transmit register empty flag goes to "1", which indicates that transmission is completed. The transfer clock stops at "H" level.
- (5) If the next transmission data is set in the UARTi transmit buffer register while transmission is in progress (before the eighth bit has been transmitted), the data is transmitted in succession.

Figure 4.1 shows the operation timing.

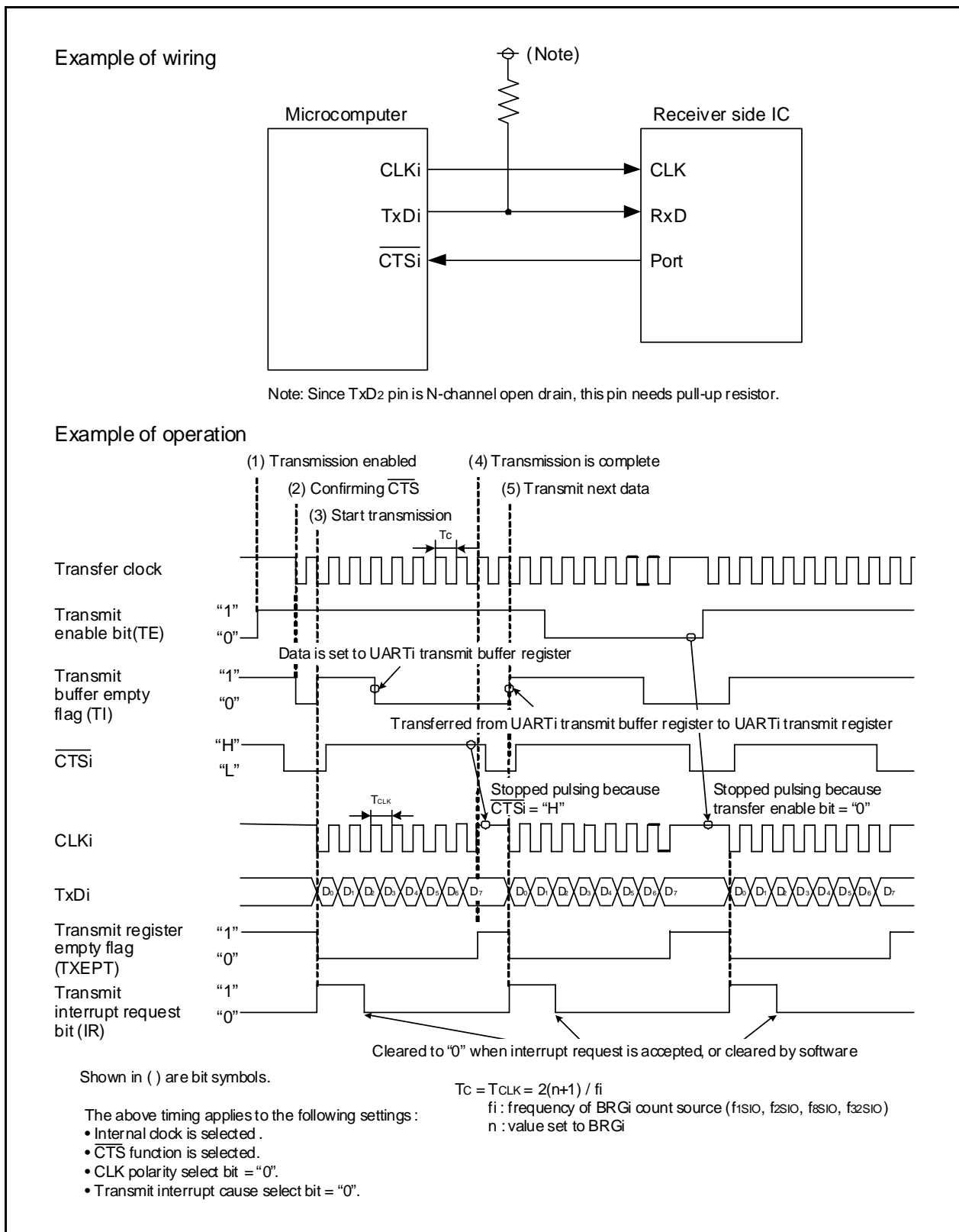
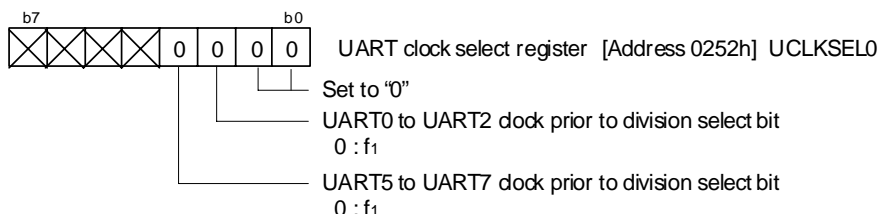


Figure 4.1 Operation Timing of Transmission in Clock-Synchronous Serial I/O Mode

5. Set-up Procedure

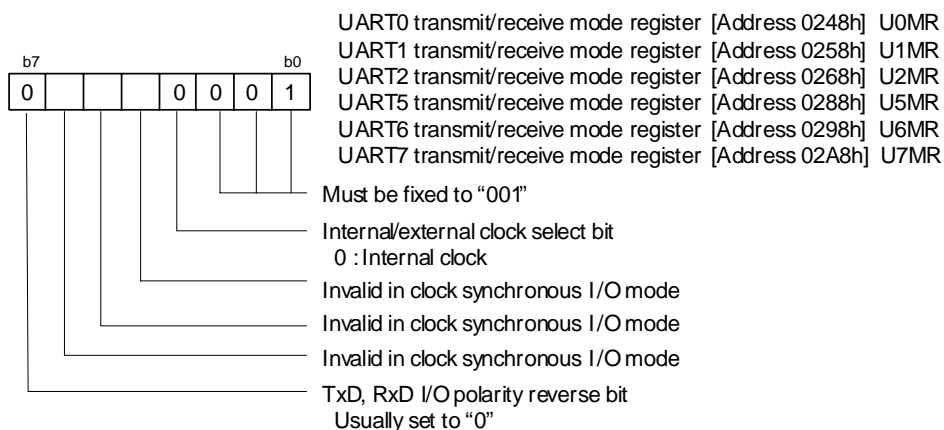
Setting UART clock select register

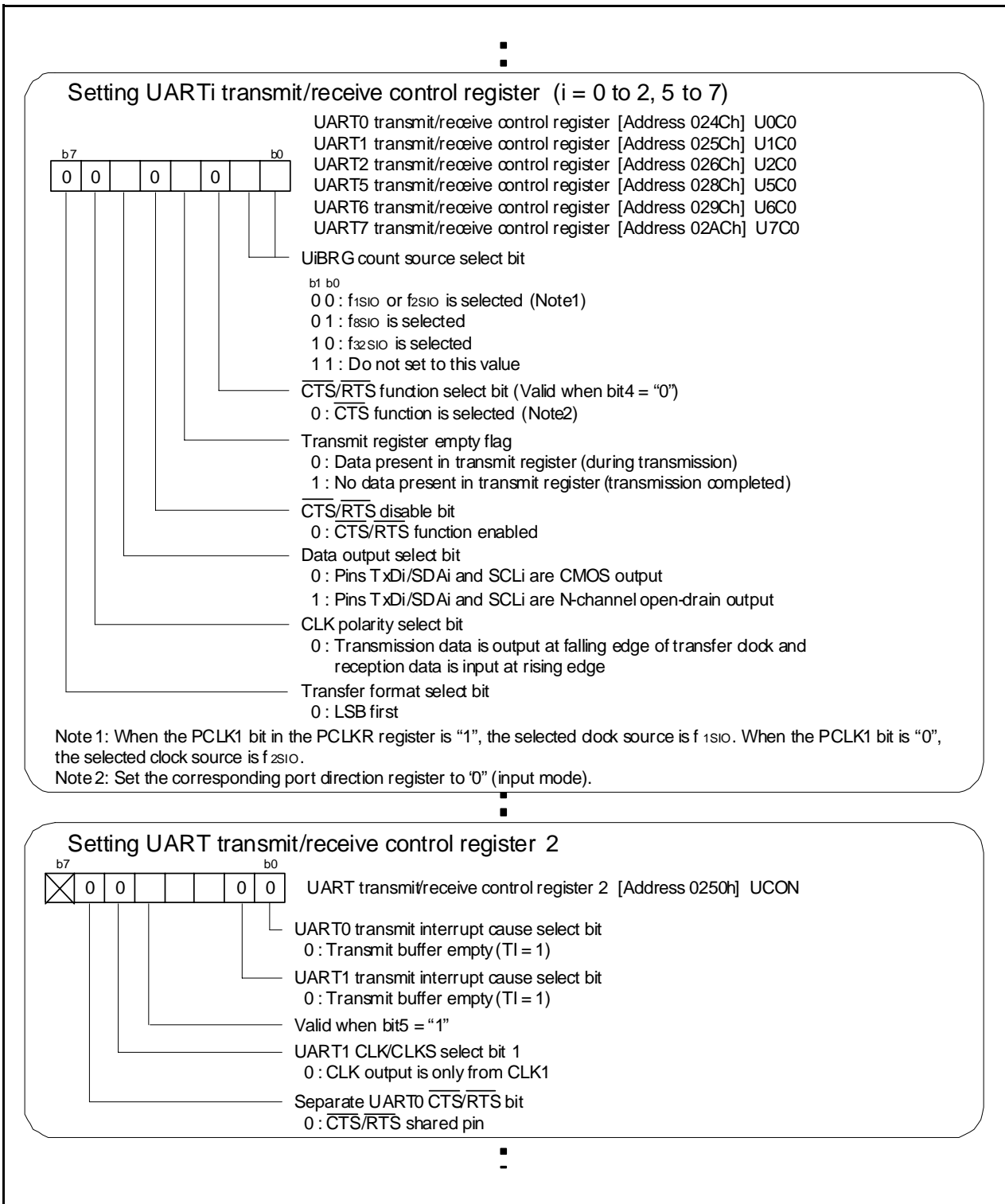
(Set the OCOSEL0 or OCOSEL1 bit before setting other registers associated with UART0 to UART2 and UART5 to UART7. After changing the OCOSEL0 or OCOSEL1 bit, set other registers associated with UART0 to UART2 and UART5 to UART7 again.)

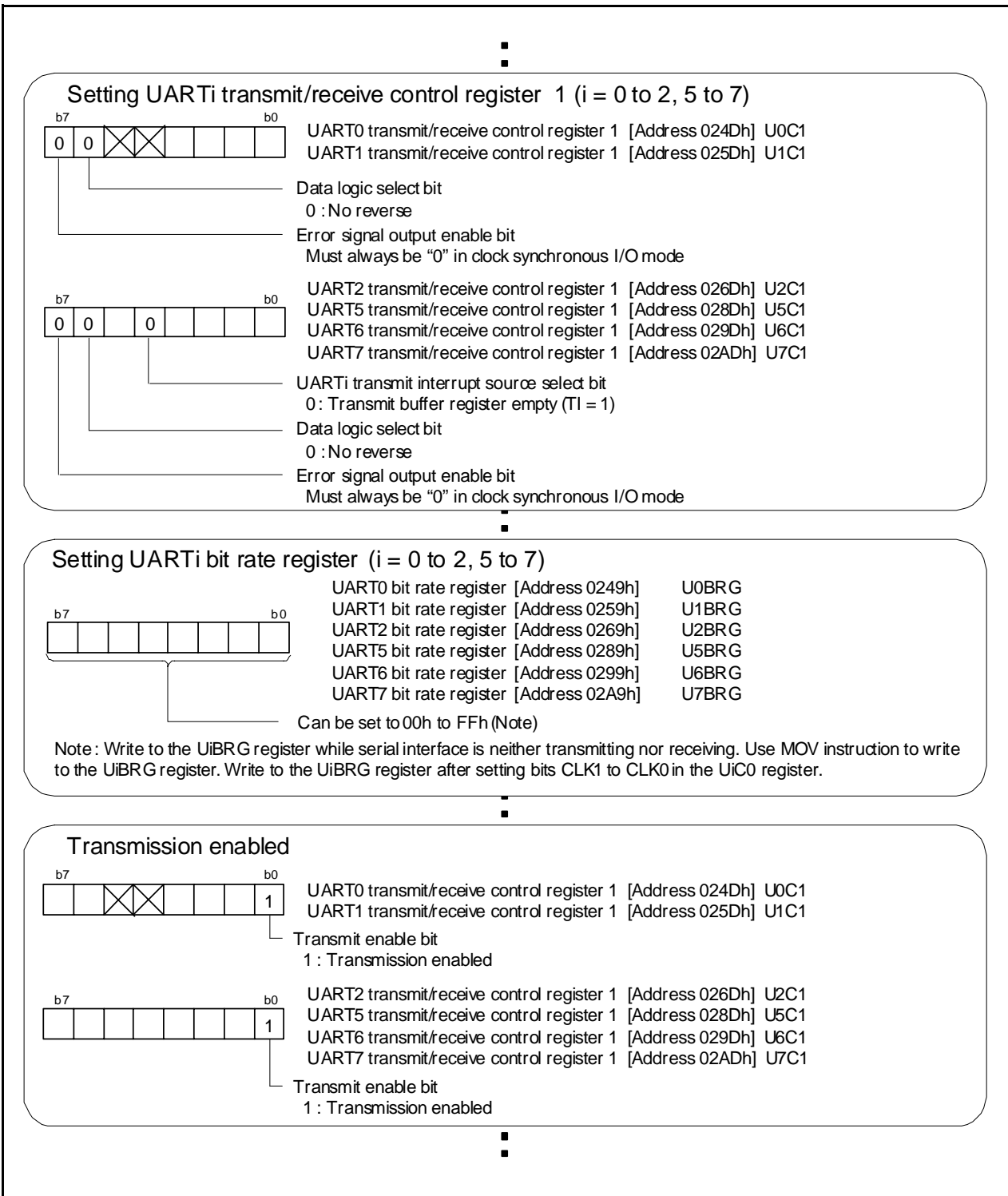


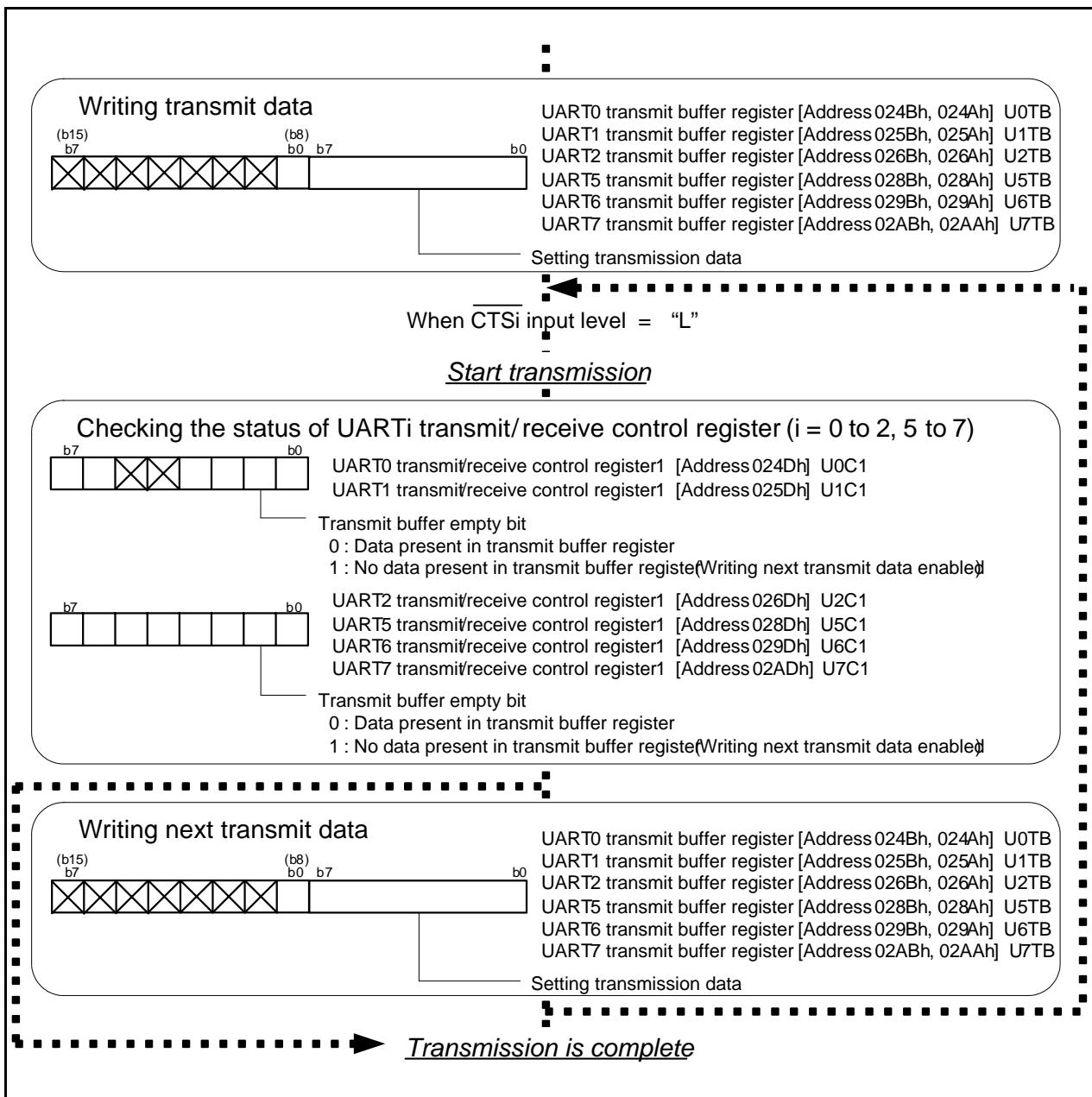
Note: Set bits OCOSEL0 and OCOSEL1 while transmission/reception of UART0 to UART2 and UART5 to UART7 stops.

Setting UART_i transmit/receive mode register (i = 0 to 2, 5 to 7)









6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

M16C/63 Group User's Manual: Hardware Rev.2.00
M16C/64A Group User's Manual: Hardware Rev.2.00
M16C/64C Group User's Manual: Hardware Rev.1.00
M16C/65 Group User's Manual: Hardware Rev.2.00
M16C/65C Group User's Manual: Hardware Rev.1.00
M16C/6C Group User's Manual: Hardware Rev.2.00
M16C/5LD Group, M16C/56D Group User's Manual: Hardware Rev.1.10
M16C/5L Group, M16C/56 Group User's Manual: Hardware Rev.1.00
M16C/5M Group, M16C/57 Group User's Manual: Hardware Rev.1.01
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual

M16C Series, R8C Family C Compiler Package V.5.45

C Compiler User's Manual Rev.2.00

The latest version can be downloaded from the Renesas Electronics website.

8. Website and Support

Renesas Electronics website

<http://www.renesas.com/>

Inquiries

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Revision History	M16C/63,64A,64C,65,65C,6C,5LD,56D,5L,56,5M,57 Groups Operation of Serial I/O (Transmission in Clock-Synchronous Serial I/O Mode)
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Rev.	Date	Description	
		Page	Summary
1.00	Sep. 27, 2009	—	First edition issued
1.01	Apr. 28, 2011	—	Add: M16C/63, M16C/64A, M16C/64C, M16C/65C, M16C/6C, M16C/5LD, M16C/56D, M16C/5L, M16C/56, M16C/5M, and M16C/57

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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