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RENESAS

M32C/83, M32C/85 Groups

Intelligent I/O - Stepping Motor Control Function

1. Abstract

This application note describes the stepping motor control that uses waveform generating function of M32C/83 group's intelligent I/O group 2 and M32C/85 group's intelligent I/O.

2. Introduction

This application note is applied to the following condition:
Applicable MCU: M32C/83 Group, M32C/85 Group

The program on this application note can also be used when operating other microcomputers within the M16C Family, provided they have the same SFRs (Special Function Registers) as the M32C/83 and M32C/85 groups. However, some functions may have been modified. Refer to each device's hardware manual for details. Use functions covered in this application note only after careful evaluation.

3. Detailed Description

3.1 Control of Stepping Motors

A stepping motor is a type of electro magnetic motor which rotates in set steps decided by inputting pulses. It does not rotate as DC motor just by connecting to a power source. Figure 1 illustrates the cross section of a 2-phase unipolar stepping motor.

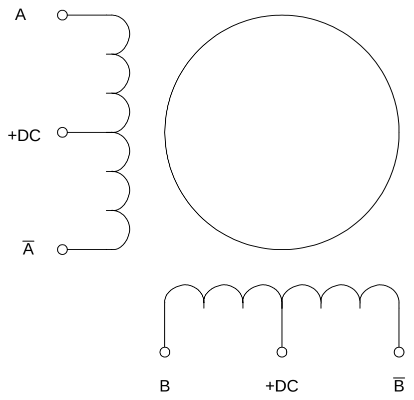


Figure 1. Unipolar Stepping Motor

Energizing each winding, A, $\overline{A}$, B, and $\overline{B}$ in set sequence will spin a stepping motor. There are several methods to energize windings.

3.2 Excitation System

3.2.1 One Phase excitation

This system will constantly allow a stepping motor to energize one phase. A stepping motor with one phase excitation results in jerky movements of the motor because of the low output torque and less dumping effect although one phase excitation stepping motor requires little power consumption to operate.

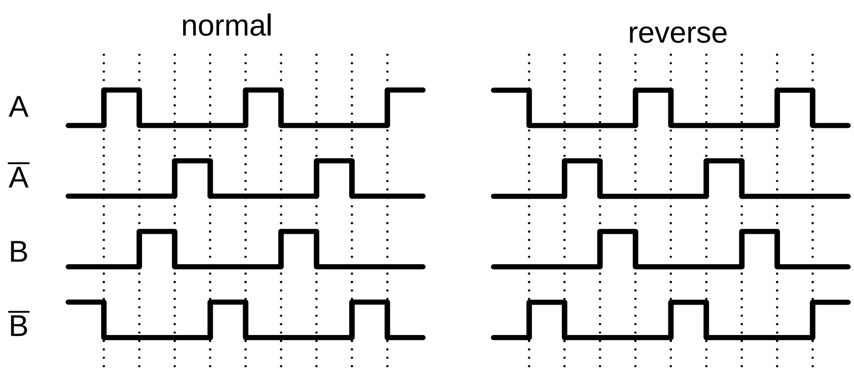


Figure 2. One Phase Excitation

3.2.2 Two-phase Excitation

This system will constantly allow a stepping motor to energize two phases. A stepping motor with two phase excitation is more commonly used because output torque is higher and dumping effect is bigger than that of a motor with one phase excitation. However, it requires power consumption twice as much as one phase excitation stepping motor.

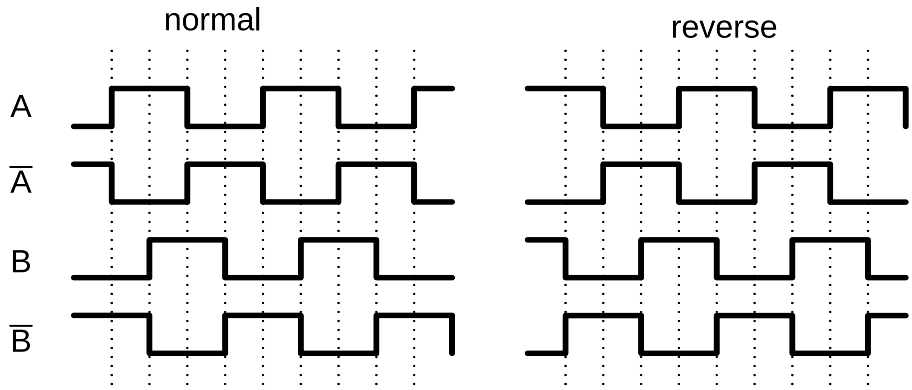


Figure 3. Two Phase Excitation

3.2.3 One-Two Phase Excitation

By combining one phase excitation and two phase excitation, this system allow a stepping motor to rotate one half of a full step angle for one excitation. The system is known as a half step drive. This drive mode improves system performance by diminishing dumping effect and resonances.

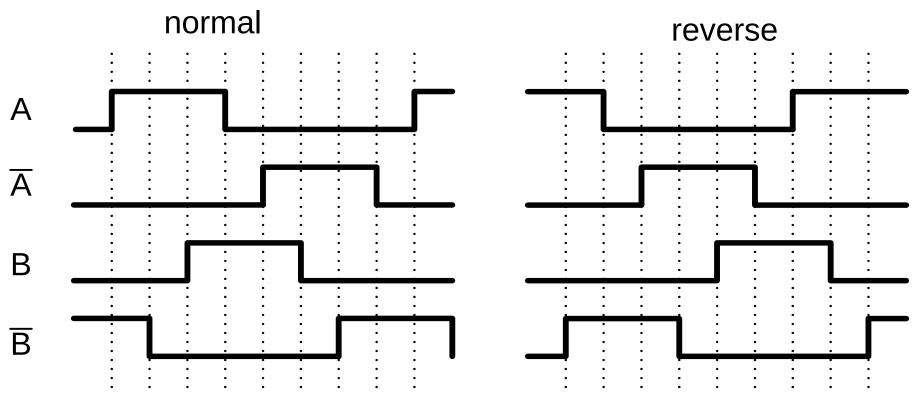


Figure 4. One-Two Phase Excitation

3.3 Microstepping Control

Microstepping reduces the bumpy movements of stepping motor operation, especially at lower speed. It can smooth the transitions between steps, comparing to standard rectangular wave control.

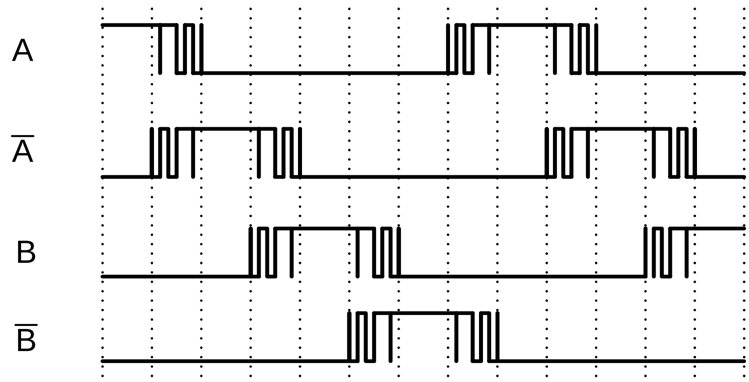


Figure 5. Microstepping Control (one-two excitation))

3.4 Waveform Generation Function

Stepping motor microstepping function of intelligent I/O is described in this application note. Figure 6 shows an example of a stepping motor connection with M32C/83. The intelligent I/O group 2 is used for the example. 3.5 Microstepping Control Setting shows register settings in group 2.

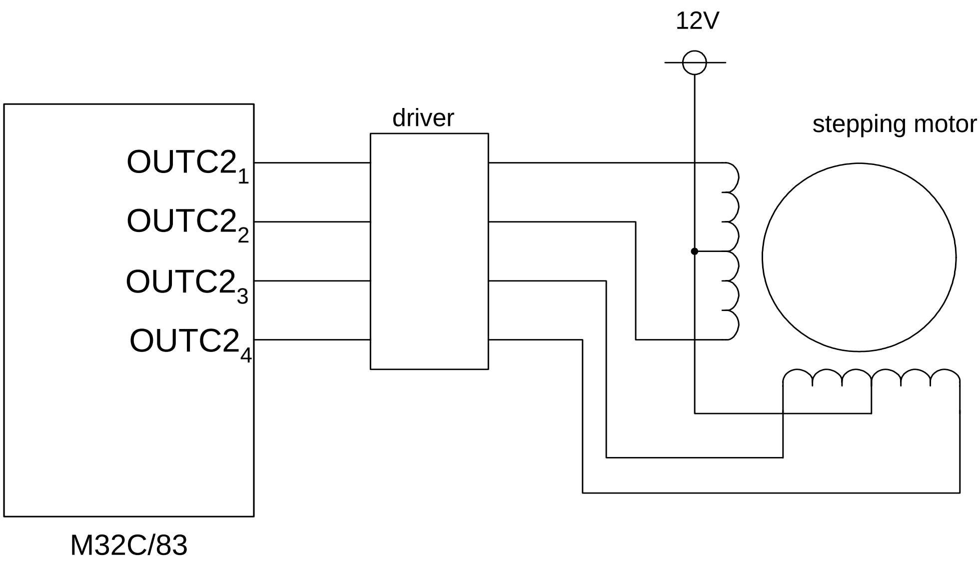


Figure 6. M32C/83 with Stepping Motor

3.4.1 Carrier Frequency

Carrier frequency is the fundamental frequency used in pulse-width modulation (PWM). The PWM duty cycle modulates based on the carrier frequency.

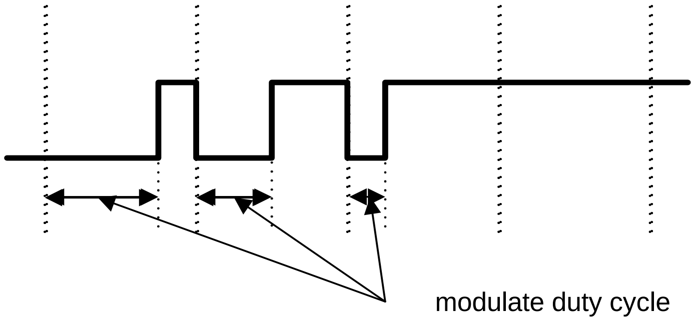


Figure 7. Carrier Frequency

Interrupt request is generated by the group 2 base timer reset. Set the G2POi (i=0 to 7) register to decide the low ("L") width of PWM output pulse. The group 2 base timer is reset by matching with the value of the G2PO0 register.

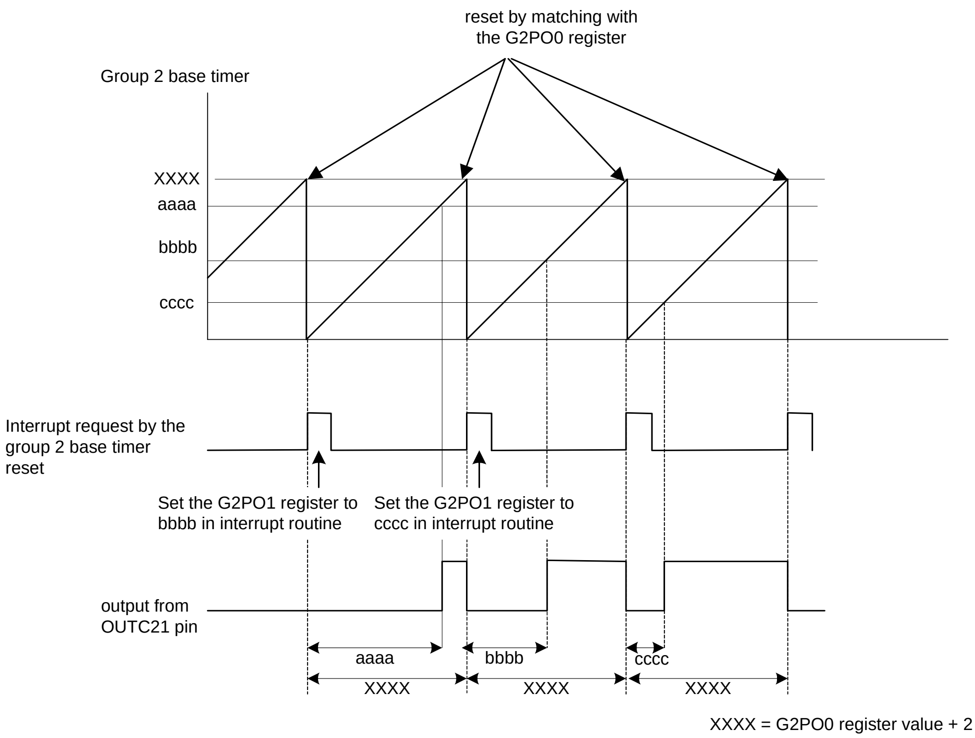


Figure 8. PWM Output Timing

3.4.2 Duty Cycle

Duty cycle of PWM is calculated by laying the PWM waveform to a sin waveform as shown in Figure 9. When a value of sin θ is negative, low-level (“L”) signal is output. When the value is positive and more than a specific value, high-level (“H”) signal is output.

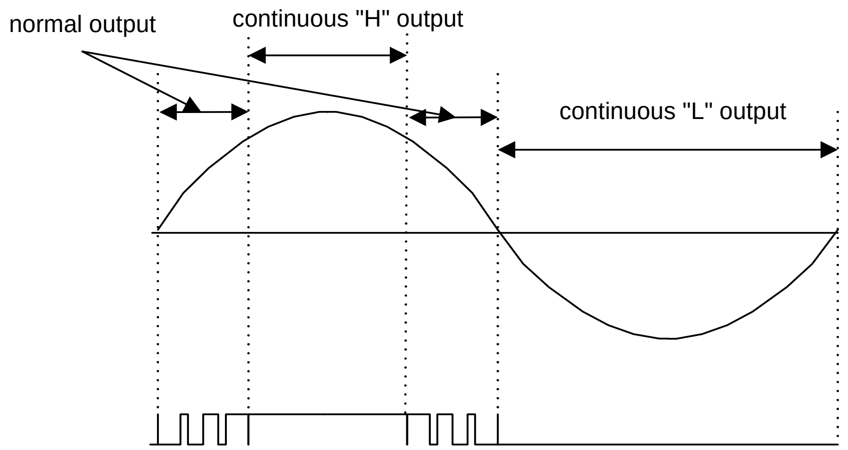


Figure 9. Sin Waveform and PWM Output

Following equations are to calculate the setting value to the G2POj (j=0 to 7) register.
Normal output time
G2POj register setting value = PWM cycle(s) – PWM cycle(s) × sinN°
Continuous “H” output time
G2POj register = 0
Continuous “L” output time
G2POj register = PWM cycle(s) + 1
The G2POj register setting value causes to output the waveforms shown in Figure 9.

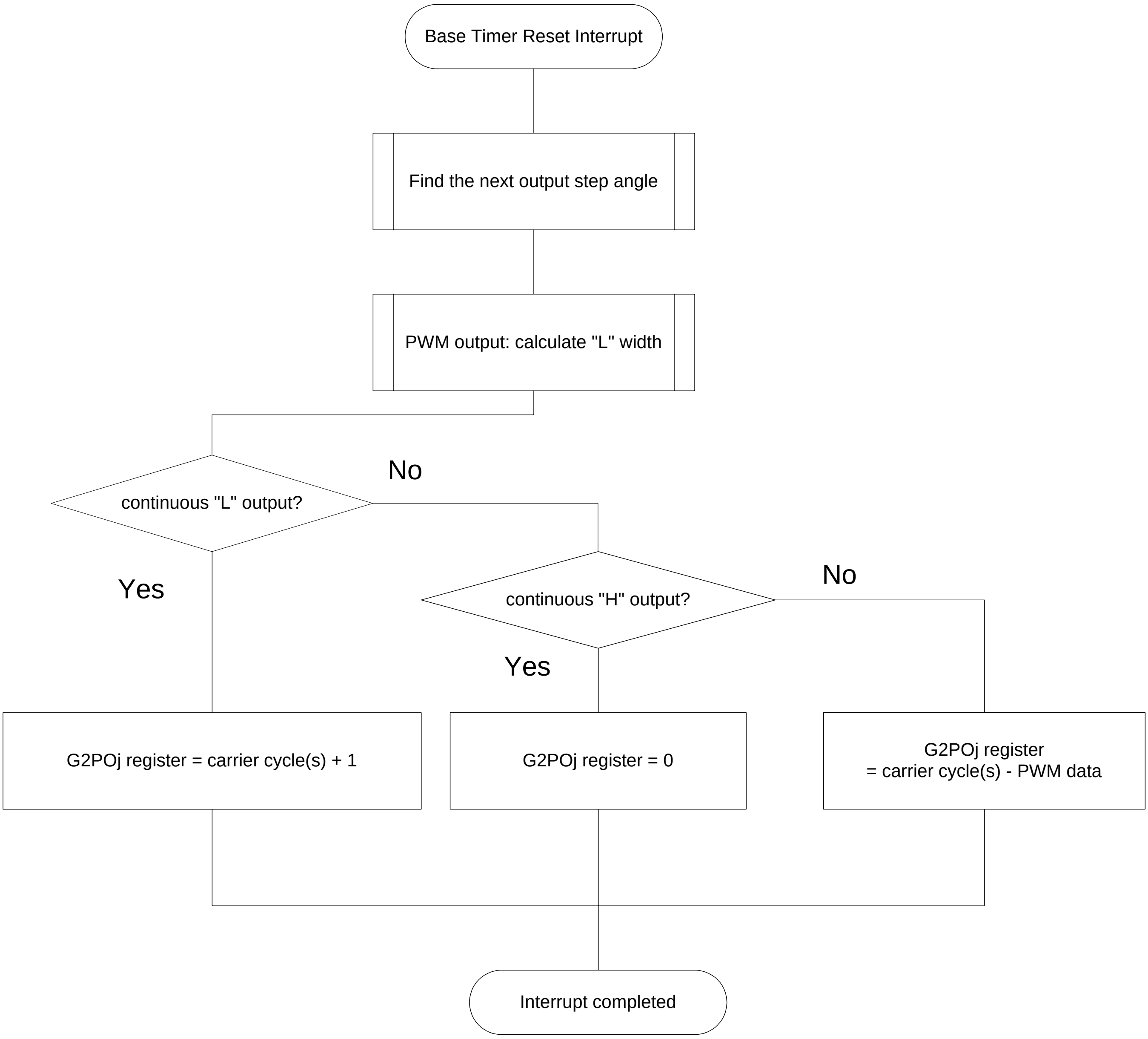


Figure 10. Example of Base Timer Reload Interrupt

3.4.3 Stepping Motor Speed

Figure 11 shows changes of stepping motor speed at the fixed carrier frequency. In the example, the motor speed can accelerate by increasing the numbers of each pulse group which has different duty rates and decelerate by decreasing the numbers.

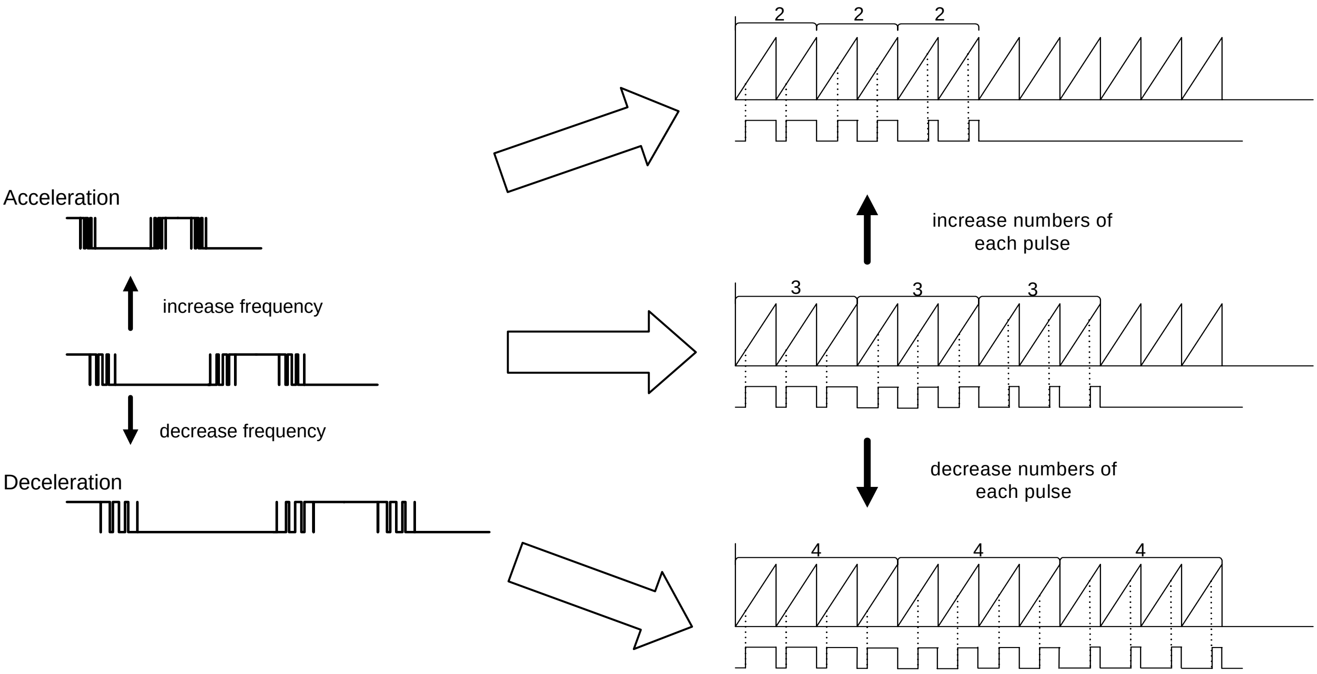


Figure 11. Changes of Stepping Motor Speed

3.4.4 Control of Rotation Direction

The rotation direction of stepping motor can be controlled by changing the reference direction of sin value table shown in Figure 12. Figure 12 uses 48 degree as a turning point of the rotation.

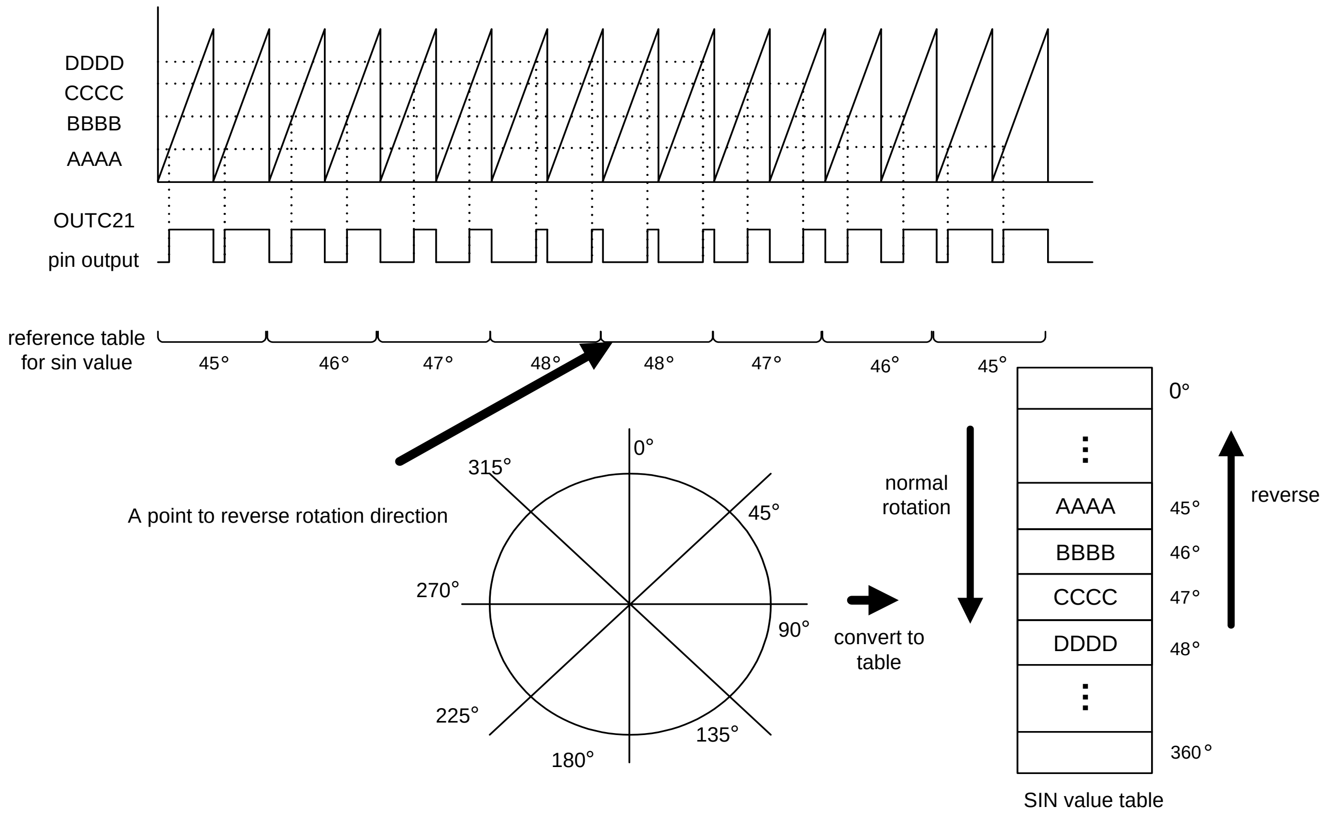


Figure 12. Control of Rotation Direction

3.5 Setting Procedure

The initial setting procedure and setting values are described as follows to perform 3.4 Waveform Generation Function. Refer to M32C/83 group hardware manual for details on each register.

1) Interrupt Disabled
Set the I flag to "0" or set the ILV2 to 0 bits in the IIOkIC register (k=0 to 11) to "000b" in order to disable the interrpt request from intelligent I/O.

2) G2BCR0 Register

b7							b0
0	1	1	1	1	1	1	1

BCK1 and 0: count source select bit
-f1

DIV4 to 0: count source divide ratio select bit
-no division

Nothing is assigned. Set to "0".

Clock is supplied to the BTSR register to enable the BTSR register setting.

3) BTSR Register

b7							b0
0	0	0	0	0	0	0	0

BT3S to BT0S: base timer start bit
-reset group i base timer (i=0 to 3)

Nothing is assigned. Set to "0000b".

Group i base timer (i=0 to 3) is reset. After setting the base timer operation clock with the GiBCR0 register, set the BTS bit in the GiBCR1 register to "1" for the group i base timer to start counting from "0000h".

4) G2BCR0 Register

b7							b0
0	0	0	0	0	0	0	0

BCK1 and 0: count source select bit
-clock stopped

Nothing is assigned. Set to "000000b".

Stop supplying clocks to the group 2 base timer when the timer and the BTSR register are not used.

5) G2BCR0 Register

b7							b0
0	1	1	1	1	1	1	1

BCK1 and 0: count source select bit
-f1

DIV4 to 0: count source divide ratio select bit
-no division

Nothing is assigned. Set to "0".

Supply to each register shown in procedures 6) to 13) and 20). To enable each register setting as soon as they are set, set the G2BCR0 register to "011111111b".

6) G2BCR1 Register

b7							b0
0	0	0	0	0	0	1	0

- Nothing is assigned. Set to "0".
- RST1: base timer reset cause select bit 1
  - reset the base timer by matching the value set in the G2PO0 register
- Nothing is assigned. Set to "0".
- Reserved bit. Set to "0".
- BTS: base timer start bit
  - base timer reset
- Reserved bit. Set to "00b".
- Nothing is assigned. Set to "0".

After the registers associated with the group 2 intelligent I/O are set, set the BTS bit to "1" (base timer start counting).

7) G2POCR0 Register

b7							b0
0	0	0	0	0	0	0	0

- MOD2 to 0: operation mode select bit
  - Single waveform output mode
- Nothing is assigned. Set to "00b".
- RLD: GiPO0 to 7 register reload timing select bit
  - Reload when value is written.
- Nothing is assigned. Set to "00b".

The GiPO0 register setting is enabled as soon as it is set. When setting the GiPO0 register at initial setting, set the RLD bit to "0".

8) G2PO0 Register

b15	b0
16 bits	

Set the carrier cycle at start-up. If setting value is n,

$$\text{PWM cycle} = \frac{\text{divide ratio}}{\text{f1}} \times (n+2)$$

9) G2POCR0 Register

b7							b0
0	0	1	0	0	0	0	0

MOD2 to 0: operating mode select bit
- Single waveform output mode

Nothing is assigned. Set to "00b".

RLD: GiPOj(j=0 to 7) register value reload timing select bit
- Reload the GiPOj register when base timer is reset

Nothing is assigned. Set to "00b".

After setting the RLD bit to "1", change the reload timing of GiPO0 and GiPOj registers when the base timer is reset.

10) G2POCR1 to 4 Registers

b7							b0
0	0	0	0	0	0	0	0

MOD2 to 0: operation mode select bit
- Single waveform output mode

Nothing is assigned. Set to "0".

IVL: Output initial value select bit
- Output "0" as default value

RLD: GiPOj register reload timing select bit
- Reload the GiPOj register when value is written

Nothing is assigned. Set to "00b".

The setting of GiPO0 register is enabled as soon as it is set. When setting the GiPO0 register at initial setting, set the RLD bit to "0".

11) G2PO1 to 4 Registers

b15	b0
16 bits	

The G2PO1 to 4 registers decide the "L" width of four PWM waveforms to control a stepping motor at start-up. Set these registers to more than the G2PO0 register value so that the output level of all PWMs is fixed to "L" as a default.

12) G2POCR1 to 4 Registers

b7							b0
0	0	1	0	0	0	0	0

MOD2 to 0: operation mode select bit
- Single waveform output mode

Nothing is assigned. Set to "00b".

RLD: GiPOj register value reload timing select bit
- Reload the GiPOj registers when the base timer is reset.

Nothing is assigned. Set to "00b".

After setting the RLD bit to "1", change the reload timing of G2PO1 to G2PO4 registers when the base timer is reset.

13) G2FE Register

b7							b0
0	0	0	1	1	1	1	1

IFE4 to 0: channel 4 to 0 function enable bit
- enable functions for channel 4 to 0

IFE7 to 5: channel 7 to 5 function enable bit
- When using channel j, set the IFEj bit to "1" (enable functions for channel j)

Set the IFEj bit of unused channel j to "0".

14) IIO6IE Register

b7							b0
0	0	0	0	0	0	0	1

IRLT: interrupt request select bit
- operate channel 0 function

bit7 to 1: interrupt enable bit 7 to 1
- Set to "0000000b".

Do not set the IRLT bit and bit 7 to 1 to "1" simultaneously.

15) IIO6IR Register

b7							b0
0	0	0	0	0	0	0	0

Nothing is assigned. Set to "0".

Initialize the interrupt request register

Set the IIO6IR register to "00h".

16) IIO6IE Register

b7							b0
0	0	0	0	0	1	0	1

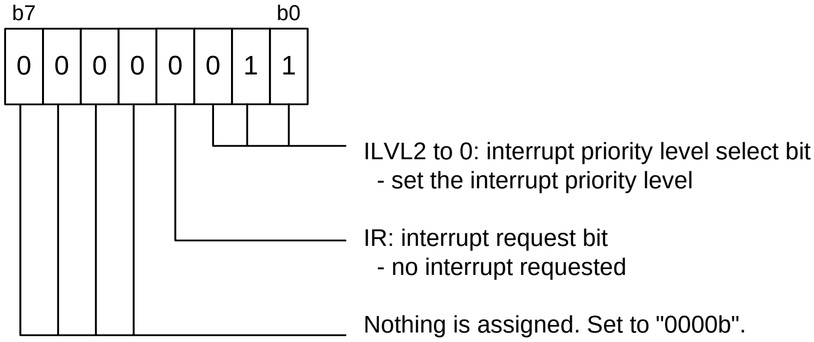
IRLT: Interrupt request select bit
- enable functions for channel 0

bit2: interrupt enable bit 2
- Set the PO20 bit to "1".

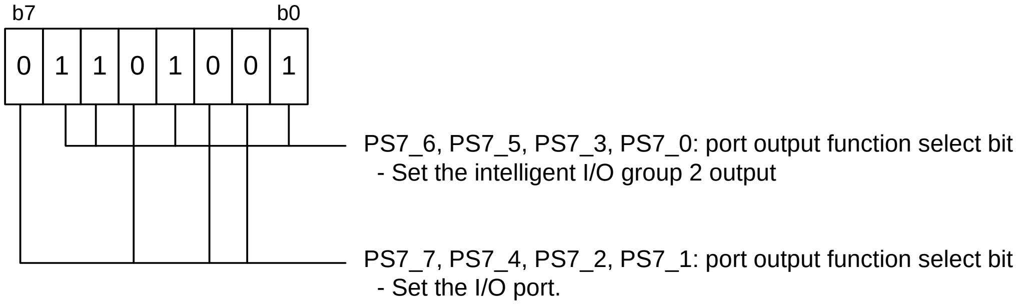
bit7 to 3, 1: interrupt enable bit 7 to 3, 1
- Nothing is assigned. Set to "0".

Set the interrupt request bit of unused interrupt to "0".

17) IIO6IC Register

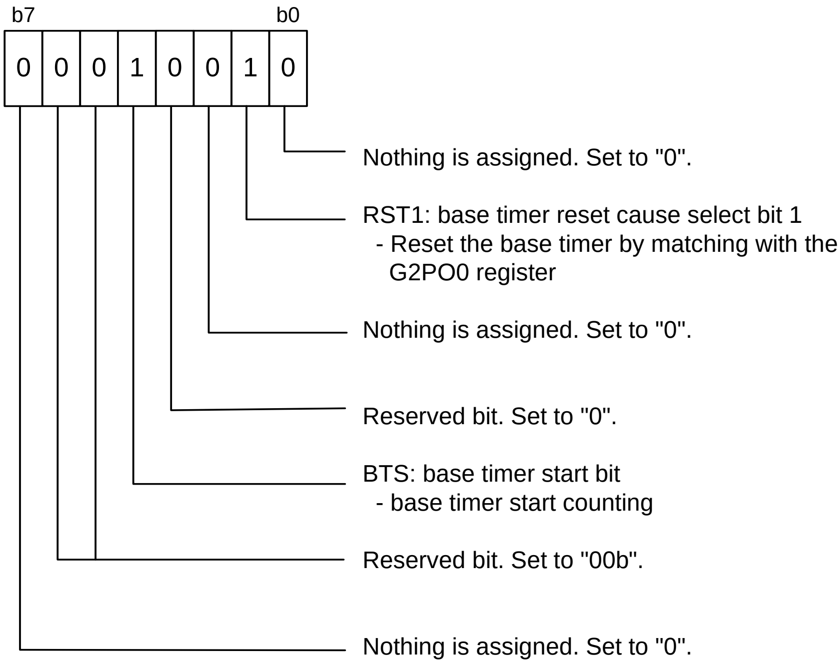


18) Function Select Register A7



19) Interrupt enable (I flag = "1")

20) G2BCR1 Register



4. Sample Program

The following is an application program for microstepping control of stepping motor. This application program is a sample, therefore, it needs to be changed or modified for an individual user's application.
Figure 14 shows an output result of sample program.

OUTC21

OUTC22

OUTC23

OUTC24

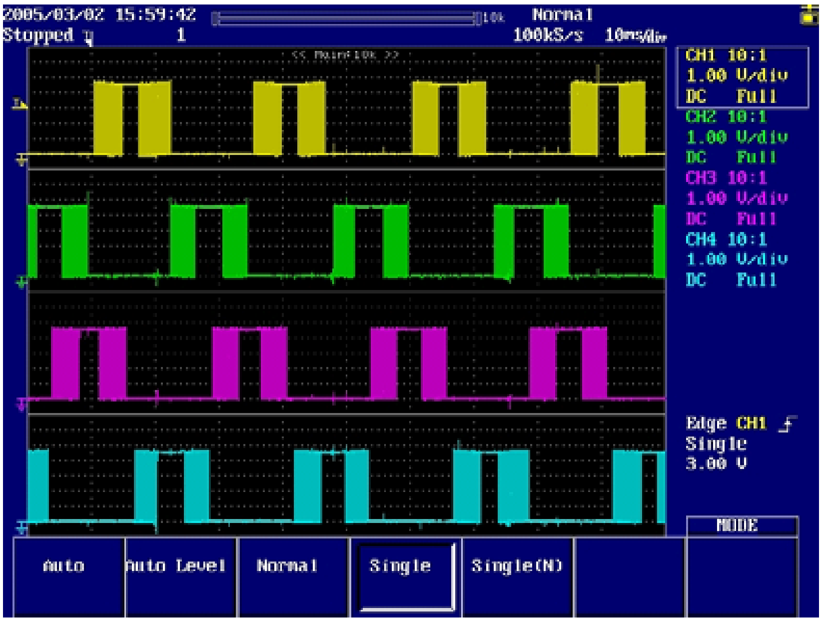


Figure 14. Oscilloscope Measurement

Main clock: 30 MHz
Carrier frequency: 20 KHz
Rotation speed: 40 PPS

5. Reference Program

Please find the reference program from the Renesas Technology Web site.
Click Application Note in the left menu of the M32C/80 Series top page.

6. Reference Documents

Hardware manual
M32C/83 Group Hardware Manual
M32C/85 Group Hardware Manual
(Use the most recent version of the document on the Renesas Technology Web site.)

Technical news/Technical update
(Use the most recent version of the document on the Renesas Technology Web site.)

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