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H8/300H Super Low Power Series

Hints on the Use of TPU PWM Mode

Introduction

This document describes the notes and hints on the use of the PWM mode of the on-chip 16-bit timer pulse unit (TPU).

Contents

1. Notes and Hints on the Use of PWM Mode

1.1 Setting the Module Standby Function

The TPUCKSTP bit of the clock stop register 2 (CKSTPR2) can be used to enable or disable the TPU. The TPU is enabled by default. When the module standby mode is canceled, the register can be accessed. Table 1 shows the function assignment of the TPUCKSTP bit of the clock stop register 2 (CKSTPR2).

Table 1 Clock Stop Register 2 (CKSTPR2)

Bit	Bit Name	Initial Value	R/W	Description
6	TPUCKSTP	1	R/W	TPU module standby Enables or disables the TPU's module standby function. 0: Sets the TPU in the module standby state. 1: Cancels the TPU from the module standby state.

1.2 Restrictions on the Input Clock

The pulse width of the input clock needs to be 1.5 states or longer for single edge and 2.5 states or longer for double-edge. The unit will not operate properly on narrower pulse width.

1.3 Notes on Setting the Period

When counter clearing on compare match is set, TCNT is cleared in the last state in which it matches the TGR value (the point at wich the count value matched by TCNT is updated). Accordingly, the actual frequency of the counter is expressed as follows:

$f = \phi / (N + 1)$

f: Counter frequency

ϕ: Operating frequency

N: Value preset in TGR

1.4 Contention between TCNT Write and Counter Clearing

If a counter clear signal occurs in the T2 state of a TCNT write cycle, the clearing of the TCNT takes priority and the write to the TCNT is not performed.

Figure 1 shows a timing example of a contention between TCNT write and counter clearing.

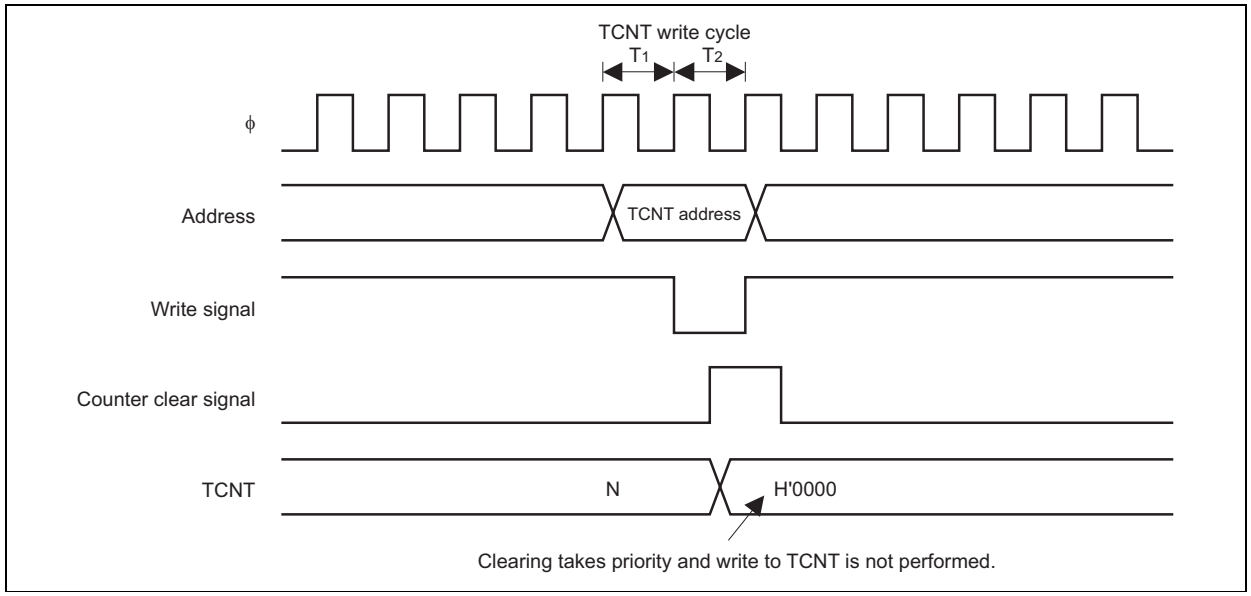


Figure 1 Contention between TCNT Write and Counter Clearing

1.5 Contention between TCNT Write and Counting up

Even when a counting up condition occurs in the T2 state of a TCNT write cycle, the write to TCNT takes priority and the counter is not performed.

Figure 2 shows a timing example of a contention between TCNT write and counting up.

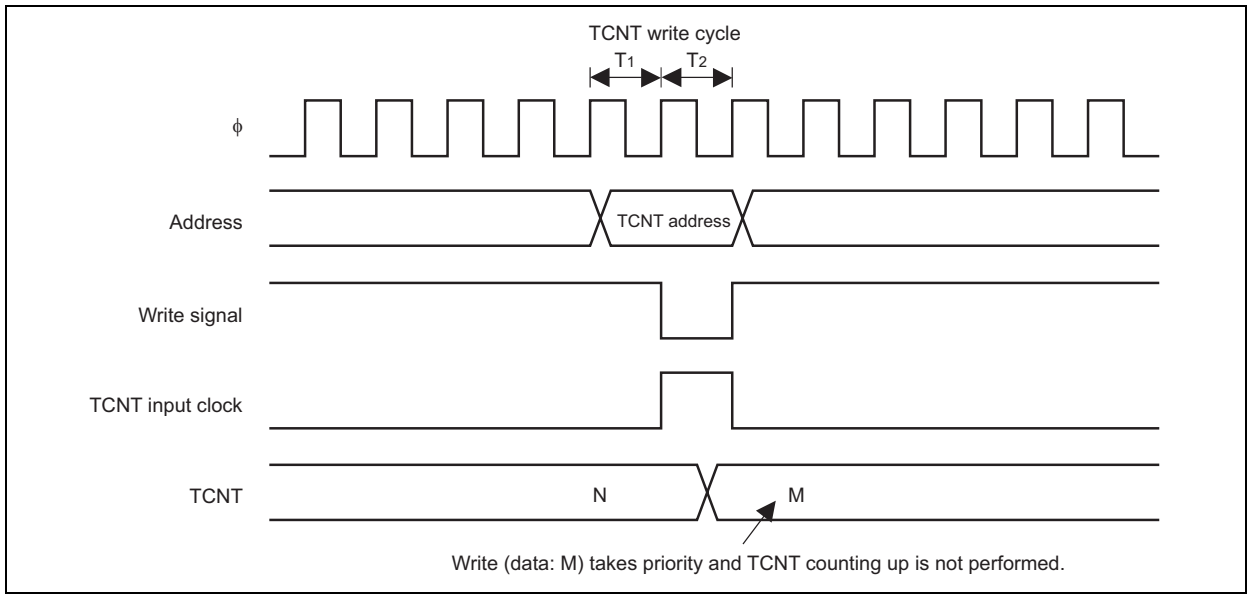


Figure 2 Contention between TCNT Write and Counting up

1.6 Contention between TGR Write and Compare Match

Even if a compare match occurs in the T2 state of a TGR write cycle, the write to TGR takes priority and the compare match signal is inhibited. No compare match will occur even if the same value is rewritten.

Figure 3 shows a timing example of a contention between TGR write and compare match.

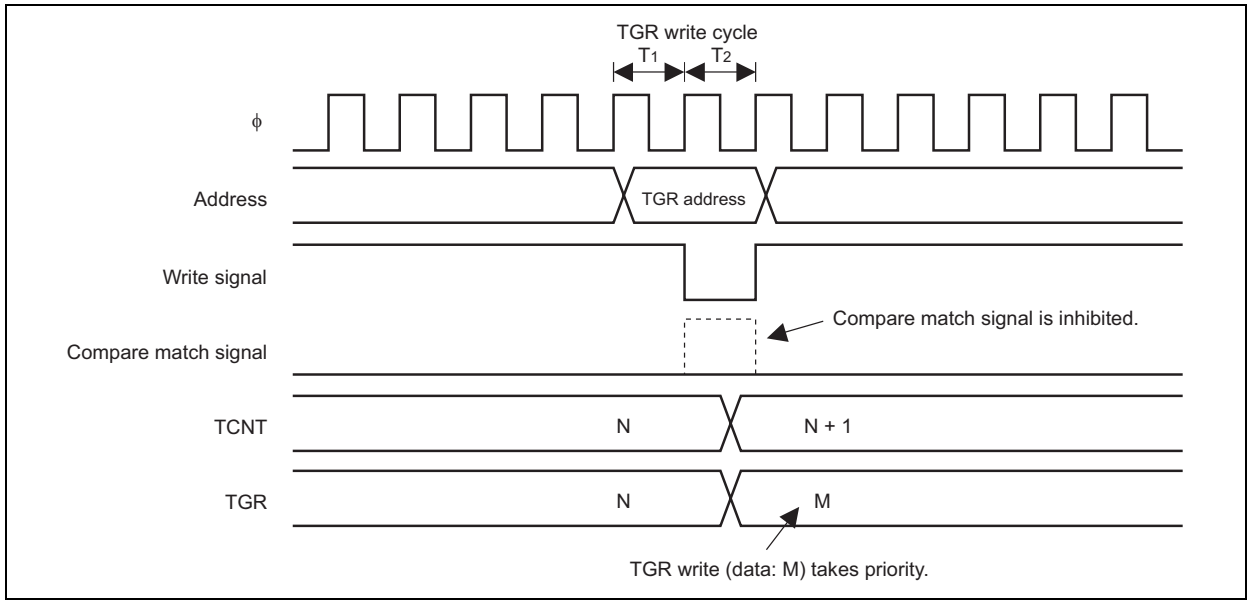


Figure 3 Contention between TGR Write and Compare Match

1.7 Contention between Overflow and Counter Clearing

If overflow and counter clearing occur at the same time, the TSR's TCFV flag is not set and the clearing of TCNT takes priority.

Figure 4 shows a timing example in which the TGR is loaded with H'FFFF as the clearing source of the TGR compare match.

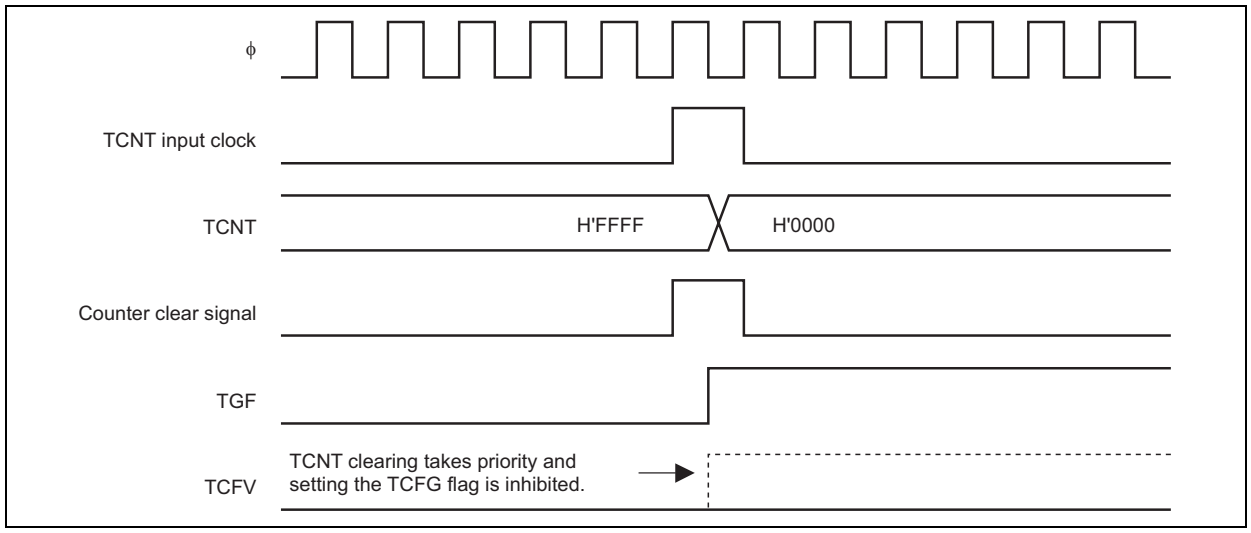


Figure 4 Contention between Overflow and Counter Clearing

1.8 Contention between TCNT Write and Overflow

Even if a counting up occurs in the T2 state of a TCNT write cycle and an overflow occurs, the write cycle takes priority and the TSR's TCFV flag is not set.

Figure 5 shows a timing example of a contention between TCNT write and overflow.

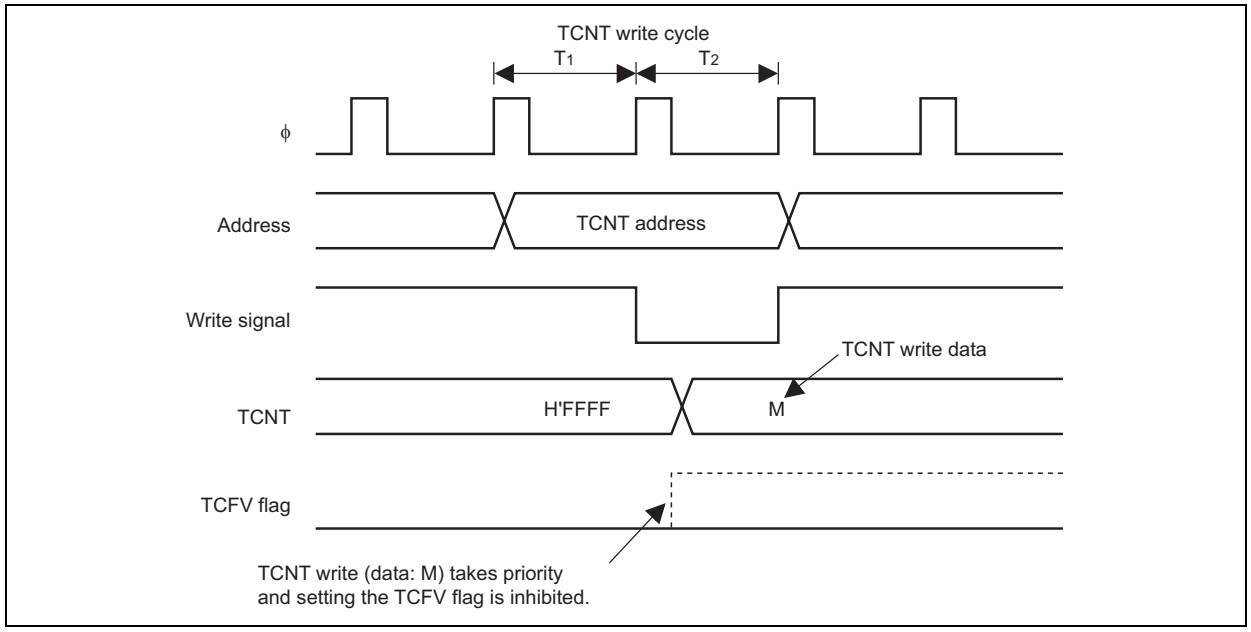


Figure 5 Contention between TCNT Write and Overflow

1.9 Multiplexing Input/Output Pins

The TIOCA1 I/O is multiplexed with the TCLKA input, the TIOCB1 I/O with the TCLKB input, and the TIOCA2 I/O with the TCLKC input. When an external clock is input, no compare match should be output from a multiplexed pin.

1.10 Interrupts in Module Standby Mode

If the module standby function is enabled when an interrupt request is requested, the CPU interrupt source cannot be cleared with the interrupt request enabled. The interrupt should be disabled before enabling the module standby function.

1.11 0% Duty and 100% Duty Output Conditions

When the duty is changed in PWM mode by rewriting TGR, there are cases in which the duty cycle is set to 0% or 100% depending on the TCNT value when rewritten, the TGR value before rewritten, and the TGR value after rewritten.

1.11.1 When the Value of the Duty Register is Greater than that of the Period Register Value

When the TGRA is set as the period register and the TGRB is set as the duty register in the PWM mode, a 0% duty is output if the duty value in the TGRB is rewritten with a value greater than the period in the TGRA. However it is presumed that the initial output at the TIOCA pin is 0, 0 is output on a TGRA compare match, 1 is output on a TGRB compare match, and a clearing source of TCNT is a compare match.

Figure 6 shows an operation example in which the duty register and the period register have the same value.

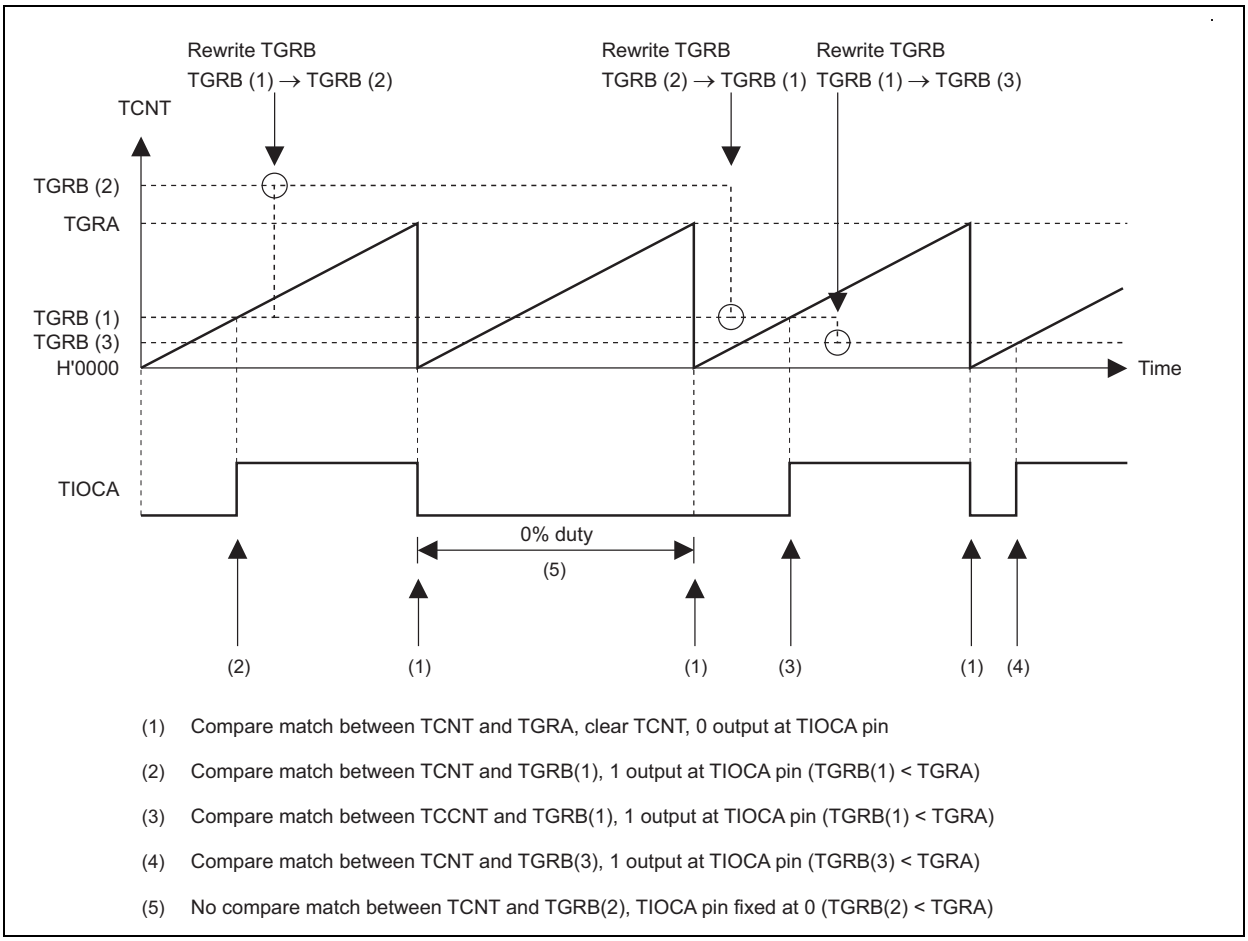


Figure 6 Operation Example in which the Duty Register Value is Greater than the Period Register Value

1.11.2 When the Duty and Period Registers Have the Same Value

When the TGRA is set as the period register and the TGRB is set as the duty register in the PWM mode, a 100% duty is output if the duty value in the TGRB is set to the equal period value in the TGRA. However it is presumed that the initial output at the TIOCA pin is 0, 0 is output on a TGRA compare match, 1 is output on a TGRB compare match, and the TCNT is cleared on a TGRA compare match.

Figure 7 shows an operation example in which the duty register and the period register have the same value.

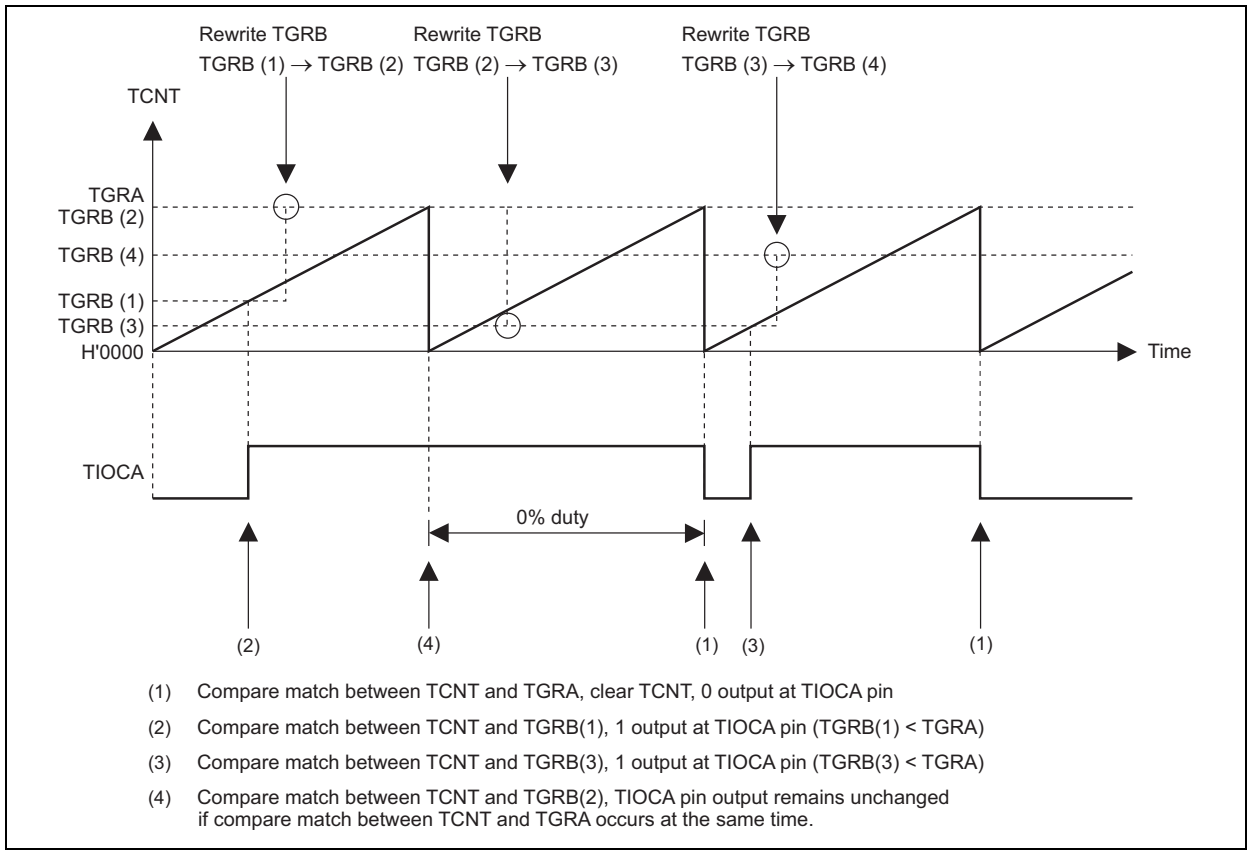
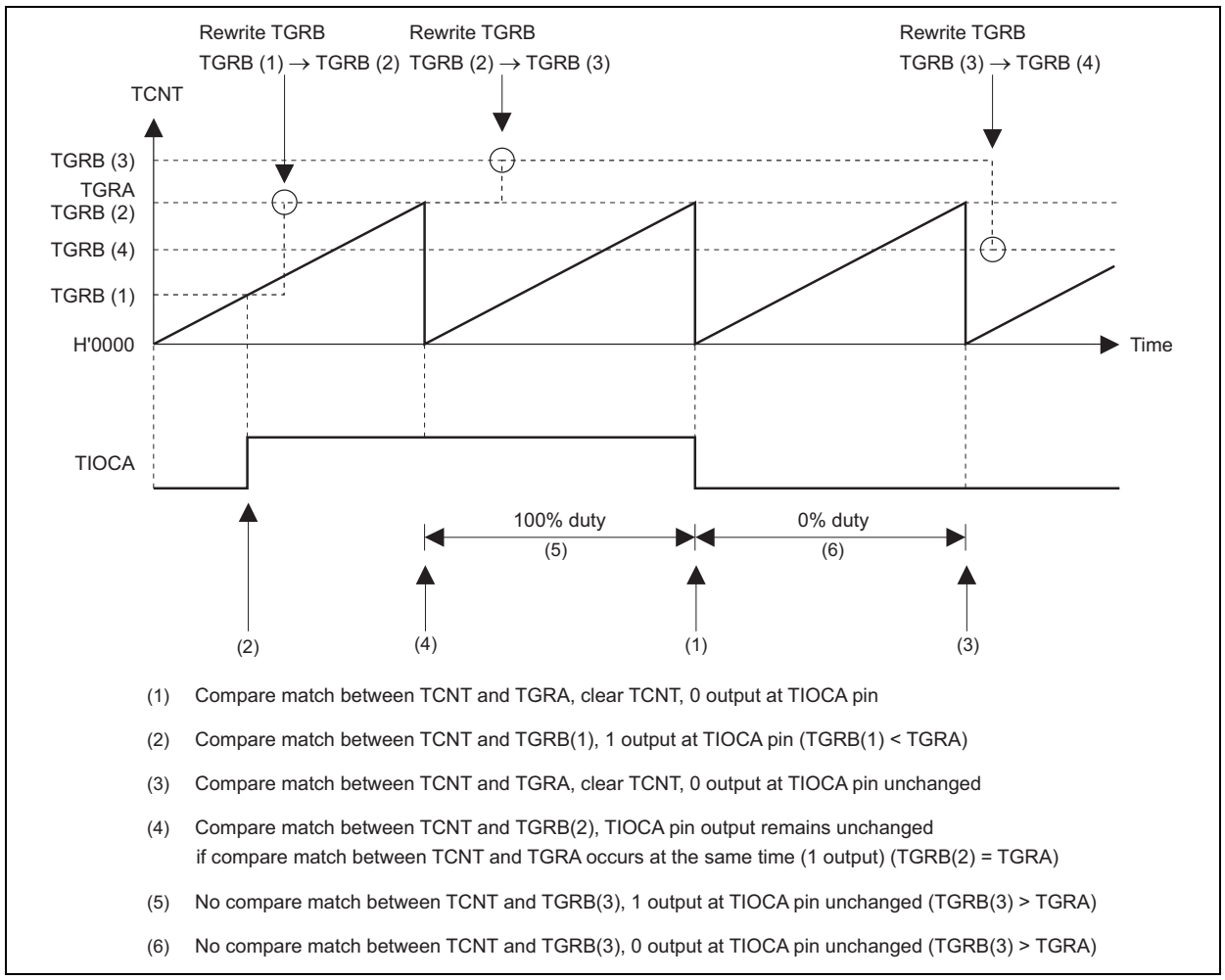


Figure 7 Operation Example in which the Duty and Period Registers Have the Same Value

1.11.3 When Duty Register Value Set to a Value Greater than Period Register Value after Setting Duty Register and Period Register to the Same Value

When the TGRA is set as the period register and the TGRB is set as the duty register in the PWM mode, a 0% duty is output after a 100% duty is output if the duty value in the TGRB is rewritten with a value that is greater than the period in the TGRA after setting the duty value of the TGRB to the same value in the TGRA. However it is presumed that initial output at the TIOCA pin is 0, 0 is output on a TGRA compare match, 1 is output on a TGRB compare match, and the TCNT is cleared on a TGRA compare match.

Figure 8 shows an operation example in which the value of the duty register is set to a value greater than that of the period register after setting the duty value of the duty register to the same value in the period register.



(1) Compare match between TCNT and TGRA, clear TCNT, 0 output at TIOCA pin

(2) Compare match between TCNT and TGRB(1), 1 output at TIOCA pin (TGRB(1) < TGRA)

(3) Compare match between TCNT and TGRA, clear TCNT, 0 output at TIOCA pin unchanged

(4) Compare match between TCNT and TGRB(2), TIOCA pin output remains unchanged if compare match between TCNT and TGRA occurs at the same time (1 output) (TGRB(2) = TGRA)

(5) No compare match between TCNT and TGRB(3), 1 output at TIOCA pin unchanged (TGRB(3) > TGRA)

(6) No compare match between TCNT and TGRB(3), 0 output at TIOCA pin unchanged (TGRB(3) > TGRA)

Figure 8 Operation Example in which Duty Register Value Set to a Value Greater than Period Register Value after Setting Duty Register and Period Register to the Same Value

1.11.4 Duty Register Value Set to a Value Smaller Than TCNT Value before Duty Register Compare Match Occurs

When the TGRA is set as the period register and the TGRB is set as the duty register in the PWM mode, a 0% duty is output if the duty value in the TGRB is set to a value smaller than the value in the TCNT before a compare match occurs on the TGRB duty value. However, it is presumend that the initial output at the TIOCA pin is 0, 0 is output on a TGRA compare match, 1 is output on a TGRB compare match, and the TCNT is cleared on a TGRA compare match.

Figure 9 shows an operation example in which the value of the duty register is set to a value smaller than the value in the TCNT before a compare match occurs in the duty register.

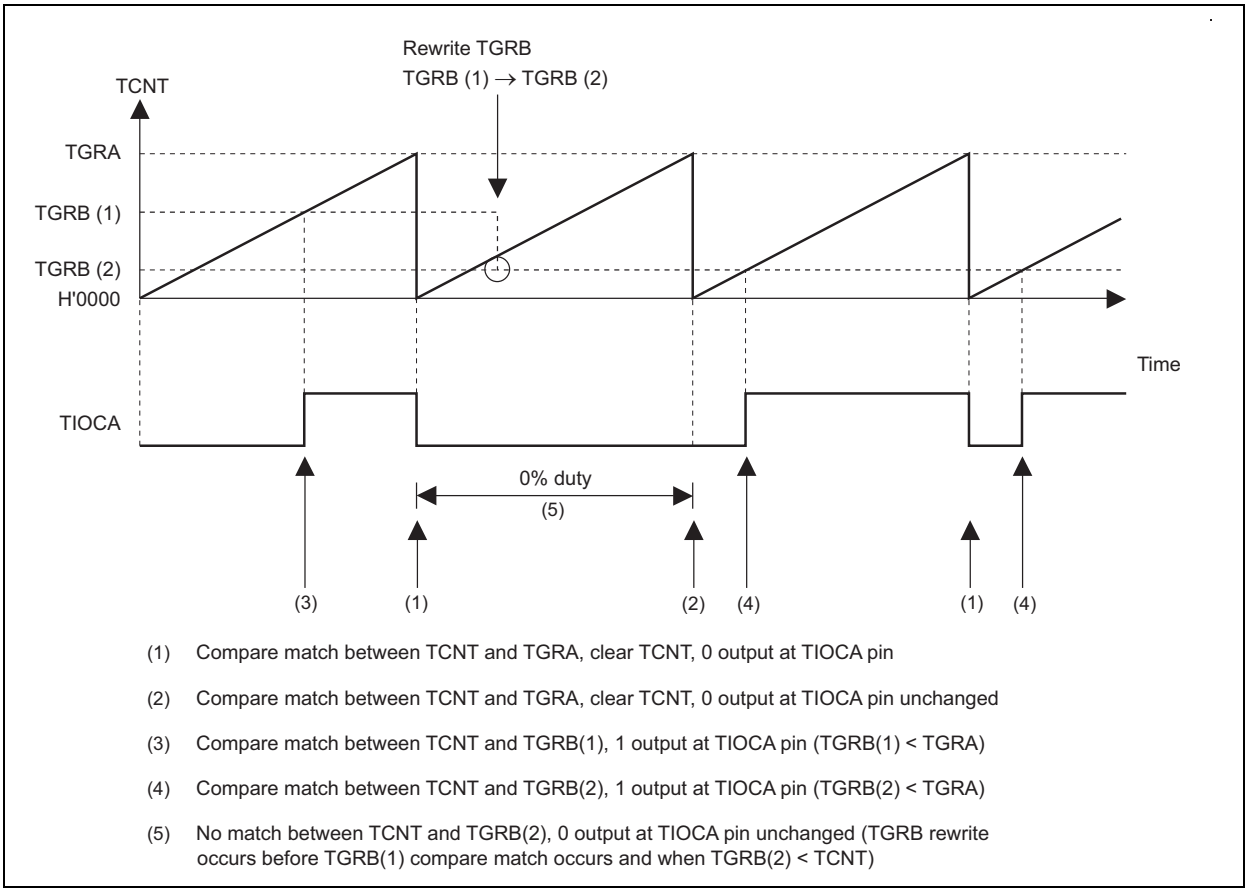


Figure 9 Operation Example in which Duty Register Value Set to a Value Smaller than TCNT Value before Duty Register Compare Match Occurs

2. Rewriting the Duty Register in PWM Mode

2.1 Avoiding 0% or 100% Duty Output when Rewriting the Duty Register

A 0% duty is output when the duty register is rewritten in PWM mode under the following cases:

- The rewrite value in the duty register is greater than the value in the period register (see 1.11.1).
- The duty register value is set to a value smaller than the value in the TCNT before a compare match occurs in the duty register (see 1.11.4).

A 100% duty is output when the duty register is rewritten in PWM mode under the following case:

- The rewrite value in the duty register is equal to that in the period register (see 1.11.2).

To avoid the 0% or 100% duty waveform output when rewriting the duty register, set as follows:

- Duty register rewrite value < Period register value
- If a duty register compare match has not yet occurred:
  Duty register rewrite value > Timer counter (TCNT) value

Since the timer counter (TCNT) continues counting when the duty register is written, however, it is necessary to take into consideration the number of states required to execute the instructions for rewriting the duty register.

It must also be noted when rewriting the duty register that even when a compare match occurs in the T2 state of the TGR write cycle, the TGR write takes priority and the compare match signal is inhibited (see section 1.6).

Figure 10 shows the timing example in which the duty register is written to avoid 0% and 100% duty outputs in PWM mode (TGRB(2) < TGRB(1) < TGRA).

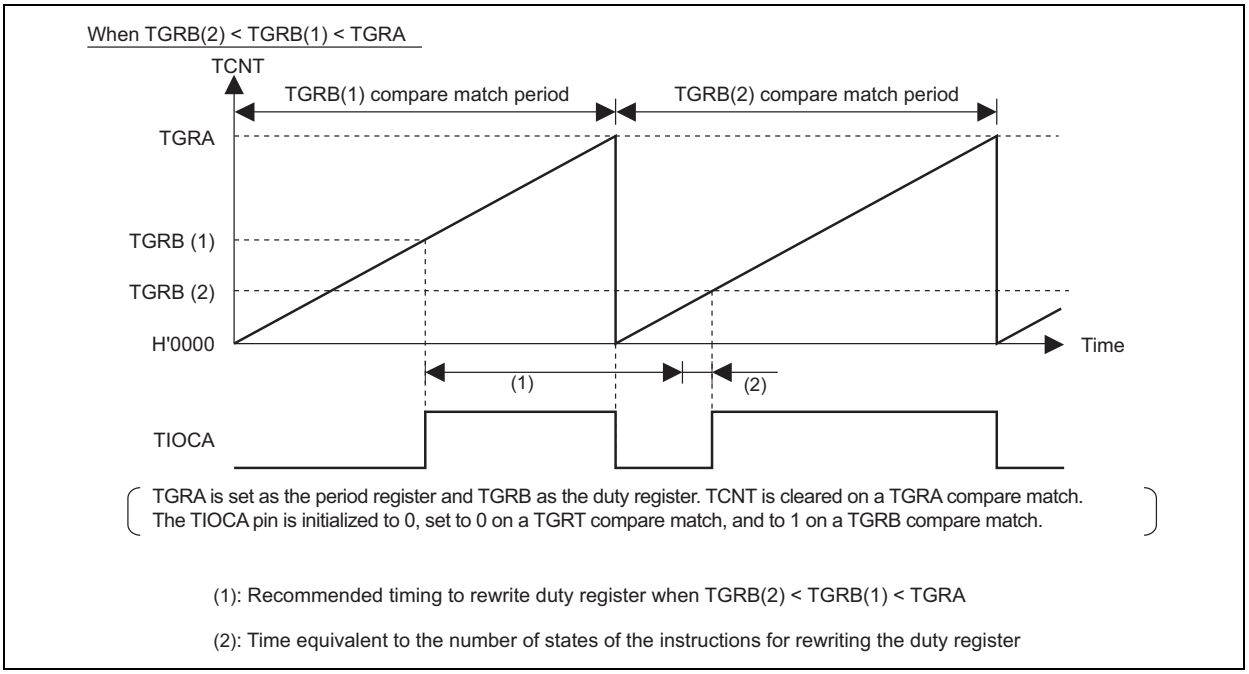


Figure 10 Timing for Rewriting Duty Register to Avoid 0% Duty and 100% Duty Outputs in PWM Mode (TGRB(2) < TGRB(1) < TGRA)

In figure 10, the period (2) denotes the time equivalent to the number of states of the instructions executed to rewrite the duty register. It is calculated from the number of clocks input to the TCNT and the number of states of the instructions taken to rewrite the duty register.

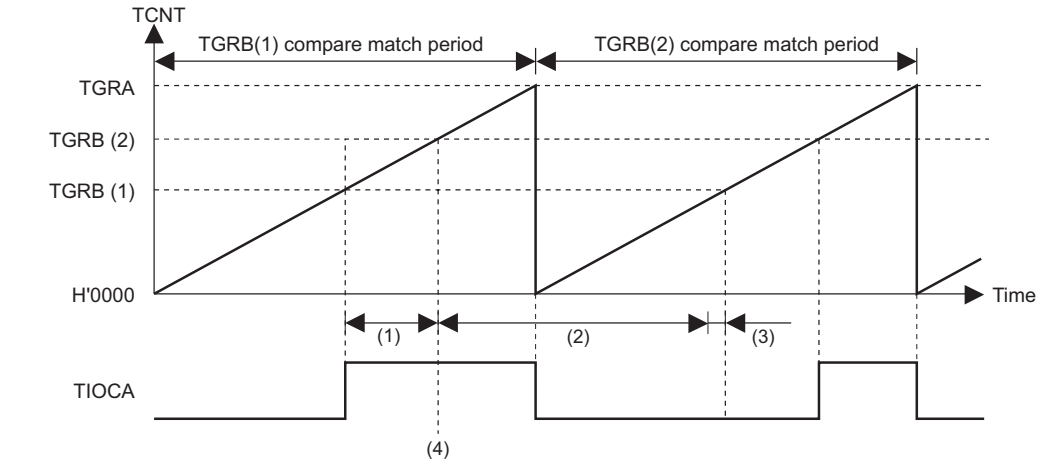
To avoid the generation of 0% or 100% duty PWM waveform output from the TIOCA pin while rewriting the duty register when the duty register values are [TGRB(2) < TGRB(1) < TGRA], rewrite the duty register value within the period that extends from the time a TGRB(1) compare match occurs till the time the TCNT countup value reaches the value that has been rewritten in the duty register (TGRB(2)).

If a contention occurs between the duty register write and compare match, however, a PWM waveform with a duty cycle of 0% is output because the compare match signal is inhibited.

If the duty register is written with the TRGB(2) value when the TCNT in the TGRB(2) compare match period has a value close to the rewritten value of TGRB(2), the TCNT is likely to count up in an execution state, causing a 0% duty PWM waveform to be output without a compare match signal being output.

To rewrite the duty register in such a situation in which the duty register values are [TGRB(2) < TGRB(1) < TGRA], it is necessary to do so during the period from the generation of the TGRB(1) compare match till the generation of the TGRB(2) compare match minus the period equivalent to the number of states taken to execute the instructions for rewriting the duty register ((2) in figure 10), i.e., ((1) in figure 10).

Figure 11 shows the timing example in which the duty register is written to avoid 0% and 100% duty outputs in PWM mode (TGRA > TGRB(2) > TGRB(1)).



TGRA is set as the period register and TGRB as the duty register. TCNT is cleared on a TGRA compare match. The TIOCA pin is initialized to 0, set to 0 on a TGRA compare match, and to 1 on a TGRB compare match.

(1): Period from the time a TGRB(1) compare match occurs till the time the TCNT value reaches the TGRB(2) value. It is likely that the second TRGB(2) compare match occurs during the compare match period for TGRB(1).

(2): Recommended timing to rewrite duty register when TGRA > TGRB(2) > TGRB(1)

(3): Time equivalent to the number of states of the instructions for rewriting the duty register

(4): TGRB(2) compare match occured during the TGRB(1) period after rewriting the duty register from TGRB(1) value to TGRB(2) value during period (1). The output at the TIOCA pin remains unchanged, however.

Figure 11 Timing for Rewriting Duty Register to Avoid 0% Duty and 100% Duty Outputs in PWM Mode (TGRA > TGRB(2) > TGRB(1))

In figure 11, the period (3) denotes the time equivalent to the number of states of the instructions executed to rewrite the duty register. It is calculated from the number of clocks input to the TCNT and the number of states of the instructions taken to rewrite the duty register.

To avoid the generation of 0% or 100% duty PWM waveform output from the TIOCA pin while rewriting the duty register when the duty register values are [TGRA > TGRB(2) > TGRB(1)], rewrite the duty register value within the period that extends from the time a TGRB(1) compare match occurs till the time the TCNT countup value reaches the value (TGRB(1)) that has been established before the duty register is rewritten.

If a contention occurs between the duty register write and compare match, however, a PWM waveform with a duty cycle of 0% is output because the compare match signal is inhibited.

If the duty register is written with the TRGB(2) value when the TCNT in the TGRB(2) compare match period has a value close to the rewritten value of TGRB(1), the TCNT is likely to count up in an execution state, causing a TGRB(1) compare match.

If the duty register is written with the TRGB(2) value during the period ((1) in figure 11) that extends from the time a TGRB(1) compare match occurs during the TGRB(1) compare match period till the time the TCNT counts up to the rewritten value of the duty register (TGRB(2)), the second compare match (TGRB(2) compare match, (4) in figure 11) is likely to occur during the compare match period for TGRB(1). The output level of the TIOCA pin remains unchanged, however.

To rewrite the duty register in such a situation in which the duty register values are [TGRA > TGRB(2) > TGRB(1)], therefore, it is necessary to do so during the period from the time the TCNT in the TGRB(1) compare match period exceeds the TGRB(2) value till the time the TCNT in the TGRB(2) compare match period reaches the old TGRB(1) value minus the period equivalent to the number of states taken to execute the instructions for rewriting the duty register ((3) in figure 11), i.e., ((2) in figure 11)).

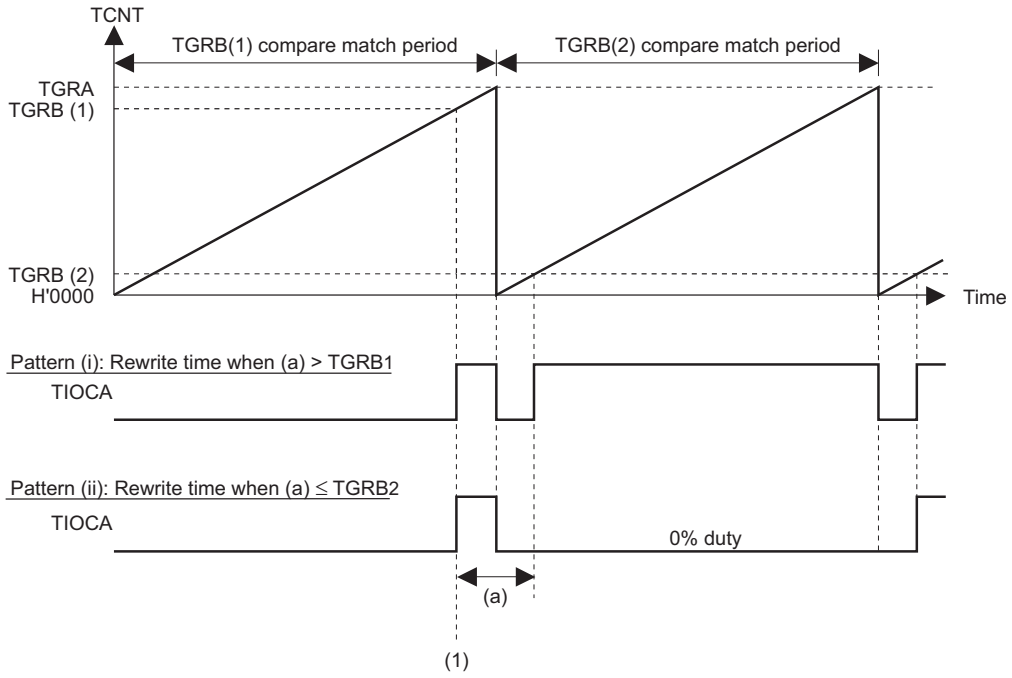
2.2 Timing for Rewriting the Duty Register in PWM Mode

This section discusses the following three timing patterns for rewriting the duty register to avoid the generation of 0% and 100% duty outputs in PWM:

(1) Rewriting at the timing of a TGRB compare match
(2) Rewriting at the timing of a TGRA compare match
(3) Rewriting asynchronously with TPU operation

2.2.1 Rewriting at the Timing of a TGRB (Duty Register) Compare Match

Figures 12 and 13 illustrate the considerations to be given to when rewriting the duty register at the timing of a TGRB duty register compare match.



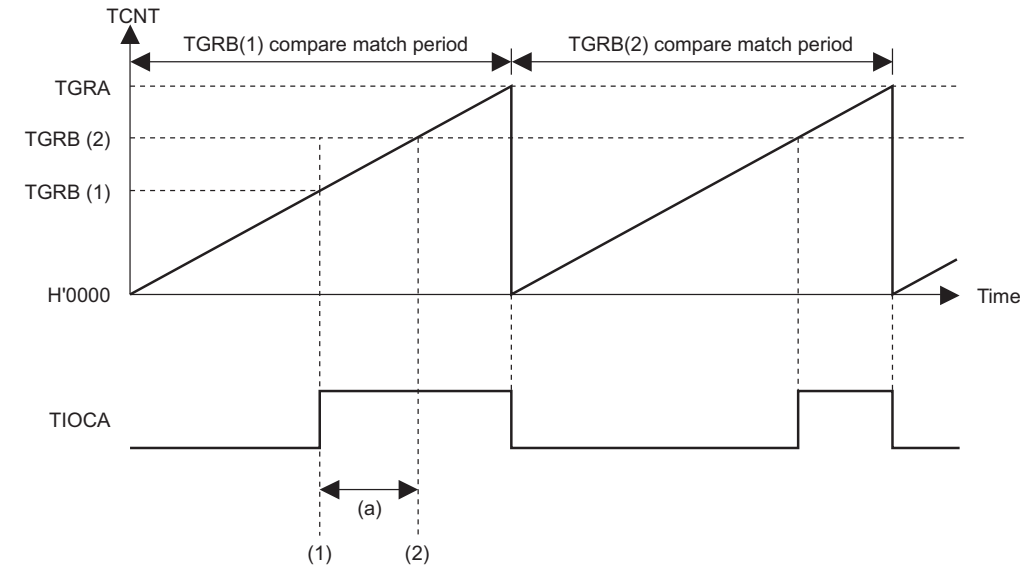
TGRA is set as the period register and TGRB as the duty register. TCNT is cleared on a TGRA compare match. The TIOCA pin is initialized to 0, set to 0 on a TGRA compare match, and to 1 on a TGRB compare match.

(1) : TGRB(1) compare match during TGRB(1) period

(a) : Period from TGRB(1) compare match during TGRB(1) period till the time the TCNT in the TGRB(2) period counts up to the rewritten TGRB(2) value

If the TGRB rewrite fails during the period from the generation of the TGRB(1) compare match till the TCNT countup to the rewritten TGRB(2) value when the TGRB(1) value is close to the TGRA value and the TGRB(2) value is close to H'0000, a PWM waveform output with a duty cycle of 0% will output as shown in pattern (ii). The TGRB(2) compare match is inhibited and a PWM waveform output with a duty cycle of 0% is also generated as shown in pattern (ii) when a contention occurs between the TGRB(2) write and TGRB(2) compare match during the TGRB(2) compare match period.

Figure 12 Considerations to be Given to when Rewriting at the Timing of a Duty Register (TGRB) Compare Match (1)



TGRA is set as the period register and TGRB as the duty register. TCNT is cleared on a TGRA compare match.
The TIOCA pin is initialized to 0, set to 0 on a TGRA compare match, and to 1 on a TGRB compare match.

(1) : TGRB(1) compare match during TGRB(1) period

(2) : TGRB(2) compare match during TGRB(2) period

(a) : Period from the TGRB(1) compare match during TGRB(1) period till the time the TCNT in the TGRTB(1) period counts up to the rewritten TGRB(2) value

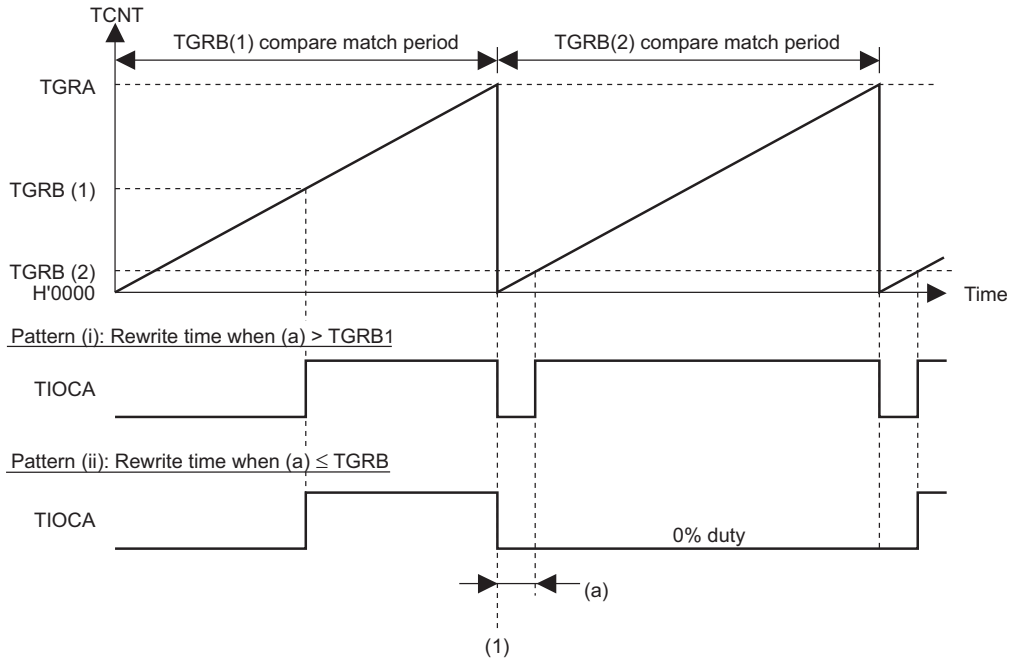
It is likely that a TGRB(2) compare match occurs during the TGRB(1) period if the TGRB(2) is written (TGRA < TGRB(2) < TGRB(1)) after a TGRB(1) compare match occurs during the TGRB(1) compare match period. The output at the TIOCA pin remains unchanged, however.

Figure 13 Considerations to be Given to when Rewriting at the Timing of a Duty Register (TGRB) Compare Match (2)

The TGRB(2) compare match during the TGRB(1) period shown in figure 13 can be avoided by writing TGRB(2) after monitoring the TCNT on the first TGRB(1) compare match and verifying the condition TCNT ≥ TGRB(2).

2.2.2 Rewriting at the Timing of a TGRA (Period Register) Compare Match

Figure 14 illustrates the considerations to be given to when rewriting the duty register at the timing of a TGRA period register compare match.



TGRA is set as the period register and TGRB as the duty register. TCNT is cleared on a TGRA compare match. The TIOCA pin is initialized to 0, set to 0 on a TGRA compare match, and to 1 on a TGRB compare match.

(1) : TGRB(1) compare match during TGRB(1) period

(a) : Period from TGRB(1) compare match during TGRB(1) period till the time the TCNT in the TGRB(2) period counts up to the rewritten TGRB(2) value

IIf the TGRB rewrite fails during the period from the generation of the TGRA(1) compare match till the TCNT countup to the TCNT-rewritten TGRB(2) value when the TGRB(2) value is close to H'0000, a PWM waveform output with a duty cycle of 0% will output as shown in pattern (ii).

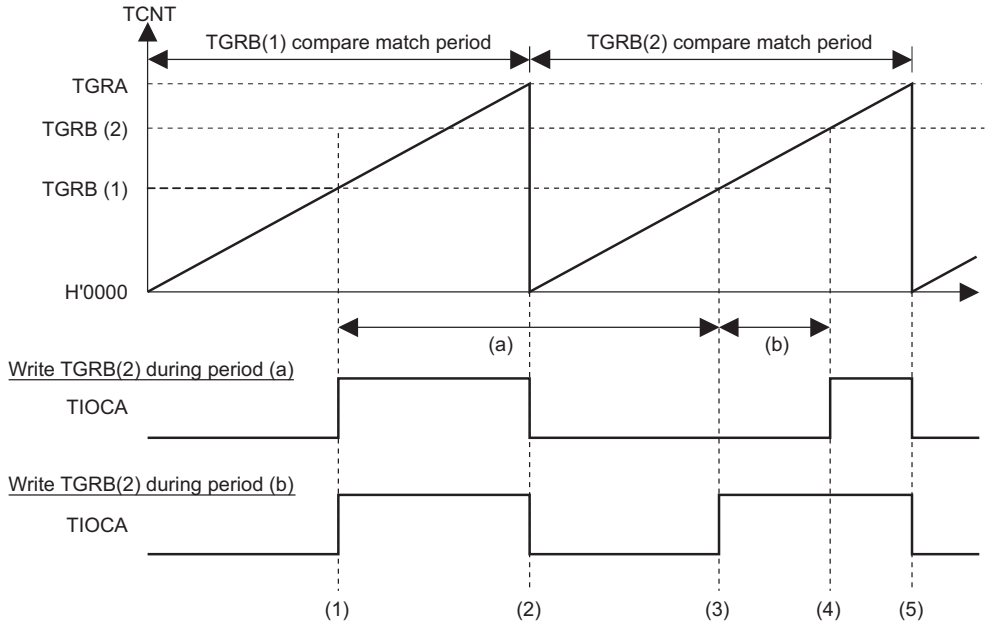
The TGRB(2) compare match is inhibited and a PWM waveform output with a duty cycle of 0% is also generated as shown in pattern (ii) when a contention occurs between the TGRB(2) write and TGRB(2) compare match during the TGRB(2) compare match period.

Figure 14 Considerations to be Given to when Rewriting at the Timing of a Period Register (TGRA) Compare Match

2.2.3 When Rewriting Asynchronously with TPU

The considerations to be given to when rewriting the duty register at an arbitrary timing, asynchronously with TPU, are explained below. When the duty register is rewritten, the PWM waveform output is likely to change at the timing depending on the count value in the TCNT, the old value in the duty register (TGRB(1)), and the duty register value established after the write (TGRB(2)).

(1) When TGRA > TGRB(2) > TGRB(1)



TGRA is set as the period register and TGRB as the duty register. TCNT is cleared on a TGRA compare match. The TIOCA pin is initialized to 0, set to 0 on a TGRA compare match, and to 1 on a TGRB compare match.

(1) : TGRB(1) compare match during TGRB(1) period

(2) : TGRA compare match during TGRB(1) period

(3) : TGRB(1) compare match during TGRB(2) period

(4) : TGRB(2) compare match during TGRB(2) period

(5) : TGRA compare match during TGRB(2) period

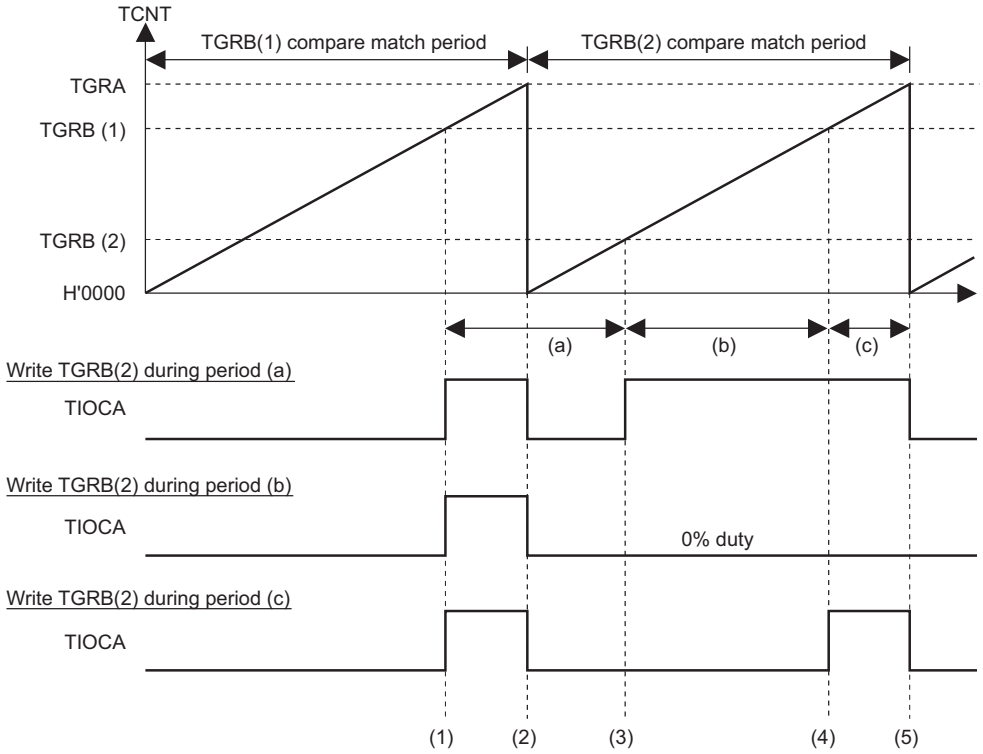
(a) : Period from TGRB(1) compare match during TGRB(1) period till the time TCNT in TGRB(2) period counts up to TGRB(1) value

(b) : Period during which TCNT in TGRB(2) period counts from old TGRB(1) value up to rewritten TGRB(2) value

If TGRB(2) is written during the above shown period (b), the compare match on the old TGRB(1) value occurs before the TGRB(2) compare match recurs. The TIOCA pin, however, is set to 1 on the preceding TGRB(1) compare match and this state remains unchanged on the second TGRB(2) compare match.

Figure 15 When Rewriting Asynchronously with TPU Operation (TGRA > TGRB(2) > TGRB(1))

(2) When TGRB(2) < TGRB(1) < TGRA



TGRA is set as the period register and TGRB as the duty register. TCNT is cleared on a TGRA compare match.
The TIOCA pin is initialized to 0, set to 0 on a TGRA compare match, and to 1 on a TGRB compare match.

(1) : TGRB(1) compare match during TGRB(1) period
(2) : TGRA compare match during TGRB(1) period
(3) : TGRB(2) compare match during TGRB(2) period
(4) : TGRB(1) compare match during TGRB(2) period
(5) : TGRA compare match during TGRB(2) period

(a) : Period from TGRB(1) compare match during TGRB(1) period till the time TCNT in TGRB(2) period counts up to rewritten TGRB(2) value

(b) : Period during which TCNT in TGRB(2) period counts from rewritten TGRB(2) value up to old TGRB(2) value

(c) : Period during which TCNT in TGRB(2) period counts up from old TGRB(1) value till before the TGRA compare match occurs

If TGRB(2) is rewritten during the above-shown period (b), no TGRB(2) compare match occurs within the TGRB(2) period and the duty cycle of the PWM waveform output from the TIOCA pin is 0%. To rewrite TGRB(2) during the above period (b) and avoid the generation of a 0% duty PWM waveform, it is necessary to make the value of TGRB(2) greater than the value in the TCNT.

If TGRB(2) is rewritten during the above-shown period (c), the TGRB(1) compare match for the preceding session occurs first and a PWM waveform with the same duty cycle as previous time is output the TIOCA pin. The compare match for TGRB(2) occurs in the next period.

Figure 16 When Rewriting Asynchronously with TPU Operation (TGRB(2) < TGRB(1) < TGRA))

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