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H8/38602R Group

Master/Slave Communication in 4-Line Bus Communication Mode and Interrupts

Introduction

This application note discusses communication by the synchronous serial communication unit (SSU) in 4-line bus communication mode with use of various SSU interrupts.

Target Device

H8/38602R

Contents

1. Specifications

- As shown in figure 1, the H8/38602R performs communication by the SSU in 4-line bus communication mode using various SSU interrupts.
- In this sample task, the master device transmits four-byte data, and the slave device receives it. The slave device transmits the received four-byte data back to the master device, and the master device receives it.
- In this sample task, the transfer clock rate is $\phi/32$ (ϕ = 10 [MHz]).

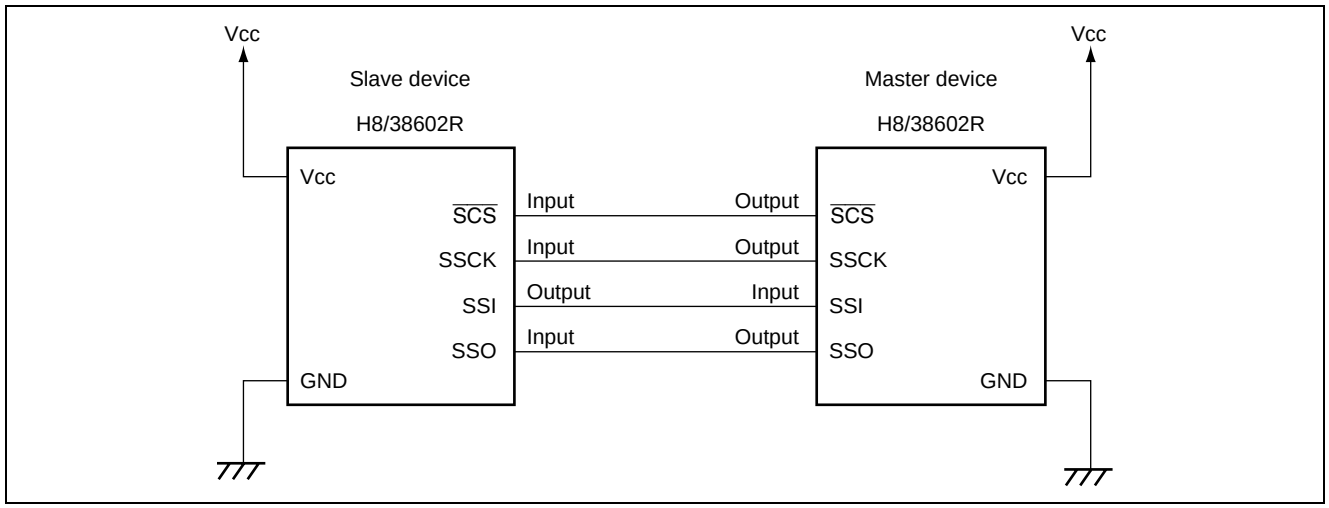


Figure 1 Connections in 4-Line Bus Communication Mode of SSU

2. Description of Functions

2.1 Functions

This sample task implements communication by the SSU in 4-line bus communication mode using various SSU interrupts. Figure 2 shows a block diagram of the SSU, and below is the functional explanation.

2.1.1 Functions of SSU in 4-Line Bus Communication Mode

The master device transmits four-byte data, and the slave device receives it. The slave device transmits the received four-byte data back to the master device, and the master device receives it. The transfer clock rate is $\phi/32$ (ϕ = 10 [MHz]).

- SS Control Register H (SSCRH)
  SSCRH is a register that selects whether the SSU operates as a master or slave device, and selects the functions of the SSCK and $\overline{SCS}$ pins.
- SS Control Register L (SSCRL)
  SSCRL is a register that selects the operating mode of the SSU.
- SS Mode Register (SSMR)
  SSMR is a register that selects MSB-first or LSB-first, and selects transfer clock rate.
- SS Enable Register (SSER)
  SSER is a register that enables transmit or receive operation.
- SS Status Register (SSSR)
  SSSR is a register that consists of interrupt flags.
- SS Receive Data Register (SSRDR)
  SSRDR is an 8-bit register that stores received serial data. When the SSU has received one byte of serial data, it transfers the data from SSTRSR to SSRDR. The SSTRSR is then ready to receive the next byte. This double-buffered configuration of SSTRSR and SSRDR allows continuous receive operation. SSRDR is a read-only register and cannot be written to by the CPU. The initial value of SSRDR is H'00.
- SS Transmit Data Register (SSTDR)
  SSTDR is an 8-bit register that stores serial data to be transmitted. SSTDR can be read or written to by the CPU at any time. When the SSU detects that SSTRSR is empty, it transfers the transmit data stored in SSTDR to SSTRSR and then starts serial transmission. By writing the next transmit data to SSTDR during serial transmission of the data in SSTRSR, continuous serial transmission is possible. The initial value of SSTDR is H'00.
- SS Shift Register (SSTRSR)
  SSTRSR is a shift register used to transmit and receive serial data. When transmit data is transferred from SSTDR to SSTRSR, bit 0 in SSTDR is transferred to bit 0 in SSTRSR if the MLS bit in SSMR is 0 (LSB-first transfer), and bit 7 in SSTDR is transferred to bit 0 in SSTRSR if the MLS bit is 1 (MSB-first transfer). SSTRSR cannot be directly accessed by the CPU.

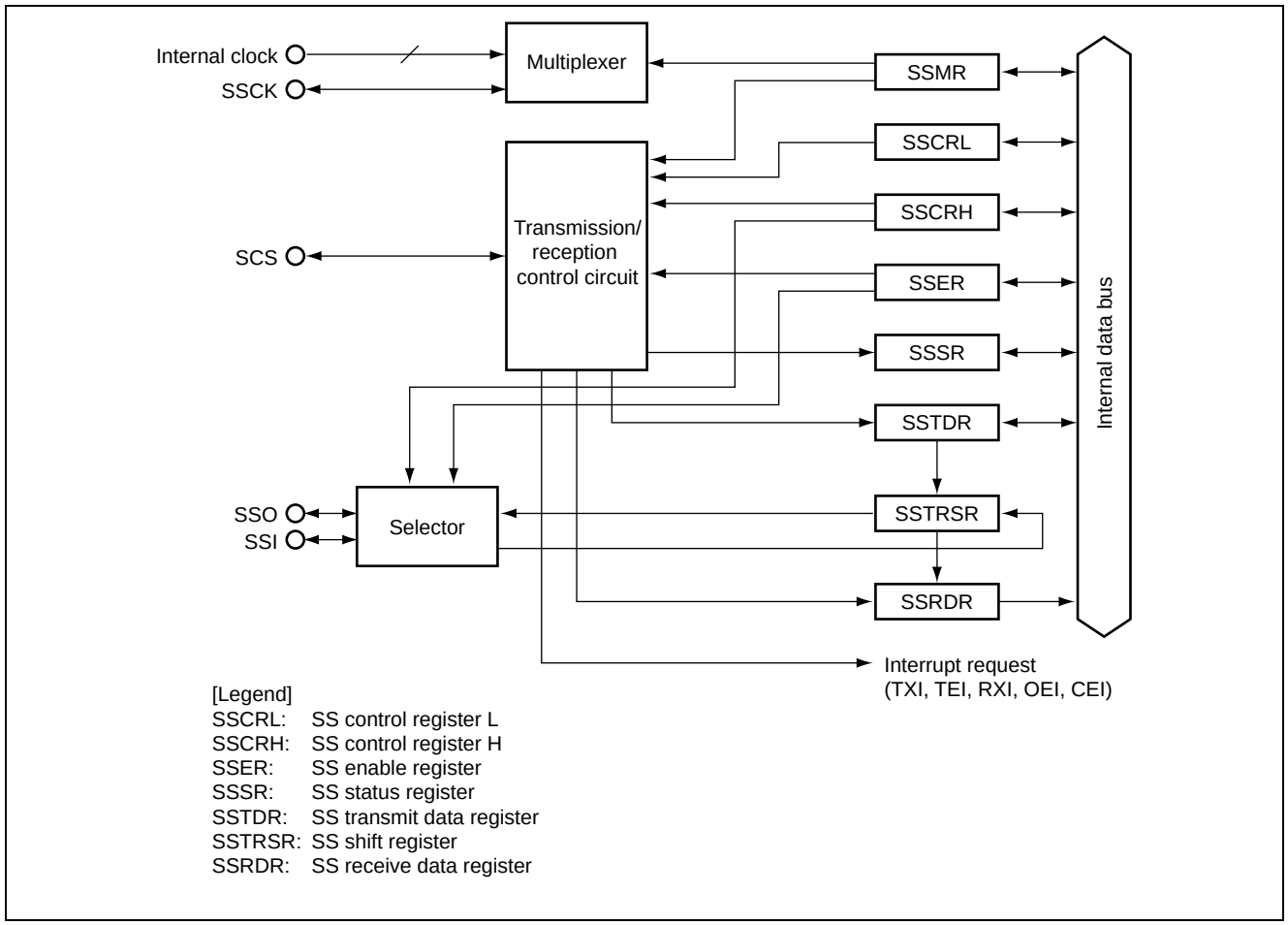


Figure 2 Block Diagram of SSU

2.1.2 Watchdog Timer Function

The H8/38602R includes a watchdog timer. The watchdog timer is active after reset. The timer counter WD (TCWD) is incremented and if the TCWD overflows, the H8/38602R is internally reset. This sample task does not use the watchdog timer function, and thus stops this timer.

- Timer Control/Status Register WD1 (TCSRWD1)
  TCSRWD1 controls writing to TCSRWD1 and TCWD. TCSRWD1 also controls the watchdog timer operation and indicates the operating status. TCSRWD1 must be rewritten by using the MOV instruction. Bit manipulation instructions cannot be used to change the setting value.

2.1.3 Module Standby Function

The module standby function places the SSU in the module standby mode after the reset is released. The module standby mode can be cancelled by setting the SSUCKSTP bit of the clock halt register 2 (CKSTPR2) to 1.

- Clock Halt Register 2 (CKSTPR2)
  CKSTPR2 allows the on-chip peripheral modules to enter standby mode in module units.

2.1.4 I/O Port Function

The P91/SSCK/SDA pin is pulled up so that the pin normally stays high (slave device only).

- Port Pull-Up Control Register 9 (PUCR9)
  PUCR9 controls the pull-up MOS of the port 9 pins in bit units.

2.2 Assignment of Functions

Functions used for this sample task are listed in tables 1 and 2. Communication by the SSU is performed in 4-line bus communication mode using various SSU interrupts by assigning the functions as shown in tables 1 and 2.

Table 1 Function Assignment of Slave Device

Elements	Category	Description
SSCK	Pin	SSU clock input
SSI	Pin	SSU data output
SSO	Pin	SSU data input
$\overline{\text{SCS}}$	Pin	SSU chip select input
SSCRH	SSU	Selects slave mode and selects the SSCK and $\overline{\text{SCS}}$ pin functions.
SSCRL	SSU	Selects 4-line bus communication mode.
SSMR	SSU	Selects MSB first and a transfer clock rate of ϕ/32.
SSER	SSU	Enables data transmission/reception, TXI, TEI, RXI, OEI and CEI.
SSSR	SSU	Status flags
SSRDR	SSU	A register that stores receive data
SSTDR	SSU	A register that stores transmit data
SSTRSR	SSU	A shift register used to transmit or receive data
PUCR9	I/O port	Pulls up the $\overline{\text{SCS}}$ pin.
CKSTPR2	Low power	Cancels module standby mode of the SSU.
TCSRWD1	WDT	Stops the watchdog timer.

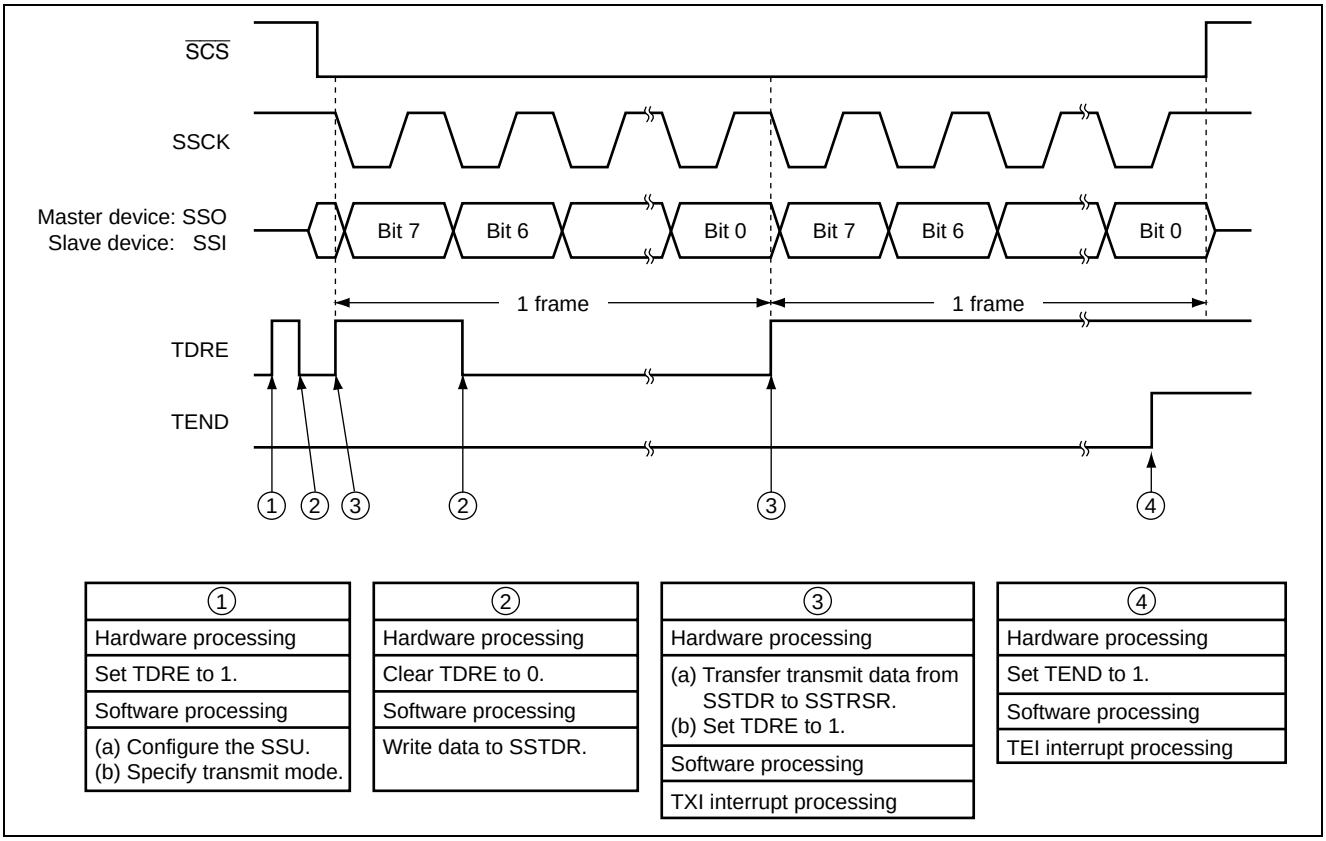
Table 2 Function Assignment of Master Device

Elements	Category	Description
SSCK	Pin	SSU clock output
SSI	Pin	SSU data input
SSO	Pin	SSU data output
$\overline{\text{SCS}}$	Pin	SSU chip-select output
SSCRH	SSU	Selects master mode and selects the SSCK and $\overline{\text{SCS}}$ pin functions.
SSCRL	SSU	Selects 4-line bus communication mode.
SSMR	SSU	Selects MSB-first and a transfer clock rate of ϕ/32.
SSER	SSU	Enables data transmission/reception, TXI, TEI, RXI, OEI and CEI. Controls RSSTP.
SSSR	SSU	Status flags
SSRDR	SSU	A register that stores received data
SSTDR	SSU	A register that stores transmit data
SSTRSR	SSU	A shift register used to transmit or receive data
CKSTPR2	Low power	Cancels module standby mode of the SSU.
TCSRWD1	WDT	Stops the watchdog timer.

3. Description of Operation

3.1 Transmit Mode

Figure 3 illustrates the operation timing in transmit mode for this sample task, with description of the hardware and software processing.



①	②	③	④
Hardware processing	Hardware processing	Hardware processing	Hardware processing
Set TDRE to 1.	Clear TDRE to 0.	(a) Transfer transmit data from SSTDR to SSTRSR. (b) Set TDRE to 1.	Set TEND to 1.
Software processing	Software processing	Software processing	Software processing
(a) Configure the SSU. (b) Specify transmit mode.	Write data to SSTDR.	TXI interrupt processing	TEI interrupt processing

Figure 3 Operation Timing in Transmit Mode

3.2 Receive Mode

Figure 4 illustrates the operation timing in receive mode for this sample task, with description of the hardware and software processing.

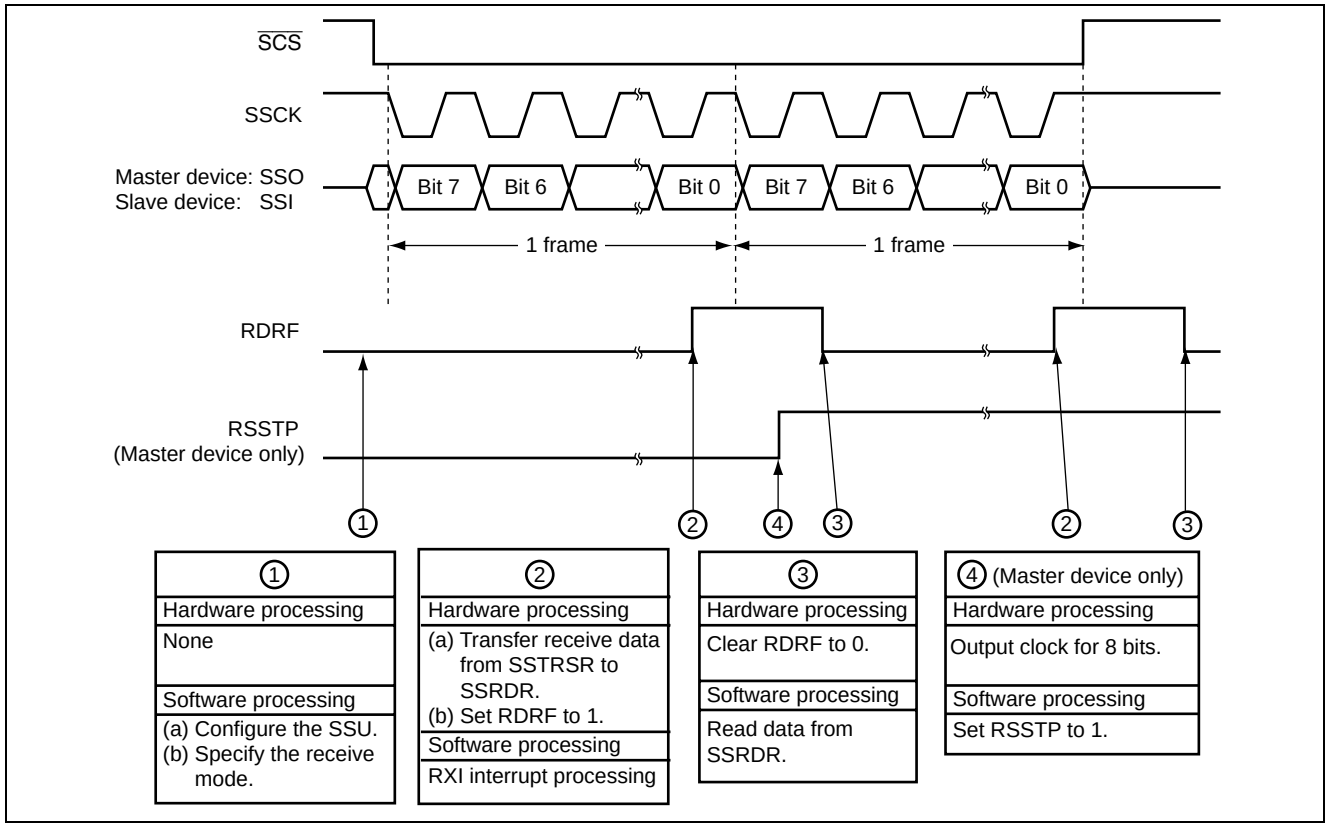


Figure 4 Operation Timing in Receive Mode

4. Description of Software (Slave)

This sample task performs slave communication by the SSU in 4-line bus communication mode (SPI mode), using SSU interrupts.

4.1 List of Functions

Table 3 Slave Program Functions

Function Name	Description
main	Stops the watchdog timer, controls slave communication and interrupts, and Initializes the RAM area for use.
SSU_spi_init	Initializes the SSU in SPI mode (4-line bus communication mode), and cancels module standby mode of the SSU.
ssu_int	SSU interrupt processing (TXI, TEI, RXI, OEI, CEI)

4.2 Constants

This sample task does not use constants.

4.3 RAM Usage

Table 4 describes the RAM usage in this sample task.

Table 4 Description of RAM

Label Name	Function	Data Length	Used In
s_rcv[4]	Buffer for storing received data	4 bytes	main, ssu_int
trs_cnt	Transmission counter used for checking the number of times transmission has been performed.	1 byte	main, ssu_int
rcv_cnt	Reception counter used for checking the number of times reception has been performed.	1 byte	main, ssu_int
error	Error status flag 0: No error occurred. 1: Error occurred.	1 byte	main, ssu_int

4.4 Description of Modules

4.4.1 main() Function

(1) Module Specifications

Function: Stops the watchdog timer, controls slave communication and interrupts, and initializes the RAM area for use.

Table 5 Module Specifications

Item	Type	Variable Name	Description
Argument	None	None	None

(2) Internal Registers

The internal registers used in this sample task are described below. The setting values in the tables below are used in this task and are different from the initial values.

- Port Pull-up Control Register 9 (PUCR9) Address: H'F087

Bit	Bit Name	Setting	R/W	Function
0	PUCR90	1	R/W	With a PCR9 bit cleared to 0, setting the corresponding PUCR9 bit to 1 turns on the pull-up MOS for the corresponding pin, while clearing the bit to 0 turns off the pull-up MOS.

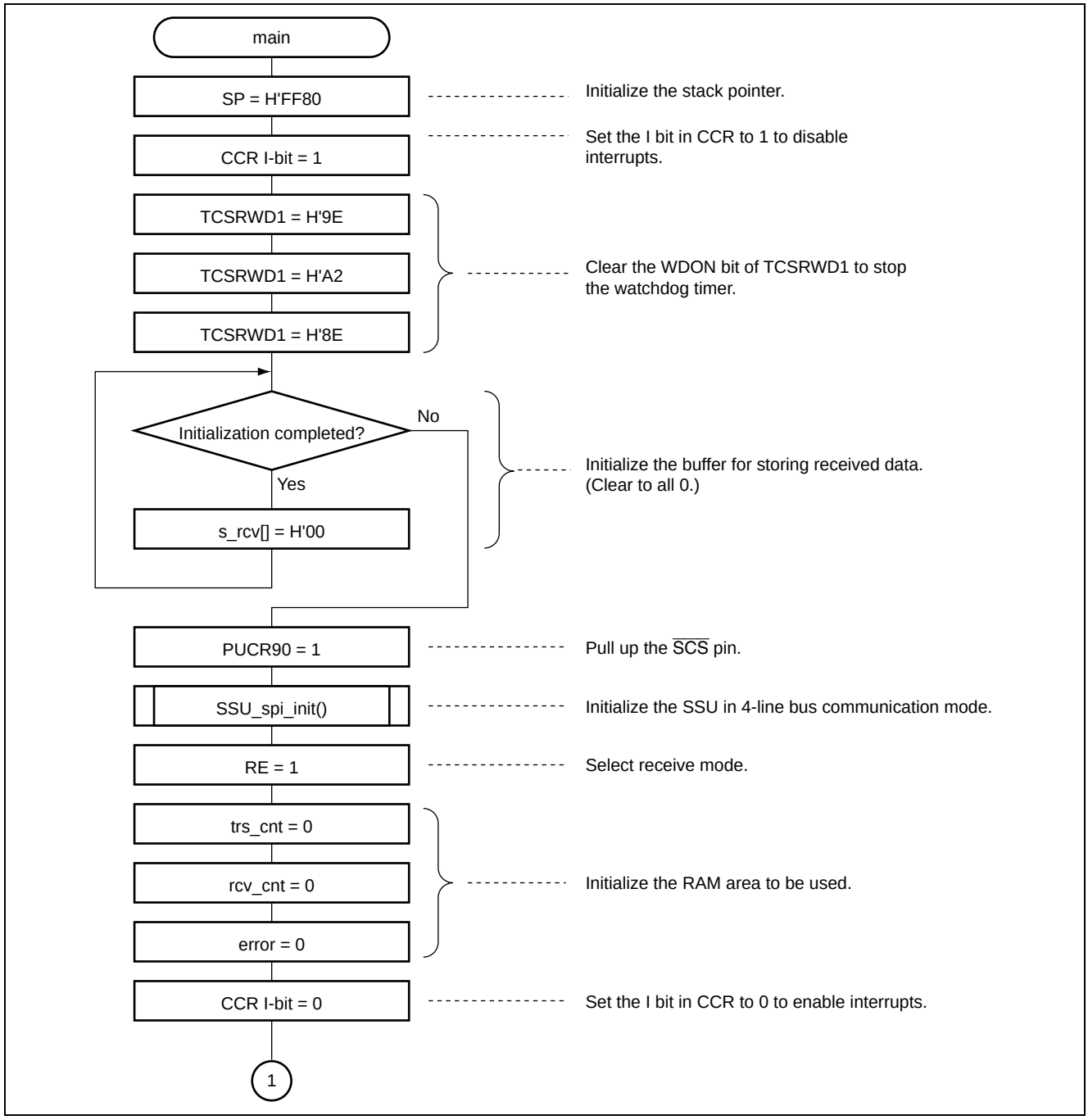
- SS Enable Register (SSER) Address: H'F0E3

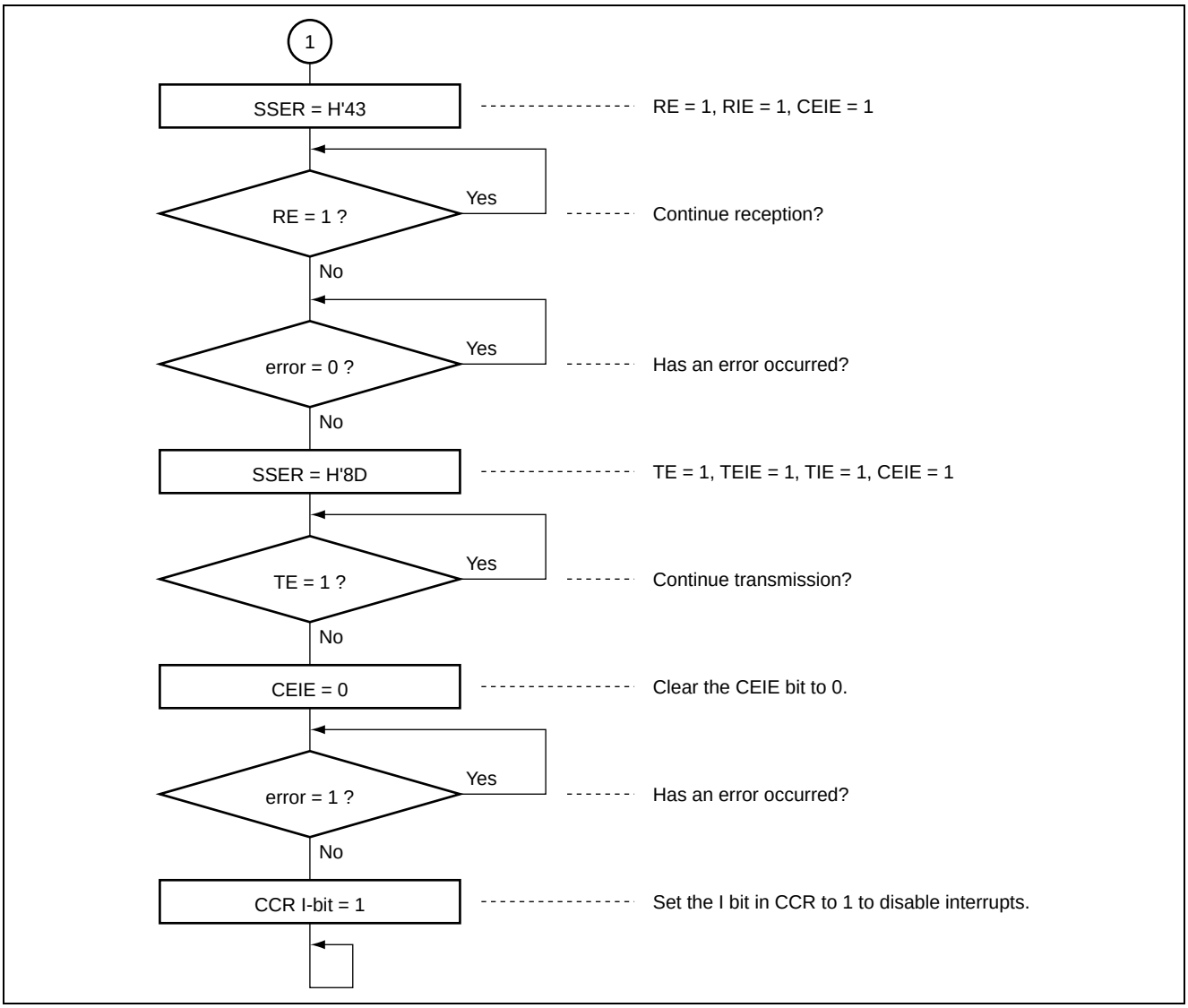
Bit	Bit Name	Setting	R/W	Function
7	TE	1	R/W	Transmit enable Enables transmit operation when this bit is 1. 0: Disables transmit operation 1: Enables transmit operation
6	RE	1	R/W	Receive enable Enables receive operation when this bit is 1. 0: Disables receive operation 1: Enables receive operation
3	TEIE	1	R/W	Transmit End Interrupt Enable Enables TEI interrupt requests when this bit is set to 1. 1: Enables TEI interrupts.
2	TIE	1	R/W	Transmit Interrupt Enable Enables TXI interrupt requests when this bit is set to 1. 1: Enables TXI interrupts.
1	RIE	1	R/W	Receive Interrupt Enable Enables RXI and OEI interrupt requests when this bit is set to 1. 1: Enables RXI and OEI interrupts.
0	CEIE	1	R/W	Conflict Error Interrupt Enable Enables CEI interrupt requests when this bit is set to 1. 1: Enables CEI interrupts.

- Timer Control Register/Status Register WD1 (TCSRWD1) Address: H'FFB1

Bit	Bit Name	Setting	R/W	Function
7	B6WI	1	R/W	Bit 6 Write Disable Writing to the TCWE bit is only enabled when 0 is written to the B6WI bit. This bit is always read as 1.
6	TCWE	0	R/W	Timer Counter WD Write Enable Writing to the timer counter WD (TCWD) is enabled when the TCWE bit is set to 1. When writing to this bit, 0 must be written to the B6WI bit.
5	B4WI	1	R/W	Bit 4 Write Disable Writing to the TCSRWE bit is only enabled when 0 is written to the B4MI bit. The B4WI bit is always read as 1.
4	TCSRWE	0	R/W	Timer Control/Status Register WD1 Write Enable Writing to the WDON and WRST bits are enabled when the TCSRWE bit is set to 1. When writing to this bit, 0 must be written to the B4WI bit.
3	B2WI	1	R/W	Bit 2 Write Disable Writing to the WDON is only enabled when 0 is written to the B2WI bit. This bit is always read as 1.
2	WDON	0	R/W	Watchdog Timer On The TDWD starts counting up when the WDON bit is set to 1 and stops counting when the WDON bit is cleared to 0. [Setting condition] • If 0 is written to the B2WI bit and 1 to the WDON bit while the TCSRWE bit is 1. • Reset [Clearing condition] • If 0 is written to the B2WI and WDON bits while the TCSRWE bit is 1.
1	B0WI	1	R/W	Bit 0 Write Disable Writing to the WRST bit is only enabled when 0 is written to the B0WI bit. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Setting condition] • When the TCWD overflows and an internal reset signal is generated. [Clearing condition] Reset by the $\overline{\text{RES}}$ pin • If 0 is written to both the BOWI and WRST bits while the TCSRWE bit is 1.

(3) Flowchart


main
SP = H'FF80
Initialize the stack pointer.
CCR I-bit = 1
Set the I bit in CCR to 1 to disable interrupts.
TCSRWD1 = H'9E
TCSRWD1 = H'A2
TCSRWD1 = H'8E
Clear the WDON bit of TCSRWD1 to stop the watchdog timer.
Initialization completed?
No
Yes
s_rcv[] = H'00
Initialize the buffer for storing received data. (Clear to all 0.)
PUCR90 = 1
Pull up the SCS pin.
SSU_spi_init()
Initialize the SSU in 4-line bus communication mode.
RE = 1
Select receive mode.
trs_cnt = 0
rcv_cnt = 0
error = 0
Initialize the RAM area to be used.
CCR I-bit = 0
Set the I bit in CCR to 0 to enable interrupts.
1


1
SSER = H'43
RE = 1, RIE = 1, CEIE = 1
RE = 1 ?
Yes
Continue reception?
No
error = 0 ?
Yes
Has an error occurred?
No
SSER = H'8D
TE = 1, TEIE = 1, TIE = 1, CEIE = 1
TE = 1 ?
Yes
Continue transmission?
No
CEIE = 0
Clear the CEIE bit to 0.
error = 1 ?
Yes
Has an error occurred?
No
CCR I-bit = 1
Set the I bit in CCR to 1 to disable interrupts.

4.4.2 SSU_spi_init() Function

(1) Module Specifications

Function: Initializes the SSU in SPI mode (4-line bus communication mode), and cancels module standby mode of the SSU.

Table 6 Module Specifications

Item	Type	Variable Name	Description
Argument	None	None	None

(2) Internal Registers

The internal registers used in this sample task are described below. The setting values in the tables below are used in this task and are different from the initial values.

- SS Control Register H (SSCRH) Address: H'F0E0

Bit	Bit Name	Setting	R/W	Function
7	MSS	0	R/W	Master/Slave Device Select Selects whether this module is used as a master device or a slave device. When this module is used as a master device, transfer clock is output from the SSCK pin. When the CE bit in SSSR is set, the MSS bit is automatically cleared. 0: Operates as a slave device.
6	BIDE	0	R/W	Bidirectional Mode Enable Selects whether two pins are used as the serial data input pin and serial data output pin each or only one pin is used in bi-directional mode. 0: Normal mode. Two pins are used separately for data input and output.
2	SCKS	1	R/W	SSCK Pin Select Selects whether the SSCK pin functions as a port pin or a serial clock pin. 1: Functions as a serial clock pin.
1	CSS1	0	R/W	$\overline{\text{SCS}}$ Pin Select
0	CSS0	1	R/W	Selects whether the $\overline{\text{SCS}}$ pin functions as a port pin or as an $\overline{\text{SCS}}$ input or $\overline{\text{SCS}}$ output pin. CSS1 = 0, CSS0 = 1: $\overline{\text{SCS}}$ pin functions as a port pin (P90).

- SS Control Register L (SSCRL) Address: H'F0E1

Bit	Bit Name	Setting	R/W	Function
6	SSUMS	1	R/W	SSU Mode Select Selects which combination of serial data input pin and serial data output pin is used. 1: 4-line bus communication mode When MSS = 0 and BIDE = 0 in SSCRH, data input: SSO pin, data output: SSI pin

- SS Mode Register (SSMR) Address: H'F0E2

Bit	Bit Name	Setting	R/W	Function
7	MLS	1	R/W	MSB-First/LSB-First Select Selects whether data transfer is performed in MSB-first or LSB-first. 1: MSB-first
2	CKS2	0	R/W	Transfer Clock Rate Select
1	CKS1	1	R/W	Sets transfer clock rate (prescaler division ratio) when the internal clock is selected. Table 7 shows the transfer rate. CKS2 = 0, CKS1 = 1, CKS0 = 1: ϕ/32
0	CKS0	1	R/W	

Table 7 Transfer Rate

Bit 2	Bit 1	Bit 0		Transfer Rate
CKS2	CKS1	CKS0	Clock	ϕ = 10 MHz
0	1	1	ϕ/32	312.5 kHz

- SS Enable Register (SSER) Address: H'F0E3

Bit	Bit Name	Setting	R/W	Function
7	TE	0	R/W	Transmit Enable When this bit is 1, transmit operation is enabled. 0: Disables transmit operation.
6	RE	0	R/W	Receive Enable When this bit is 1, receive operation is enabled. 0: Disables receive operation.

- SS Status Register (SSSR) Address: H'F0E4

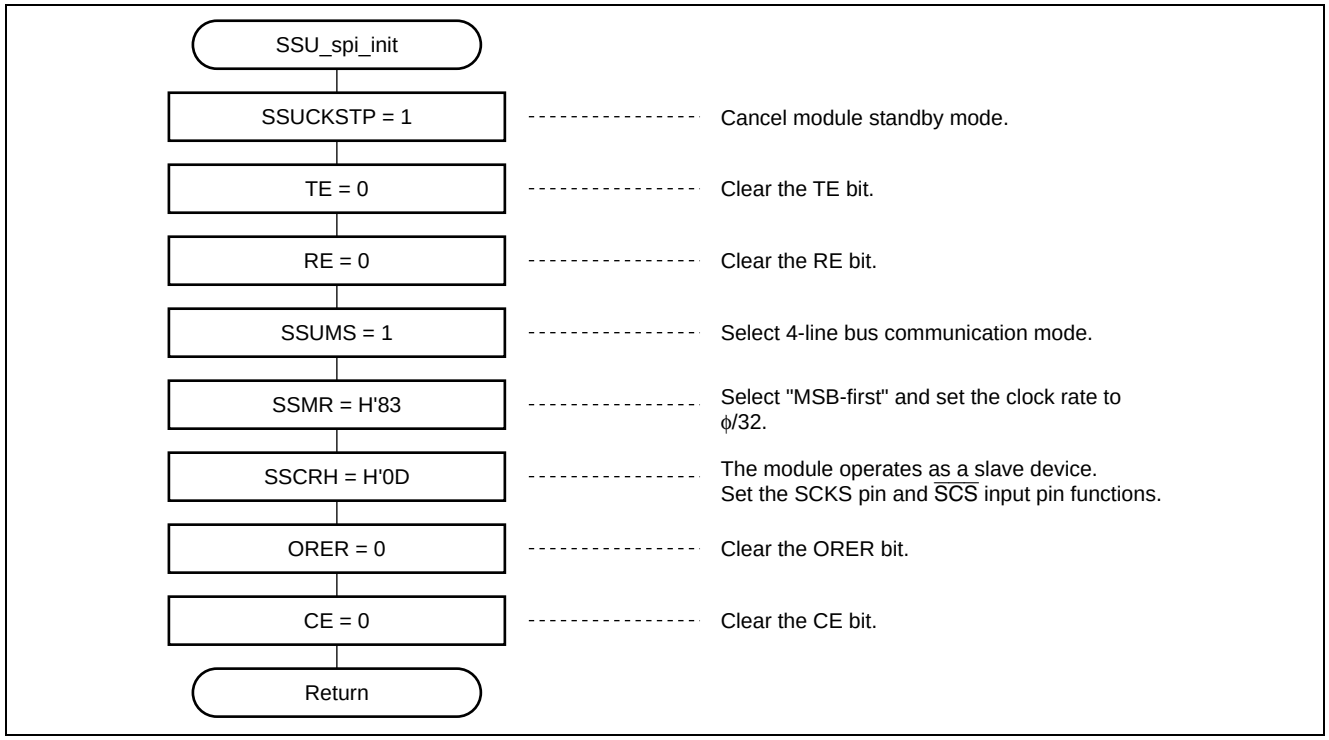
Bit	Bit Name	Setting	R/W	Function
6	ORER	0	R/(W)*	Overrun Error Flag Indicates that reception has ended abnormally because of an overrun error. SSRDR retains the data received before the overrun error occurs, and the data received after the overrun error will be lost. In addition, subsequent serial reception cannot be continued when this bit is 1. If the MSS bit in SSCRH is 1, serial transmission also cannot be continued. [Setting condition] • When the next serial reception is completed while RDRF = 1. [Clearing condition] • When 0 is written to this bit after reading 1.
0	CE	0	R/(W)*	Conflict Error Flag [Setting condition] • If the input on the $\overline{SCS}$ pin is low when serial communication is attempted to be started with SSUMS = 1 and MSS = 1. • When the $\overline{SCS}$ pin changes from low to high during serial communication with SSUMS = 1 and MSS = 0. [Clearing condition] • When 0 is written to this bit after reading 1.

Note: * Only 0 can be written to clear the flag.

- Clock Halt Register 2 (CKSTPR2) Address: H'FFFB

Bit	Bit Name	Setting	R/W	Function
4	SSUCKSTP	1	R/W	SSU Module Standby SSU enters module standby mode when this bit is cleared to 0. 1: Cancels SSU module standby mode.

(3) Flowchart


SSU_spi_init
SSUCKSTP = 1
Cancel module standby mode.
TE = 0
Clear the TE bit.
RE = 0
Clear the RE bit.
SSUMS = 1
Select 4-line bus communication mode.
SSMR = H'83
Select "MSB-first" and set the clock rate to ϕ/32.
SSCRH = H'0D
The module operates as a slave device.
Set the SCKS pin and SCS input pin functions.
ORER = 0
Clear the ORER bit.
CE = 0
Clear the CE bit.
Return

4.4.3 SSU_int() Function

(1) Module Specifications

Function: Performs the SSU interrupt processing.

Table 8 Module Specifications

Item	Type	Variable Name	Description
Argument	None	None	None

(2) Internal Registers

The internal registers used in this sample task are described below. The setting values in the tables below are used in this task and are different from the initial values.

- SS Enable Register (SSER) Address: H'F0E3

Bit	Bit Name	Setting	R/W	Function
7	TE	0	R/W	Transmit Enable Enables transmit operation when this bit is 1. 0: Disables transmit operation
6	RE	0	R/W	Receive Enable Enables receive operation when this bit is 1. 0: Disables receive operation
3	TEIE	0	R/W	Transmit End Interrupt Enable Enables TEI interrupt requests when this bit is set to 1. 0: Disables TEI interrupts.
2	TIE	0	R/W	Transmit Interrupt Enable Enables TXI interrupt requests when this bit is set to 1. 0: Disables TXI interrupts.
1	RIE	0	R/W	Receive Interrupt Enable Enables RXI and OEI interrupt requests when this bit is set to 1. 0: Disables RXI and OEI interrupts.
0	CEIE	0	R/W	Conflict Error Interrupt Enable Enables CEI interrupt requests when this bit is set to 1. 0: Disables CEI interrupts.

- SS Status Register (SSSR) Address: H'F0E4

Bit	Bit Name	Setting	R/W	Function
6	ORER	—	R/(W)*	Overrun Error Flag Indicates that reception has ended abnormally because of an overrun error. SSRDR retains the data received before the overrun error occurs, and the data received after the overrun error will be lost. In addition, subsequent serial reception cannot be continued when this bit is 1. If the MSS bit in SSCRH is 1, serial transmission also cannot be continued. [Setting condition] • When the next serial reception is completed while RDRF = 1. [Clearing condition] • When 0 is written to this bit after reading 1.
3	TEND	—	R/(W)*	Transmit end [Setting condition] • When the last bit of data is transmitted with the TDRE bit set to 1. [Clearing conditions] • 0 is written to this bit after reading 1. • Data is written to SSTDR.
2	TDRE	—	R/(W)*	Transmit Data Empty [Setting condition] • When the TE bit of SSER is 0. • When data is transferred from SSTDR to SSTRSR and SSTDR has become ready to be written to. [Clearing condition] • When 0 is written to this bit after reading 1 • When data is written to SSTDR
1	RDRF	—	R/(W)*	Receive Data Register Full [Setting condition] • When serial reception ended normally and received data has been transferred from SSTRSR to SSRDR. [Clearing condition] • When 0 is written to this bit after reading 1 • When data is read from SSRDR.
0	CE	—	R/(W)*	Conflict Error Flag [Setting condition] • If the input on the $\overline{SCS}$ pin is low when serial communication is attempted to be started with SSUMS = 1 and MSS = 1. • When the $\overline{SCS}$ pin changes from low to high during serial communication with SSUMS = 1 and MSS = 0. [Clearing condition] When 0 is written to this bit after reading 1.

Note: * Only 0 can be written to clear the flag.

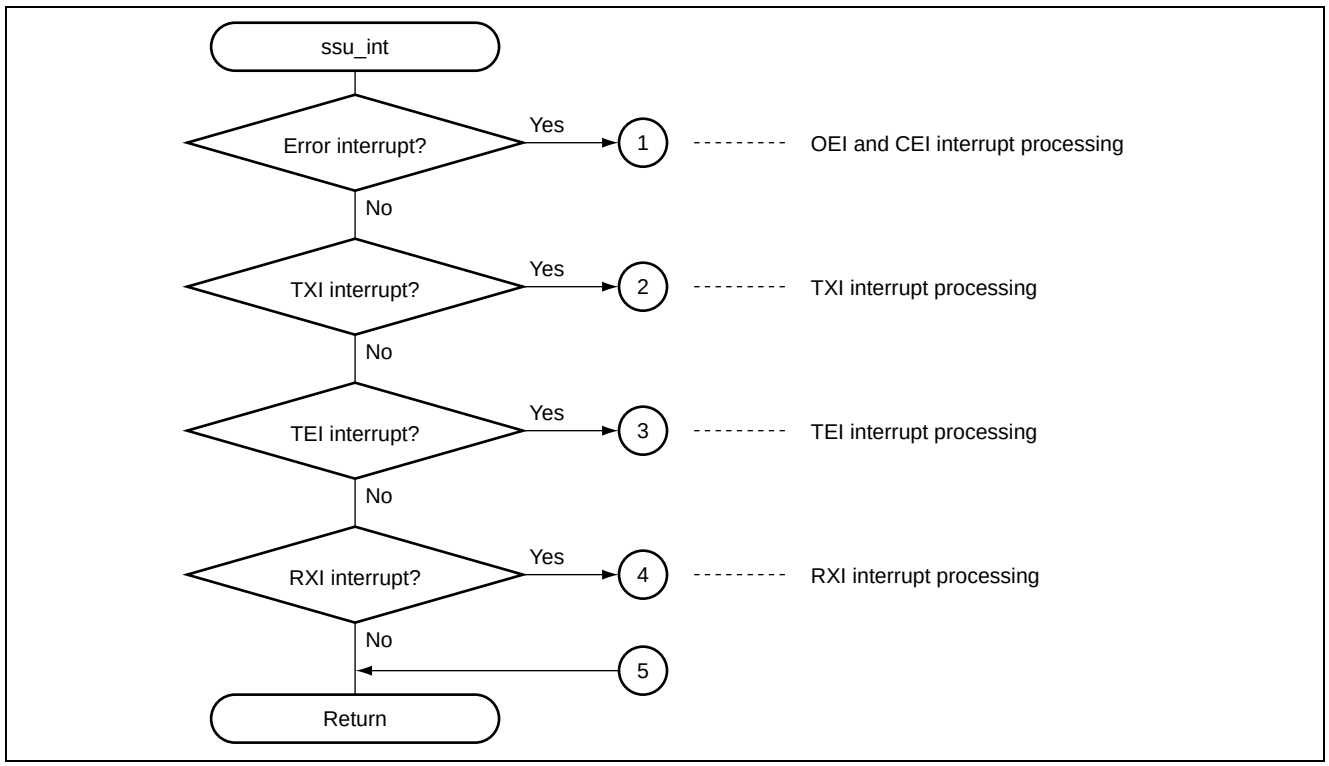
- SS Receive Data Register (SSRDR) Address: H'F0E9

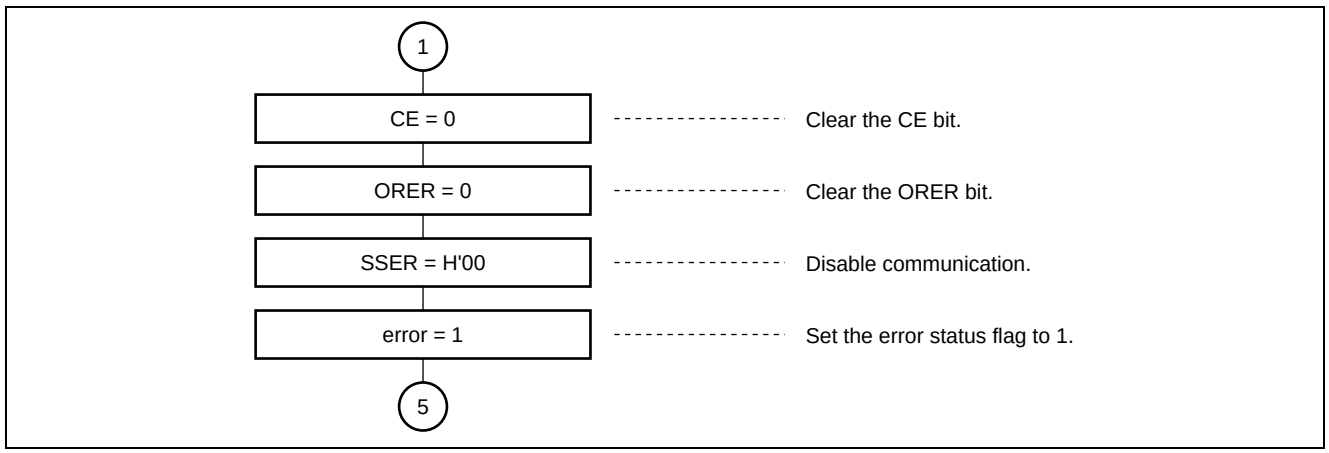
Bit	Bit Name	Setting	R/W	Function
7	bit7	—	R	SSRDR is an 8-bit register that stores received serial data. When the SSU has received one byte of serial data, it transfers the received serial data from SSTRSR to SSRDR. SSTRSR is then ready to receive the next data. This double-buffered configuration of SSTRSR and SSRDR allows continuous receive operation. SSRDR is a read-only register and cannot be written to by the CPU. The initial value of SSRDR is H'00.
6	bit6	—	R	
5	bit5	—	R	
4	bit4	—	R	
3	bit3	—	R	
2	bit2	—	R	
1	bit1	—	R	
0	bit0	—	R	

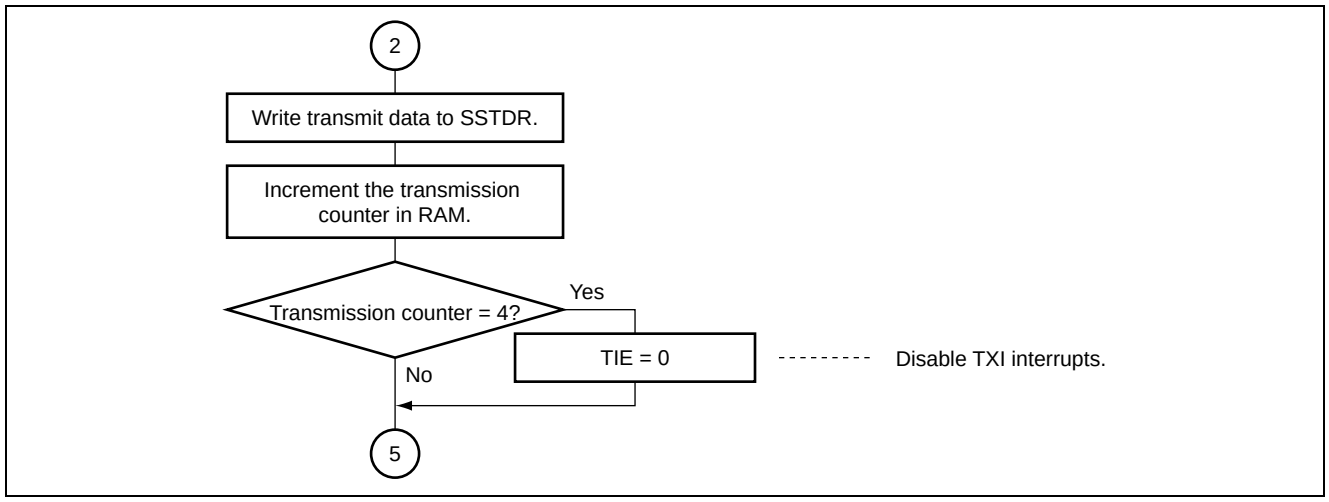
- SS Transmit Data Register (SSTDR) Address: H'F0EB

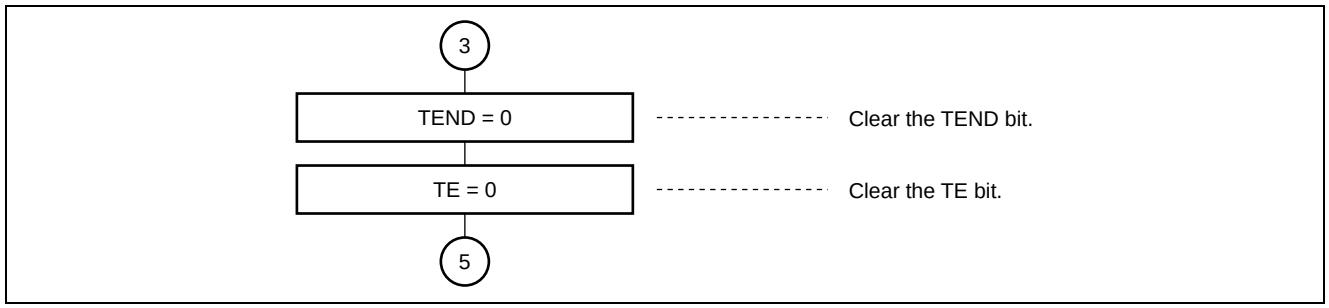
Bit	Bit Name	Setting	R/W	Function
7	bit7	—	R/W	SSTDR is an 8-bit register that stores serial data to be transmitted. SSTDR can be read from or written to by the CPU at any time. When the SSU detects that SSTRSR is empty, it transfers the transmit data stored in SSTDR to SSTRSR to start serial transmission. If the next transmit data has already been written to SSTDR during serial transmission, continuous serial transmission is possible. The initial value of SSTDR is H'00.
6	bit6	—	R/W	
5	bit5	—	R/W	
4	bit4	—	R/W	
3	bit3	—	R/W	
2	bit2	—	R/W	
1	bit1	—	R/W	
0	bit0	—	R/W	

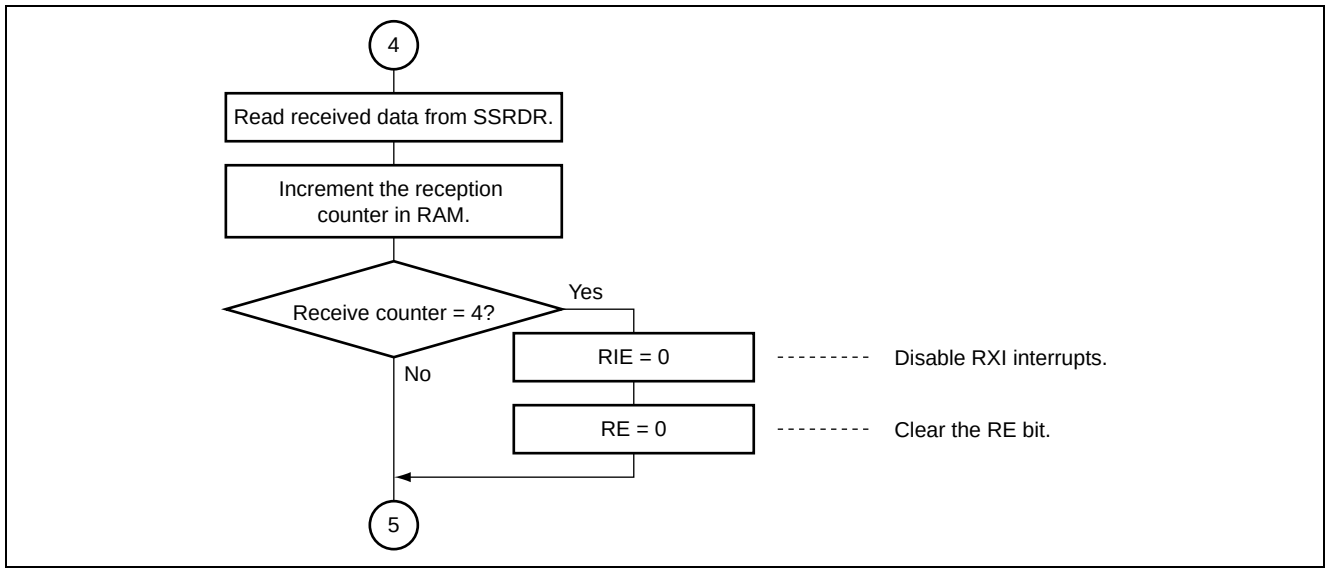
(3) Flowchart


ssu_int
Error interrupt?
Yes
1
OEI and CEI interrupt processing
No
TXI interrupt?
Yes
2
TXI interrupt processing
No
TEI interrupt?
Yes
3
TEI interrupt processing
No
RXI interrupt?
Yes
4
RXI interrupt processing
No
5
Return


1
CE = 0
Clear the CE bit.
ORER = 0
Clear the ORER bit.
SSER = H'00
Disable communication.
error = 1
Set the error status flag to 1.
5







4.5 Link Address Specification

Section Name	Address
CVECT	H'0000
P	H'0100
B	H'FB80

5. Description of Software (Master)

This sample task performs master communication by the SSU in 4-line bus communication mode (SPI mode), using SSU interrupts.

5.1 List of Functions

Table 9 Master Program Functions

Function Name	Description
main	Stops the watchdog timer, controls master communication and interrupts, and Initializes the RAM area for use.
SSU_spi_init	Initializes the SSU in SPI mode (4-line bus communication mode), and cancels module standby mode of the SSU.
ssu_int	SSU interrupt processing (TXI, TEI, RXI, OEI, CEI)

5.2 Constants

This sample task does not use constants.

5.3 RAM Usage

Table 10 describes the RAM usage in this sample task.

Table 10 Description of RAM

Label Name	Function	Data Length	Used In
m_trs[4]	Buffer for storing transmit data	4 bytes	main, ssu_int
m_rcv[4]	Buffer for storing received data	4 bytes	main, ssu_int
trs_cnt	Transmission counter used for checking the number of times transmission has been performed.	1 byte	main, ssu_int
rcv_cnt	Reception counter used for checking the number of times reception has been performed.	1 byte	main, ssu_int
error	Error status flag 0: No error occurred. 1: Error occurred.	1 byte	main, ssu_int

5.4 Description of Modules

5.4.1 main() Function

(1) Module Specifications

Function: Stops the watchdog timer, controls master communication and interrupts, and initializes the RAM area for use.

Table 11 Module Specifications

Item	Type	Variable Name	Description
Argument	None	None	None

(2) Internal Registers

The internal registers used in this sample task are described below. The setting values in the tables below are used in this task and are different from the initial values.

- SS Enable Register (SSER) Address: H'F0E3

Bit	Bit Name	Setting	R/W	Function
7	TE	1	R/W	Transmit enable Enables transmit operation when this bit is 1. 0: Disables transmit operation 1: Enables transmit operation
6	RE	1	R/W	Receive enable Enables receive operation when this bit is 1. 0: Disables receive operation 1: Enables receive operation
3	TEIE	1	R/W	Transmit End Interrupt Enable Enables TEI interrupt requests when this bit is set to 1. 1: Enables TEI interrupts.
2	TIE	1	R/W	Transmit Interrupt Enable Enables TXI interrupt requests when this bit is set to 1. 1: Enables TXI interrupts.
1	RIE	1	R/W	Receive Interrupt Enable Enables RXI and OEI interrupt requests when this bit is set to 1. 1: Enables RXI and OEI interrupts.
0	CEIE	1	R/W	Conflict Error Interrupt Enable Enables CEI interrupt requests when this bit is set to 1. 1: Enables CEI interrupts.

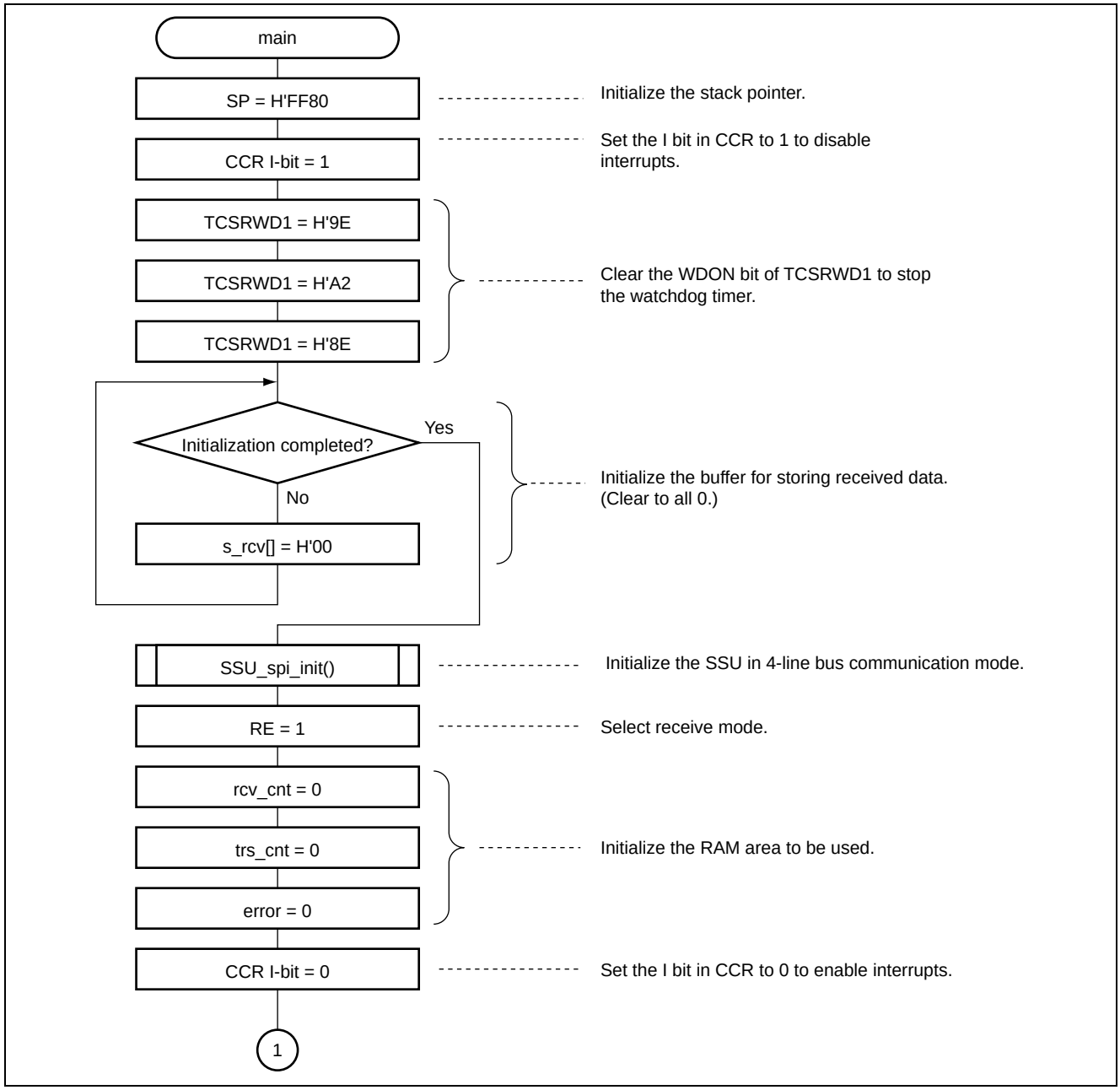
- SS Receive Data Register (SSRDR) Address: H'F0E9

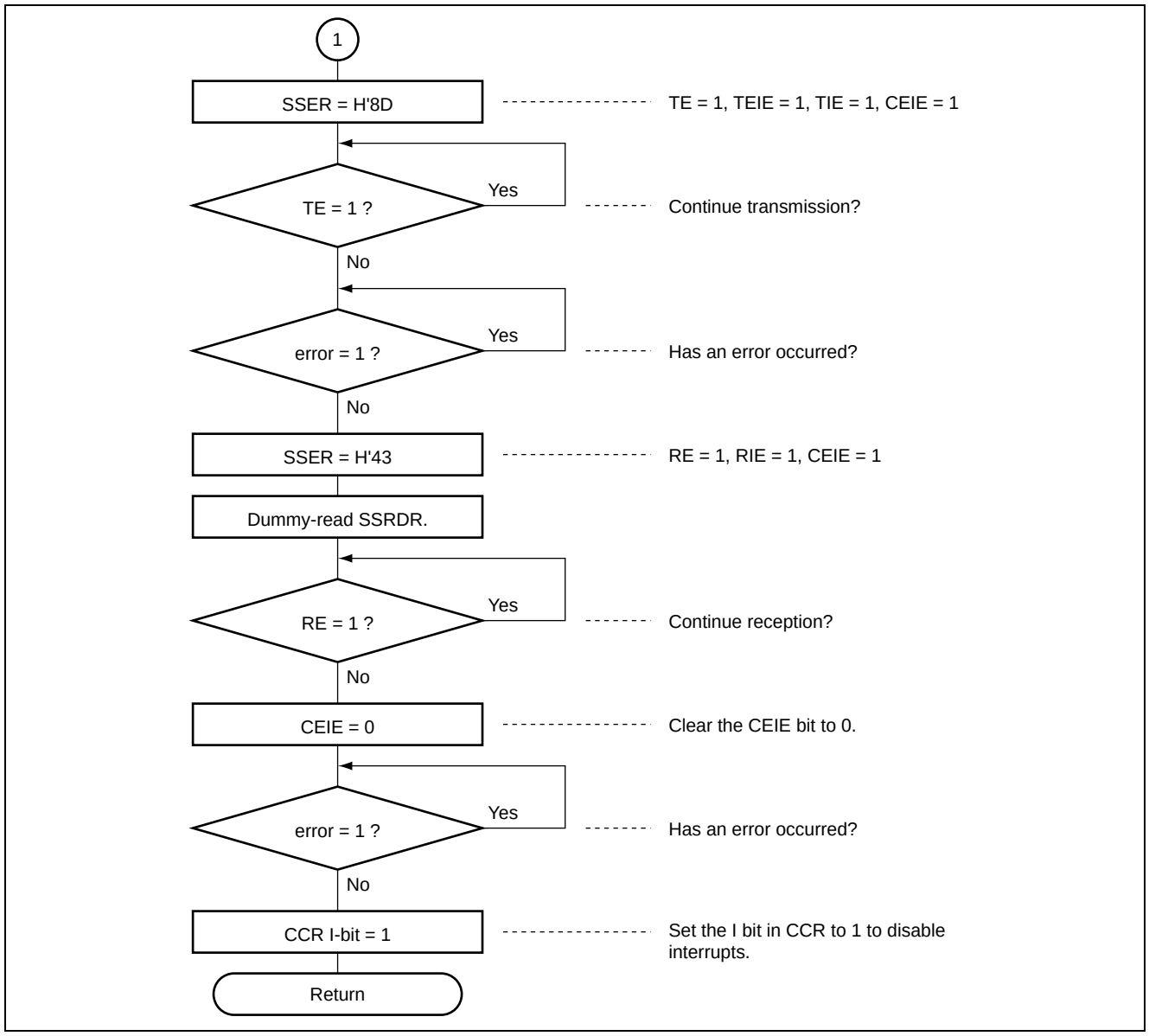
Bit	Bit Name	Setting	R/W	Function
7	bit7	—	R	SSRDR is an 8-bit register that stores received serial data. When the SSU has received one byte of serial data, it transfers the received serial data from SSTRSR to SSRDR. SSTRSR is then ready to receive the next data. This double-buffered configuration of SSTRSR and SSRDR allows continuous receive operation. SSRDR is a read-only register and cannot be written to by the CPU. The initial value of SSRDR is H'00.
6	bit6	—	R	
5	bit5	—	R	
4	bit4	—	R	
3	bit3	—	R	
2	bit2	—	R	
1	bit1	—	R	
0	bit0	—	R	

- Timer Control Register/Status Register WD1 (TCSRWD1) Address: H'FFB1

Bit	Bit Name	Setting	R/W	Function
7	B6WI	1	R/W	Bit 6 Write Disable Writing to the TCWE bit is only enabled when 0 is written to the B6WI bit. This bit is always read as 1.
6	TCWE	0	R/W	Timer Counter WD Write Enable Writing to the timer counter WD (TCWD) is enabled when the TCWE bit is set to 1. When writing to this bit, 0 must be written to the B6WI bit.
5	B4WI	1	R/W	Bit 4 Write Disable Writing to the TCSRWE bit is only enabled when 0 is written to the B4MI bit. The B4WI bit is always read as 1.
4	TCSRWE	0	R/W	Timer Control/Status Register WD1 Write Enable Writing to the WDON and WRST bits are enabled when the TCSRWE bit is set to 1. When writing to this bit, 0 must be written to the B4WI bit.
3	B2WI	1	R/W	Bit 2 Write Disable Writing to the WDON is only enabled when 0 is written to the B2WI bit. This bit is always read as 1.
2	WDON	0	R/W	Watchdog Timer On The TDWD starts counting up when the WDON bit is set to 1 and stops counting when the WDON bit is cleared to 0. [Setting condition] • If 0 is written to the B2WI bit and 1 to the WDON bit while the TCSRWE bit is 1. • Reset [Clearing condition] • If 0 is written to the B2WI and WDON bits while the TCSRWE bit is 1.
1	B0WI	1	R/W	Bit 0 Write Disable Writing to the WRST bit is only enabled when 0 is written to the B0WI bit. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Setting condition] • When the TCWD overflows and an internal reset signal is generated. [Clearing condition] Reset by the $\overline{\text{RES}}$ pin • If 0 is written to both the BOWI and WRST bits while the TCSRWE bit is 1.

(3) Flowchart


main
SP = H'FF80
Initialize the stack pointer.
CCR I-bit = 1
Set the I bit in CCR to 1 to disable interrupts.
TCSRWD1 = H'9E
TCSRWD1 = H'A2
TCSRWD1 = H'8E
Clear the WDON bit of TCSRWD1 to stop the watchdog timer.
Initialization completed?
Yes
No
s_rcv[] = H'00
Initialize the buffer for storing received data. (Clear to all 0.)
SSU_spi_init()
Initialize the SSU in 4-line bus communication mode.
RE = 1
Select receive mode.
rcv_cnt = 0
trs_cnt = 0
error = 0
Initialize the RAM area to be used.
CCR I-bit = 0
Set the I bit in CCR to 0 to enable interrupts.
1


1
SSER = H'8D
TE = 1, TEIE = 1, TIE = 1, CEIE = 1
TE = 1 ?
Yes
Continue transmission?
No
error = 1 ?
Yes
Has an error occurred?
No
SSER = H'43
RE = 1, RIE = 1, CEIE = 1
Dummy-read SSRDR.
RE = 1 ?
Yes
Continue reception?
No
CEIE = 0
Clear the CEIE bit to 0.
error = 1 ?
Yes
Has an error occurred?
No
CCR I-bit = 1
Set the I bit in CCR to 1 to disable interrupts.
Return

5.4.2 SSU_spi_init() Function

(1) Module Specifications

Function: Initializes the SSU in SPI mode (4-line bus communication mode), and cancels SSU module standby mode.

Table 12 Module Specifications

Item	Type	Variable Name	Description
Argument	None	None	None

(2) Internal Registers

The internal registers used in this sample task are described below. The setting values in the tables below are used in this task and are different from the initial values.

- SS Control Register H (SSCRH) Address: H'F0E0

Bit	Bit Name	Setting	R/W	Function
7	MSS	1	R/W	Master/Slave Device Select Selects whether this module is used as a master device or a slave device. When this module is used as a master device, transfer clock is output from the SSCK pin. When the CE bit in SSSR is set, the MSS bit is automatically cleared. 1: Operates as a master device
6	BIDE	0	R/W	Bidirectional Mode Enable Selects whether two pins are used as the serial data input pin and serial data output pin each or only one pin is used in bi-directional mode. 0: Normal mode. Two pins are used separately for data input and output.
2	SCKS	1	R/W	SSCK Pin Select Selects whether the SSCK pin functions as a port pin or a serial clock pin. 1: Functions as a serial clock pin.
1	CSS1	1	R/W	$\overline{\text{SCS}}$ Pin Select
0	CSS0	1	R/W	Selects whether the $\overline{\text{SCS}}$ pin functions as a port pin or as an $\overline{\text{SCS}}$ input or $\overline{\text{SCS}}$ output pin. CSS1 = 1, CSS0 = x: The $\overline{\text{SCS}}$ pin functions as an $\overline{\text{SCS}}$ output pin (however, functions as an $\overline{\text{SCS}}$ input before transfer is started).

[Legend] X: Don't care

- SS Control Register L (SSCRL) Address: H'F0E1

Bit	Bit Name	Setting	R/W	Function
6	SSUMS	1	R/W	SSU Mode Select Selects which combination of the serial data input pin and serial data output pin is used. 1: Four-line bus communication mode When MSS = 1 and BIDE = 0 in SSCRH, data input: SSI pin, data output: SSO pin.

- SS Mode Register (SSMR) Address: H'F0E2

Bit	Bit Name	Setting	R/W	Function
7	MLS	1	R/W	MSB-First/LSB-First Select Selects whether data transfer is performed in MSB-first or LSB-first. 1: MSB-first
2	CKS2	0	R/W	Transfer Clock Rate Select
1	CKS1	1	R/W	Sets transfer clock rate (prescaler division ratio) when the internal clock is selected. Table 13 shows the transfer rate.
0	CKS0	1	R/W	CKS2 = 0, CKS1 = 1, CKS0 = 1: ϕ/32

Table 13 Transfer Rate

Bit 2	Bit 1	Bit 0		Transfer Rate
CKS2	**CKS1**	**CKS0**	**Clock**	**ϕ = 10 MHz**
0	1	1	ϕ/32	312.5 kHz

- SS Enable Register (SSER) Address: H'F0E3

Bit	Bit Name	Setting	R/W	Function
7	TE	0	R/W	Transmit Enable When this bit is 1, transmit operation is enabled. 0: Disables transmit operation.
6	RE	0	R/W	Receive Enable When this bit is 1, receive operation is enabled. 0: Disables receive operation.

- SS Status Register (SSSR) Address: H'F0E4

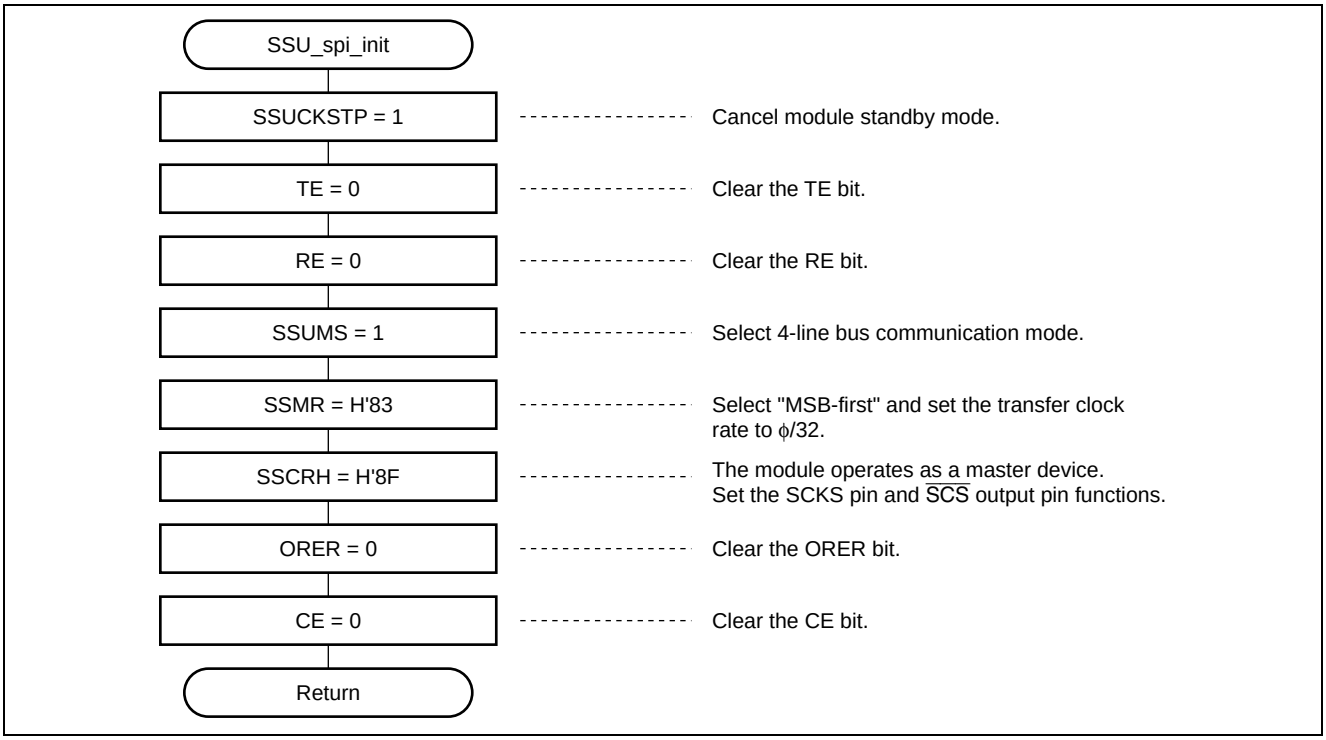
Bit	Bit Name	Setting	R/W	Function
6	ORER	0	R/(W)*	Overrun Error Flag Indicates that reception has ended abnormally because of an overrun error. SSRDR retains the data received before the overrun error occurs, and the data received after the overrun error will be lost. In addition, subsequent serial reception cannot be continued when this bit is 1. If the MSS bit in SSCRH is 1, serial transmission also cannot be continued. [Setting condition] • When the next serial reception is completed while RDRF = 1. [Clearing condition] • When 0 is written to this bit after reading 1.
0	CE	0	R/(W)*	Conflict Error Flag [Setting condition] • If the input on the $\overline{SCS}$ pin is low when serial communication is attempted to be started with SSUMS = 1 and MSS = 1. • When the $\overline{SCS}$ pin changes from low to high during serial communication with SSUMS = 1 and MSS = 0. [Clearing condition] • When 0 is written to this bit after reading 1.

Note: * Only 0 can be written to clear the flag.

- Clock Halt Register (CKSTPR2) Address: H'FFFB

Bit	Bit Name	Setting	R/W	Function
4	SSUCKSTP	1	R/W	SSU Module Standby SSU enters module standby mode when this bit is cleared to 0. 1: Cancels SSU module standby mode.

(3) Flowchart


SSU_spi_init
SSUCKSTP = 1
Cancel module standby mode.
TE = 0
Clear the TE bit.
RE = 0
Clear the RE bit.
SSUMS = 1
Select 4-line bus communication mode.
SSMR = H'83
Select "MSB-first" and set the transfer clock rate to ϕ/32.
SSCRH = H'8F
The module operates as a master device.
Set the SCKS pin and SCS output pin functions.
ORER = 0
Clear the ORER bit.
CE = 0
Clear the CE bit.
Return

5.4.3 SSU_int() Function

(1) Module Specifications

Function: Performs the SSU interrupt processing.

Table 14 Module Specifications

Item	Type	Variable Name	Description
Argument	None	None	None

(2) Internal Registers

The internal registers used in this sample task are described below. The setting values in the tables below are used in this task and are different from the initial values.

- SS Enable Register (SSER) Address: H'F0E3

Bit	Bit Name	Setting	R/W	Function
7	TE	0	R/W	Transmit Enable Enables transmit operation when this bit is 1. 0: Disables transmit operation
6	RE	0	R/W	Receive Enable Enables receive operation when this bit is 1. 0: Disables receive operation
3	TEIE	0	R/W	Transmit End Interrupt Enable Enables TEI interrupt requests when this bit is set to 1. 0: Disables TEI interrupts.
2	TIE	0	R/W	Transmit Interrupt Enable Enables TXI interrupt requests when this bit is set to 1. 0: Disables TXI interrupts.
1	RIE	0	R/W	Receive Interrupt Enable Enables RXI and OEI interrupt requests when this bit is set to 1. 0: Disables RXI and OEI interrupts.
0	CEIE	0	R/W	Conflict Error Interrupt Enable Enables CEI interrupt requests when this bit is set to 1. 0: Disables CEI interrupts.

- SS Status Register (SSSR) Address: H'F0E4

Bit	Bit Name	Setting	R/W	Function
6	ORER	—	R/(W)*	Overrun Error Flag Indicates that reception has ended abnormally because of an overrun error. SSRDR retains the data received before the overrun error occurs, and the data received after the overrun error will be lost. In addition, subsequent serial reception cannot be continued when this bit is 1. If the MSS bit in SSCRH is 1, serial transmission also cannot be continued. [Setting condition] • When the next serial reception is completed while RDRF = 1. [Clearing condition] • When 0 is written to this bit after reading 1.
3	TEND	—	R/(W)*	Transmit end [Setting condition] • When the last bit of data is transmitted with the TDRE bit set to 1. [Clearing conditions] • 0 is written to this bit after reading 1. • Data is written to SSTDR.
2	TDRE	—	R/(W)*	Transmit Data Empty [Setting condition] • When the TE bit of SSER is 0. • When data is transferred from SSTDR to SSTRSR and SSTDR has become ready to be written to. [Clearing condition] • When 0 is written to this bit after reading 1 • When data is written to SSTDR
1	RDRF	—	R/(W)*	Receive Data Register Full [Setting condition] • When serial reception ended normally and received data has been transferred from SSTRSR to SSRDR. [Clearing condition] • When 0 is written to this bit after reading 1 • When data is read from SSRDR.
0	CE	—	R/(W)*	Conflict Error Flag [Setting condition] • If the input on the $\overline{SCS}$ pin is low when serial communication is attempted to be started with SSUMS = 1 and MSS = 1. • When the $\overline{SCS}$ pin changes from low to high during serial communication with SSUMS = 1 and MSS = 0. [Clearing condition] When 0 is written to this bit after reading 1.

Note: * Only 0 can be written to clear the flag.

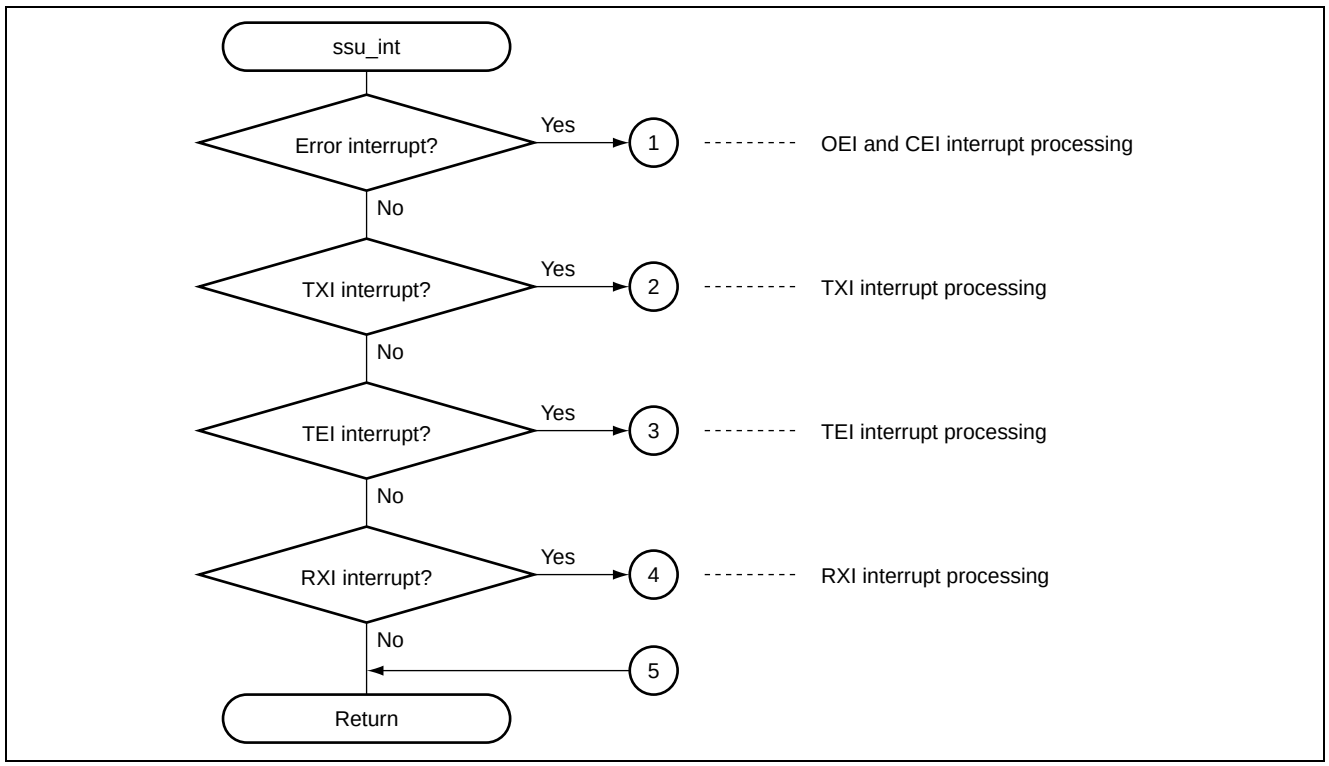
- SS Receive Data Register (SSRDR) Address: H'F0E9

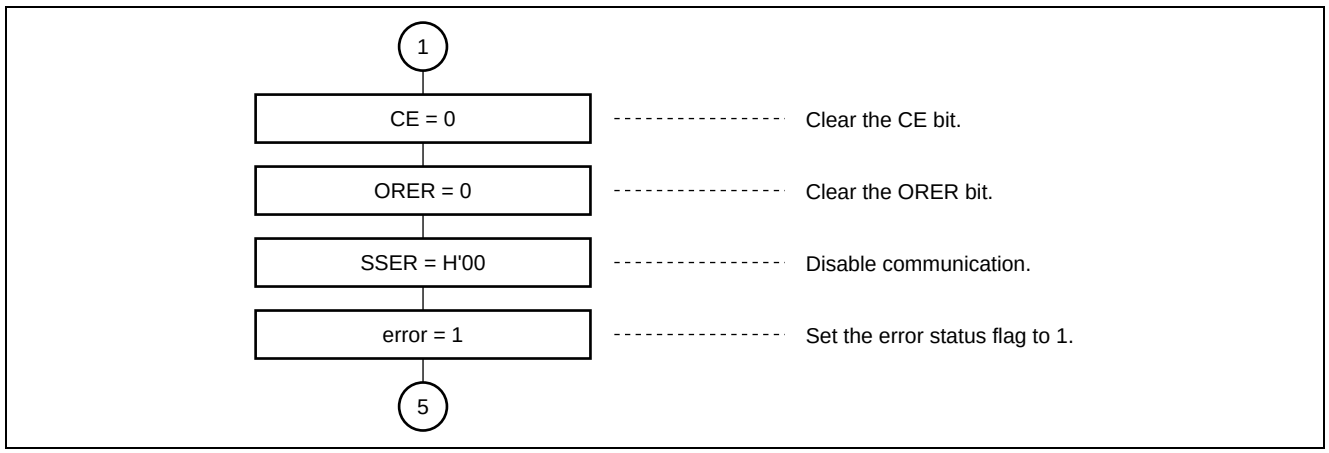
Bit	Bit Name	Setting	R/W	Function
7	bit7	—	R	SSRDR is an 8-bit register that stores received serial data. When the SSU has received one byte of serial data, it transfers the received serial data from SSTRSR to SSRDR. SSTRSR is then ready to receive the next data. This double-buffered configuration of SSTRSR and SSRDR allows continuous receive operation. SSRDR is a read-only register and cannot be written to by the CPU. The initial value of SSRDR is H'00.
6	bit6	—	R	
5	bit5	—	R	
4	bit4	—	R	
3	bit3	—	R	
2	bit2	—	R	
1	bit1	—	R	
0	bit0	—	R	

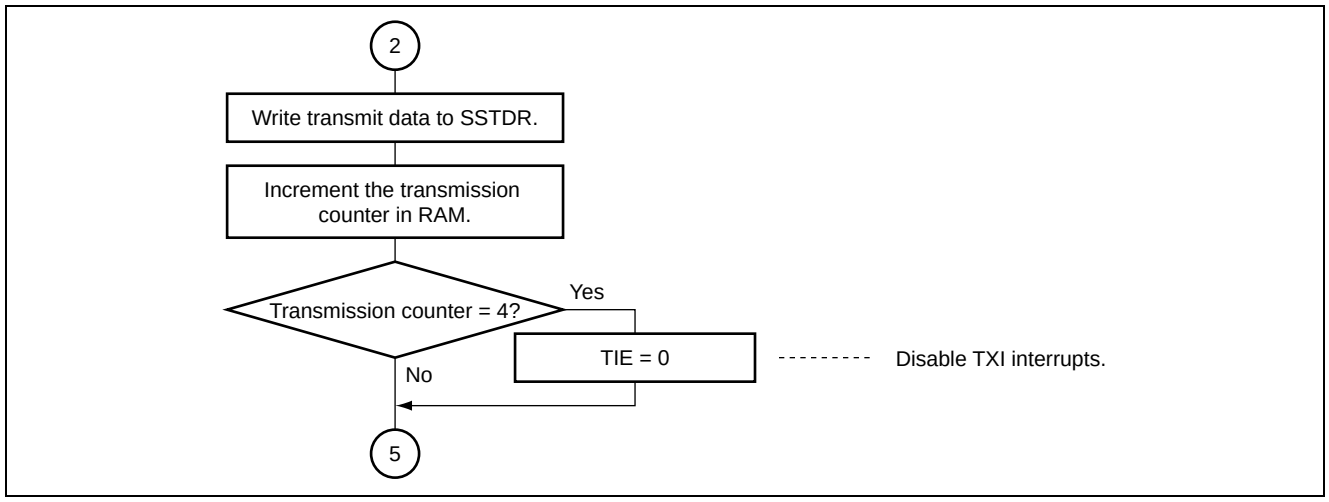
- SS Transmit Data Register (SSTDR) Address: H'F0EB

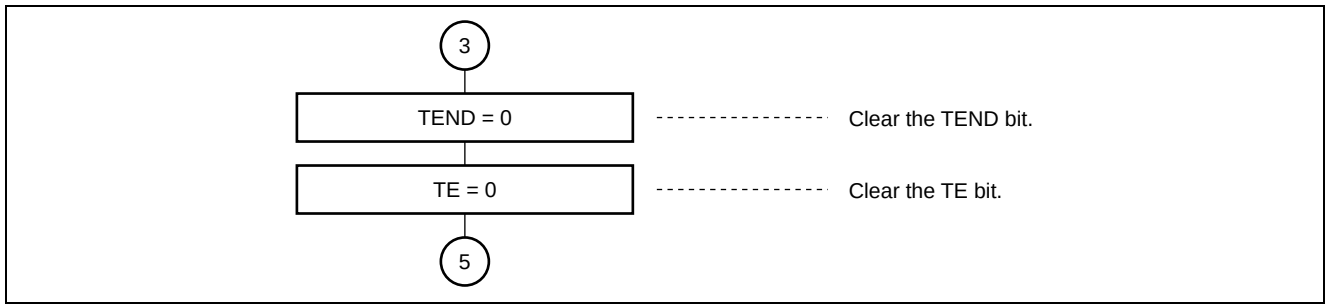
Bit	Bit Name	Setting	R/W	Function
7	bit7	—	R/W	SSTDR is an 8-bit register that stores serial data to be transmitted. SSTDR can be read from or written to by the CPU at any time. When the SSU detects that SSTRSR is empty, it transfers the transmit data stored in SSTDR to SSTRSR to start serial transmission. If the next transmit data has already been written to SSTDR during serial transmission, continuous serial transmission is possible. The initial value of SSTDR is H'00.
6	bit6	—	R/W	
5	bit5	—	R/W	
4	bit4	—	R/W	
3	bit3	—	R/W	
2	bit2	—	R/W	
1	bit1	—	R/W	
0	bit0	—	R/W	

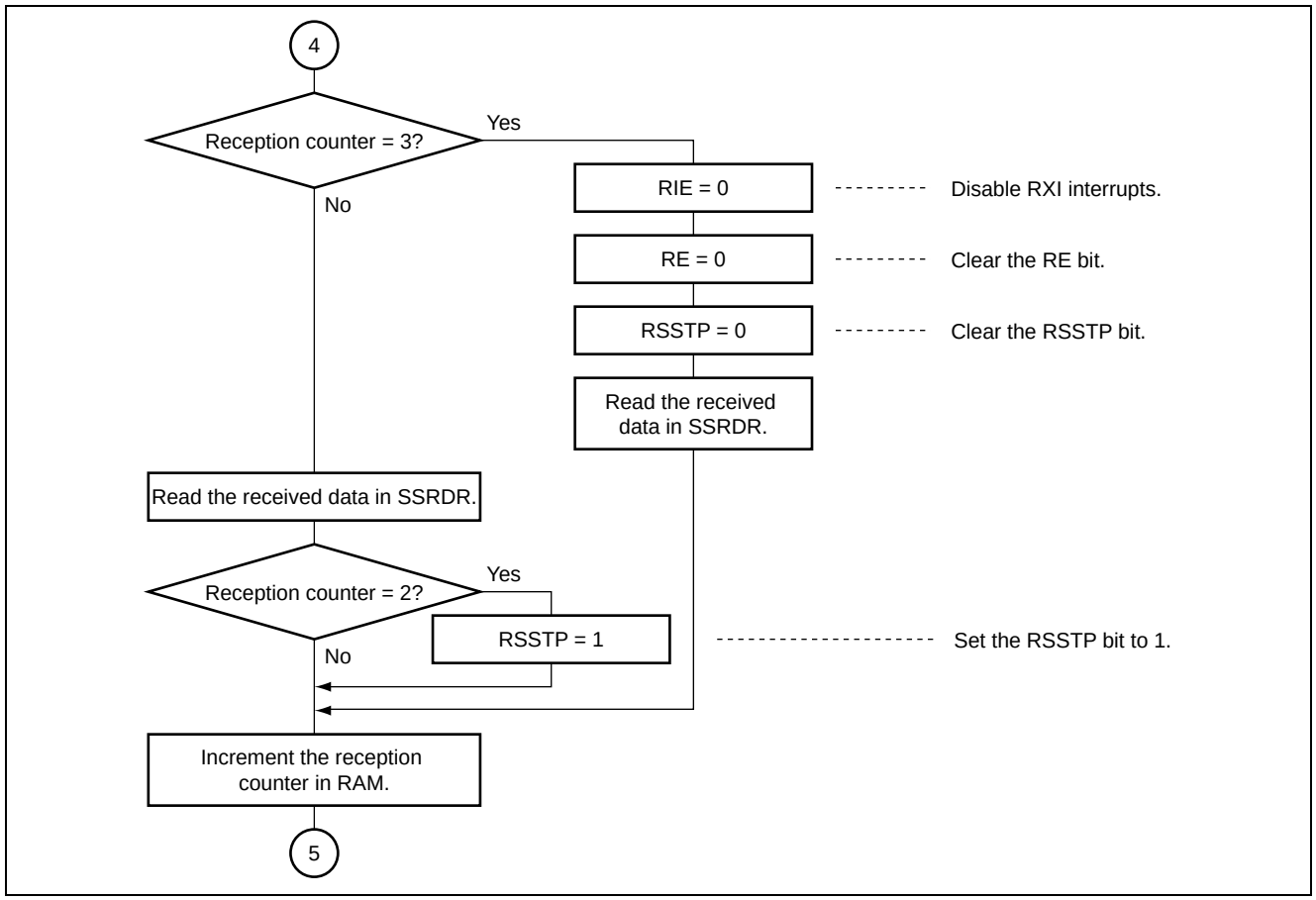
(3) Flowchart


ssu_int
Error interrupt?
Yes
1
OEI and CEI interrupt processing
No
TXI interrupt?
Yes
2
TXI interrupt processing
No
TEI interrupt?
Yes
3
TEI interrupt processing
No
RXI interrupt?
Yes
4
RXI interrupt processing
No
5
Return


1
CE = 0
Clear the CE bit.
ORER = 0
Clear the ORER bit.
SSER = H'00
Disable communication.
error = 1
Set the error status flag to 1.
5


2
Write transmit data to SSTDR.
Increment the transmission counter in RAM.
Transmission counter = 4?
Yes
No
TIE = 0
Disable TXI interrupts.
5


3
TEND = 0
Clear the TEND bit.
TE = 0
Clear the TE bit.
5



5.5 Link Address Specification

Section Name	Address
CVECT	H'0000
P	H'0100
D,B	H'FB80

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Mar.18.05	—	First edition issued

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