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H8/38076R

Watchdog Timer Operation Using Internal Oscillator

Introduction

The watchdog timer is operated using the internal oscillator.

Target Device

H8/38076R

Contents

1. Specifications

- An internal reset is generated when the timer counter WD (TCWD) of the watchdog timer overflows.
- During normal operation TCWD is reset before it overflows. In this sample task TCWD is reset while performing the job of repeatedly turning an LED connected to pin P93 in port 9 on and off at a set interval.
- If the timing of the TCWD reset is too late to anticipate the overflow an internal reset is generated. In this sample task an internal reset is generated deliberately by turning on a switch connected to the $\overline{\text{IRQ0}}$ input pin that extends the job cycle duration.
- In this sample task operation following an internal reset is distinguished from operation following a reset triggered by the $\overline{\text{RES}}$ pin by changing the interval at which the LED flashes.
- A sample connection diagram is shown in figure 1.

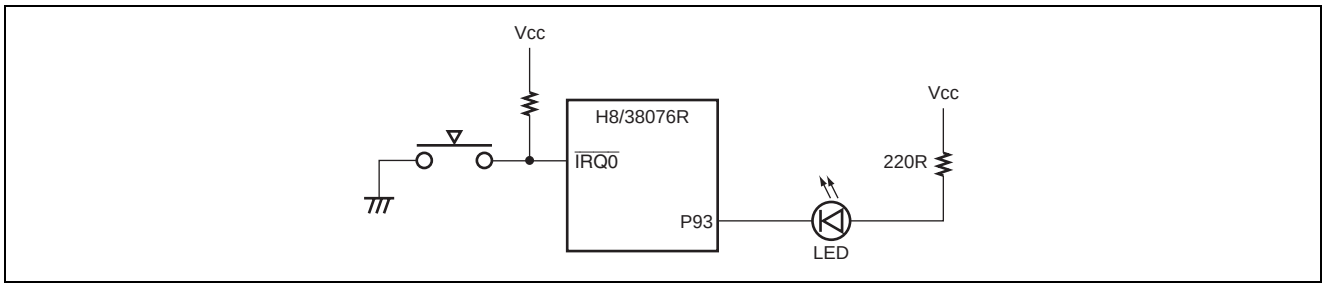


Figure 1 Connection Diagram

2. Description of Functions

2.1 Functions Used

In this sample task the watchdog timer is operated using the internal oscillator. A block diagram of the watchdog timer is shown in figure 2. The watchdog timer function is described below.

1. Watchdog Timer Function
   This LSI incorporates the watchdog timer (WDT). The WDT is an 8-bit timer that can generate an internal reset signal if a system becomes uncontrolled and prevents the CPU from writing to the timer counter, allowing it to overflow.
   When this watchdog timer function is not needed, the WDT can be used as an interval timer. In interval timer operation, an interval timer interrupt is generated each time the counter overflows.

- Timer control/status register WD1 (TCSRWD1)
  TCSRWD1 performs TCSRWD1 and TCWD write control. TCSRWD1 also controls the watchdog timer operation and indicates the operating state. TCSRWD1 must be rewritten by using the MOV instruction. Bit manipulation instructions cannot be used to change its setting values. In this sample task TCSRWD1 controls the enabling/disabling of write operations to various registers, depending on conditions, and controls the start of count-up operation by the counter.
- Timer control/status register WD2 (TCSRWD2)
  TCSRWD2 performs TCSRWD2 write control, mode switching, and interrupt control. TCSRWD2 must be rewritten by using the MOV instruction. Bit manipulation instructions cannot be used to change its setting values. In this sample task TCSRWD2 is used to select watchdog timer mode operation.
- Timer counter WD (TCWD)
  Timer counter WD is an 8-bit readable/writable up-counter. When TCWD overflows from H'FF to H'00 in the watchdog timer mode, an internal reset signal is generated and the WRST bit in TCSRWD1 is set to 1. The initial value of TCWD is H'00. In this sample task TCWD is reset at regular intervals before overflow occurs.
- Timer mode register WD (TMWD)
  TMWD selects the input clock. In this sample task the internal oscillator is selected as the input clock and ϕ/2,048 is used as the division setting.

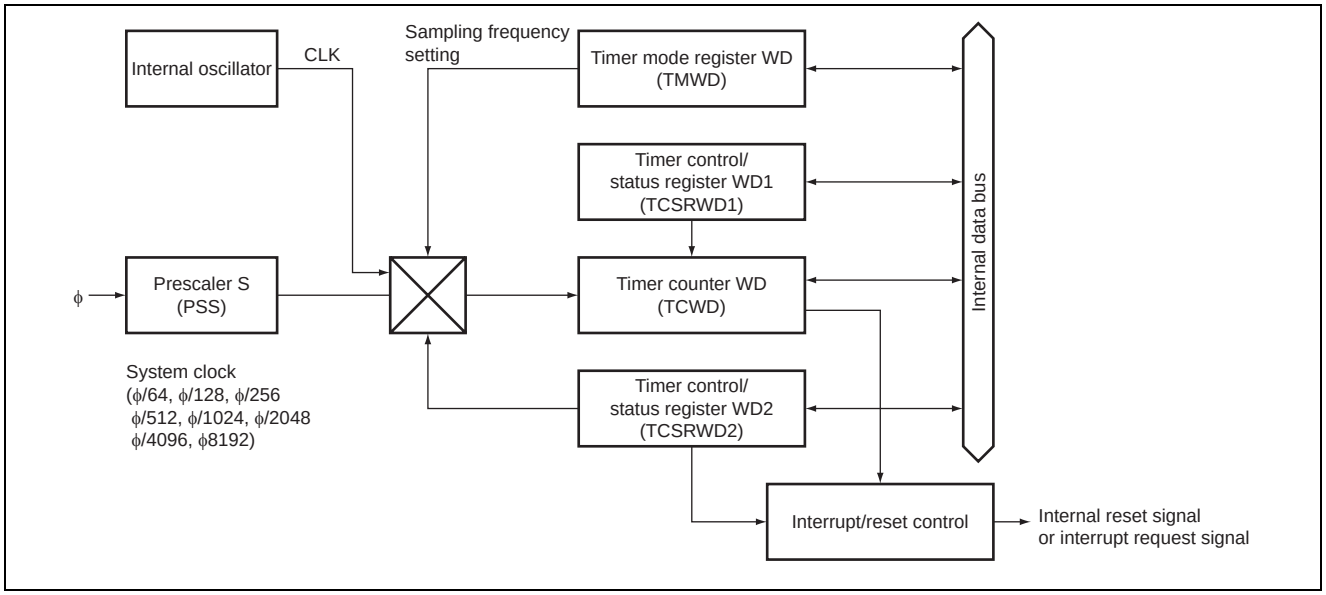


Figure 2 Block Diagram of Watchdog Timer

2. Watchdog Timer Operation

The watchdog timer is provided with an 8-bit up-counter. To use the counter as a watchdog timer clear the WT/$\overline{IT}$ bit in TCSRWD2 to 0. (Two write accesses are required to write to the WT/$\overline{IT}$ bit.) If 1 is written to the WDON bit and 0 to the B2WI bit simultaneously when the TCSRWE bit in TCSRWD1 is set to 1, TCWD starts counting up. (Two write accesses to TCSRWD1 are required to operate the watchdog timer.) When the TCWD counter value overflows from H'FF an internal reset signal is generated. The internal reset signal is output for a period of 512 ϕosc clock cycles. TCWD is a writable counter, and when a value is set in TCWD the count-up starts from that value. An overflow period in the range of 1 to 256 input clock cycles can therefore be set according to the TCWD set value. An example of how to calculate the overflow period is shown below.

System clock ϕ: 10 MHz
Division: ϕ/2048
TCWD set value: H'00

$$\text{TCWD overflow period} = \frac{1}{\text{System clock } \phi/2{,}048} \times (256 - \text{TCWD set value})$$

$$= 0.2048 \text{ ms} \times (256 - 0)$$
$$= 52.4 \text{ ms}$$

3. Usage Note

- Switching between the watchdog timer mode and the interval timer mode
  If the mode is switched between the watchdog timer mode and the interval timer mode while WDT is operating, Errors could occur. Always halt the WDT (by clearing the WDON bit to 0) before switching the timer mode.

4. Port 9

Port 9 is a general I/O port with pins that function as both external interrupt input pins and PWM output pins.

- Port data register 9 (PDR9)
  PDR9 is an 8-bit register that stores data for pins P93 to P90 of port 9. If port 9 is read, the values stored in PDR9 are read directly, regardless of the actual pin states.
- Port control register 9 (PCR9)
  PCR9 selects inputs/outputs in bit units for pins to be used as I/O ports of port 9.Setting a PCR9 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the corresponding pin an input pin. The settings in PCR9 and in PDR9 are valid when the corresponding pins are set as I/O ports of port 9. PCR9 is a write-only register. These bits are always read as 1.
- Port mode register 9 (PMR9)
  PMR9 controls the selection of functions for port 9 pins.

5. Port B

Port B is an input-only port with pins that function as both interrupt input pins and analog input pins.

- Port mode register B (PMRB)
  PMRB controls the selection of functions for port B pins. In this sample task it is used as the $\overline{IRQ0}$ input pin function.

6. Interrupt Controller

The device's interrupt controller controls the following interrupts.

- Interrupt edge select register (IEGR)
  IEGR selects the sense of an edge that generates interrupt request of the $\overline{\text{IRQ0}}$ pin.
- Interrupt enable register 1 (IENR1)
  IENR1 enables the $\overline{\text{IRQ0}}$ interrupt.
- Interrupt request register 1 (IRR1)
  IRR1 indicates the $\overline{\text{IRQ0}}$ interrupt request status.

2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. The watchdog timer is operated using functions assigned as shown in table 1.

Table 1 Assignment of Functions

Elements	Description
TCSRWD1	Starts the WDT, controls enabling of writing initial and reset values to TCWD
TCRWD2	Sets the watchdog timer mode
TCWD	Writes initial and reset values for up-counter and overflow interval
TMWD	Selects the input clock
PDR9	Stores output data for P93
PCR9	Sets P93 as an output pin
P93	Connected to an external LED, which flashes to show the program's operating status. Changes flash interval when internal reset is generated by overflow
PMRB	Sets PB0/AN0/$\overline{\text{IRQ}}$ pin to $\overline{\text{IRQ}}$ input pin function
$\overline{\text{IRQ0}}$	Connected to an external switch. The main routine processing time is lengthened when the switch is turned on, causing the watchdog timer to overflow
IEGR	Detects the falling edge of the $\overline{\text{IRQ}}$ pin input signal
IENR1	Enables $\overline{\text{IRQ0}}$ interrupt requests
IRR1	$\overline{\text{IRQ0}}$ interrupt request flag

3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 3. Using the hardware and software processing shown in figure 3 the internal oscillator is used to operate the watchdog timer.

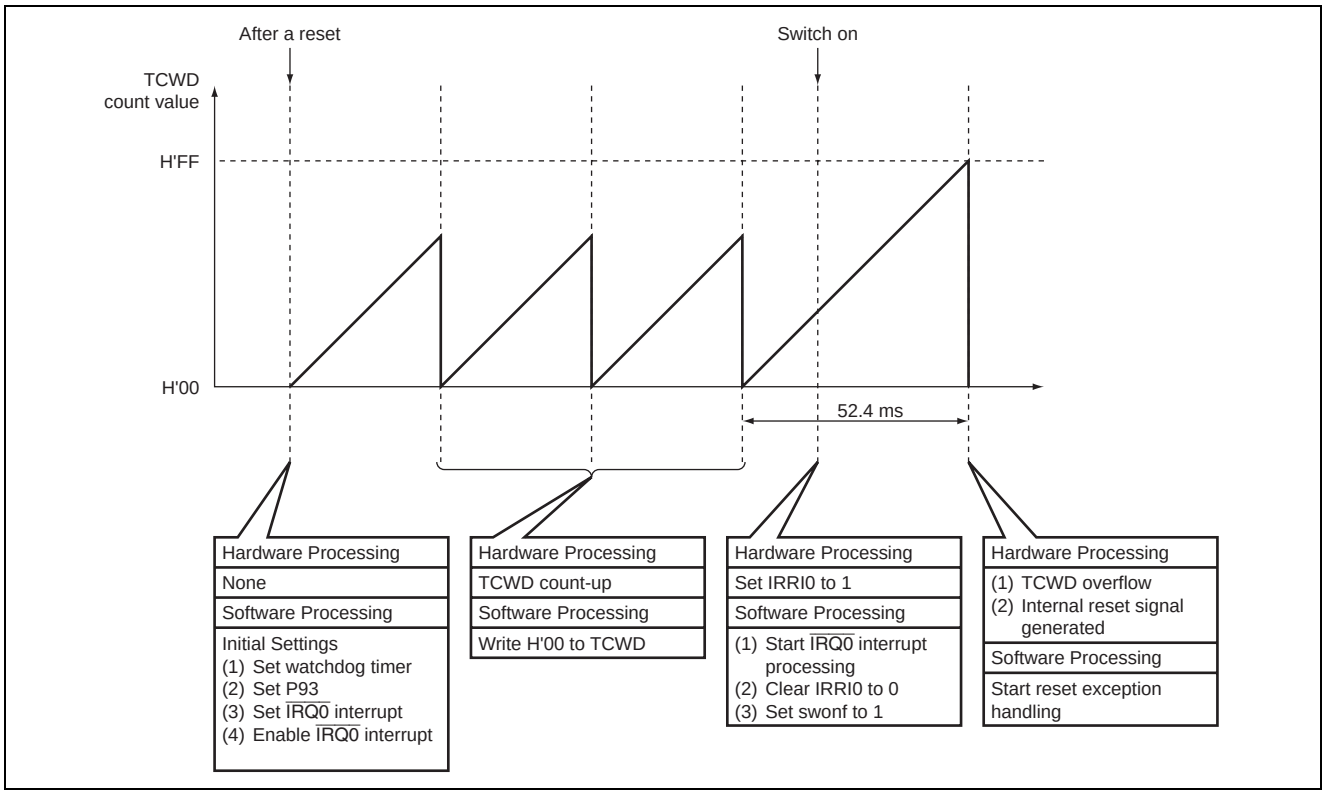


Figure 3 Principles of Operation of Watchdog Timer

3.1 Interrupt Source

$\overline{\text{IRQ0}}$ interrupt is requested by an input signal at $\overline{\text{IRQ0}}$ pin.

Whether $\overline{\text{IRQ0}}$ is triggered by sensing the rising or falling edge of the input signal can be specified using IEG0 in IEGR.

When the specified edge is input when $\overline{\text{IRQ0}}$ pin function is selected by PMRB, the corresponding bit to IRR1 is set to 1 and an interrupt request is generated.

Clearing the IEN0 pin in IENR1 to 0 disables the interrupt request to be accepted.

Furthermore, setting the I bit in CCR to 1 masks all interrupts.

4. Description of Software

4.1 Functions

Table 2 shows the functions used in this sample task.

Table 2 List of Functions

Function Name	Description
main	Performs initial settings of P93 and $\overline{\text{IRQ0}}$ pin, sets $\overline{\text{IRQ0}}$ interrupt, processes LED flashing
init_wdt	Performs initial setting of WDT, sets TCWD, and starts WDT count
reinit_wdt	Resets TCWD
int_irq0	Processes $\overline{\text{IRQ0}}$ interrupt

4.2 Constants

No constants are used in this sample task.

4.3 RAM Usage

No RAM is used in this sample task.

4.4 Modules

4.4.1 main() Function

1. Module Specifications

- Initial settings of P93and $\overline{\text{IRQ0}}$ pin, $\overline{\text{IRQ0}}$ interrupt setting, and processing of LED flashing

Table 3 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- PDR9 Port Data Register 9 Address: H'FFDC

Bit	Bit Name	Set Value	R/W	Description
3	P93	0	R/W	If port 9 is read while PCR9 is set to 1 the corresponding value stored in PDR9 is read directly, regardless of the actual pin state. If port 9 is read while PCR9 is cleared to 0 the corresponding pin state is read.

- PCR9 Port Control Register 9 Address: H'FFEC

Bit	Bit Name	Set Value	R/W	Description
3	PCR93	1	W	Setting a PCR9 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCR9 and in PDR9 are valid when the corresponding pin is designated as a general I/O pin. PCR9 is a write-only register. These bits are always read as 1. 1: Output pin

- PMRB Port Mode Register B Address: H'FFCA

Bit	Bit Name	Set Value	R/W	Description
0	IRQ0	1	R/W	PB0/AN0/$\overline{\text{IRQ0}}$ pin function switch Selects whether pin PB0/AN0/$\overline{\text{IRQ0}}$ is used as PB0/AN0 or as $\overline{\text{IRQ0}}$. 1: Functions as $\overline{\text{IRQ0}}$ input pin

- IEGR Interrupt Edge Select Register Address: H'FFF2

Bit	Bit Name	Set Value	R/W	Description
0	IEG0	0	R/W	$\overline{\text{IRQ0}}$ edge select 0: Detects the falling edge of the $\overline{\text{IRQ0}}$ pin input

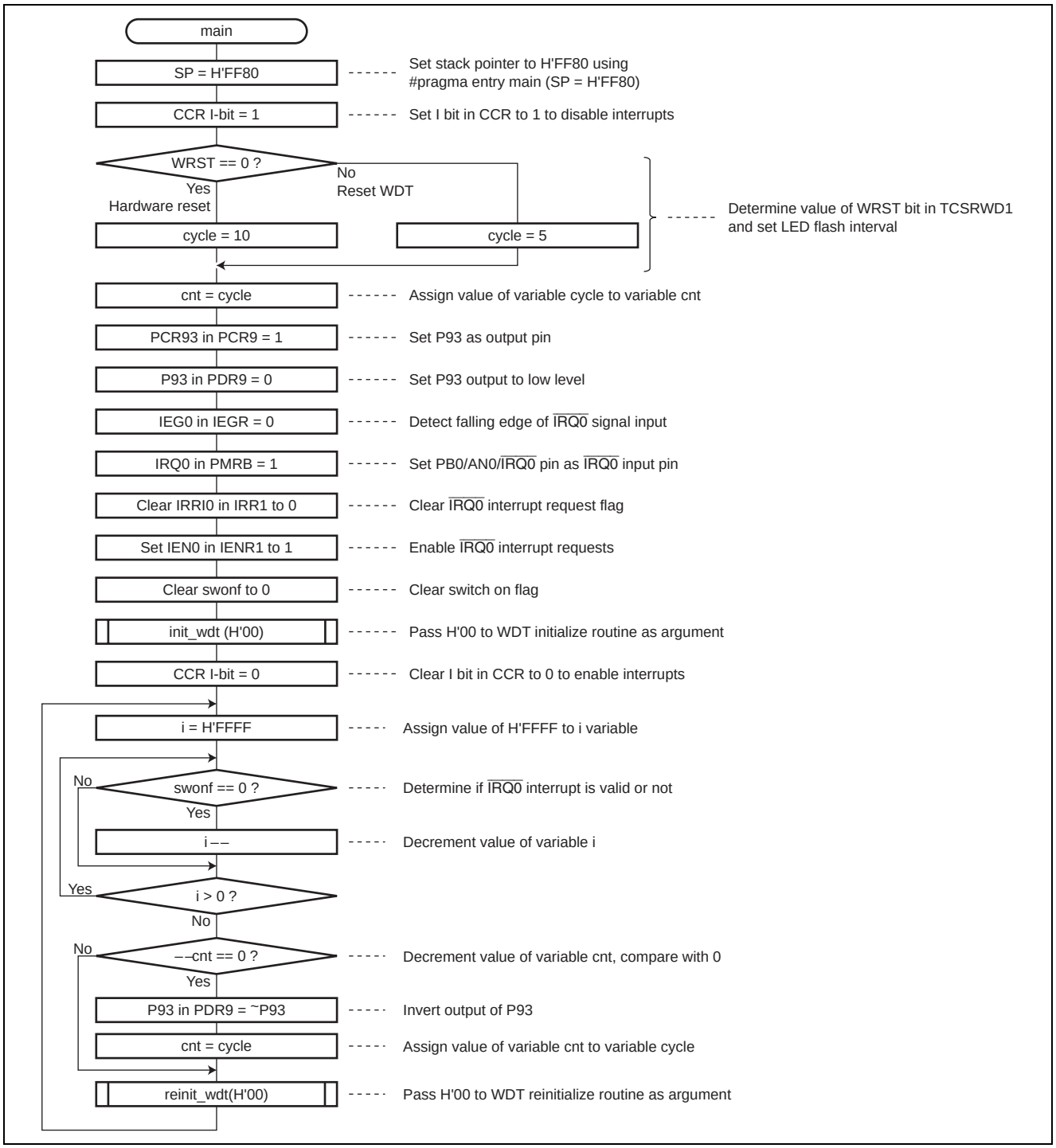
- IENR1 Interrupt Enable Register 1 Address: H'FFF3

Bit	Bit Name	Set Value	R/W	Description
0	IEN0	1	R/W	$\overline{\text{IRQ0}}$ interrupt request enable $\overline{\text{IRQ0}}$ interrupt requests are enabled when this bit is set to 1.

- IRR1 Interrupt Request Register 1 Address: H'FFF6

Bit	Bit Name	Set Value	R/W	Description
0	IRRI0	0	R/W	$\overline{\text{IRQ0}}$ interrupt request flag [Setting condition] When the $\overline{\text{IRQ0}}$ pin is set as the interrupt input pin and the specified edge is detected [Clearing condition] When 0 is written to this bit

3. Flowchart


main
SP = H'FF80
Set stack pointer to H'FF80 using
#pragma entry main (SP = H'FF80)
CCR I-bit = 1
Set I bit in CCR to 1 to disable interrupts
WRST == 0 ?
No
Reset WDT
Yes
Hardware reset
cycle = 10
cycle = 5
Determine value of WRST bit in TCSRWD1
and set LED flash interval
cnt = cycle
Assign value of variable cycle to variable cnt
PCR93 in PCR9 = 1
Set P93 as output pin
P93 in PDR9 = 0
Set P93 output to low level
IEG0 in IEGR = 0
Detect falling edge of IRQ0 signal input
IRQ0 in PMRB = 1
Set PB0/AN0/IRQ0 pin as IRQ0 input pin
Clear IRRI0 in IRR1 to 0
Clear IRQ0 interrupt request flag
Set IEN0 in IENR1 to 1
Enable IRQ0 interrupt requests
Clear swonf to 0
Clear switch on flag
init_wdt (H'00)
Pass H'00 to WDT initialize routine as argument
CCR I-bit = 0
Clear I bit in CCR to 0 to enable interrupts
i = H'FFFF
Assign value of H'FFFF to i variable
No
swonf == 0 ?
Determine if IRQ0 interrupt is valid or not
Yes
i – –
Decrement value of variable i
Yes
i > 0 ?
No
No
– –cnt == 0 ?
Decrement value of variable cnt, compare with 0
Yes
P93 in PDR9 = ~P93
Invert output of P93
cnt = cycle
Assign value of variable cnt to variable cycle
reinit_wdt(H'00)
Pass H'00 to WDT reinitialize routine as argument

4.4.2 init_wdt() Function

1. Module Specifications

- Initial setting of WDT, TCWD setting, and WDT count start

Table 4 Module Specifications

Item	Type	Variable	Description
Arguments	unsigned char	tc	Initial set value for TCWD. H'00 in this sample task.
Return value	None	None	None

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- TCSRWD1 Timer Control/Status Register WD1 Address: H'FFB1

Bit	Bit Name	Set Value	R/W	Description
7	B6WI	0	R/W	Bit 6 Write Disable Bit 6 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
6	TCWE	1	R/W	Timer Counter WD Write Enable TCWD can be written when this bit is set to 1. When writing data to this bit the write value for bit 7 must be 0.
5	B4WI	0	R/W	Bit 4 Write Disable Bit 4 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
4	TCSRWE	1	R/W	Timer Control/Status Register WD Write Enable Writing to bits 2 and 0 of the register is enabled when this bit is set to 1. When writing data to this bit the write value for bit 5 must be 0.
3	B2WI	0	R/W	Bit 2 Write Disable Bit 2 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
2	WDON	1	R/W	Watchdog Timer On TCWD starts counting up when this bit is set to 1 and halts when it is cleared to 0. [Clearing conditions] • Reset • When 0 is written to the B2WI bit and 0 to the WDON bit while the TCSRWE bit is 1 [Setting condition] • When 1 is written to the B2WI bit and 0 to the WDON bit while the TCSRWE bit is 1
1	B0WI	0	R/W	Bit 0 Write Disable Bit 0 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Clearing conditions] • Reset by $\overline{\text{RES}}$ pin • When 0 is written to the B0WI bit and 0 to the WRST bit while the TCSRWE bit is 1 [Setting condition] • When TCWD overflows and an internal reset signal is generated

- TCSRWD2 Timer Control/Status Register WD2 Address: H'FFB2

Bit	Bit Name	Set Value	R/W	Description
7	OVF	0	R/(W)*[1]	Overflow Flag Indicates that TCWD has overflowed (changed from H'FF to H'00). [Setting condition] When TCWD overflows (changes from H'FF to H'00) However, when internal reset request generation is selected in the watchdog timer mode, this bit is cleared automatically by an internal reset after it has been set. [Clearing condition] When TCSRWD2 is read when OVF = 1, then 0 is written to OVF*[4]
6	B5WI	0	R/(W)*[2]	Bit 5 Write Disable Bit 5 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
5	WT/$\overline{IT}$	0	R/(W)*[3]	Timer Mode Select Selects whether the WDT is used as a watchdog timer or interval timer. 0: Watchdog timer mode 1: Interval timer mode
4	B3WI	0	R/(W)*[2]	Bit 3 Write Disable Bit 3 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
3	IEOVF	0	R/(W)*[3]	Overflow Interrupt Enable Enables or disables overflow interrupt requests in the interval timer mode. 0: Disables an overflow interrupt 1: Enables an overflow interrupt
2-0	—	All 1	—	Reserved These bits are always read as 1.

Notes: 1. Only 0 can be written to clear the flag.
2. Write operation is necessary because this bit controls data writing to another bit. This bit is always read as 1.
3. Writing is possible only when the write conditions are satisfied.
4. In the subactive mode, clear this flag after setting the CKS3 to CKS0 bits in TMWD to B'0XXX (internal oscillator).

- TCWD Timer Counter WD Address: H'FFB3

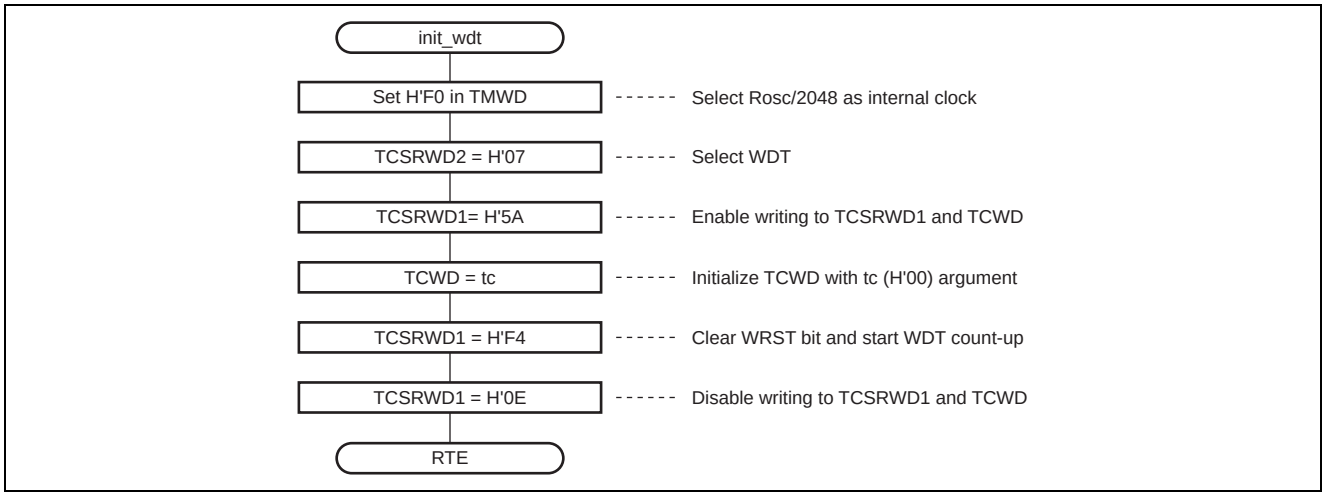
Bit	Bit Name	Set Value	R/W	Description
7	TCW7	0	R/W	TCWD is an 8-bit readable/writable up-counter.
6	TCW6	0	R/W	
5	TCW5	0	R/W	
4	TCW4	0	R/W	
3	TCW3	0	R/W	
2	TCW2	0	R/W	
1	TCW1	0	R/W	
0	TCW0	0	R/W	

- TMWD Timer Mode WD Address: H'FFB0

Bit	Bit Name	Set Value	R/W	Description
7-4	—	All 1	—	These bits are reserved. They are always read as 1.
3	CKS3	0	R/W	Clock Select 3 to 0
2	CKS2	0	R/W	Select the clock to be input to TCWD.
1	CKS1	0	R/W	1000: Internal clock: counts on ϕ/64
0	CKS0	0	R/W	1001: Internal clock: counts on ϕ/128 1010: Internal clock: counts on ϕ/256 1011: Internal clock: counts on ϕ/512 1100: Internal clock: counts on ϕ/1,024 1101: Internal clock: counts on ϕ/2,048 1110: Internal clock: counts on ϕ/4,096 1111: Internal clock: counts on ϕ/8,192 0XXX: Internal oscillator: counts on R_{OSC}/2,048 For details on the internal oscillator overflow periods, see section 24, Electrical Characteristics, in the Hardware Manual. In the active (medium-speed) mode or the sleep (medium-speed) mode, the setting of B'0XXX and the interval timer mode is disabled.

[Legend] X: Don't care.

3. Flowchart



4.4.3 reinit_wdt() Function

1. Module Specifications

- Resets TCWD

Table 5 Module Specifications

Item	Type	Variable	Description
Arguments	unsigned char	tc	Set value for TCWD. H'00 in this sample task.
Return value	None	None	None

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

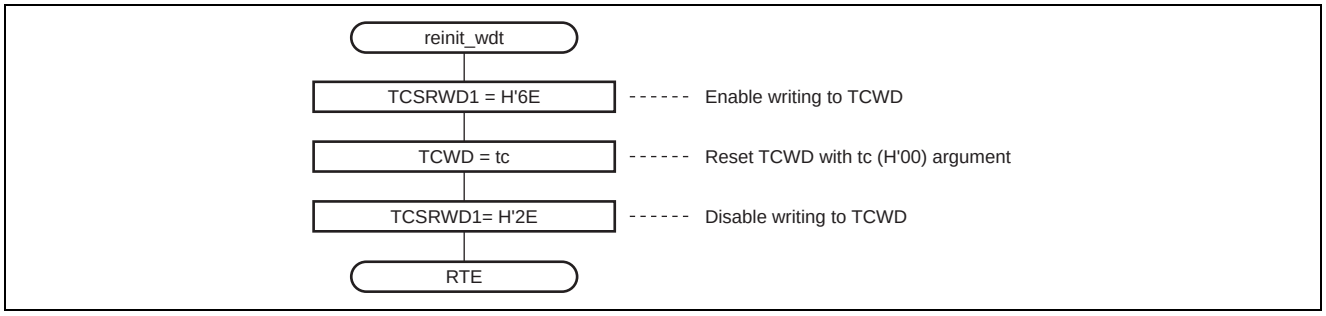
- TCSRWD1 Timer Control/Status Register WD1 Address: H'FFB1

Bit	Bit Name	Set Value	R/W	Description
7	B6WI	0	R/W	Bit 6 Write Disable Bit 6 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
6	TCWE	1	R/W	Timer Counter WD Write Enable TCWD can be written when this bit is set to 1. When writing data to this bit the write value for bit 7 must be 0.
5	B4WI	1	R/W	Bit 4 Write Disable Bit 4 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
4	TCSRWE	0	R/W	Timer Control/Status Register WD Write Enable Bits 2 and 0 of the register can be written when this bit is set to 1. When writing data to this bit the write value for bit 5 must be 0.
3	B2WI	1	R/W	Bit 2 Write Disable Bit 2 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
2	WDON	1	R/W	Watchdog Timer On TCWD starts counting up when this bit is set to 1 and halts when it is cleared to 0. [Clearing conditions] • Reset • When 0 is written to the B2WI bit and 0 to the WDON bit while the TCSRWE bit is 1 [Setting condition] • When 1 is written to the B2WI bit and 0 to the WDON bit while the TCSRWE bit is 1
1	B0WI	1	R/W	Bit 0 Write Disable Bit 0 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Clearing conditions] • Reset by $\overline{\text{RES}}$ pin • When 0 is written to the B0WI bit and 0 to the WRST bit while the TCSRWE bit is 1 [Setting condition] • When TCWD overflows and an internal reset signal is generated

- TCWD Timer Counter WD Address: H'FFB3

Bit	Bit Name	Set Value	R/W	Description
7	TCW7	0	R/W	TCWD is an 8-bit readable/writable up-counter.
6	TCW6	0	R/W	
5	TCW5	0	R/W	
4	TCW4	0	R/W	
3	TCW3	0	R/W	
2	TCW2	0	R/W	
1	TCW1	0	R/W	
0	TCW0	0	R/W	

3. Flowchart



4.4.4 int_irq() Function

1. Module Specifications

- $\overline{\text{IRQ0}}$ interrupt processing

Table 6 Module Specifications

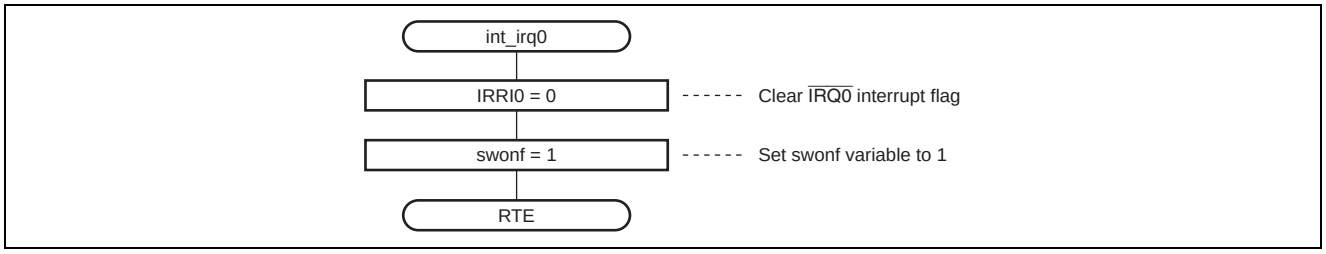
Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used
   The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- IRR1 Interrupt Request Register 1 Address: H'FFF6

Bit	Bit Name	Set Value	R/W	Description
0	IRRI0	0	R/W	$\overline{\text{IRQ0}}$ Interrupt Request Flag [Setting condition] When the $\overline{\text{IRQ0}}$ pin is set as an interrupt input pin and the specified edge is detected [Clearing condition] When 0 is written to this bit

3. Flowchart



4.5 Link Address Specifications

Section Name	Address
CVECT	H'0000
P	H'0100

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Mar.18.05	—	First edition issued

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