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H8/38076R

Transition to the Sleep (High-Speed) Mode

Introduction

In this example a transition is made from the active (high-speed) mode to the sleep (high-speed) mode, one of the power-down modes of the H8/38076R.

Target Device

H8/38076R

Contents

1. Specifications

After a reset is cleared the H8/38076R can transition to any of seven power-down modes, in which power consumption is reduced substantially, in addition to the normal active (high-speed) mode. In this sample task a transition is made from the active (high-speed) mode to the sleep (high-speed) mode, one of the power-down modes.

2. Description of Functions

2.1 Functions Used

In this sample task a transition is made from the active (high-speed) mode to the sleep (high-speed) mode, one of the power-down modes.

The state of the H8/38076R in the sleep (high-speed) mode is shown in table 1, and the functions used as described below.

1. System Clock (ϕ)
   This 10-MHz oscillation clock is a reference clock for operation of the CPU and peripheral functions.

2. Subclock (ϕ_W)
   This 32.768-kHz oscillation clock is a reference clock for operation of the CPU and peripheral functions.

3. Power-Down Mode (Sleep (High-Speed) Mode) Function
   In the sleep (high-speed) mode CPU operation is halted, but the system clock oscillator, subclock oscillator, and internal peripheral modules continue to function. CPU register contents are retained.
   The sleep (high-speed) mode is cleared by an interrupt. When an interrupt is requested, the sleep mode is cleared and interrupt exception handling starts. The sleep mode is not cleared if the I bit in CCR is set to 1 or the requested interrupt is disabled by an interrupt enable bit. After the sleep mode is cleared a transition is made from the sleep (high-speed) mode to the active (high-speed) mode. If the $\overline{\text{RES}}$ signal goes low in the sleep (high-speed) mode, the H8/38076R enters the reset state and the sleep (high-speed) mode is cleared. Since interrupt request signals are synchronous with the system clock, a maximum delay of $2/\phi$ (s) may occur from the point at which an interrupt request signal occurs until interrupt exception handling starts.

- System control register 1 (SYSCR1)
  Together with SYSCR2, SYSCR1 controls the power-down modes.

- System control register 2 (SYSCR2)
  Together with SYSCR1, SYSCR2 controls the power-down modes.

Table 1 State of the H8/38076R in the Sleep (High-Speed) Mode

Function		Sleep (High-Speed) Mode
System clock oscillator		Functioning
Subclock oscillator		Functioning
CPU	Instructions	Halted
	RAM	Retained
	Registers	Retained
	I/O	Retained
External interrupts	IRQ0	Functioning
	IRQ1	Functioning
	IRQ3	Functioning
	IRQ4	Functioning
	IRQAEC	Functioning
	WKP0 to WKP7	Functioning
Peripheral modules	Timer F	Functioning
	Asynchronous event counter	Functioning
	RTC (realtime clock)	Functioning
	TPU (timer pulse unit)	Functioning
	WDT (watchdog timer)	Functioning
	SCI3/IrDA module	Functioning
	I^2C2 module	Functioning
	PWM module	Functioning
	A/D converter	Functioning
	LCD controller/driver	Functioning

2.2 Assignment of Functions

Table 2 shows the assignment of functions in this sample task. A transition is made from the active (high-speed) mode to the sleep (high-speed) mode, one of the power-down modes, using functions assigned as shown in table 2.

Table 2 Assignment of Functions

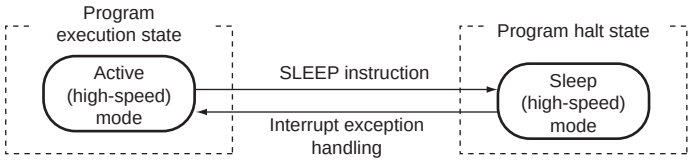
Elements	Description
SYSCR1	Together with SYSCR2, controls transition to the sleep (high-speed) mode
SYSCR2	Together with SYSCR1, controls transition to the sleep (high-speed) mode

3. Principles of Operation

The principles of operation of this sample task are described below. Using the procedure shown, a transition is made from the active (high-speed) mode to the sleep (high-speed) mode, one of the power-down modes. The mode transitions in this sample task are illustrated in figure 1.

1. Transition to the sleep (high-speed) mode
   a. Clear the SSBY and LSON bits in SYSCR1 to 0.
   b. Clear the DTON and MSON bits in SYSCR2 to 0.
   c. Execute the SLEEP instruction.

2. Clearing the sleep (high-speed) mode
   a. Receive an interrupt request in the sleep (high-speed) mode.
   b. Perform interrupt handling. (The recovery destination of the interrupt will be the active (high-speed) mode.)



Conditions at execution of SLEEP instruction

LSON	MSON	SSBY	TMA3	DTON
0	0	0	x	0

Note: x: Don't care

Condition for mode clearing by interrupt exception processing

Interrupt source
All interrupts

Note: A transition between different modes cannot be made to occur simply because of an interrupt source. Make sure that interrupt handling is performed after the interrupt request is accepted.

Figure 1 Mode Transition Diagram

4. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- SYSCR1 System control register 1 Address: H'FFF0

Bit	Bit Name	Set Value	R/W	Description
7	SSBY	0	R/W	Software standby Selects the mode to transition to after execution of the SLEEP instruction. 0: A transition is made to the sleep mode or the subsleep mode. 1: A transition is made to the standby mode or the watch mode.
3	LSON	0	R/W	Selects the system clock (ϕ) or subclock (ϕ_{SUB}) as the CPU operating clock when the watch mode is cleared. 0: The CPU operates on the system clock (ϕ) 1: The CPU operates on the subclock (ϕ_{SUB})

- SYSCR2 System control register 2 Address: H'FFF1

Bit	Bit Name	Set Value	R/W	Description
3	DTON	0	R/W	Direct transfer on flag Selects the mode to transition to after the SLEEP instruction is executed with bits SSBY, TMA3, and LSON in SYSCR1 and bit MSON in SYSCR2.
2	MSON	0	R/W	Medium speed on flag Selects whether operation continues in the active (high-speed) or the active (medium-speed) mode after the standby mode, the watch mode, or the sleep mode is cleared. 0: Active (high-speed) mode 1: Active (medium-speed) mode

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Mar.18.05	—	First edition issued

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