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Renesas Electronics Corporation

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H8/38076R

Oscillation Stabilization Time

Introduction

This application note describes the oscillation stabilization time of the H8/38076R.

Target Device

H8/38076R

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1. Functions Used

1. Definition of Oscillation Stabilization Wait Time

Figure 1 shows the oscillation waveform (OSC2), system clock (ϕ), and H8/38076R operating mode when a transition is made from the standby mode, the watch mode, or the subactive mode to the active (high-speed or medium-speed) mode, with a resonator connected to the system clock oscillator.

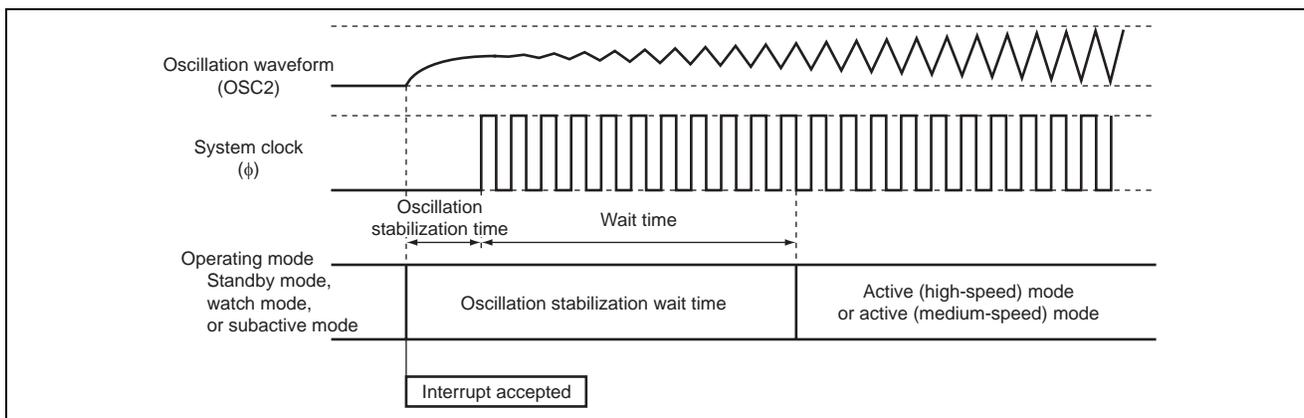


Figure 1 Block Diagram of Power-On Reset Circuit

As shown in figure 1, as the system clock oscillator is halted in the standby mode, the watch mode, and the subactive mode, a transition to the active (high-speed or medium-speed) mode requires the sum of the following two times (oscillation stabilization time and wait time).

- **Oscillation Stabilization Time (t_{rc})**
The duration from the point at which the system clock oscillator oscillation waveform starts to change when an interrupt is generated, until the amplitude of the oscillation waveform increases and the oscillation frequency stabilizes.
- **Wait Time**
The time required for the CPU and peripheral functions to begin operating after the oscillation waveform frequency and system clock have stabilized. The wait time is selected by bits STS2 to STS0 in SYSCR1.

When the standby mode, the watch mode, or the subactive mode is cleared by an interrupt or a reset, and a transition is made to the active mode, the oscillation waveform begins to change at the point when the interrupt is accepted. Therefore, when a resonator is connected in the standby mode, the watch mode, or the subactive mode, the oscillation stabilization time is necessary because the system clock oscillator is halted.

The oscillation stabilization time for these state transitions is the same as the oscillation stabilization time at power-on (the duration from the point at which the power supply voltage reaches the prescribed level until oscillation stabilizes) specified as "oscillation stabilization time t_{rc} " in the AC characteristics.

Once the system clock has halted, a wait time of at least 8 states is necessary for the CPU and peripheral functions to operate normally.

Thus, the time required from interrupt generation until operation of the CPU and peripheral functions is the sum of the oscillation stabilization time and wait time described above. This total time is called the oscillation stabilization wait time and is expressed by equation (1) below.

$$\begin{aligned} \text{Oscillation stabilization wait time} &= \text{oscillation stabilization time} + \text{wait time} \\ &= t_{rc} + (8 \text{ to } 16,384 \text{ states}) \dots\dots\dots (1) \end{aligned}$$

Therefore, when a transition is made from the standby mode, the watch mode, or the subactive mode to the active (high-speed/medium-speed) mode, with a resonator connected to the system clock oscillator, the mounted circuit components must be evaluated carefully before deciding the oscillation stabilization wait time. Specifically, a suitable value should be determined in consultation with the resonator manufacturer, since the oscillation stabilization time may differ depending on the mounted circuit component constants, stray capacitance, and so on.

Confirm that the OSC amplitude is approximately 1 V or greater during the wait time.

2. Setting of Wait Time

The settings for bits STS2 to STS0 in system control register 1 (SYSCR1) are described below. Table 2 shows oscillation stabilization time from the AC characteristics, and a resonator equivalent circuit is shown in figure 2.

- Standby timer select 2 to 0 (STS2 to STS0 bits) in system control register 1 (SYSCR1)

These bits designate the number of wait states, when entering the active mode or the sleep mode from the standby mode, the subactive mode, the subsleep mode, or the watch mode, from the start of system clock oscillator operation until the clock is supplied. The setting should be made according to the operating frequency so that the wait time is at least equal to the oscillation stabilization time. The minimum value (STS2 = 1, STS1 = 0, STS0 = 1) is recommended if an external clock is used. If a setting other than the recommended value is made, operation may start before the end of the wait time. Table 1 shows the relationship between the settings of bits STS2 to STS0, the operating frequency, and the wait time.

Table 1 Settings of Bits STS2 to STS0, Operating Frequency, and Wait Time

Bit			Number of Wait States	Wait Time	
STS2	STS1	STS0		Operating Frequency: 5 MHz	Operating Frequency: 2 MHz
0	0	0	8,192 states	1.638 ms	4.1 ms
0	0	1	16,384 states	3.277 ms	8.2 ms
0	1	0	1,024 states	0.205 ms	0.512 ms
0	1	1	2,048 states	0.410 ms	1.024 ms
1	0	0	4,096 states	0.819 ms	2.048 ms
1	0	1	2 states (External clock input)	0.0004 ms	0.001 ms
1	1	0	8 states	0.002 ms	0.004 ms
1	1	1	16 states	0.003 ms	0.008 ms

Note: When an external clock is input, bits STS2 to STS0 should be set for the external clock input mode before mode transition is executed. These bits should not be set for the external clock input mode if no external clock is used.

Table 2 AC Characteristics (Oscillation Stabilization Time)

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Reference Diagram
				min.	typ.	max.		
Oscillation stabilization time	t_{rc}	OSC1 , OSC2	Crystal resonator (Vcc = 2.7 to 3.6 V)	—	0.8	2.0	ms	Figure 2
			Crystal resonator (Vcc = 2.2 to 3.6 V)	—	1.2	3	ms	Figure 2
			Ceramic resonator (Vcc = 2.7 to 3.6 V)	—	20	45	μ s	Figure 2
			Ceramic resonator (Other than above)	—	80	—	μ s	Figure 2
			Other than above	—	—	50	ms	Figure 2

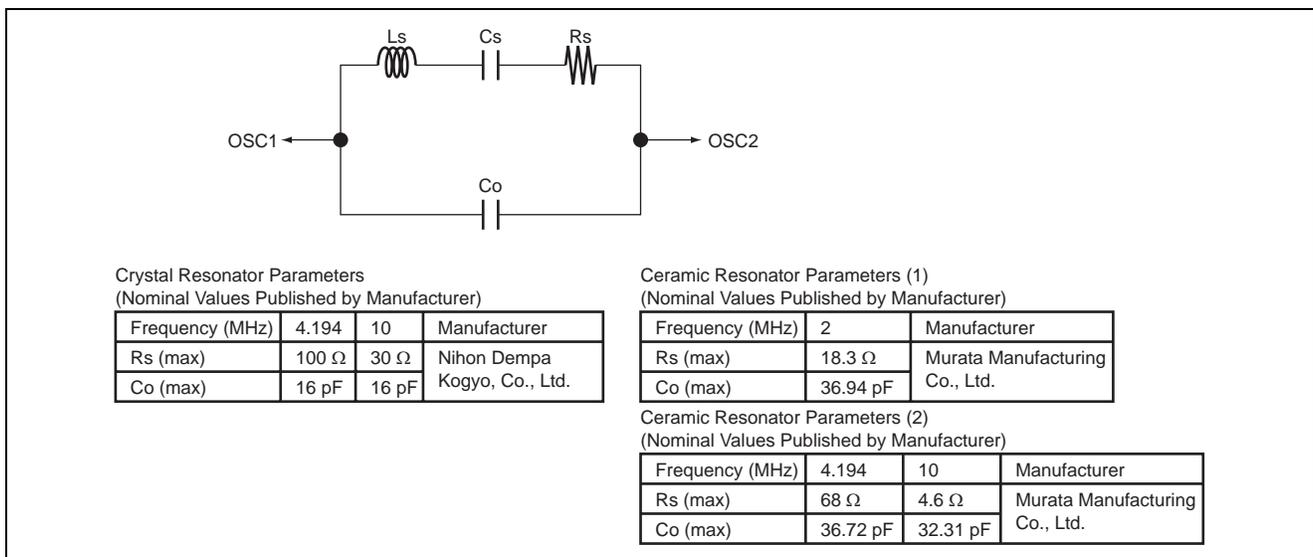


Figure 2 Resonator Equivalent Circuit

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.18.05	—	First edition issued

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