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H8/38076R

Clock Operation Using Timer F

Introduction

The 32.768-kHz subclock (ϕ_W) is used to implement clock operation with timer F.

Target Device

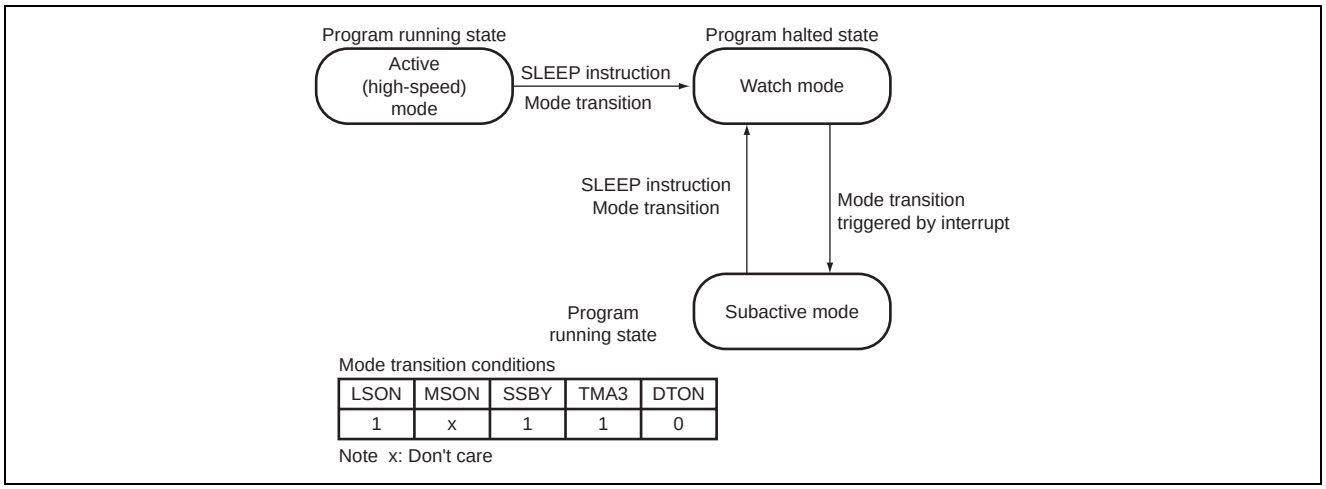
H8/38076R

Contents

1. Specifications

In this sample task clock operation is implemented by generating a timer F interrupt once per second and incrementing a clock counter set in RAM. The clock counter set in RAM uses 8 bits for seconds and 8 bits for minutes. It begins counting from 00 minutes 00 seconds. When the counter value is 59 minutes 59 seconds, the next count initializes it to 00 minutes 00 seconds and counting up continues. The operation steps in this sample task are listed below, and the mode transitions are shown in figure 1.

1. Make initial settings.
2. Transition from the active (high-speed) mode to the watch mode.
3. Transition to the subactive mode, triggered by a timer F interrupt, and increment the counter set in RAM.
4. Transition back to the watch mode and wait for timer F interrupt.
5. Return to step (3).



Mode transition conditions

LSON	MSON	SSBY	TMA3	DTON
1	x	1	1	0

Note x: Don't care

Figure 1 Mode Transitions in This Task Example

2. Description of Functions

2.1 Functions

In this sample task timer F is used to increment a counter set in RAM once per second to implement clock operation. The functions of timer F are described below.

1. System Clock (ϕ)
   This 10-MHz clock is the reference clock for operation of the CPU and peripheral functions.

2. Prescaler S (PSS)
   PSS is a 13-bit counter that takes ϕ as input and counts up once per period.

3. Timer F Functions
   This 16-bit timer has an output compare function. It can be used for external event counting or as a multifunction timer for a variety of applications, including counter resetting, interrupt request, and toggle output using compare match signals. It can also be used as two independent 8-bit timers (timer FH and timer FL).

- Timer counter F (TCF)
  TCF is a 16-bit readable/writeable up-counter that is incremented by input of an internal or an external clock. Five input clock options are available: the system clock divided by 4, 16, or 32; the subclock divided by 4; or an external clock. When $\phi_W/4$ is selected as the internal clock the available operation modes are the watch mode, the subactive mode, and the sleep mode.
  In this sample task the subclock divided by 4 ($\phi_W/4$) is selected as the TCF input clock.
- Timer control register F (TCRF)
  TCRF switches between 16-bit mode and 8-bit mode, selects among the four internal clocks and an external event, and selects the output level of the TMOFH and TMOFL pins.
- Timer control/status register F (TCSRF)
  TCSRF performs counter clear selection, overflow flag and compare match flag settings, and controls enabling of overflow interrupt requests.

4. Interrupt Controller Functions
   The following registers are used to control interrupts.

- Interrupt enable register 2 (IENR2)
  IENR2 controls direct transitions and timer F interrupts.
- Interrupt request register 2 (IRR2)
  IRR2 is the interrupt request status register for direct transitions and timer F interrupts.

5. Power-Down Mode (Subactive Mode) Function

   In the subactive mode the system clock oscillator stops, but internal peripheral modules other than the A/D converter and PWM function. As long as the required voltage is applied, the contents of some registers of the internal peripheral modules are retained.

   The subactive mode is cleared by the SLEEP instruction. After the subactive mode is cleared a transition is made to the subsleep mode, the active mode, or the watch mode, depending on the combination of bits SSBY, LSON, and TMA3 in system control register 1 (SYSCR1) and bits MSON and DTON in system control register 2 (SYSCR2). The subactive mode is not cleared if the I bit in the condition-code register (CCR) is set to 1 or if the relevant interrupt is disabled by the interrupt enable register.

   The operating frequency of subactive mode is selected from among watch clock (ϕ_W) divided by 2 ($\phi_W/2$), by 4 ($\phi_W/4$), and by 8 ($\phi_W/8$) by the SA1 and SA0 bits in SYSCR2. After the SLEEP instruction is executed the operating frequency changes to the frequency which was set before execution.

   In this sample task operation transitions from the active (high-speed) mode to the watch mode. Then a transition is made to the subactive mode when a timer F interrupt is issued. Operation transitions back to the watch mode after timer F interrupt handling, and the task waits for the next timer F interrupt.

   The transition from the active (high-speed) mode to the watch mode takes place when the SLEEP instruction is executed while the SSBY, TMA3, and LSON bits in SYSCR1 are set to 1. After the transition to the watch mode the interrupt is cleared, after which operation transitions to the subactive mode.

- System control register 1 (SYSCR1)
  Together with SYSCR2, SYSCR1 controls the power-down modes.
- System control register 2 (SYSCR2)
  Together with SYSCR1, SYSCR2 controls the power-down modes.

Figure 2 shows a block diagram of the 16-bit output compare function of timer F.

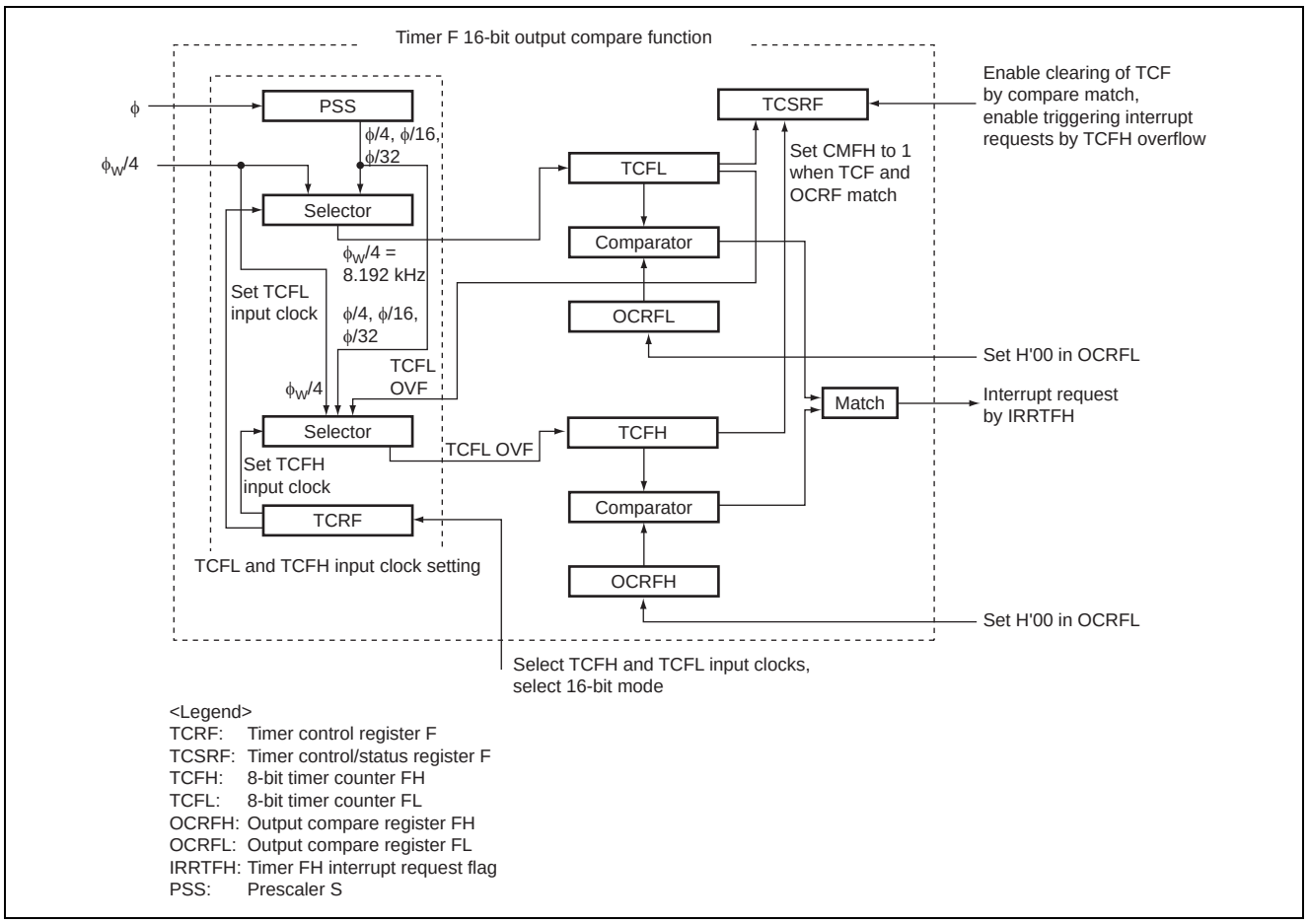


Figure 2 Block Diagram of 16-Bit Output Compare Function of Timer F

2.1.1 Timer F Operation in 16-Bit Timer Mode

The 16-bit operation mode of timer F is described below.

Timer F is a 16-bit counter that increments on each input clock pulse. The timer counter F value is constantly compared with the value set in output compare register F, and the counter can be cleared, an interrupt requested, or port output toggled, when the two values match. Timer F can also function as two independent 8-bit timers.

Timer F operates as a 16-bit timer when the CKSH2 bit in timer control register F (TCRF) is cleared to 0.

Following a reset, timer counter F (TCF) is initialized to H'0000, output compare register F (OCRF) to H'FFFF, and timer control register F (TCRF) and timer control status register F (TCSRF) to H'00. The counter begins to count up at an input signal from an external event (TMIF pin). The TMIFEG bit in the interrupt edge select register (IEGR) selects which edge of the external event signal is used for counting.

The timer F operating clock can be selected from among the three internal output from PSS, the $\phi_W/4$ internal clock, or an external clock by the settings of bits CKSL2 to CKSL0 in TCRF.

The contents of OCRF are constantly compared with TCF, and CMFH in TCSRF is set to 1 when both values match. If IENTFH in IENR2 is 1 at this time, an interrupt request is sent to the CPU, and at the same time TMOFH pin output is toggled. TCF is cleared if CCLRH in TCSRF is 1. The output level of the TMOFH pin can be set by the TOLH bit in TCRF.

When TCF overflows from H'FFFF to H'0000, OVFH in TCSRF is set to 1. If OVIEH in TCSRF and IENTFH in IENR2 are both 1 at this point, an interrupt request is sent to the CPU.

2.1.2 Method of Setting Timer F Interrupt Interval

The method used to set the timer F interrupt interval is described below.

In this sample task the ϕ_W frequency is 32.768 kHz and timer F is used as the clock time base. The TCF input clock is set to $\phi_W/4$ by setting CKSL2, CKSL1, and CKSL0 in TCRF to 1. The $\phi_W/4$ frequency is

$\phi_W/4 = 32.768\ \text{kHz}/4 = 8.192\ \text{kHz}$

Consequently, the TCF input clock cycle is

$1/8.192\ \text{kHz} \approx 122.07\ \mu\text{s}$

When OCRF is set to H'2000, the duration until TCL and OCRF match can be calculated as

$\text{H'2000} \times (1/8.192\ \text{kHz}) = 8192 \times 122.07\ \mu\text{s} = 1\ \text{s}$

Therefore, the OCRF setting value for setting the timer F interrupt cycle T_F can be calculated using the following equation.

$\text{OCRF setting value} = T_F/(1/8.192\ \text{kHz}) = T_F \times 8.192\ \text{kHz}$

Table 1 shows example timer F interrupt cycle T_F and OCRF setting values.

Table 1 Timer F Interrupt Cycle T_F and OCRF Setting Value Examples

T_F (s)	Calculation Method	OCRF Setting Value
0.125	0.125 s × 8.192 kHz = 1024	H'0400
0.250	0.250 s × 8.192 kHz = 2048	H'0800
0.500	0.500 s × 8.192 kHz = 4096	H'1000
1.000	1.000 s × 8.192 kHz = 8192	H'2000
2.000	2.000 s × 8.192 kHz = 16384	H'4000

2.1.3 Timer F Operating Modes

The operating modes of timer F are shown in table 2.

Table 2 Timer F Operating Modes

Operating Mode	Reset	Active	Sleep	Watch	Subactive	Subsleep	Standby	Module Standby
TCF	Reset	Functions	Functions	Functions/ halted*	Functions/ halted*	Functions/ halted*	Halted	Halted
OCRF	Reset	Functions	Retained	Retained	Functions	Retained	Retained	Retained
TCRF	Reset	Functions	Retained	Retained	Functions	Retained	Retained	Retained
TCSRF	Reset	Functions	Retained	Retained	Functions	Retained	Retained	Retained

Note: * When $\phi_W/4$ is selected as the TCF internal clock in the active mode or the sleep mode, synchronization is maintained by a synchronization circuit since the system clock and internal clock are mutually asynchronous. This results in a maximum count cycle error of $1/\phi$ (s).
An external clock must be selected or $\phi_W/4$ selected as the internal clock when the counter is operated in the subactive mode, the watch mode, or the subsleep mode. The counter will not operate if any other internal clock is selected.

2.2 Assignment of Functions

Table 3 shows the assignment of functions in this sample task. Timer F functions are allocated as shown in table 3 to perform clock operation.

Table 3 Assignment of Functions

Elements	Description
TCRF	Sets TCF to 16-bit mode, selects $\phi_W/4$ as TCF input clock
TCSRF	Enables TCF overflow interrupts, enables clearing TCF by compare match, TCF status register
TCF	16-bit counter using $\phi_W/4$ as input clock
OCRF	Compared with TCF, set so compare match with TCF occurs at 1-second intervals
SYSCR1	Controls transitions to the watch mode and the subactive mode together with SYSCR2
SYSCR2	Controls transitions to the watch mode and the subactive mode together with SYSCR1
IENTFH	Enables timer F interrupt requests
IRRTFH	Timer F interrupt request flag

2.3 Timer F Usage Notes

The following types of contention and operation can occur when timer F is used in 16-bit mode.

1. In toggle output, TMOFH pin output is toggled when all 16 bits match and a compare match signal is generated. If a TCRF write by a MOV instruction and generation of the compare match signal occur simultaneously, data is output at the level set by TOLH to the TMOFH pin as a result of the TCRF write. TMOFL pin output is unstable in 16-bit mode and should not be used; the TMOFL pin should be used as a port pin.

2. If an OCRFL write and compare match signal generation occur simultaneously, the compare match signal is invalid. However, if the written data and the counter value match, a compare match signal will be generated at that point. As the compare match signal is output in synchronization with the TCFL clock, a compare match will not result in compare match signal generation if the clock is stopped.

3. Compare match flag CMFH is set when all 16 bits match and a compare match signal is generated. Compare match flag CMFL is set if the setting conditions for the lower 8 bits are satisfied.

4. OVFH is set when TCF overflows. OVFL is set when the lower 8 bits overflow if the setting conditions are satisfied. No overflow signal is output if a TCFL write and overflow signal output occur simultaneously.

5. When $\phi_W/4$ is selected as the TCF internal clock in the active mode or the sleep mode, synchronization is maintained by a synchronization circuit since the system clock and internal clock are mutually asynchronous. This results in a maximum count cycle error of $1/\phi$ (s). It is necessary to use the subactive mode, the subsleep mode, or the watch mode to eliminate cycle error.

3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 3. Using the hardware and software processing shown in figure 3 clock operation is implemented using timer F.

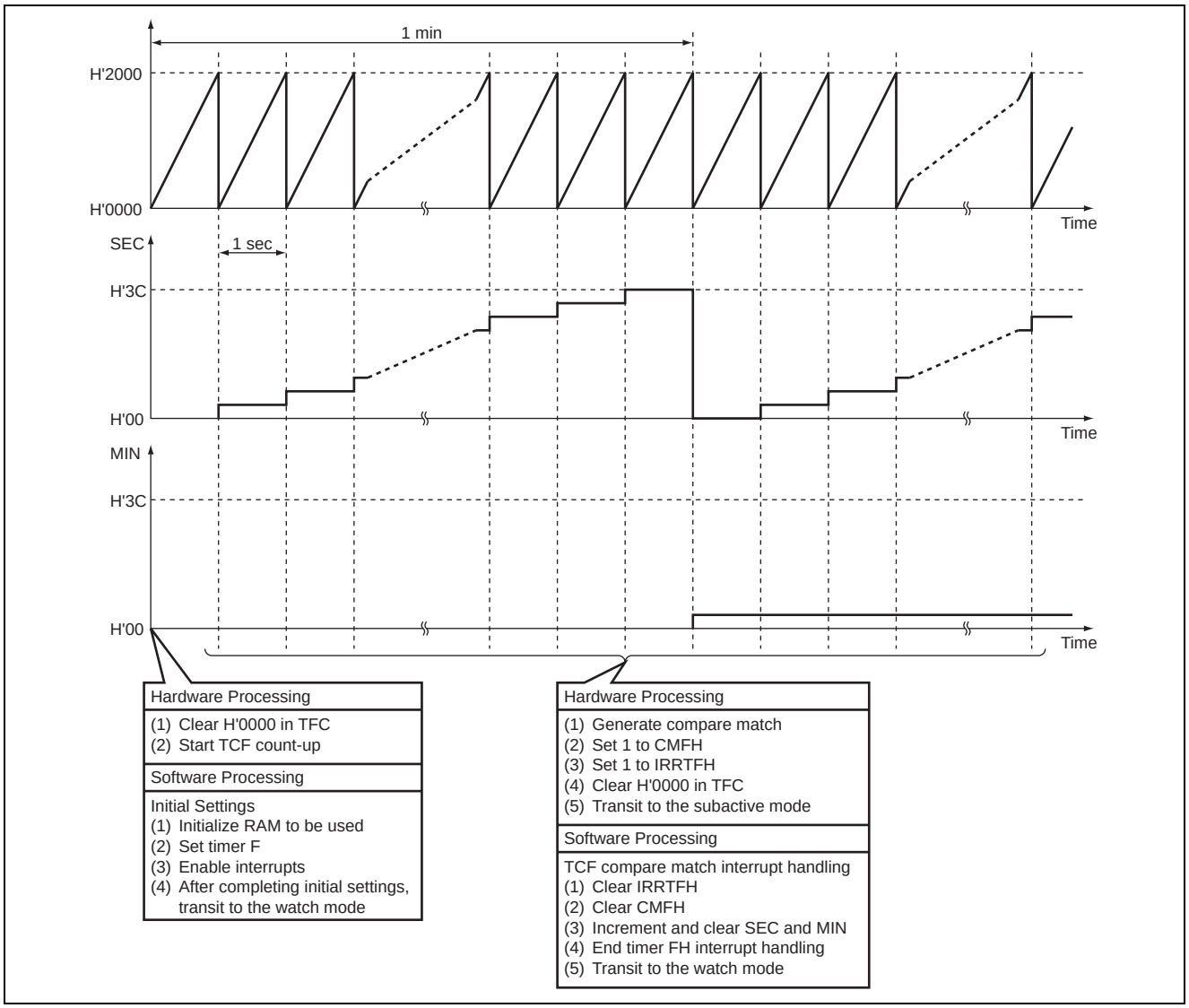


Figure 3 Principles of Operation for Clock Operation Using Timer F

4. Description of Software

4.1 Description of Modules

Table 4 shows the modules used in this sample task.

Table 4 Modules

Function Name	Description
main	Initializes RAM to be used, sets timer F to function as a 16-bit counter, selects $\phi_W/4$ as the TCF clock source, enables clearing TCF by compare match, enables timer F interrupts, enables interrupts, and transits to the watch mode
tfint	Clears IRRTFH and CMFH, increments and clears SEC and MIN settings in RAM

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers Used

The internal registers used in this sample task are shown below.

- TCRF Timer Control Register F Address: H'FFB6

Bit	Bit Name	Set Value	R/W	Description
6	CKSH2	0	W	Clock Select H
5	CKSH1	0	W	Selects the clock input to TCFH from among internal clock
4	CKSH0	0	W	sources or TCFL overflow. 000: 16-bit mode, counting on TCFL overflow signal 001: 16-bit mode, counting on TCFL overflow signal 010: 16-bit mode, counting on TCFL overflow signal
2	CKSL2	1	W	Clock Select L
1	CKSL1	1	W	Select the clock input to TCFL from among internal clock
0	CKSL0	1	W	sources or external event input. 111: Internal clock: counting on $\phi_W/4$

- TCSRF Timer Control/Status Register F Address: H'FFB7

Bit	Bit Name	Set Value	R/W	Description
6	CMFH	Undefined	R/W*	Compare Match Flag H This is a status flag indicates a match between TCFH and OCRFH. [Setting condition] • When the TCF value matches the OCRF value [Clearing condition] • When 0 is written to this bit after reading it as 1
4	CCLRH	1	R/W	Counter Clear H In 16-bit mode this bit selects whether TCF is cleared when TCF and OCRF match. In 16-bit mode: 1: TCF clearing by compare match enabled

Note: * Only 0 can be written to clear the flag.

- TCF Timer Counter F Address: H'FFB8

Bit	Bit Name	Set Value	R/W	Description
15	Bit 15	Undefined	R/W	Output Compare Register F
14	Bit 14	Undefined	R/W	When CKSH2 in TCRF is cleared to 0 TCF operates as a 16-bit counter. The TCF input clock is selected by bits CKSL2 to CKSL0 in TCF.
13	Bit 13	Undefined	R/W	
12	Bit 12	Undefined	R/W	
11	Bit 11	Undefined	R/W	TCF can be cleared in the event of a compare match by CCLRH in TCSRF.
10	Bit 10	Undefined	R/W	
9	Bit 9	Undefined	R/W	When TCF overflows from H'FFFF to H'0000, OVFH in TCSRF is set to 1. If the value of OVIEH in TCSRF is 1 at this time, IRRTFH in IRR2 is set to 1, and if in addition the value of IENTFH in IENR2 is 1, an interrupt request is sent to the CPU.
8	Bit 8	Undefined	R/W	
7	Bit 7	Undefined	R/W	
6	Bit 6	Undefined	R/W	
5	Bit 5	Undefined	R/W	
4	Bit 4	Undefined	R/W	
3	Bit 3	Undefined	R/W	
2	Bit 2	Undefined	R/W	
1	Bit 1	Undefined	R/W	
0	Bit 0	Undefined	R/W	

- OCRF Output Compare Register F Address: H'FFBA

Bit	Bit Name	Set Value	R/W	Description
15	Bit 15	0	R/W	Output Compare Register F
14	Bit 14	0	R/W	When CKSH2 in TCRF is cleared to 0 OCRF operates as a 16-bit register. The contents of OCRF are constantly compared with TCF, and when both values match, CMFH in TCSRF is set to 1. At the same time IRRTFH in IRR2 is set to 1. If IENTFH in IENR2 is 1 at this time an interrupt request is sent to the CPU. Setting value in this sample task: OCRF = H'2000
13	Bit 13	1	R/W	
12	Bit 12	0	R/W	
11	Bit 11	0	R/W	
10	Bit 10	0	R/W	
9	Bit 9	0	R/W	
8	Bit 8	0	R/W	
7	Bit 7	0	R/W	
6	Bit 6	0	R/W	
5	Bit 5	0	R/W	
4	Bit 4	0	R/W	
3	Bit 3	0	R/W	
2	Bit 2	0	R/W	
1	Bit 1	0	R/W	
0	Bit 0	0	R/W	

- SYSCR1 System Control Register 1 Address: H'FFF0

Bit	Bit Name	Set Value	R/W	Description
7	SSBY	1	R/W	Software Standby Selects the mode to transit after execution of the SLEEP instruction. 0: A transition is made to the sleep mode or the subsleep mode. 1: A transition is made to the standby mode or the watch mode.
3	LSON	1	R/W	Low Speed on Flag Selects the system clock (ϕ) or subclock (ϕ_{SUB}) as the CPU operating clock when the watch mode is cleared. 0: The CPU operates on the system clock (ϕ) 1: The CPU operates on the subclock (ϕ_{SUB})
2	TMA3	1	R/W	Selects the mode to transit after the SLEEP instruction is executed with bits SSBY and LSON in SYSCR1 and bits DTON and MSON in SYSCR2.

- SYSCR2 System Control Register 2 Address: H'FFF1

Bit	Bit Name	Set Value	R/W	Description
3	DTON	0	R/W	Direct Transfer on Flag Selects the mode to transit after the SLEEP instruction is executed with bits SSBY, TMA3, LSON in SYSCR1, and bit MSON in SYSCR2.
2	MSON	0	R/W	Medium Speed on Flag This bit selects whether operation continues in the active (high-speed) or the active (medium-speed) mode after the standby mode, the watch mode, or the sleep mode is cleared when the CPU is operating on the system clock. 0: Active (high-speed) mode 1: Active (medium-speed) mode
1	SA1	0	R/W	Subactive Mode Clock Select 1 and 0
0	SA0	0	R/W	Select the operating clock frequency in the subactive and subsleep modes. The operating clock frequency changes to the set frequency after the SLEEP instruction is executed. 00: $\phi_W/8$ 01: $\phi_W/4$ 1x: $\phi_W/2$

- IENR2 Interrupt enable register 2 Address: H'FFF4

Bit	Bit Name	Set Value	R/W	Description
3	IENTFH	1	R/W	Timer FH Interrupt Enable Timer FH interrupt requests are enabled when this bit is set to 1. 1: Timer FH interrupt requests enabled

- IRR2 Interrupt Request Register 2 Address: H'FFF7

Bit	Bit Name	Set Value	R/W	Description
3	IRRTFH	Undefined	R/W	Timer FH Interrupt Request Flag [Setting condition] • When timer FH compare match or overflow occurs [Clearing condition] • When 0 is written to this bit

4.4 RAM Usage

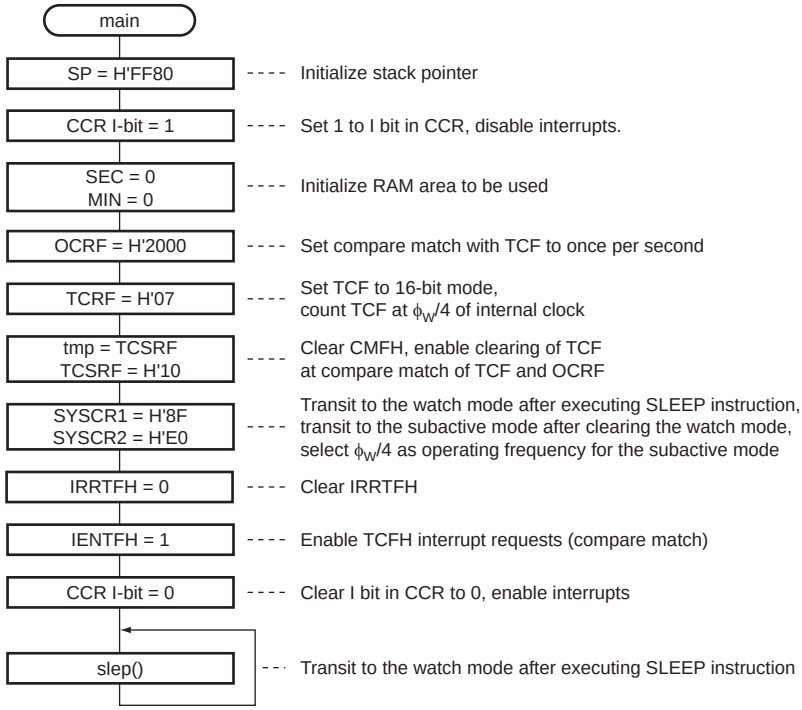
The RAM usage in this sample task is shown in table 5.

Table 5 RAM Usage

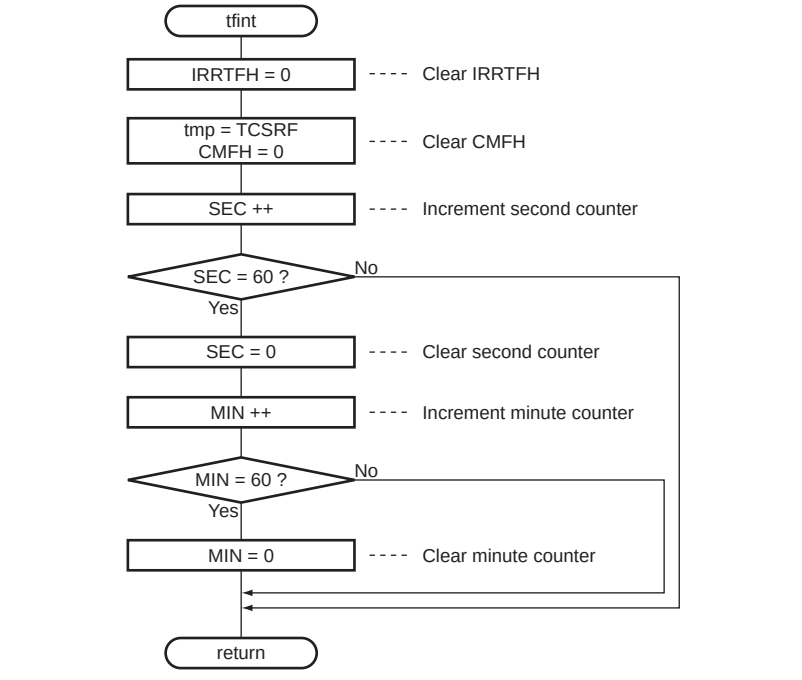
Label	Description	Amount of Memory Used	Used in
SEC	Clock counter, counts seconds	1 byte	main tfint
MIN	Clock counter, counts minutes	1 byte	main tfint

5. Flowchart

5.1 main



5.2 tfint



5.3 Link Address Specifications

Section Name	Address
CVECT	H'0000
P	H'0100
B	H'F780

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Mar.18.05	—	First edition issued

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