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Renesas Electronics Corporation

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H8/300H Tiny Series

Transition to Standby Mode upon Detecting Low Voltage

Introduction

An internal low-voltage detection circuit is used, and depending on the voltage level, transitions to standby mode or to the reset state are made.

Target Device

H8/3687G

Contents

1. Specifications

1. An internal low-voltage detection circuit is used, and the operating state is changed.
2. While in active mode, when the voltage falls to 3.7 V or lower, a transition to standby mode is made.
3. If, while in standby mode, the voltage rises to 4.0 V or higher, the system is returned to active mode.
4. When the voltage falls to 2.3 V or below, an internal reset signal is generated.
5. In order to confirm the operating/reset state, connect an LED to pin P74. In the operating state, the LED is turned on (P74 = 0), and in the reset state the LED is turned off (P74 = 1).
6. If the IRQ1 switch is turned on, the low-voltage detection circuit is canceled.
7. A connection example for this task is shown in figure 1.1.

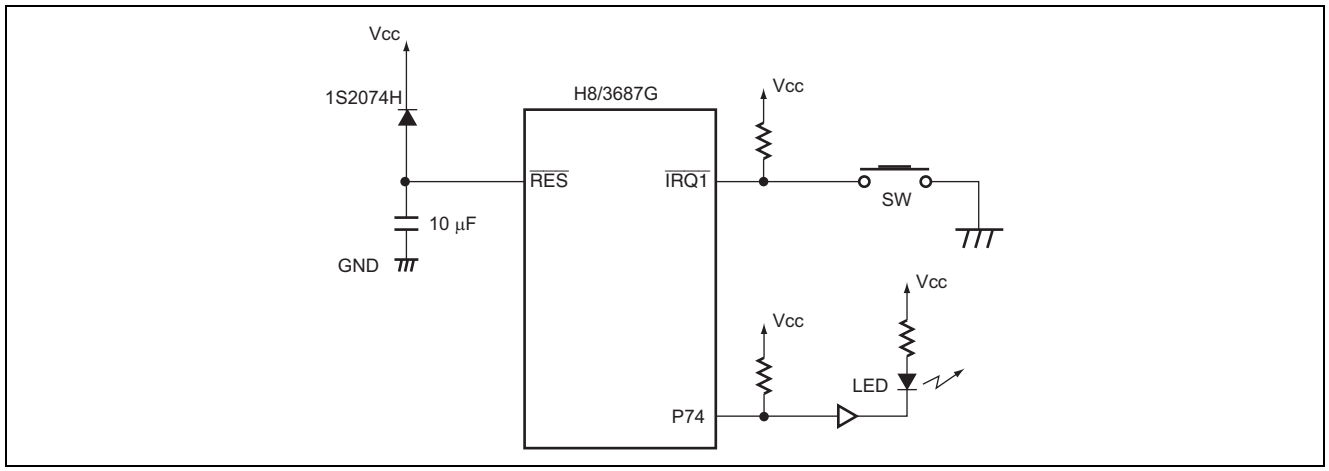


Figure 1.1 Connection example for this task

2. Description of Functions

1. In this sample task, the optional internal low-voltage detection circuit is used to control the operating state at low voltages. A block diagram of the low-voltage detection circuit is shown in figure 2.1. Below, the block diagram of the low-voltage detection circuit is described.

- System clock (ϕ) is a 16 MHz clock which serves as the reference clock for operation of the CPU and peripheral functions.
- Prescaler S (PSS)is functions as a 13-bit counter with ϕ as an input, counting up one each cycle.
- Low-voltage detection control register (LVDCR)is controls the low-voltage detection circuit. In this sample task, the low-voltage detection circuit is used to generate an IRQ0 interrupt when the voltage rises or falls, and sets the reset detection voltage to 2.3 V.
- Low-voltage detection status register (LVDSR)is flags indicating whether the power supply voltage has risen or fallen from a constant voltage.

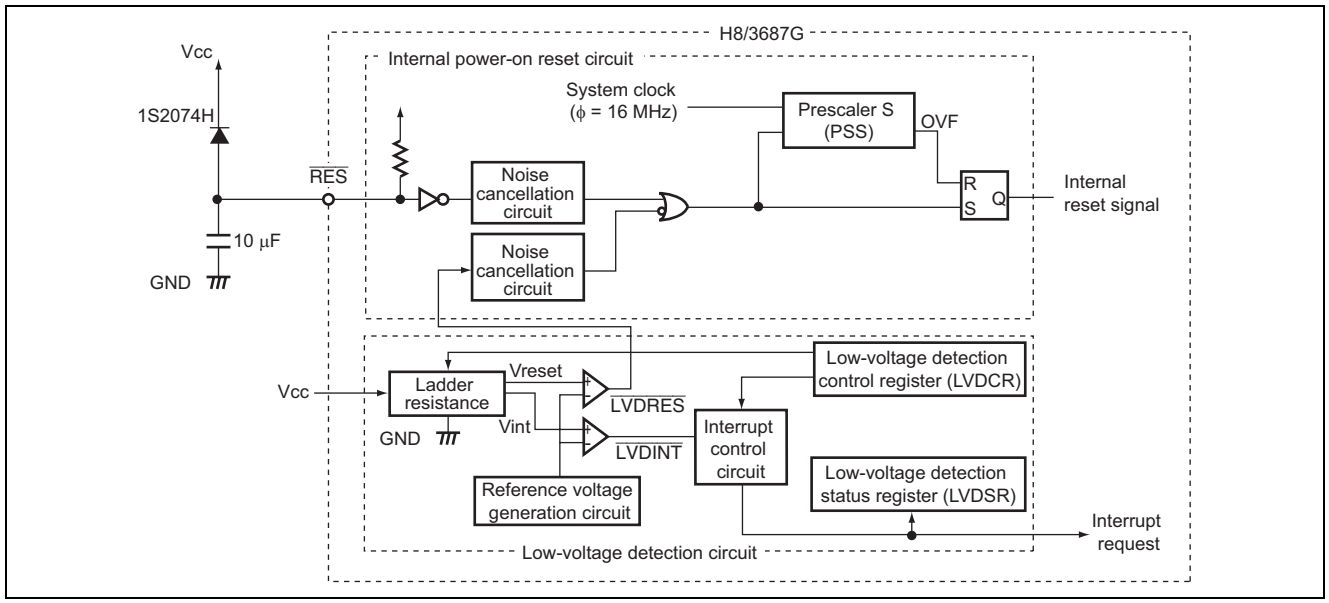


Figure 2.1 Block diagram of the low-voltage detection circuit

2. Function allocations in this sample task are shown in table 2.1. Functions are allocated as shown in table 2.1, and upon low voltage detection there is a transition to standby mode.

Table 2.1 Function allocations

Function	Function allocation
PSS	A 13-bit counter with the system clock used as an input signal
LVDCR	Controls operation/cancellation of the low-voltage detection circuit
LVDSR	Flags indicating whether the power supply voltage has risen or fallen from a certain constant voltage
PDR7	In order to confirm the operating mode, an LED connected to pin P74 is lit
PCR7	Pin P74 is set to an output pin
SYSCR1	Controls low-power consumption modes
SYSCR2	Controls low-power consumption modes
IRQ1	Low-voltage detection circuit operation/cancellation switch

3. Description of Operation

1. Figure 3.1 shows the procedure for setting and canceling LVDI, and transitions to standby mode triggered by low-voltage detection interrupts.

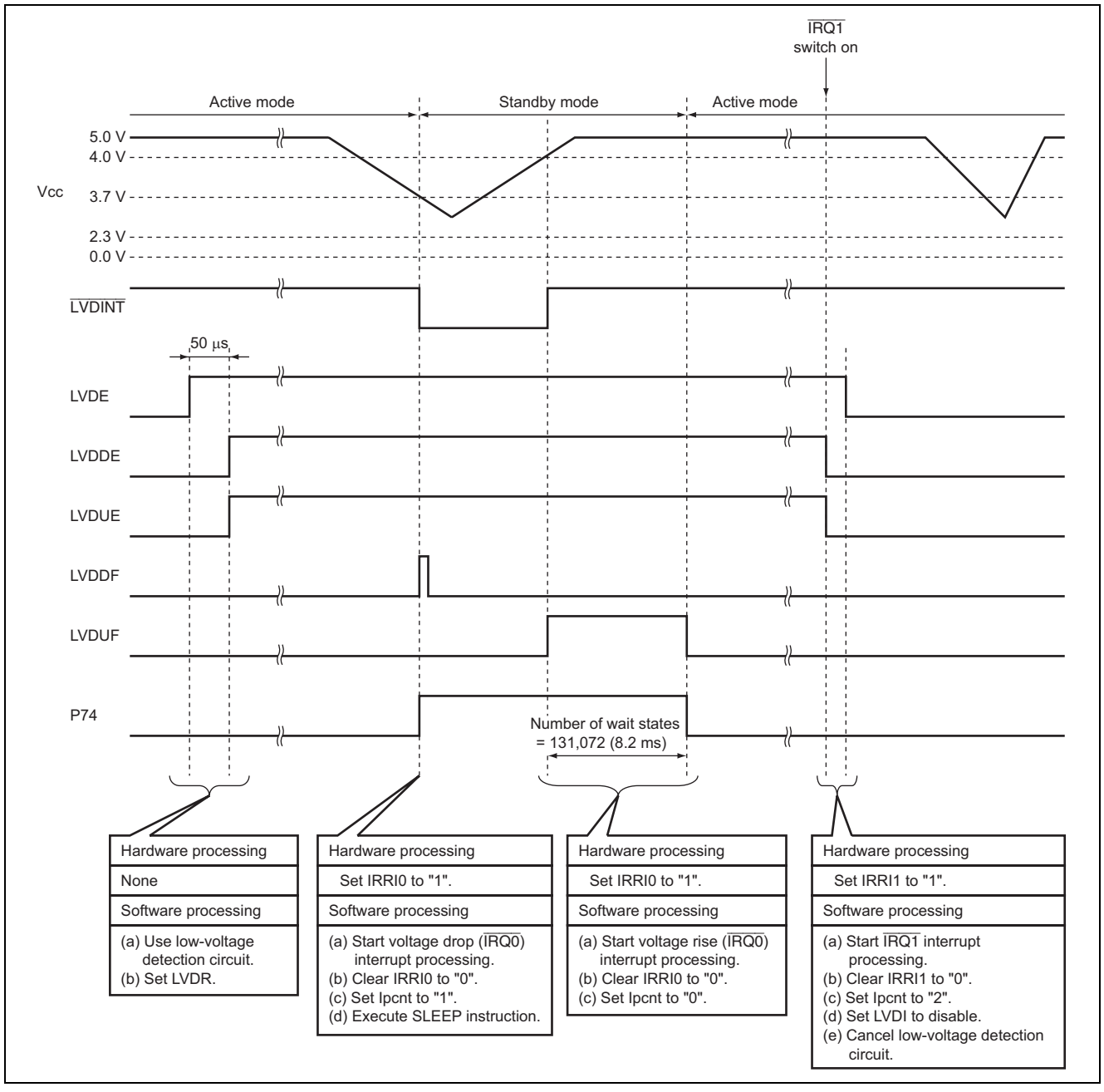


Figure 3.1 Description of operation (1)

2. Figure 3.2 illustrates a transition to standby mode triggered by a low-voltage detection interrupt, and reset operation on low voltage detection.

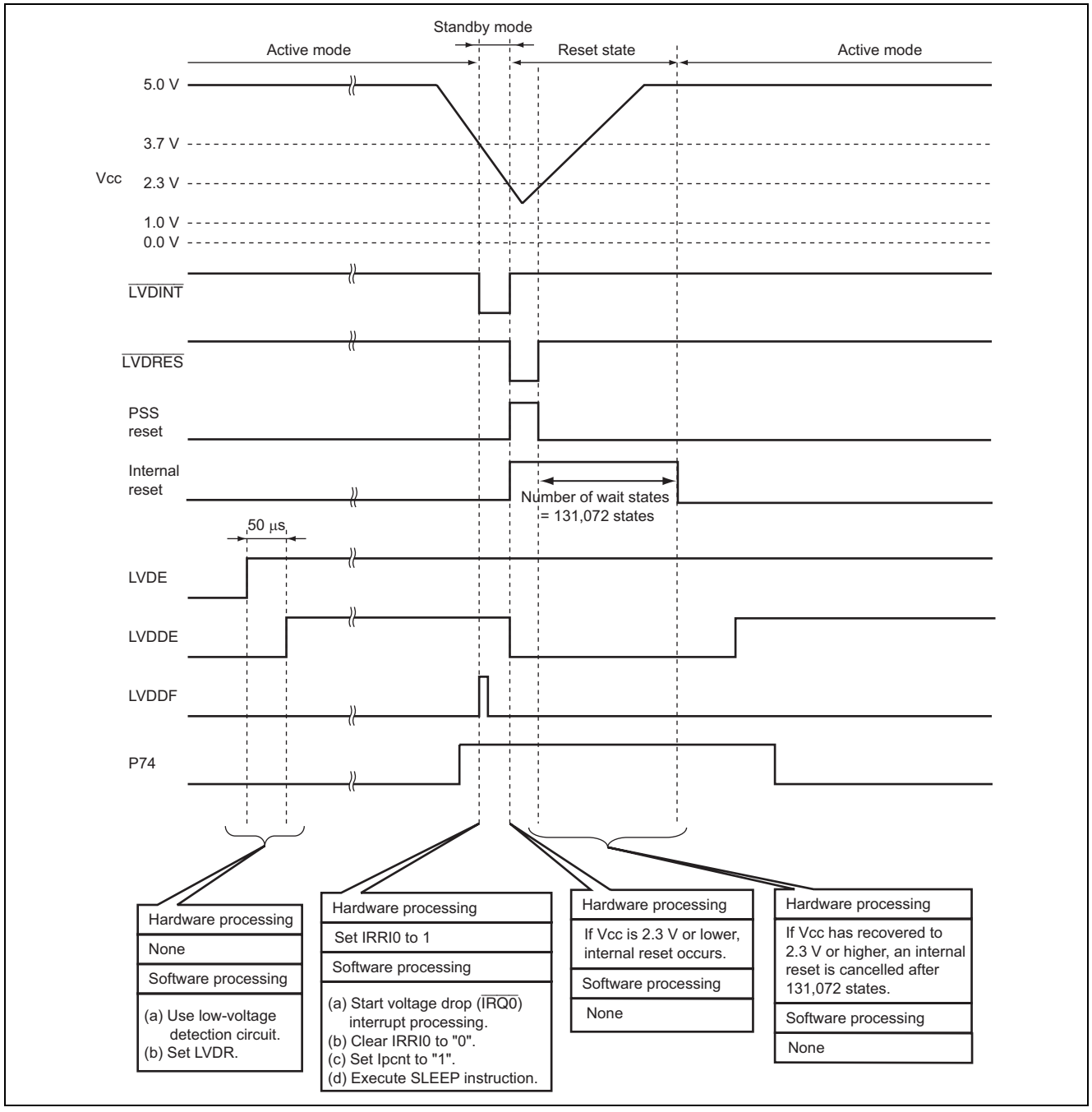


Figure 3.2 Description of operation (2)

4. Description of Software

4.1 Description of modules

Modules in this sample task are listed in table 4.1.

Table 4.1 Description of modules

Module name	Label name	Function
Main routine	main	Set low-voltage detection circuit, enable interrupts, control LED (P74), and judge switch connected to IRQ0
Low-voltage detection interrupt	irq0int	IRQ0 interrupt processing Clear LVD flag, set lpcnt to 0 or 1
Switch on	irq1int	IRQ1 interrupt processing Set lpcnt to 2

4.2 Description of arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers Used

Internal registers used in this sample task are indicated below.

- LVDCR Low-voltage detection control register Address: 0xF730

Bit	Bit name	Setting	Function
7	LVDE	1	LVD enable LVDE = 0: Low-voltage detection circuit is not used (standby state) LVDE = 1: Low-voltage detection circuit is used
3	LVDSEL	0	LVDR detection level selection LVDSEL = 0: Sets reset detection voltage to 2.3 V LVDSEL = 1: Sets reset detection voltage to 3.6 V
2	LVDRE	1	LVDR enable LVDRE = 0: Disables reset by LVDR LVDRE = 1: Enables reset by LVDR
1	LVDDE	1	LVDR enable LVDDE = 0: Disables interrupt requests when voltage falls LVDDE = 1: Enables interrupt requests when voltage falls
0	LVDUE	1	LVDR enable LVDUE = 0: Disables interrupt requests when voltage rises LVDUE = 1: Enables interrupt requests when voltage rises

- LVDSR Low-voltage detection status register Address: 0xF731

Bit	Bit name	Setting	Function
1	LVDDF	0	LVD power supply voltage drop flag LVDDF = 0: Cleared to 0 state LVDDF = 1: Power supply voltage has fallen to 3.7 V or below
0	LVDUF	0	LVD power supply voltage rise flag LVDUF = 0: Cleared to 0 state LVDUF = 1: While the LVDUE flag of LVDCR is set to 1, the power supply voltage has fallen to 3.7 V or below, and risen again to 4.0 V or above before falling to V reset (2.3 V) or below

- PDR7 Port data register 7 Address: 0xFFDA

Bit	Bit name	Setting	Function
4	P74	0	Port data register 74 P74 = 0: Pin P74 output level Low P74 = 1: Pin P74 output level High

- PMR1 Port mode register 1 Address: 0xFFE0

Bit	Bit name	Setting	Function
5	IRQ1	1	Selects function of pin P15/IRQ1 IRQ1 = 0: Sets pin P15/IRQ1 to P15 I/O pin function IRQ1 = 1: Sets pin P15/IRQ1 to IRQ1 input pin function

- PCR7 Port control register 7 Address: 0xFFEA

Bit	Bit name	Setting	Function
4	PCR74	0	Port control register 74 PCR74 = 0: Sets pin P74 to P74 input pin function PCR74 = 1: Sets pin P74 to P74 output pin function

- SYSCR1 System control register 1 Address: 0xFFF0

Bit	Bit name	Setting	Function
7	SSBY	1	Software standby DTON = 0, SSBY = 1: After executing SLEEP instruction in active mode, makes transition to standby mode
6	STS2	STS2 = 1	Standby timer select 2 to 0
5	STS1	STS1 = 0	When STS2 = 1, STS1 = 0 and STS0 = 0, the number of wait states is set to
4	STS0	STS0 = 0	131,072 states

- SYSCR2 System control register 2 Address: 0xFFF1

Bit	Bit name	Setting	Function
5	DTON	0	Direct transfer on flag DTON = 0, SSBY = 1: After executing SLEEP instruction in active mode, makes transition to standby mode
4	MA2	MA2 = 0	Active mode clock select 2 to 0
3	MA1	MA1 = x	MA2 = 0, MA1 = x, MA0 = x:
2	MA0	MA0 = x	Sets the operating clock in active mode/sleep mode to ϕosc (x: don't care)

- IEGR1 Interrupt edge select register 1 Address: 0xFFF2

Bit	Bit name	Setting	Function
0	IEG1	1	IRQ1 edge select IEG1 = 0: Selects falling edge as IRQ1 pin input detection edge IEG1 = 1: Selects rising edge as IRQ1 pin input detection edge

- IENR1 Interrupt enable register 1 Address: 0xFFF4

Bit	Bit name	Setting	Function
1	IEN1	1	IRQ1 interrupt request enable IEN1 = 0: Disables interrupt requests at pin IRQ1 IEN1 = 1: Enables interrupt requests at pin IRQ1

- IRR1 Interrupt flag register 1 Address: 0xFFF6

Bit	Bit name	Setting	Function
1	IRRI1	0	IRQ1 interrupt request flag IRR1 = 0: IRQ1 pin interrupt not requested IRR1 = 1: IRQ1 pin interrupt requested
0	IRRI0	0	IRQ0 interrupt request flag IRR0 = 0: IRQ0 pin interrupt not requested IRR0 = 1: IRQ0 pin interrupt requested

4.4 Description of RAM Used

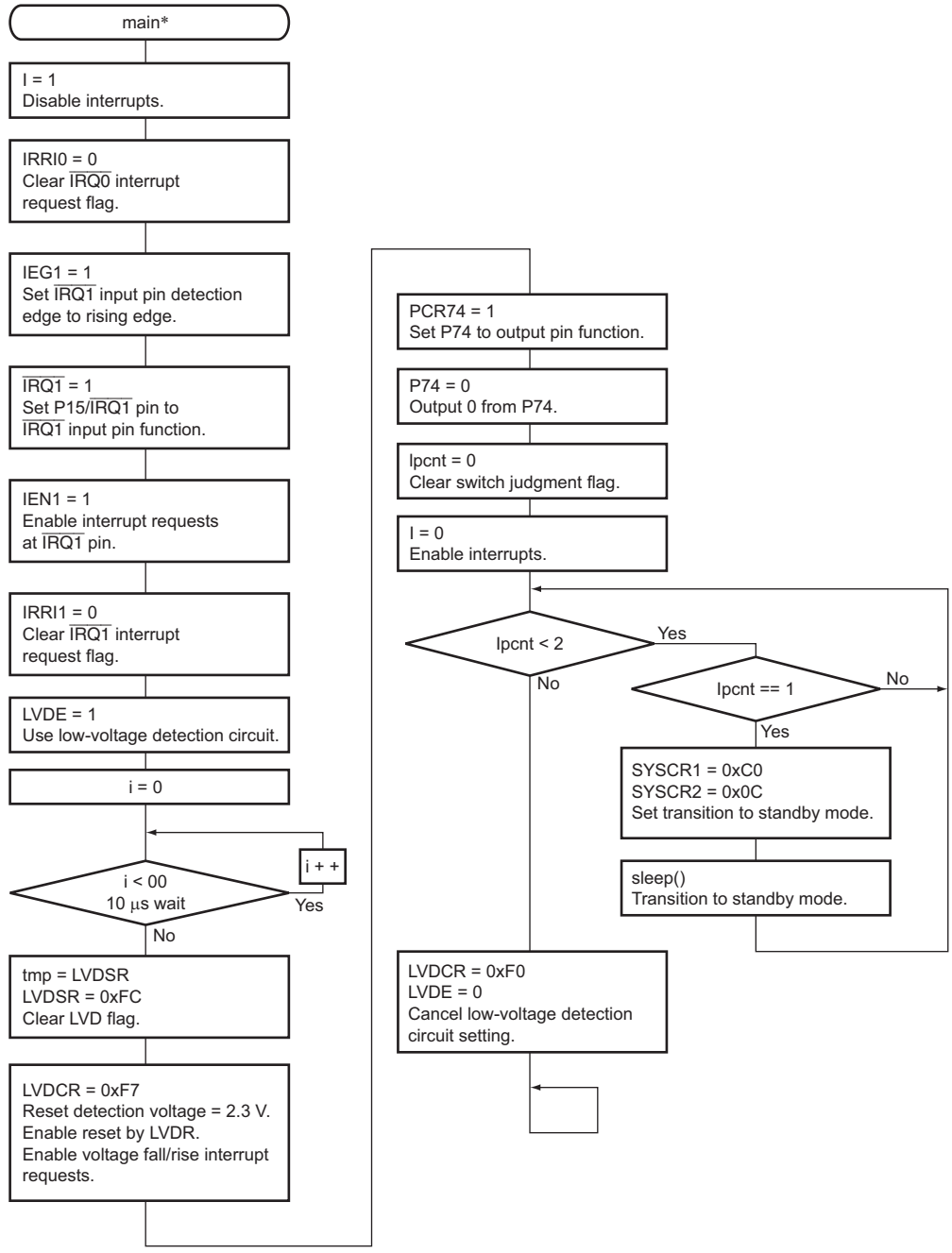
The RAM used in this sample task is described in table 4.2.

Table 4.2 Description of RAM used

Label name	Function	Size	Used in
lpcnt	Flag to discriminate low-voltage detection states lpcnt = 0: Returned to normal mode lpcnt = 1: Low power voltage, module standby lpcnt = 2: IRQ1 interrupt, low-voltage detection circuit disabled	1 byte	Main routine Low-voltage detection interrupt Switch on

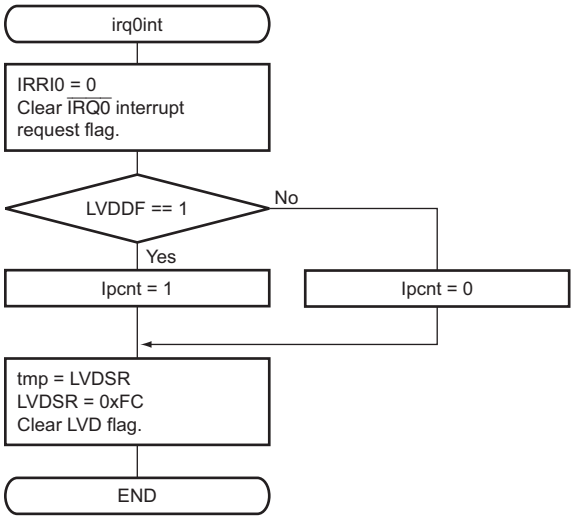
5. Flowcharts

1. Main routine

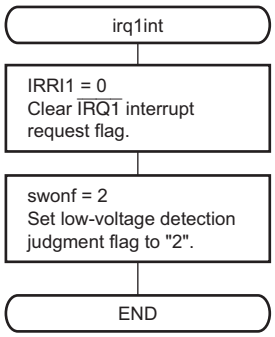


Note: * The stack pointer is set using INIT.SRC (assembly language).

2. Low-voltage Detection Interrupts



3. Switch-on



6. Program Listing

```
/************************************************************************************************************************/
/*                                                                                                                      */
/*   H8/300HN Series -H8/3687G-                                                                                         */
/*   Application Note                                                                                                   */
/*                                                                                                                      */
/*   'Reset by lowvoltage'                                                                                              */
/*                                                                                                                      */
/*   Function                                                                                                           */
/*   : Low-voltage detection circuit                                                                                    */
/*                                                                                                                      */
/*   External Clock : 16MHz                                                                                             */
/*   Internal Clock : 16MHz                                                                                             */
/*   Sub Clock      : 32.768kHz                                                                                         */
/*                                                                                                                      */
/************************************************************************************************************************/

#include    <machine.h>

/************************************************************************************************************************/
/*   Symbol Definition                                                                                                  */
/************************************************************************************************************************/
struct BIT {
     unsigned char   b7:1;         /* bit7 */
     unsigned char   b6:1;         /* bit6 */
     unsigned char   b5:1;         /* bit5 */
     unsigned char   b4:1;         /* bit4 */
     unsigned char   b3:1;         /* bit3 */
     unsigned char   b2:1;         /* bit2 */
     unsigned char   b1:1;         /* bit1 */
     unsigned char   b0:1;         /* bit0 */
};

#define     LVDCR        *(volatile unsigned char *)0xF730                    /* Low-voltage-detection control register   */
#define     LVDCR_BIT    (*(struct BIT *)0xF730)                              /* Low-voltage-detection control register   */
#define     LVDE         LVDCR_BIT.b7                                         /* LVD Enable                               */
#define     LVDSEL       LVDCR_BIT.b3                                         /* LVDI Detection Level Select              */
#define     LVDRE        LVDCR_BIT.b2                                         /* LVDR Enable                              */
#define     PDR7_BIT     (*(struct BIT *)0xFFDA)                              /* Port Data Register 7                     */
#define     P74          PDR7_BIT.b4                                          /* Port Data Register 7 bit4                */
#define     PMR1_BIT     (*(struct BIT *)0xFFE0)                              /* Port mode register 1                     */
#define     IRQ1         PMR1_BIT.b5                                          /* P15/IRQ1 Pin Function Switch             */
#define     PCR7_BIT     (*(struct BIT *)0xFFEA)                              /* Port Control Register 7                  */
#define     PCR74        PCR7_BIT.b4                                          /* Port Control Register 7 bit4             */
#define     IEGR1_BIT    (*(struct BIT *)0xFFF2)                              /* Interrupt Edge Select Register 1         */
#define     IEG1         IEGR1_BIT.b1                                         /* IRQ1 Edge Select                         */
#define     IENR1_BIT    (*(struct BIT *)0xFFF4)                              /* Interrupt Enable Register 1              */
#define     IEN1         IENR1_BIT.b1                                         /* IRQ1 Interrupt Enable                    */
#define     IRR1_BIT     (*(struct BIT *)0xFFF6)                              /* Interrupt Request Register 1             */
#define     IRRI1        IRR1_BIT.b1                                          /* IRQ1 Interrupt Request Flag              */

#pragma interrupt   (irq1int)
```

```
/************************************************************************************************************************/
/*   Function define                                                                                                    */
/************************************************************************************************************************/
extern void INIT ( void );                                          /* SP Set                                           */
void main ( void );
void irq1int ( void );

/************************************************************************************************************************/
/*   RAM define                                                                                                         */
/************************************************************************************************************************/
volatile unsigned char swonf;

/************************************************************************************************************************/
/*   Vector Address                                                                                                     */
/************************************************************************************************************************/
#pragma section     V1                                              /* VECTOR SECTOIN SET                               */
void (*const VEC_TBL1[])(void) = {                                  /* 0x00 - 0x0f                                      */
     INIT                                                           /* 00 Reset                                         */
};
#pragma section     V2                                              /* VECTOR SECTOIN SET                               */
void (*const VEC_TBL2[])(void) = {
     irq1int                                                        /* 1E IRQ1 Interrupt                                */
};

#pragma section                                                     /* P                                                */
/************************************************************************************************************************/
/*   Main Program                                                                                                       */
/************************************************************************************************************************/
void main ( void )
{
     unsigned short i;

     set_imask_ccr(1);                                              /* Interrupt Disable                                */

     IEG1 = 1;                                                      /* IRQ1 pin input is Rising edge                    */
     IRQ1 = 1;                                                      /* Select IRQ1 pin                                  */
     IEN1 = 1;                                                      /* IRQ1 Interrupt Enabie                            */
     IRRI1 = 0;                                                     /* IRQ1 Flag Clear                                  */

     LVDE = 1;                                                      /* LVD Enable                                       */
     for(i=0; i<800; i++);                                          /* 50us Wait                                        */
     LVDCR = 0xFC;                                                  /* LVD = 3.6V LVD Reset Enable                      */

     PCR74 = 1;                                                     /* P74 Output Pin                                   */
     P74 = 0;                                                       /* P74 is Low                                       */
     swonf = 0;                                                     /* Initialize swonf                                 */
     set_imask_ccr(0);                                              /* Interrupt Enable                                 */
     while(swonf == 0);

     LVDCR = 0xF0;                                                  /* clearing LVDRE, LVDDE, LVDUE to 0                */
     LVDE = 0;                                                      /* clear LVDE 0                                     */

     while(1);
}
```

```
/*****************************************************************************************************************************************************/
/*   IRQ1 Interrupt                                                                                                                                  */
/*****************************************************************************************************************************************************/
void irq1int ( void )
{
     IRRI1 = 0;                                                                  /* Clear IRRI1                                                      */
     swonf = 1;                                                                  /* Set swonf                                                        */
}
```

Link address specifications

Section Name	Address
CV1	0x0000
CV2	0x001C
CV3	0x0100
P	0x0100
B	0xFB80

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.29.03	—	First edition issued
2.00	May.07.04	—	Clerical error correction

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